A High-Efficiency Control Method With Lossless Current Sensing and Seamless Transition for Four-Switch Buck–Boost Converter

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***Abstract*—The quadrilateral control method for four-switch Buck–Boost converter can enable all of the power switches to achieve zero-voltage-switching (ZVS), thereby achieving high power density. However, the inductor current requires to be sensed and regulated to ensure the realization of ZVS, which will introduce the additional losses and degrade the efficiency. In this article, a high-efficiency control strategy based on lossless current sampling is proposed, which can achieve the minimum height of the inductor current over the whole working conditions. Moreover, to ensure the smooth switching between different modes, a transition mode is inserted when the input voltage is close to the output voltage. Finally, a prototype with input voltage of 40–60V and output parameters of 48V/6A is built to verify the effectiveness of the proposed sampling circuit and control strategy. The peak efficiency is 98.88%, while the full-load efficiency at the nominal input voltage is 98.14%. Meanwhile, a video material is provided to demonstrate the extremely low root mean square (RMS) value of the inductor current and the smooth switching process under different input voltage and load conditions.**

***Index Terms*—Four-switch Buck–Boost (FSBB), high efficiency, high power density, high switching frequency, lossless current sampling, smooth switching, zero-voltage-switching (ZVS).**

I. Introduction

With the rapid development of artificial intelligence and cloud computing, the power consumption of data centers has been increasing significantly. The 48 V power architecture for servers has increasingly demonstrated its efficiency advantages [1], [2], [3], [4], [5], [6]. As illustrated in Fig. 1, a typical two-stage 48 V architecture consists of a preregulation stage and a step-down stage [7]. The preregulation stage converts a wide-range input voltage of 48 V into a regulated 48 V, while the step-down stage converts the regulated 48 to 1 V that required by the central processing unit (CPU). Compared with the conventional method that adopts multiphase Buck converter, this architecture can achieve higher efficiency as all of the power switches can realize zero-voltage-switching (ZVS). The four-Switch Buck–Boost (FSBB) converter, shown in Fig. 2, is particularly suitable for application in the preregulation stage of 48 V architecture due to its benefits of efficiency and power density.

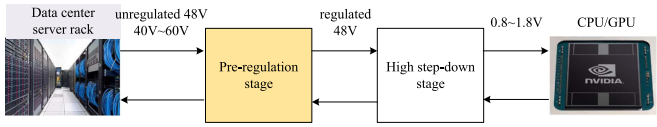

Fig. 1. Topology of FSBB converter.

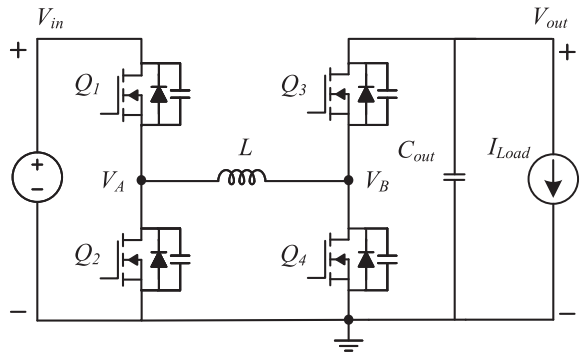

Fig. 2. Topology of FSBB converter.

Early research on the control strategies of the FSBB converter primarily focuses on two- or three-mode control strategies [8], [9], [10], [11], [12]. In these strategies, Q_1 keeps turning-ON when $V_{\text{in}} < V_o$, making the FSBB converter equivalent to a Boost converter, while Q_3 remains conducted-on when $V_{\text{in}} > V_o$, making it equivalent to a Buck converter. When V_{in} is close to V_o, the issues of discontinuity will occur due to the switching between Buck and Boost mode, which requires the extra smooth mode operation. This type of control method typically operates in continuous conduction mode (CCM), where one of the power transistor can not achieve ZVS. Consequently, the two- or three-mode control method is usually adopted in the applications with low input voltage or low switching frequency [13], [14], [15]. In the literature [16], ZVS is achieved by regulating the valley current below 0. However, this method may result in

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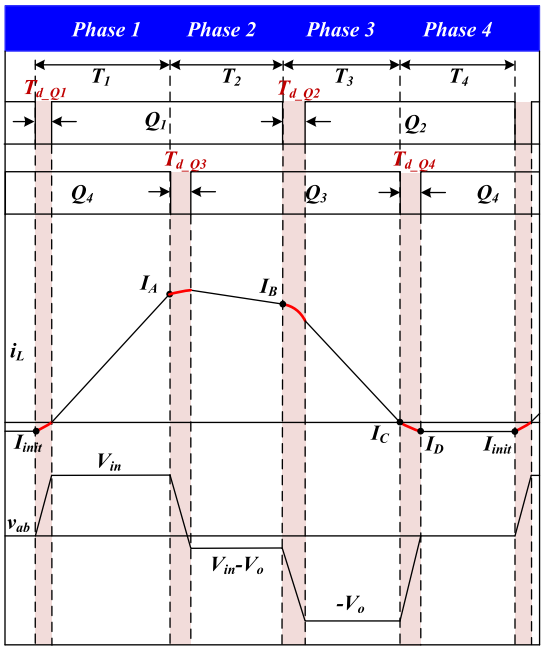

Fig. 3. Waveform of quadrilateral control scheme for FSBB converter.

large inductor current ripple under heavy load, compensating switching losses with conduction losses.

Recently, the quadrilateral current control strategy for FSBB converters [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], has become popular. As shown in Fig. 3, the inductor current waveform for this control method resembles a quadrilateral. FSBB converter consistently operates in pseudo-continuous conduction mode (PCCM), with the inductor current containing both positive and negative portions. The four vertices I_{init}, I_A, I_B, and I_C of the inductor current i_L are used to achieve soft switching for Q_1, Q_3, Q_2, and Q_4, respectively. This control strategy owns higher degrees of freedom, as the lengths of the four sides of the quadrilateral T_1, T_2, T_3, and T_4 can be tuned. Achieving ZVS of all power switches and minimum root mean square (RMS) current are the two main control objectives.

According to different implementation, the quadrilateral current control strategy can be divided into three categories: 1) digital-calculation-based method [17], [18], [19], [20], [21]; 2) look-up-table-based method [22], [23], [25], [27]; 3) physical-circuit-based method [24], [26], [28].

For the digital-calculation-based method, a detailed mathematical model for the FSBB converter is required. Based on the desired control objectives, precise expressions for various control variables are derived. These expressions involve parameters such as input voltage V_{in}, output voltage V_{out}, output current I_o, and the sampled inductor current i_{L_sample}. In [18], a unified one-cycle control method is proposed to achieve ZVS for bidirectional power flow operation. In [17], a solution using the Lagrange multiplier is proposed to reduce the current ripple. In [20], the analytical solution for phase shift control is proposed and the control strategy is implemented in the digital controller with the aid of an analog comparator. In [19], a closed-form solution based on average inductor current control scheme is proposed, which can get rid of the requirement for wide-bandwidth current sensing.

These control expressions are implemented through the digital computation on platforms such as digital signal processor (DSP), microcontroller unit (MCU), or field programmable gate array (FPGA). First, the signals V_{in}, V_{out}, I_o, or i_{L_sample} of FSBB converter are sampled and converted to digital values via ADC. Then, the control variables can be calculated in real-time based on these sampled digital signals. Meanwhile, the calculation operation incorporates a Proportional–Integral (PI) controller to achieve output voltage regulation. Finally, these control variables are integrated into the driving signals for the four power switches to realize overall control.

The advantage of this control scheme lies in its high flexibility. Different control expressions can be adopted under different input voltages or load currents, thereby enabling more diverse function. However, the disadvantage is the computational speed. Due to the complexity of the mathematical model for FSBB converter, the control expressions involve numerous multiplications, divisions, and even square root calculations, which require significant computation time. In [21], the control expressions are simplified to achieve real-time control strategy. However, the control accuracy is degraded. In general, the digital-calculation-based method is more suitable for low-switching-frequency applications.

The LUT-based scheme is a variant of the digital-calculation-based method. This approach also requires precise control expressions. Differently, the control variables are precalculated offline and stored in a LUT. During the actual control, the most suitable control value for the current operating condition is retrieved based on the sampled parameters such as input voltage V_{in} and output current I_o.

The advantage of this control scheme is its excellent real-time performance, with the switching frequency of FSBB converter reaching above 1 MHz [25], [27]. However, the disadvantage is the tradeoff between control precision and storage capacity. In order to improve the control accuracy, the index precision of the LUT should be increased, thereby storage requirements will be significantly enlarged. This issue is particularly pronounced in 3D-LUTs. In literature [22], [23], the mathematical model for FSBB converter is optimized to convert the 3D-LUT to a 2D-LUT, significantly decreasing storage requirements and correspondingly improving control accuracy.

A common issue with the two above schemes is that parameter deviations in inductor can lead to discrepancies between the calculated or retrieved control values and the desired values, thus degrading the control performance. In physical-circuit-based method, this issue does not arise since the converter's state is detected in real-time. The solution of control variables is obtained through the regulation of the voltage or current loop. In literature [26], [28], a PWM and phase-shift control method is proposed, where the duty cycle and phase shift are approached through the two loops with the sampled output voltage and inductor current. In literature [24], a quasi-peak current control method is proposed, where the control variables is regulated by the V_{err} signal from the outer voltage loop.

The physical-circuit-based scheme is not affected by parameter deviations, resulting in the highest control precision and better real-time performance. However, this method can only perform the simple calculation such as the Boolean

operations, simple additions, and multiplications. Therefore, the control logic should be simplified as much as possible.

Although there are extensive research on FSBB converters, the following issues still remain unresolved.

1) All of the aforementioned schemes can not avoid the current sampling circuit, which degrades the efficiency.
2) The current state whether is Boost or Buck mode should be detected since the calculation algorithm varies under different modes. The mode transition when the input voltage changes may lead to the potential discontinuities.

The contributions of this article are as follows.

1) A lossless current sampling scheme for FSBB converters is proposed, where the inductor current is indirectly sampled through volt–second methods.
2) The minimum height of inductor current is achieved over the whole operating conditions, which can improve the efficiency.
3) A seamless switching between different modes is proposed, allowing the FSBB converter to achieve smooth and continuous transitions across a wide input voltage and load range.

This rest of this article is organized as follows. The working principle of the quadrilateral control scheme, including the analysis of dead time, is briefly introduced in Section II. In Section III, the lossless sampling method is proposed to eliminate the sampling loss. Then, the regulation logic for minimizing the RMS current of both Buck and Boost modes is derived in Section IV. Subsequently, loop regulation and a seamless transition scheme between Buck and Boost modes are proposed. In Section V, the overall implementation of the proposed control strategy is detailed. In Section VI, a prototype is built to validate the effectiveness of the proposed control strategy and implementation. Finally, Section VII concludes this article.

II. Operational Principle and ZVS Analysis of FSBB Converter

Fig. 2 delineates the topology of the FSBB converter, characterized by a set of dual half-bridge and an inductor linked at the half-bridges' midpoints. The topology comprises a leading half-bridge, consisting of switches Q_1 and Q_2, and a lagging half-bridge, composed of Q_3 and Q_4. It is notable that both the duty cycles and phase shifts of these half-bridges are independently adjustable, facilitating nuanced control over power transmission. The modulation of the phase shift between the leading and lagging half-bridges is imperative for efficient forward power transmission. In addition, the switching frequency of the half-bridges can also be adjusted for improving the efficiency. In the FSBB converter, numerous control variables are adjustable, offering a high degree of control flexibility. How to find the optimal control form the extensive combination over the various parameters, which is the core of our investigation.

Fig. 3 illustrates the operational waveform of the FSBB converter employing a quadrilateral control scheme. This scheme engenders a quadrilateral-shape inductor current waveform, as a consequence of the phase shift between the two half-bridges.

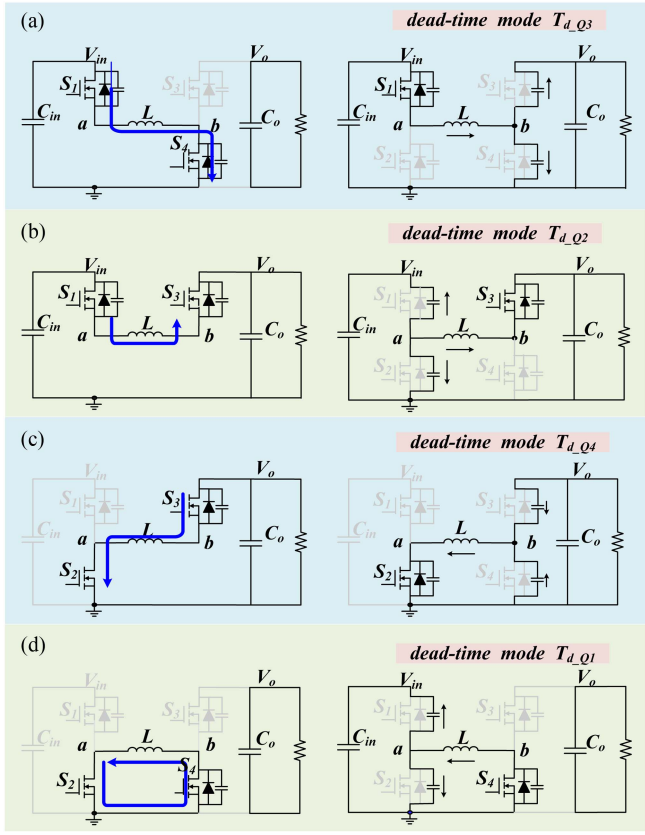

Fig. 4. Equivalent circuits for the four phases of FSBB converter. (a) Q_1 and Q_4 are ON. (b) Q_1 and Q_3 are ON. (c) Q_2 and Q_3 are ON. (d) Q_2 and Q_4 are ON. (a) Main mode T_1. (b) Main mode T_2. (c) Main mode T_3. (d) Main mode T_4.

Such a configuration enables the inductor current to include both positive and negative components, facilitating ZVS for all power switches. This scheme can be split into four main operational phases and four dead-time modes, denominated T_1, T_2, T_3, T_4, T_{d_Q1}, T_{d_Q2}, T_{d_Q3}, and T_{d_Q4}. To facilitate clarity in discussion, the inductor current's turning points are labeled as I_{init}, I_A, I_B, and I_C. Meanwhile, v_a and v_b represent the switching node voltages of the leading and lagging half-bridges, respectively. A brief description of these phases is provided subsequently.

Phase 1: As depicted in Fig. 4(a), this phase initiates with simultaneous conduction of Q_1 and Q_4, wherein V_{in} is applied directly across the inductor, precipitating a swift ascent of the inductor current i_L from 0 to I_A. This increment facilitates ZVS for Q_3 by ensuring I_A remains above I_{ZVS}.

For T_{d_Q3}: I_A is the initial value of i_L during the dead-time mode of Q_3. The inductor L resonates with the junction capacitance of Q_3 and Q_4 ($C_{oss\_Q3} + C_{oss\_Q4}$) after Q_4 is turned OFF. The expressions for i_L and v_B can be represented as follows:

$$\begin{cases} i_L(t) = \frac{V_{\text{in}}}{Z}\sin(\omega t) + I_A\cos(\omega t) \\ v_B(t) = V_{\text{in}} - V_{\text{in}}\cos(\omega t) + I_A Z\sin(\omega t) \end{cases} \tag{1}$$

where $\omega = \frac{1}{\sqrt{L\cdot 2C_{\text{oss}}}}$, $Z = \sqrt{\frac{L}{2C_{\text{oss}}}}$ and assuming that the junction capacitance of Q_1, Q_2, Q_3, and Q_4 equal to C_{oss}. ZVS of Q_3 can be achieved when v_B(t) reaches V_{out}. Then, T_{d_Q3} can be

obtained that

$$T_{d\_Q3}=\frac{1}{\omega}\left(\arctan\frac{\sqrt{I_A^2Z^2+2V_{\text{in}}V_{\text{out}}-V_{\text{out}}^2}}{V_{\text{in}}-V_{\text{out}}}-\arctan\frac{I_AZ}{V_{\text{in}}}\right). \tag{2}$$

During this stage, v_B(t) will quickly reach V_{out}, and then the body diode of Q_3 will be conducted-on and v_B(t) will be clamped. As long as T_{d_Q3} satisfies (2) and is as close as possible, ZVS and lower body diode loss can be guaranteed. Since Q_3 is driven by synchronous rectification in this article, Q_3 is turned ON when v_{ds_Q3} is reached to be threshold voltage. Therefore, the dead-time of Q_3 is set automatically by the synchronous rectification and ZVS can always be achieved.

Phase 2: Fig. 4(b) illustrates the scenario wherein Q_1 and Q_3 are conducted-on concurrently, facilitating direct power transfer from the input to the load. The inductor current transitions smoothly from I_A to I_B, influenced by the value of $V_{\text{in}}-V_{\text{out}}$. To optimize energy transfer efficiency and minimize conduction losses, it is advantageous to maximize the T_2/T_1 ratio.

For T_{d_Q2}: I_B is the initial value of i_L during the dead-time mode of Q_2. The inductor L resonates with the junction capacitance of Q_1 and Q_2 ($C_{\text{oss\_Q1}}$ + $C_{\text{oss\_Q2}}$) after Q_1 is turned OFF. The expressions for i_L and v_A can be represented as follows:

$$\begin{cases} i_L(t)=\frac{V_{\text{in}}-V_{\text{out}}}{Z}\sin(\omega t)+I_B\cos(\omega t) \\ v_A(t)=(V_{\text{in}}-V_{\text{out}})\cos(\omega t)-I_BZ\sin(\omega t)+V_{\text{out}}. \end{cases} \tag{3}$$

ZVS of Q_2 can be achieved when v_A(t) decreases to 0. Then, T_{d_Q2} can be obtained that

$$T_{d\_Q2}=\frac{1}{\omega}\left(\arctan\frac{V_{\text{out}}}{\sqrt{V_{\text{in}}^2-2V_{\text{in}}V_{\text{out}}+I_B^2Z^2}}-\arctan\frac{V_{\text{out}}-V_{\text{in}}}{I_BZ}\right). \tag{4}$$

If the value of I_B is too small, the minimum value of v_A(t) will always be greater than 0. At that time, no matter what dead time T_{d_Q2} is set, ZVS of Q_2 cannot be achieved. Therefore, the value of I_B should meet the the following:

$$I_B\geq\frac{\sqrt{2V_{\text{in}}V_{\text{out}}-V_{\text{in}}^2}}{Z} \tag{5}$$

When I_B is set to be the critical value, the minimum value of v_A(t) equals to be 0. At that time, T_{d_Q2} should strictly equal to (6), and any deviation, whether too large or too small, will result in lead to partial ZVS.

$$T_{d\_Q2}=\frac{1}{\omega}\left(\frac{\pi}{2}-\arctan\frac{V_{\text{out}}-V_{\text{in}}}{\sqrt{2V_{\text{in}}V_{\text{out}}-V_{\text{in}}^2}}\right). \tag{6}$$

Phase 3: Fig. 4(c) shows the equivalent circuit for Phase 3, which features simultaneous conduction by Q_2 and Q_3, resulting in a sharp decline in the inductor current from I_B to I_C. Since the turn-OFF point of Q_3 is regulated by synchronous rectification in this article, the value of I_C is actually set at the zero-crossing point ($I_C=0$).

For T_{d_Q4}: I_C is the initial value of i_L during the dead-time mode of Q_4. The inductor L resonates with the junction capacitance of Q_3 and Q_4 (C_{oss_Q3} + C_{oss_Q4}) after Q_3 is turned OFF. Both i_L and v_B decreases and their expressions can be presented as follows:

$$\begin{cases} i_L(t)=-\frac{V_{\text{out}}}{Z}\sin(\omega t)+I_C\cos(\omega t) \\ v_B(t)=V_{\text{out}}\cos(\omega t)+I_CZ\sin(\omega t). \end{cases} \tag{7}$$

ZVS of Q_4 can be achieved when v_B(t) reaches 0. Then, T_{d_Q4} can be obtained in (8). The final value of i_L during this stage will decrease to I_D

$$T_{d\_Q4}=\frac{\pi}{2}\cdot\frac{1}{\omega}. \tag{8}$$

Phase 4: As shown in Fig. 4(d), this phase involves concurrent conduction of Q_2 and Q_4. The inductor current keeps constant and negative, which equals to $I_D(I_{\text{init}})$. Given its negligible contribution to energy transfer, minimizing the duration of T_4 is crucial in heavy-load scenarios to reduce conduction losses. In addition, T_4 is adjusted to keep the switching frequency constant under light load.

For $T_{d\cdot Q1}$: The initial value I_{init} of the inductor current i_L is negative. The inductor L resonates with the junction capacitance of Q_1 and Q_2 (C_{oss_Q1} + C_{oss_Q2}) after Q_2 is turned OFF. The expressions for i_L and v_A can be represented as follows:

$$\begin{cases} i_L(t)=I_{\text{init}}\cos(\omega t) \\ v_A(t)=-I_{\text{init}}Z\sin(\omega t). \end{cases} \tag{9}$$

If the value of -I_{init} is small than V_{in}/Z, the maximum value of v_A(t) is always lower than V_{in}. At that time, no matter what dead time is set, only partial ZVS can be achieved. Therefore, I_{init} should meet the requirement that

$$I_{\text{init}}\leq-\frac{V_{\text{in}}}{Z}. \tag{10}$$

ZVS of Q_1 can be achieved when v_A reaches V_{in}. Then, T_{d_Q1} can be obtained as follows:

$$T_{d\_Q1}=\frac{1}{\omega}\arcsin\frac{V_{\text{in}}}{-I_{\text{init}}Z}. \tag{11}$$

In summary, the ZVS current and the corresponding dead-time for Q_1, Q_2, Q_3, and Q_4 are summarized in Table I.

III. Proposed Current Sampling Method to Reduce the Sampling Loss

To achieve ZVS of power switches in FSBB converter, it is necessary to sample the inductor current in real-time. To simplify the regulation, the vertices of the inductor current I_{init}, I_A, and I_B can be set to a fixed value I_{ZVS}, which is represented in equation (12). The ZVS currents adopted in this article are shown in Table I.

$$\begin{cases} I_{\text{init}}=-I_{\text{ZVS}} \\ I_{A,B}\geq I_{\text{ZVS}} \\ I_C=0 \\ I_{\text{ZVS}}=\frac{V_{\text{in\_max}}}{Z}. \end{cases} \tag{12}$$

In the literature [19], [22], [23], [24], [27], a sampling resistor is connected in series into the main power path of the FSBB

TABLE I
SUMMARIZING OF ZVS CURRENT AND DEAD-TIME FOR POWER SWITCHES

	Theoretical value	Implementation in this paper
$I_{\text{init}}(I_D)$	(10)	$I_{\text{init}} = -\sqrt{\frac{2C_{\text{oss}} + C_{\text{EX}}}{L}} V_{\text{out}} = -\frac{V_{\text{in\_max}}}{Z}$
T_{d_Q1}	(11)	$T_{d\_Q1} = \frac{1}{\omega} \arcsin \frac{V_{\text{in}}}{V_{\text{in\_max}}}$
I_A	Unrestricted	$I_A \geq \frac{V_{\text{in\_max}}}{Z}$
T_{d_Q3}	(2)	Synchronous Rectification
I_B	(5)	$I_B \geq \frac{V_{\text{in\_max}}}{Z}$
T_{d_Q2}	(4)	(4)
I_C	0	0
T_{d_Q4}	(8)	v_B sensing circuit in Fig. 14

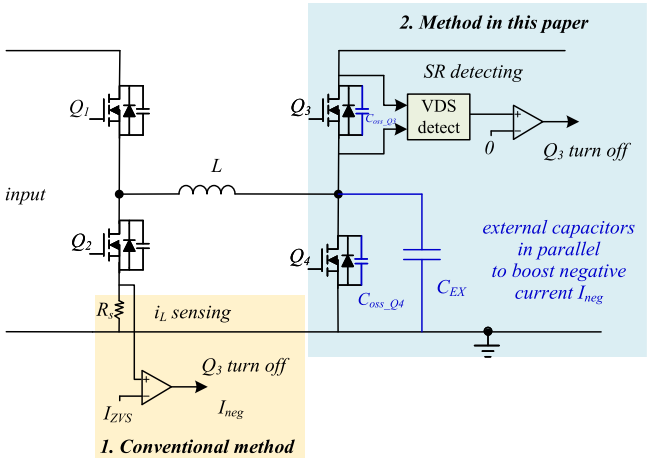

Fig. 5. Comparison of current sampling circuits for the negative current I_{init} between the previous work and this article.

converter. Then, the voltage value across the sampling resistor is used to represent the inductor current, thereby achieving the regulation of ZVS current. Such a current sampling circuit will introduce additional losses. In this article, a set of lossless current sampling methods are proposed to reduce the sampling loss while achieving the similar regulation of ZVS current. The specific operations are as follows.

A. Operation to Regulate the Negative Current I_{init}

The conventional current sampling circuit is shown in the yellow-shadowed area of Fig. 5. By sampling the voltage across R_s and comparing it with I_{ZVS}, the generated signal can be used to turn OFF Q_3. Then, the negative current I_{init} will remain in -I_{ZVS} during T_4 stage so that ZVS of Q_1 can be achieved in the next cycle. The loss of the sampling resistor R_s can be expressed as

$$P_{\text{sen\_loss\_neg}} = \frac{R_s}{T_{\text{sw}}} \int_{T_1+T_2}^{T_{\text{sw}}} i_L(t)^2 dt. \tag{13}$$

In this article, the regulation of I_{init} is achieved through the synchronous rectification of Q_3 to avoid current sampling loss, which is marked as the blue-shadowed area of Fig. 5. The drain-source voltage of Q_3 is detected in the synchronous rectification ICs. When v_{ds_Q3} rises from negative to 0, Q_3 is turned OFF. Then, V_b will drop to 0 through LC resonance, and the energy stored in the junction capacitance will be converted into negative current I_D. Since i_L remains almost unchanged in Phase 4, I_{init} is approximately equal to I_D. To ensure that I_{init} is sufficient to achieve ZVS of Q_1 under conditions that $V_{\text{in}} = V_{\text{in\_max}}$, an external capacitor needs to be paralleled with Q_4. As show in (14), $I_D(I_{\text{init}})$ can be regulated by the external parallel capacitor C_{EX}

$$I_{\text{init}} = -\sqrt{\frac{C_{\text{EX}} + C_{\text{oss\_Q3}} + C_{\text{oss\_Q4}}}{L}} V_{\text{out}}. \tag{14}$$

The value of the external parallel capacitor C_{EX} can be presented as follows:

$$C_{\text{EX}} = 2C_{\text{OSS}} \frac{V_{\text{in max}}^2 - V_{\text{out}}^2}{V_{\text{out}}^2} \tag{15}$$

Since the method adopted in this article is to detect the voltage across the ON-resistance of Q_3, the additional sampling loss is avoided.

B. Operation to Regulate the Positive Current I_A and I_B

The most direct method [19], [22], [23], [24] to sampling the positive current I_A and I_B is to connect a sampling resistor R_s in series in the main current path, and then sensing the differential signal across R_s to reflect the values of I_A and I_B. Then, the sampling loss can be expressed as

$$P_{\text{sen\_loss\_pos}} = \frac{R_s}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} i_L(t)^2 dt. \tag{16}$$

An indirect sampling circuit based on voltage–second method is proposed in this article to reduce the sampling loss. Since I_A is proportional to T_1, we only need to limit the minimum value of T_1 to ensure that I_A is always greater than I_{ZVS}. Therefore, there are no additional sampling loss for regulating I_A.

The difficulty of positive current regulation lies in I_B. Since the value of I_B is related to V_{in}, V_{out}, L, T_1, and T_2, using the similar method for regulating I_A will cause the value of I_B to be lower than I_{ZVS} during the dynamic transient process, resulting in non-ZVS of Q_2. This is due to the parameters V_{out} and T_1 will change rapidly during the dynamic process.

In this article, a lossless current sampling circuit is proposed, which can indirectly represent the inductor current based on the principle that the constant current source charging the capacitor. As shown in Fig. 6, the circuit consists of two voltage-controlled current sources (VCCS1 and VCCS2), a charging capacitor C_t, a reset switch SW1, and a comparator COMP3. In VCCS1, I_{source} is proportional to the switching node voltage v_a. Then, I_{source} equals V_{in}/R_1 when Q_1 is on and equals 0 when Q_2 is ON. In VCCS2, I_{sink} is proportional to the switching node voltage v_b. I_{sink} equals V_{out}/R_2 when Q_3 is ON and equals 0 when Q_4 is ON. The difference between the two current source, $I_{\text{source}} - I_{\text{sink}}$, charges the capacitor C_t, and the voltage across C_t during T_2

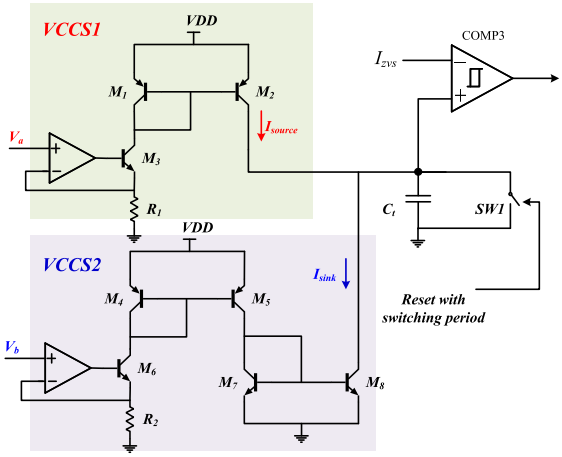

Fig. 6. Diagram of the proposed lossless current sensing circuit.

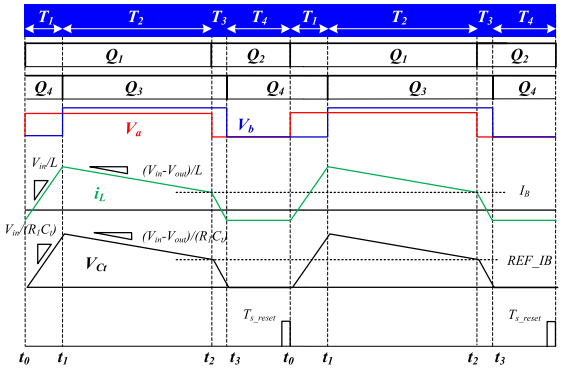

Fig. 7. Waveform of the proposed lossless current sensing circuit.

stage can be expressed as

$$V_{Ct} = \frac{1}{C_t}\left(I_{\text{source}}T_1 + (I_{\text{source}} - I_{\text{sink}})\,(t - T_1)\right) = \frac{V_{\text{in}}}{C_t R_1}T_1 + \left(\frac{V_{\text{in}}}{C_t R_1} - \frac{V_{\text{out}}}{C_t R_2}\right)(t - T_1)\,. \tag{17}$$

Correspondingly, the inductor current i_L in the T_2 stage can be expressed as

$$i_L = -I_{\text{ZVS}} + \frac{V_{\text{in}}}{L}T_1 + \frac{V_{\text{in}} - V_{\text{out}}}{L}(t - T_1) \ldots t \in (T_1, T_1 + T_2)\,. \tag{18}$$

As long as $R_1 = R_2$ and L is proportional to $C_t R_1$, the slopes of V_{Ct} and i_L will be consistent and the only difference is the offset $-I_{\text{ZVS}}$. After equivalent conversion, the voltage V_{Ct} can be adopted to represent the value of the inductor current i_L.

Fig. 7 shows the effect of the proposed current sensing circuit. It can be seen that the waveform of V_{Ct} can be pretty consistent with the waveform of i_L. When V_{Ct} decreases to be REF_IB during the T_2 stage, i_L reaches I_{ZVS} at the same time. Then, the output of comparator COMP3 will be high, triggering the turn-OFF signal of Q_1.

Since there are no sampling resistor R_s connected in series in the main current path, the regulations of the positive current I_A and I_B in this article are lossless. The proposed current sensing circuits are achieved by the current mirror circuits, which are easy to be integrated into an IC. Fig. 8 shows the comparison

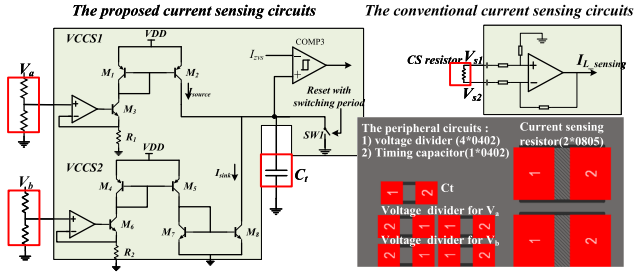

Fig. 8. Comparison of the peripheral circuits between the proposed current sensing circuits and the conventional ones.

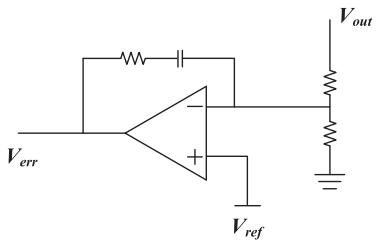

Fig. 9. Outer voltage loop to represent the output current.

of the peripheral circuits between the proposed current sensing circuits and the conventional ones. Both of the green shaded parts can be integrated into the IC and the red rectangle are the peripheral components. For the proposed current sensing circuits, three pins (V_a, V_b, and C_t) and two voltage dividers and one timing capacitor are required. The package of 0402 can be chosen for the voltage dividers and the capacitor due to the loss of these components are low. For the conventional one, two pins and a current sensing resistor are required. Assuming the current sampling loss ranges from 0.5 to 1W, two sampling resistors with package of 0805 (rated power 0.5W) are required according to the derating design. It can be seen that the area of five components with package of 0402 is smaller than the area of two 0805 resistors. The complexity and cost of implementation of the proposed current sensing circuits is relatively low and can be accepted.

C. Operation to Obtain the Information of I_o

In the previous work of FSBB converter, the signal of the output current I_{out} is sampled to be the index [27] of the lookup table for the control variables, or to be the boundary signal between different control modes [17], [19]. The sampling loss can be presented that

$$P_{\text{sen\_loss\_Iout}} = I_o^2 R_s. \tag{19}$$

In literature [25], a method of using the output signal V_{err} of the outer voltage loop to indirectly represent the information of I_o is proposed. In this article, the same method is adopted to reduce the sampling loss of I_o. As illustrated in Fig. 9, the output voltage V_{out} is sampled through a voltage divider, and compared with a reference voltage V_{ref}. The comparison generates a voltage error signal V_{err} after the PI compensation. The magnitude of V_{err} indirectly reflects the magnitude of the output current I_{o}. As I_{o} increases, V_{out} decreases, and V_{err} increases. In contrast, as I_{o} decreases, V_{out} increases and V_{err} decreases correspondingly.

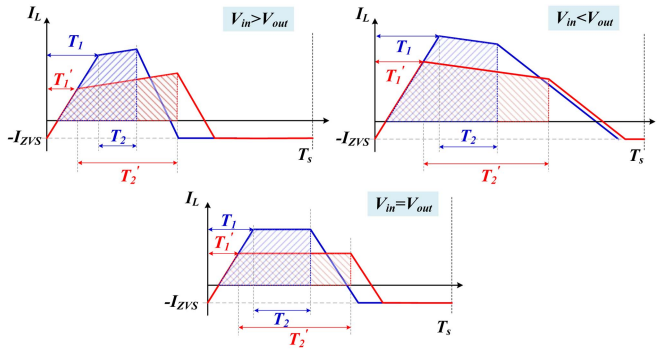

Fig. 10. Influence of different T_1 on the inductor waveform.

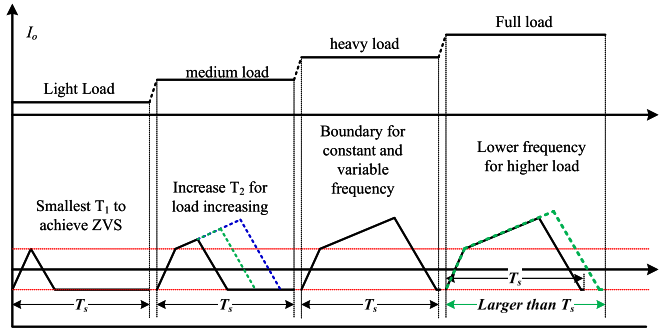

Fig. 11. Waveform of inductor current from light load to full load at Buck mode.

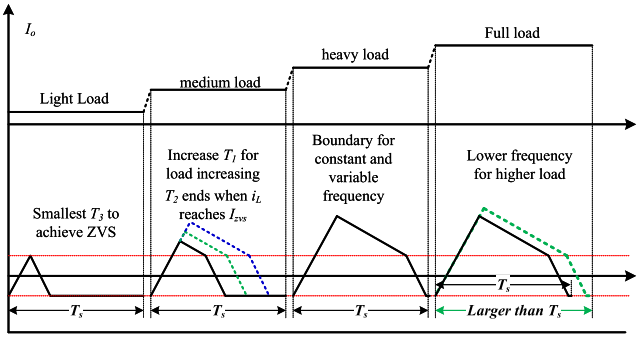

Fig. 12. Waveform of inductor current from light load to full load at Boost mode.

Consequently, there is a positive correlation between V_{err} and I_o. Therefore, the sampling method to obtain the information of I_o in this article is also lossless.

In summary, we adopt a variety of method to avoid all of the current sampling losses in this article, which is one of our contributions compared to all previous works.

IV. Optimal Control to Achieve the Lowest Conduction Loss and Seamless Transient

A. Optimal Current Waveforms for Buck and Boost Modes

In conventional control methodologies, regulation are typically executed on parameters such as the duty cycle, phase shift, or switching frequency. For the quadrilateral control method, the duration of four operational phases, designated as T_1, T_2, T_3, and T_4 are modulated to realize the voltage regulation and the inductor current sculpt.

Research detailed in [27] establishes a correlation between the losses and T_1, indicating that losses are proportional to the duration of T_1. The minimum duration of T_1 that satisfies the conditions for ZVS ensures minimal losses. Fig. 10 illustrates a comparative analysis of different T_1 under identical operational conditions, where the shaded areas represent the energy conveyed in one switching period. Although the areas shaded in blue and red are equivalent, their geometric forms and RMS values of $i_L$differ. The blue one exhibits a high and narrow profile of the inductor current (T_2/T_1 is small), whereas the red one is low and wide (T_2/T_1 is large). Despite transferring equivalent energy, the red one yields a significantly reduced effective current and, correspondingly, lower losses. The key for the minimum RMS current is to keep the coefficient $k = T_2/T_1$ is as large as possible under the ZVS conditions.

According to the analysis above, the current waveforms with the minimum RMS current when $V_{\text{in}} > V_{\text{out}}$ and $V_{\text{in}} < V_{\text{out}}$ are, respectively, shown in Figs. 11 and 12.

Fig. 11 illustrates the trend of optimal inductor current under different loads when $V_{\text{in}} < V_{\text{out}}$. T_1 keeps a constant value at different loads to achieve ZVS, which is marked as red dash line. T_2 is modulated with the load. As the load current increases, T_2 proportionately extends to accommodate the increased output power, which is illustrated as the curve from black line, to green and blue dash lines under medium load conditions. During the T_3 phase, the inductor current $i_L$is reverted to a negative value to achieve ZVS for Q_4 and Q_1.

When $T_1 + T_2 + T_3$ is smaller than the pre-established period T_s, an appropriate T_4 will be inserted to preserve a constant switching period. Conversely, if $T_1 + T_2 + T_3$ is larger than T_s, the subsequent cycle commences forthwith, and the switching period equals to $T_1 + T_2 + T_3$. The boundary between fixed switching frequency and variable switching frequency is reached when $T_1 + T_2 + T_3$ aligns with T_s. If the load continues to increase, $T_1 + T_2 + T_3$ will exceed T_s, propelling the FSBB converter into variable frequency mode, transitioning from the black solid line to the green dash line.

Assuming that the resonance of the inductor L, the junction capacitance C_{oss} and the parallel external capacitor C_{EX} is completed within the dead time, the initial value of Phase 1 and the final value of Phase 3 is almost 0. Then, the duration of T_1 and T_3 should satisfy the following:

$$\begin{cases} T_1 \geq \frac{I_{\text{ZVS}} L}{V_{in}} \\ T_3 \geq \frac{I_{\text{ZVS}} L}{V_{\text{out}}}. \end{cases} \tag{20}$$

In accordance with the delineation aforementioned, the mathematical expressions for the four control variables are outlined as follows:

$$\begin{cases} T_1 = \frac{I_{\text{ZVS}} L}{V_{\text{in}}} \\ T_2 = f\left(V_{\text{in}}, I_o\right) \\ T_3 = \frac{V_{\text{in}}(T_1+T_2)}{V_{\text{out}}} - T_2 \\ T_4 = \max\left(T_s - T_1 - T_2 - T_3, 0\right). \end{cases} \tag{21}$$

As shown in Fig. 12, due to the continuous decline of the inductor current during Phase T_2 in Boost mode, T_3 must be larger than a certain value to ensure that I_B is sufficient to achieve the ZVS of Q_2. As the load increases, T_1 extends proportionately to accommodate the increased output power, as illustrated by the waveform in medium load, transitioning from the black solid line to the green dashed line and then to the blue dashed line. T_2 is controlled through a current sensing circuit, which is terminated once the inductor current reaches I_{ZVS}. The setups for phase T_3 and T_4 are similar to that in Buck mode. Based on the descriptions above, the expressions for the four control variables are as follows:

$$\begin{cases} T_1 = g\left(V_{\text{in}}, I_o\right) \\ T_2 = \frac{V_{\text{in}} T_1 - I_{\text{ZVS}} L}{V_{\text{out}} - V_{\text{in}}} \\ T_3 = \frac{I_{\text{ZVS}} L}{V_{\text{out}}} \\ T_4 = \max\left(T_s - T_1 - T_2 - T_3, 0\right). \end{cases} \tag{22}$$

In summary, T_1 is maintained a fixed minimum value in Buck mode, while T_3 is held constant at a minimal value in Boost mode. In both modes, the "height" of the inductor current is limited to a small value, the "width" of the inductor current is regulated to accommodate the output power. This control strategy can guarantee the maximum ratio T_2/T_1 under various load conditions, improving the efficiency.

B. Closed-Loop Regulation and the Seamless Switching Between Buck and Boost Mode

Based on the analysis in Section III, there is a positive correlation between the signal V_{err} of the outer voltage loop and I_o. As shown in (21) and (22), T_1 and T_2 are proportional to the output current I_o. Therefore, T_1 and T_2 can be modulated through V_{err}, which can indirectly achieve the desired control effect that T_1 and T_2 controlled by the output current I_o. Meanwhile, T_1 and T_2 are inversely proportional to V_{in}. Therefore, T_1 and T_2 can be represented through the following control expressions:

$$\begin{cases} T_1 = g\left(V_{\text{in}}, I_o\right) = \frac{v_{\text{err}}}{k_1 \cdot V_{\text{in}}} \ldots \text{Boost mode} \\ T_2 = f\left(V_{\text{in}}, I_o\right) = \frac{v_{\text{err}}}{k_2 \cdot V_{\text{in}}} \ldots \text{Buck mode} \end{cases}. \tag{23}$$

From the analysis in Section II, the coefficient $k = T_2/T_1$ should be as large as possible to enhance efficiency. Thus, it is necessary that the ratios of k_1 to k_2 are set sufficiently high.

In Buck mode, T_1 is limited to a fixed value, while in Boost mode, T_3 is limited to a fixed value. Therefore, the control variables T_1 and T_3 between Buck Mode and Boost Mode are discontinuous. When V_{in} is close to V_{out}, direct abrupt switching between the two modes will cause the control variables T_1 and T_3 to change suddenly. Therefore, a transient mode should be inserted between Buck and Boost Mode, so that the monotonic continuous change of the control variables can be achieved during the mode switching process. When V_{in} gradually decreases from larger than V_{out} to near V_{out}, T_1 is no longer limited to the minimum value, but gradually increases to the value related to the load, which is represented in (24). Then, T_2 and T_1 keep a fixed ratio and are adjusted together with the load, that is, entering the transition mode. As V_{in} continues to decrease to the area of $V_{\text{in}} < V_{\text{out}}$, in order to ensure that I_B is larger than I_{ZVS}, the duration of T_2 is no longer regulated by the load, but is regulated by the current sampling circuit, which is represented in (25). At this time, T_3 is limited at the minimum value and FSBB converter enters Boost Mode

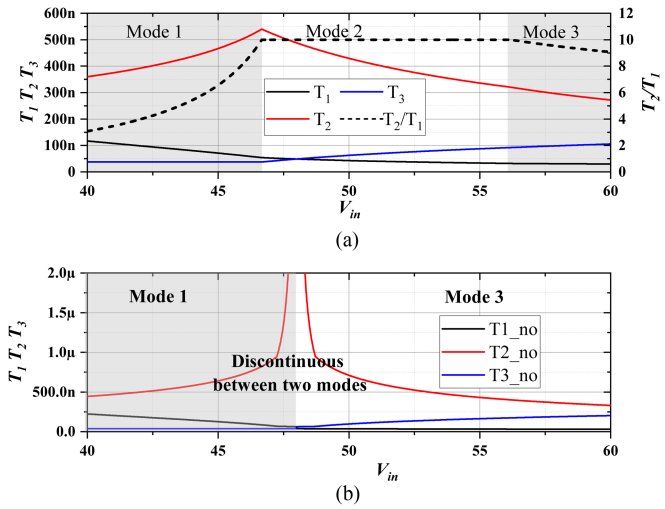

Fig. 13. Change trajectory of the control variable T_1, T_2, and T_3 with the increasing of V_{in}. (a) with transient mode. (b) without transient mode.

$$T_1 = \max\left(\frac{v_{\text{err}}}{k_1 \cdot V_{\text{in}}}, \frac{I_{\text{ZVS}} L}{V_{\text{in}}}\right). \tag{24}$$

$$T_2 = \min\left(\frac{v_{\text{err}}}{k_2 \cdot V_{\text{in}}}, \frac{V_{\text{in}} T_1 - I_{\text{ZVS}} L}{V_o - V_{\text{in}}}\right). \tag{25}$$

Fig. 13 shows the change trajectory of the control variable T_1, T_2, and T_3 with the increasing of V_{in}. There are no sudden changes in the control variables when the transition mode is added. While for the condition without the transition mode, the control variables have a sudden change when V_{in} equals V_{out}.

Based on the equation (24) and (25), the working modes can be divided into three types. The configuration when T_1 equals $I_{\text{zvs}}L/V_{\text{in}}$ and T_2 equals $v_{\text{err}}/(k_2 V_{\text{in}})$, is referred to as Mode 1 (Buck Mode), which corresponds to the condition when $V_{\text{in}} > V_{\text{out}}$. The configuration when T_1 equals $v_{\text{err}}/(k_1 V_{\text{in}})$ and T_2 equals $(V_{\text{in}} T_1 - I_{\text{ZVS}} L)/(V_{\text{out}} - V_{\text{in}})$, is designated as Mode 3 (Boost Mode), relating to the scenario where $V_{\text{in}} < V_{\text{out}}$. These two operational modes can achieve ZVS and the lowest conduction losses when the difference between V_{in} and V_{out} is large.

The mode when T_1 and T_2 equal to $v_{\text{err}}/(k_1 V_{\text{in}})$ and $v_{\text{err}}/(k_2 V_{\text{in}})$ is identified as Mode 2, which acts as a transition mode when V_{in} is close to V_{out}. In this mode, the coefficient $k = T_2/T_1$ can reach k_1/k_2, also enabling high-efficiency power transmission. The values of T_1 and T_2 are seamlessly regulated when the input voltage changes. T_1 gradually increases from $I_{\text{zvs}}L/V_{\text{in}}$ to $v_{\text{err}}/(k_1 V_{\text{in}})$, while T_2 gradually switches from $v_{\text{err}}/(k_2 V_{\text{in}})$ to $(V_{\text{in}} T_1 - I_{\text{ZVS}} L)/(V_{\text{out}} - V_{\text{in}})$, when V_{in} decreases from $V_{\text{in\_max}}$ to $V_{\text{in\_min}}$.

TABLE II
CONTROL EQUATIONS FOR DIFFERENT MODES

	Mode 1	Mode 2	Mode 3
Fixed switching frequency T_s	$\begin{cases} T_1 = \dfrac{I_{\text{ZVS}} L}{V_{\text{in}}} \\ T_2 = \dfrac{v_{\text{err}}}{k_2 V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = T_s - T_1 - T_2 - T_3 \end{cases}$	$\begin{cases} T_1 = \dfrac{v_{\text{err}}}{k_1 V_{\text{in}}} \\ T_2 = \dfrac{v_{\text{err}}}{k_2 V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = T_s - T_1 - T_2 - T_3 \end{cases}$	$\begin{cases} T_1 = \dfrac{v_{\text{err}}}{k_1 V_{\text{in}}} \\ T_2 = \dfrac{V \ T_1 - I_{\text{ZVS}} L}{V_o - V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = T_s - T_1 - T_2 - T_3 \end{cases}$
Variable switching frequency T_1+T_2+T_3	$\begin{cases} T_1 = \dfrac{I_{\text{ZVS}} L}{V_{\text{in}}} \\ T_2 = \dfrac{v_{\text{err}}}{k_2 V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = 0 \end{cases}$	$\begin{cases} T_1 = \dfrac{v_{\text{err}}}{k_1 V_{\text{in}}} \\ T_2 = \dfrac{v_{\text{err}}}{k_2 V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = 0 \end{cases}$	$\begin{cases} T_1 = \dfrac{v_{\text{err}}}{k_1 V_{\text{in}}} \\ T_2 = \dfrac{V_{\text{in}} T_1 - I_{\text{ZVS}} L}{V_o - V_{\text{in}}} \\ T_3 \rightarrow \text{SR} \\ T_4 = 0 \end{cases}$

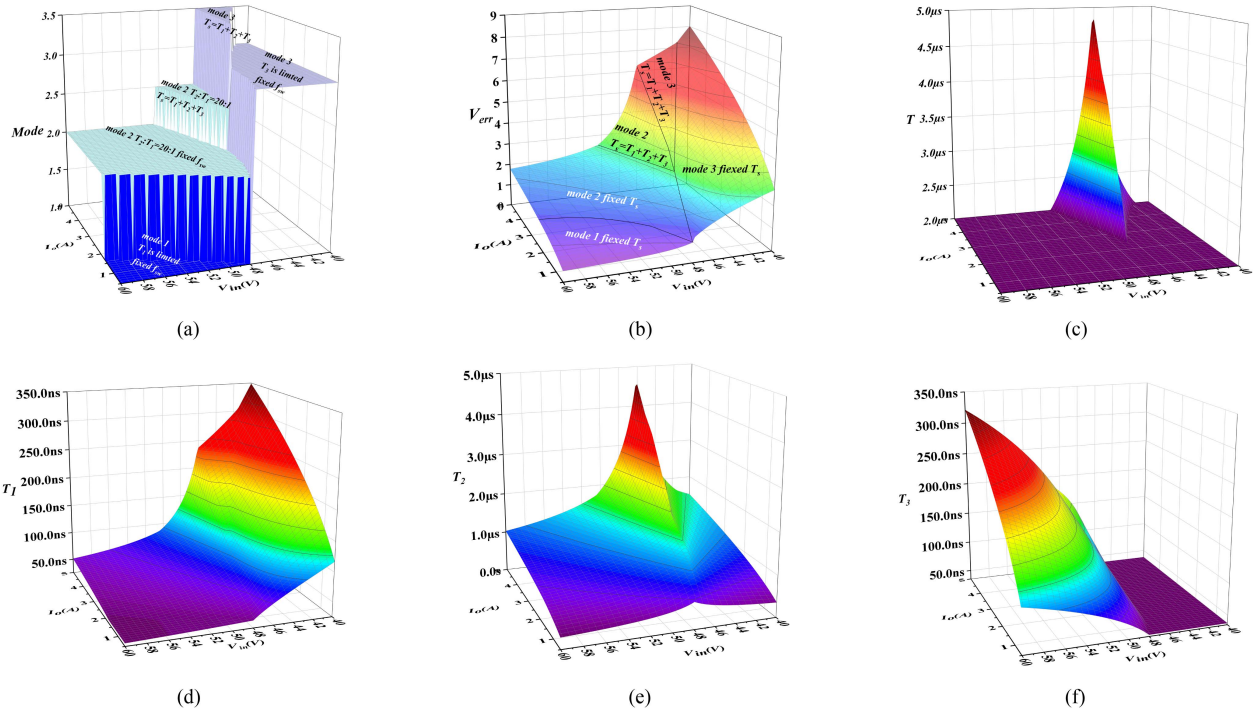

Fig. 14. Modeling of the proposed control method over the whole working conditions: (a) the working modes; (b) the value of v_{err}; (c) the value of T_{sw}; (d) the value of T_1; (e) the value of T_2; (f) the value of T_3.

Moreover, considering the variable frequency mode that occurs when the load increases, the overall control mode can be further subdivided into six types. The corresponding control equations are shown in Table II.

C. Illustrations of the Control Variables Over the Whole Working Conditions

Based on the control equations above, the input voltage range are set to be 40 to 60 V, the output voltage to be 48 V, the maximum load current to be 6 A, the maximum switching frequency to be 500 kHz, the inductor to be 1.2 μH, I_{ZVS} to be 1.5 A, and $k_1 : k_2$ to be 20:1. The distributions of key control parameters such as v_{err}, T_{sw}, T_1, T_2, and T_3 under different working conditions are illustrated in Fig. 14. Fig. 14(a) demonstrates that under conditions of high input voltage and light load, the converter operates in Mode 1 with a minimum constraint on T_1 [shown in Fig. 14(d)]. Under conditions of low input voltage, the converter consistently operates in Mode 3, where T_3 is constrained to a minimum value [shown in Fig. 14(f)]. In conditions where V_{in} is close to V_{out} and the load is heavy, the converter operates in Mode 2, where T_1 and

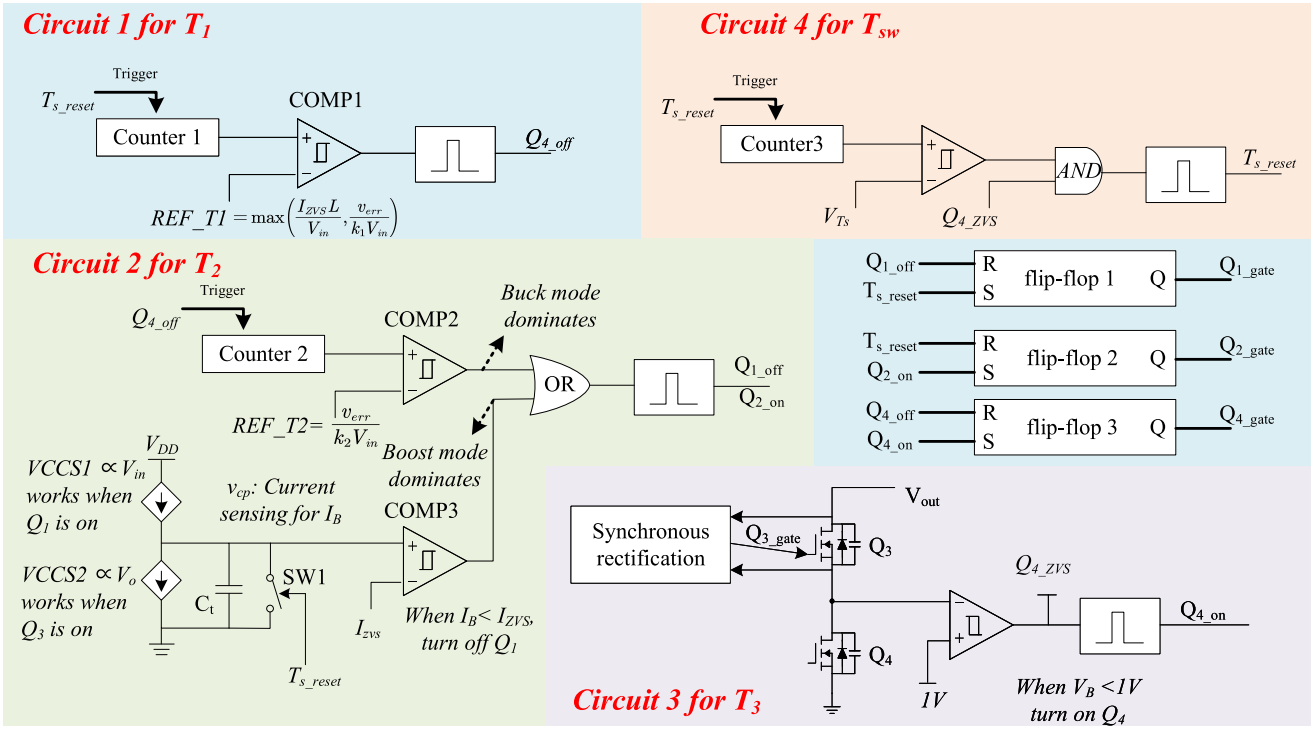

Fig. 15. Circuit diagram of the proposed control method.

TABLE III
TURN-ON AND TURN-OFF POINT OF THE FOUR POWER SWITCHES

	$Q_{1\_on}(Q_{2\_off})$	$Q_{1\_off}(Q_{2\_on})$	Q_3	Q_{4_on}	Q_{4_off}
Circuit in Fig. 15	Circuit 4 for T_{s_rest}	Crcuit 2 for T_2	synchronous rectification	Circuit 3 for T_3	Circuit 1 for T_1

T_2 are adjusted in a predetermined ratio k_1/k_2. With the load increasing, the switching period T_{sw} will increase automatically to meet the output power, which is shown in Fig. 14(c). The boundaries between fixed and variable frequency is smooth. It can be seen that all of the control parameters (T_{sw}, T_1, T_2, and T_3) are seamlessly transitioned with the proposed control method.

V. Implementation of the Proposed Control Strategy

Based on the control logic introduced above, the implementation of the proposed control method is presented in this section. Fig 15 shows the circuits of the proposed control method, which are composed of four parts of subcircuits. The turn-ON and turn-OFF points of the four power switches Q_1, Q_2, Q_3, and Q_4 are shown in the Table III. Q_1 and Q_2 are completely complementary, and an appropriate dead time will be inserted between them. The turn-ON point of Q_1 is realized through *Circuit 4*, and the turn-OFF point of Q_1 is realized through *Circuit 2*. The turn-ON and turn-OFF points of Q_2 are the turn-OFF and turn-ON points of Q_1 plus the preset dead time. The turn-ON and turn-OFF points of Q_3 are achieved through the synchronous rectification circuits. The turn-ON of Q_4 is realized through *Circuit 3*, and the turn-OFF point of Q_4 is realized through *Circuit 1*.

A. Circuits to Regulate the Control Variable T_1

The function of this module is to generate the turn-OFF point of Q_4, that is, to determine the duration of T_1. There is a counter in this module that triggers at the beginning of each switching period. When its count value reaches the reference value REF_T1, a narrow pulse signal Q_{4_off} is generated and transmitted to the RS flip-flop 3, thereby turning OFF Q_4. The period from the start of the cycle T_{s_reset} to the signal Q_{4_off} is the duration of the control variable T_1, which determines the "height" of the inductor current. The duration of T_1 can be adjusted by setting the reference value REF_T1. According to the previous analysis, in Buck mode, the optimal inductor current waveform requires the control variable T_1 to be set to the minimum value that just achieves ZVS. Therefore, in Buck mode, REF_T1 should be set to $I_{ZVS}L/V_{in}$. In Boost mode, the control variable T_1 needs to be adjusted to meet the output power. Therefore, REF_T1 should be set to be $v_{err}/(k_1 V_{in})$, which is the output value of the voltage loop and is proportional to the load current.

B. Circuits to Regulate the Control Variable T_2

The function of this circuit is to generate the turn-OFF point of Q_1, thus determining the duration of T_2. There is also a counter in this part of circuit which is triggered by the signal

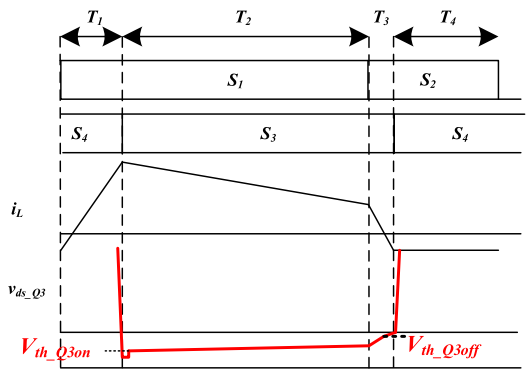

Fig. 16. Waveform of turning-ON and turning-OFF logic for Q_3.

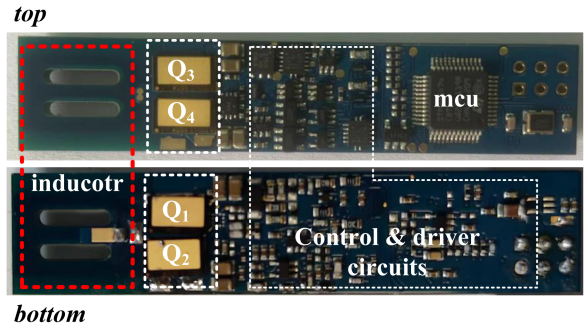

Fig. 17. Designed FSBB prototype.

Q_{4_off}. When the counter's value reaches the reference value REF_$T2 = v_{err}/(k_2 V_{in})$, the output of comparator COMP2 becomes positive. The result will be combined with another signal through an OR gate, and a narrow pulse signal Q_{1_off} will be generated and transmitted to RS flip-flop 1, thus turning off the power transistor Q_1. The two branches of the OR gate dominate under different modes. The counter branch is dominant in Buck mode, where T_1 is fixed and T_2 is regulated with the load to meet the output power. When the load increases, the output voltage V_{out} decreases, leading to an increase in v_{err}, thereby extending the duration of T_2 to satisfy the increasing output power.

Another branch of the OR gate is the dominant factor in Boost mode, where T_1 is proportional to the load and T_2 is limited to ensure that I_B is greater than I_{ZVS} at the end of T_2, thereby achieving the ZVS of Q_2. This operation is consistent with the description of ensuring the minimum T_3 in the Boost mode in the previous section, which is beneficial to reducing the "height" of the inductor current and the conduction loss. The lossless current sampling circuit described in Section III is the key to implement this branch. When the sampled V_{Ct} decreases to be REF_IB, the output of comparator COMP3 will be high, triggering the turn-OFF signal of Q_1 through the OR gate.

The function of the current sensing branch is to ensure that I_B is sufficient to achieve the ZVS of Q_2 in Boost mode. Together with the counter branch, it forms the turn-OFF signal for Q_1. In Buck mode, I_B is always greater than I_{ZVS}, and the output of the current sensing branch is always 0. Only when the counter branch reaches v_{err}, Q_1 will be turned OFF. In Boost mode, the current sensing branch will dominate, thus determining the turn-OFF point of Q_1.

C. Circuits to Regulate the Control Variable T_3

Q_3 is controlled by synchronous rectification, where drain-to-source voltage $V_{ds\_Q_3}$ is sampled. As shown in Fig. 16, Q_3 will be turned ON when $V_{ds\_Q_3}$ is lower than the threshold $V_{th\_Q_3 on}$, and turned OFF when it exceeds the threshold $V_{th\_Q_3 off}$. $V_{th\_Q_3 off}$ is always set to be zero, and Q_3 is turned OFF when the inductor current i_L crosses zero. The energy stored in the junction capacitance C_{oss} is resonantly fed back into the inductor, generating a reverse current to provide sufficient energy for achieving ZVS of Q_1 in the next cycle. An external capacitor C_{EX} is parallel to Q_4 to ensure the sufficient energy to achieve ZVS of Q_1 even in Buck mode.

After Q_3 is turned OFF, the switching node voltage V_b of the lagging bridge will gradually decrease from V_{out} to 0. As shown in the *Circuit 3* in Fig. 15, V_b is monitored, and when it falls below 1V, a narrow pulse signal is generated to turn ON Q_4 for achieving ZVS.

D. Circuits to Regulate the Control Variable T_{sw}

The function of this module is to regulate the operating period T_{sw}. There is a counter in this part of circuit which is triggered by the self-generated signal T_{s_reset}. When the count value exceeds V_{ts}, the preset operating cycle T_s is reached. At this point, it is necessary to check whether the signal Q_{4_ZVS} is high. If so, it indicates that i_L has become negative, and then the signal T_{s_reset} is generated to reset the cycle. If the signal Q_{4_ZVS} is still low, it indicates that i_L is still positive, and the signal T_{s_reset} keeps inactive until Q_{4_ZVS} goes high. This situation typically occurs under heavy load conditions when the preset operating period T_s is insufficient to transfer the input power, meaning $T_s < T_1 + T_2 + T_3$. In this case, the operating period T_{sw} will equal to $T_1 + T_2 + T_3$, and the converter will not enter the T_4 stage. This module can achieve the effect that keeping the fixed switching period T_s at the light and medium load and increasing the switching period $T_1 + T_2 + T_3$ at heavy load.

Based on the analysis above, the control logic of the four power switches can be summarized in Table IV.

VI. Experimental Results

To verify the effectiveness of the proposed control circuit and method, a prototype has been built in Fig. 17. The specifications of the prototype are as follows: input voltage $V_{in} = 40V \sim 60V$, output voltage $V_{out} = 48V$, maximum output current $I_o = 6A$, the switching frequency $f_{sw} = 330 \sim 500$ kHz. Table VI shows the specific parameters of the FSBB converter. GaN devices (GS61008T from Gan systems Inc.) are chosen to be the power switches for the high-frequency switching. The half-bridge driver LM5113 from Texas Instruments is chosen for Q_1 and Q_2, while the low-side driver UCC27512 is chosen for Q_4.

TABLE IV
SUMMARY OF THE CONTROL LOGIC OF FOUR POWER SWITCHES IN DIFFERENT WORKING CONDITIONS

Mode	Load	Q_{1_on} (Q_{2_off})	Q_{1_off} (Q_{2_on})	Q_3	Q_{4_on}	Q_{4_off}
Mode 1 ($V_{in} > V_o$)	light load heavy load	T_s $T_1+T_2+T_3$	Circuit 2 $v_{err}/(k_2V_{in})$	synchronous rectification	Circuit 3 for T_3	Circuit 1 $I_{ZVS}\,L/V_{in}$ Circuit 1 $v_{err}/(k_1V_{in})$
Mode 2 ($V_{in} \approx V_o$)	light load heavy load	T_s $T_1+T_2+T_3$	Circuit 2 $v_{err}/(k_2V_{in})$	synchronous rectification	Circuit 3 for T_3	Circuit 1 $v_{err}/(k_1V_{in})$
Mode 3 ($V_{in} < V_o$)	light load heavy load	T_s $T_1+T_2+T_3$	Circuit 2 current sensing branch	synchronous rectification	Circuit 3 for T_3	Circuit 1 $v_{err}/(k_1V_{in})$

TABLE V
COMPARISON WITH EXISTING WORKS

Reference	Year	Input	Output	Power	switching frequency	peak efficiency	implementation	Lossless Current sensing
This paper	2024	40–60 V	48 V	288 W	300–500 kHz (variable)	98.88%	analog circuit	Yes
Previous work [27]	2021	36–72 V	48 V	288 W	1 MHz (constant)	98.1%	3D-LUT	No
NUAA [26], [28]	2022 2024	60–120 V	84 V	420 W	500 kHz (constant)	98.7%	analog circuit	No
ZJU [25], [21]	2019 2022	36–60 V	36-60 V	300 W	700–800 kHz (variable)	98.5%	3D-LUT Simplified calculation	No
Khalifa University [17]	2024	55 V	50 V	275 W	100 kHz (constant)	98.06%	complex floating calculation	No
HIT [24]	2023	40–60 V	48 V	200 W	0.590–1.25 MHz (variable)	98.3%	analog circuit	No

TABLE VI
DESIGN SPECIFICATION OF THE FSBB PROTOTYPE

Components	Parameters
Switches S_1-S_4	GaN System GS61008T 100V, 90A R_{dson}=10mΩ
Switching Frequency f_{sw}	300-500kHz
Inductor L	EQ_25-3F36 ferrite core; L_m= 1.2μH, 2Oz;
Gate Driver	LM5113 for Q_1 & Q_2 NCP4306 for Q_3 UCC27512 for Q_4
Current sensing circuits	opAMP: AD8061 PNP:BCM857 NPN:BMC847 Ct=10pF
Voltage loop opAMP	AD8565
Microcontroller	STM32G474
Size	3.93*0.53*0.43 in^3
Power Density	218.8W/in^3

NCP4306 is chosen for Q_3 to achieve synchronous rectification. Ferrite core material 3F36 from Ferroxcube is selected for inductor due to its performance for high-frequency applications. Planar cores are selected for the consideration of high power density. STM32G474 from ST Corporation is selected as the microcontroller due to its integrated high-resolution PWM generator.

Table V compares the existing work on quadrilateral control scheme for FSBB converter. The proposed scheme realizes the variable frequency control through analog circuits, while completely eliminating the current sampling loss and achieving high efficiency.

Fig. 18 shows the main waveforms of FSBB converter under different working conditions. It can be seen that the negative current keeps the fixed value no matter the operating conditions. Meanwhile, the output voltage can always be maintained at 48 V in the wide input range. Both the pulse widths of V_A and V_B are gradually increasing when the load steps up, which means that the energy transferring proportion is increasing. When $V_{in} = 40$V, the converter works in Mode 3. The length of T_1 increases with the load, and I_B is maintained to be I_{ZVS} through the regulation of current sensing circuits. At this time, the length of T_3 can always be maintained at a fixed minimum value. When $V_{in} = 60$V, the converter works in Mode 1. The length of T_1 always keeps a fixed minimum value, and I_A is maintained to be I_{ZVS}. The length of T_2 increases with the load, and the length of T_3 ensures that i_L will be reset to 0. When $V_{in} = 48$V, the converter works in Mode 3 under light load conditions to ensure that the values of I_A and I_B are greater than I_{ZVS}. When the load increases, the converter works in Mode 2, T_2 and T_1 increase with a fixed ratio of 20:1, and T_1 and T_3 no longer maintain the minimum value.

Fig. 19 shows the waveforms of the current sensing circuits in different modes, where the green line represents the inductor current i_L and the blue line represents the voltage V_{Ct} on the sampling capacitor. It can be seen that V_{Ct} is consistent with the inductor current i_L under different working conditions. The

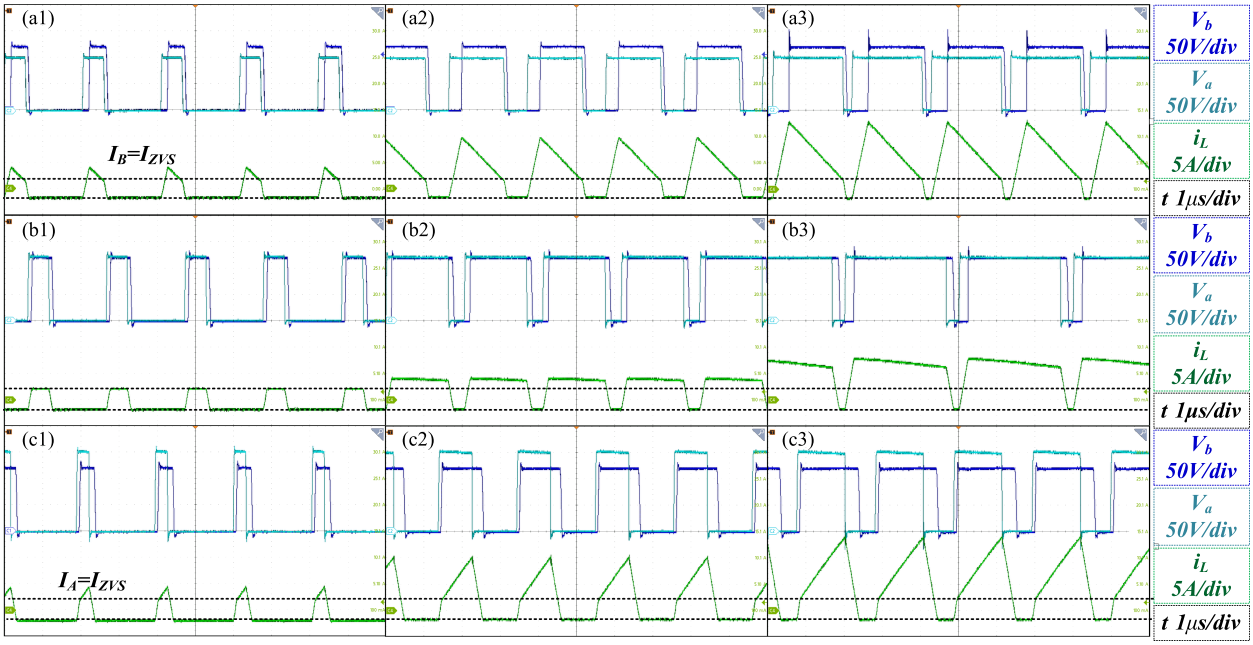

Fig. 18. Main waveforms of the proposed control method under (a.1) $V_{\text{in}} = 40$ V $I_o = 0.5$ A; (a.2) $V_{\text{in}} = 40$ V $I_o = 3$ A; (a.3) $V_{\text{in}} = 40$ V $I_o = 6$ A; (b.1) $V_{\text{in}} = 48$ V $I_o = 0.5$ A; (b.2) $V_{\text{in}} = 48$ V $I_o = 3$ A; (b.3) $V_{\text{in}} = 48$ V $I_o = 6$ A; (c.1) $V_{\text{in}} = 60$ V $I_o = 0.5$ A; (c.2) $V_{\text{in}} = 60$ V $I_o = 3$ A; (c.3) $V_{\text{in}} = 60$ V $I_o = 6$ A.

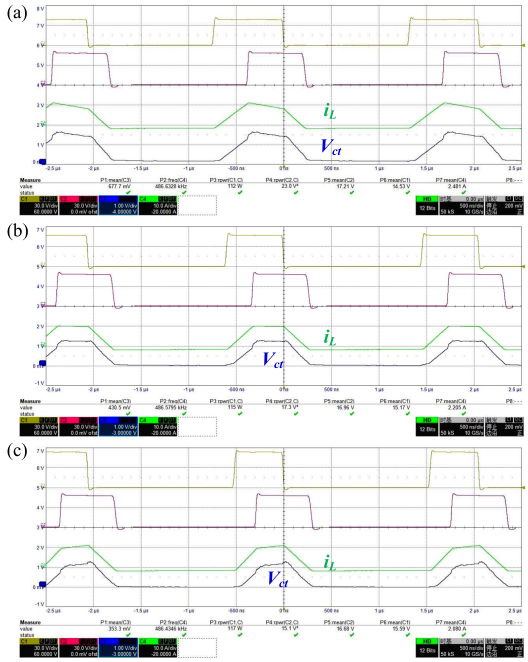

Fig. 19. Current sampling waveforms under (a) $V_{\text{in}} < V_{\text{out}}$; (b) $V_{\text{in}} = V_{\text{out}}$; (c) $V_{\text{in}} > V_{\text{out}}$.

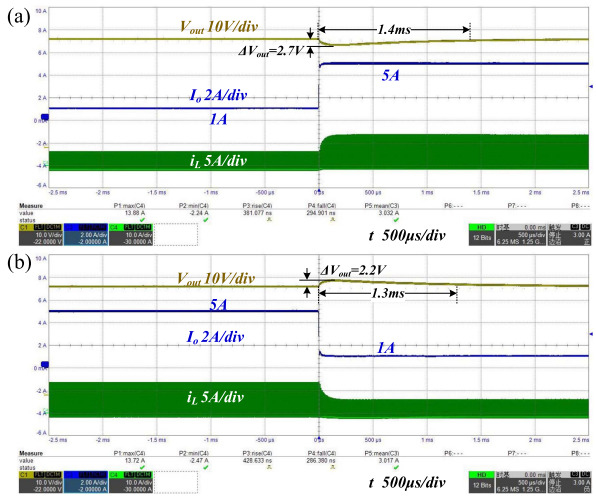

Fig. 20. Waveforms of load transient process: (a) load step up from 1 to 5A; (b) load step down from 5 to 1A.

inductor current i_L can be indirectly represented by V_{Ct}, thereby realizing the regulation of the inflection point I_B of the inductor current.

Fig. 20 shows the dynamic responses of the FSBB converter with 60 V input as load steps up and down between 1 and 5 A. When a step load variation occurs, the control loop responses immediately, then the signal v_{err} changes with load and the output voltage v_{out} will be tightly regulated to 48 V. The output voltage undershoot and overshoot are 2.7 and 2.2 V, which is less than 6%*V_{out}. The settling times of the step up and down process are 1.4 and 1.3 ms, respectively.

Fig. 21 shows the measured efficiency curves of the proposed control method for FSBB converter at the different line and load conditions. The peak efficiency is 98.88% at 48 V input 3.5 A load, while the full-load efficiency at the nominal input voltage is 98.14%. The loss distribution under the 4 A load is shown in Fig. 22. The method for loss analysis is from [27]. The reasons of

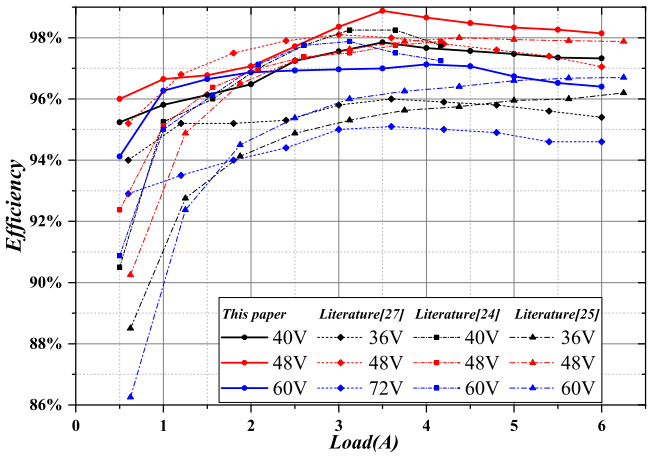

Fig. 21. Comparison of the efficiency curves between the proposed control method and the existing works.

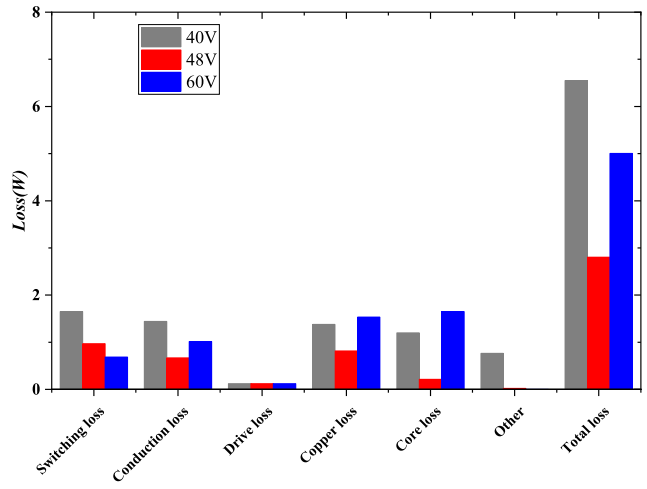

Fig. 22. Loss distribution under the load of 4 A.

the FSBB converter with the proposed control method to achieve high efficiency are analyzed as follows. First, the height of i_L (T_1 for Buck mode and T_3 for Boost mode) is regulated to be as small as possible to realize both ZVS and the lowest RMS current. Thus, both conduction loss and copper loss are reduced. Second, the current sensing circuits is lossless and the sensing loss is almost eliminated.

VII. Conclusion

In this article, a high-efficiency control strategy with lossless current sensing and seamless transition is proposed for FSBB converter. The benefits of the proposed control strategy are as follows. 1) The current sensing loss can be eliminated due to the proposed volt–second sensing circuits. 2) The conduction loss over the whole operating conditions is reduced due to the geometry of i_L is optimized. 3) A seamless switching between different input voltages and loads is achieved. Finally, a prototype with input voltage of 40–60V and output parameters of 48V/6A is built to verify the effectiveness of the proposed sampling circuit and control strategy. The peak efficiency is 98.88%, while the full-load efficiency at the nominal input voltage is 98.14%.

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