A Generalized Multi-Loop Controller With Enhanced Robustness and Its Design Guideline

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***Abstract*—Feedback control is ubiquitous in engineering applications and is a powerful tool to achieve automatic regulation of the outputs of a system. Existing closed-loop control methods typically employ a single feedback loop to regulate each output. This article proposes a new generalized multiloop control structure, which utilizes more than one feedback loops to control one output. The control performance of an existing single-loop controller can be boosted by closing extra feedback loops outside the original loop. The main advantage of the multiloop structure is enhanced robustness without necessarily sacrificing the stability and dynamics of the original control system. The proposed multiloop structure is a general control technique that can potentially be combined with any existing control methods. A straightforward design guideline for minimum-phase systems is provided to implement the multiloop controller and determine the control parameters. The proposed idea is illustrated with a power-factor-correction circuit and is validated in simulation and experiments.**

***Index Terms*—Additional feedback loops, disturbance rejection, double-loop, multiloop, robust control, triple-loop.**

I. Introduction

FEEDBACK control is a powerful tool to achieve automatic regulation of a system. Since the publication of a rigorous mathematical analysis by Maxwell, the theory of automatic control has advanced substantially [1]. Nowadays, feedback control has become ubiquitous and is applied widely in various engineering applications. In the field of power electronics, feedback control is commonly utilized to regulate the current and voltage in power converters for achieving accurate power conversion [2], [3], [4]. The most dominant category of control methods is linear control due to its simplicity, low cost, and long-established application [5]. Nonlinear control methods such as sliding mode control [6], model predictive control [7], and fuzzy logic control [8] have also been developed to improve the performance of the control system and have found increasing application in power electronics.

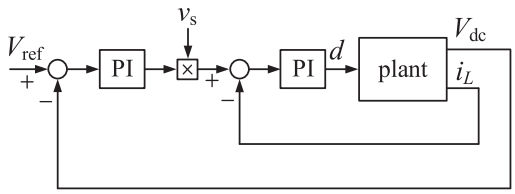

Fig. 1. Controller of the PFC circuit [11].

Regarding the control structure, existing control methods, including both linear and nonlinear methods, typically employ a single feedback loop to regulate each output of the control system [9]. This single-loop structure closes the loop by feeding back the measured output, comparing it with a reference signal, and amplifying the error with a regulator to control the plant. It should be noted that a controller that contains multiple feedback loops is not unusual. Some examples are current-mode control of a dc–dc converter [10], dc-link voltage control of a power-factor-correction (PFC) circuit [11], and position control of an electrical motor [12]. Despite the existence of multiple feedback loops, these loops are utilized to control different outputs. For instance, the controller for the PFC circuit in [11] is shown in Fig. 1. There are two feedback loops in the controller, arranged in a nested configuration. The inner loop controls the inductor current while the outer loop regulates the dc-link voltage. As each output is controlled by only one feedback loop, this controller is still categorized as a single-loop controller for each control objective in this article.

There are limited reports of using multiple feedback loops for regulating the same output. One example of multiloop controllers in the literature is the series-feedback compensation scheme, as given in Fig. 2(a) [13]. The controller employs two regulators, $H(s)$ in the minor loop and $C(s)$ in the major loop. The purpose of using two regulators is to achieve two degrees of freedom in the control design. However, the properties of the double-loop controller and its design are not explained in [13]. The second example is the internal model control (IMC) based control method, which also adopts two feedback loops, as shown

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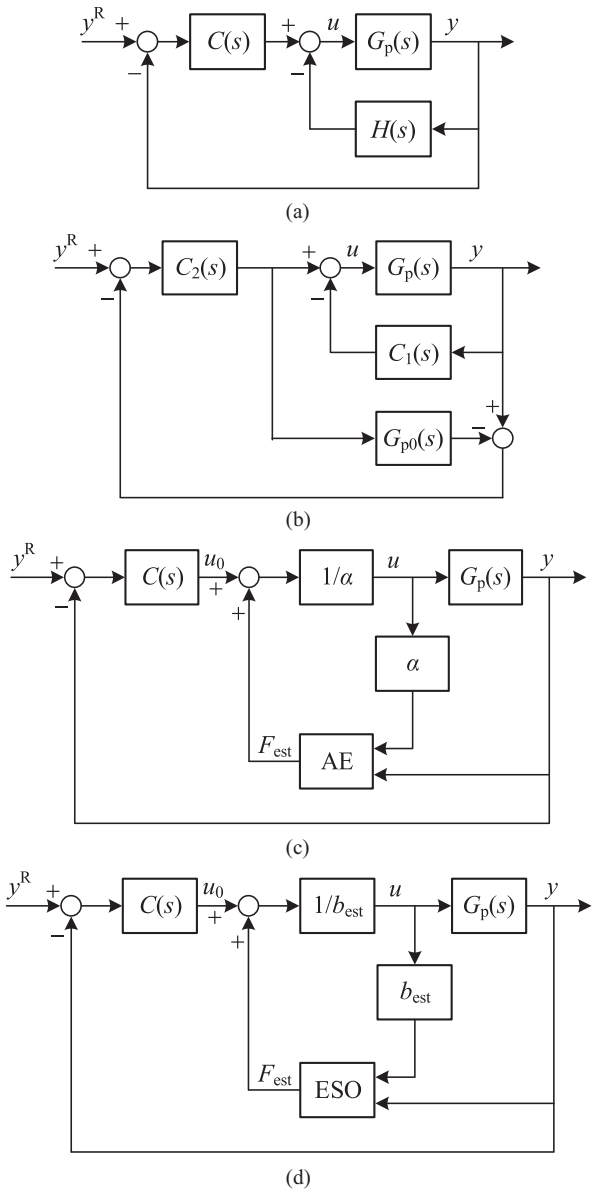

Fig. 2. Reported multiloop control structures. (a) Series-feedback control scheme. (b) IMC-based method, (c) Model-free control. (d) Active disturbance rejection control.

in Fig. 2(b) [14]. The controller is designed specifically for inherently unstable systems, such as continuously stirred tank reactors and bioreactors in chemical industries. The inner-loop regulator $C_1(s)$ stabilizes the plant while the outer-loop regulator $C_2(s)$ achieves reference tracking based on pole-zero placement. The outer loop feeds back any mismatch between estimated plant model and the real plant to improve the control performance.

Another example of using two feedback loops is the method of model-free control (MFC) shown in Fig. 2(c) [15]. The idea of this method is to treat all the unknown or poorly known parts in the plant model as a lumped disturbance to the plant, estimate the disturbance using algebraic estimation (AE), and use this estimate to neutralize the effect of the disturbance in the control. MFC is able to simplify the control design and enhance the performance of the control system. A similar control idea is adopted in active disturbance rejection control (ADRC), where the AE is replaced by an extended state observer (ESO) [16]. Thus, the convergency of the ESO must be ensured in the design process. The control structure of ADRC is displayed in Fig. 2(d). Similar to MFC, a double-loop structure can also be observed in ADRC. The inner loop is responsible for estimating the lumped disturbance, and the outer loop is for set point tracking.

Compared to the single-loop structure, control structures with more than one feedback loops have limited application and still lack a thorough investigation. Moreover, existing double-loop structures are the result of rational design of advanced control algorithms for improving the control performance and are not designed on purpose. It is revealed in [17] that a more essential reason for the robustness improvement of MFC is the adoption of the double-loop structure. Nonetheless, the design of control parameters is not presented. This article directly studies the effect of multiloop structures on the control performance and discusses the design of control parameters, which, to the best knowledge of the authors, are not reported in the literature. It is an extended version of a short conference paper [18]. Unlike [18], this article: generalizes the multiloop control structure from two loops to an arbitrary number of loops; introduces a more comprehensive analysis of the generalized multiloop control structure; and sets up a straightforward design guideline for minimum-phase systems to implement the multiloop controller and determine the control parameters. It is also discovered that adding extra feedback loops does not necessarily sacrifice the stability and dynamics of the original control system.

The rest of this article is organized as follows. Section II compares the characteristics of the single-loop and multiloop control structures. Section III discusses the design of the multiloop controller. A simple implementation of the multiloop controller based on proportional-integral (PI) control is also introduced. Section IV illustrates the proposed control idea with a PFC circuit. A double-loop controller and a triple-loop controller are designed for both input current control and output voltage control. Section V presents simulation and experimental verification. Finally, Section VI concludes this article.

II. Comparison of Different Control Structures

A. Conventional Structure With a Single Feedback Loop

The conventional control structure is explained using a typical linear single-input single-output system, which is described by the following model:

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{b}u + \mathbf{w} \\ y = \mathbf{c}^{\mathrm{T}}\mathbf{x} \end{cases}. \tag{1}$$

Here, $\mathbf{x}$, u, and y represent the states, control input, and control output of the system. $\mathbf{w}$ stands for external disturbances. $\mathbf{A}$, $\mathbf{b}$, and $\mathbf{c}$ are coefficient matrix and vectors.

The transfer function of the plant in the control system can be derived as

$$G_{\mathrm{p}}(s) = \mathbf{c}^{\mathrm{T}}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b}. \tag{2}$$

Based on $G_p(s)$, a feedback controller $C_1(s)$ can be designed. The block diagram of the closed-loop system is displayed in

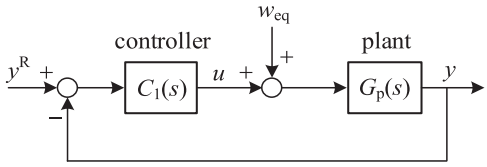

Fig. 3. Conventional controller structure with a single feedback loop.

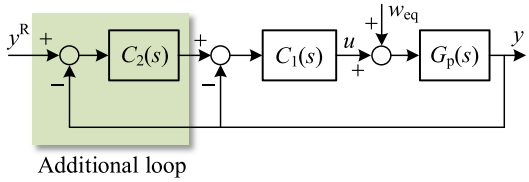

Fig. 4. Proposed control structure with two feedback loops.

Fig. 3, in which y^R is the reference for y, and w_{eq} denotes the equivalent disturbance expressed by

$$w_{\text{eq}} = \mathbf{c}^T(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{w}. \tag{3}$$

It is obvious that Fig. 3 exhibits a control structure with a single feedback loop.

It is well recognized that the inclusion of a feedback loop in the control system can effectively achieve accurate reference tracking and disturbance suppression [19]. In the frequency domain, the output of the closed-loop system can be derived as

$$Y(s) = G_{\text{RT1}}(s)Y^R(s) + G_{w1}(s)W_{\text{eq}}(s) \tag{4}$$

where

$$G_{\text{RT1}}(s) = \frac{L_1(s)}{1 + L_1(s)} \tag{5}$$

$$G_{w1}(s) = \frac{G_p(s)}{1 + L_1(s)} \tag{6}$$

$$L_1(s) = C_1(s)G_p(s) \tag{7}$$

where $Y^R(s)$ and $W_{eq}(s)$ are the Laplace transforms of y^R and w_{eq}, respectively. $G_{\text{RT1}}(s)$ and $G_{w1}(s)$ represent the reference tracking gain and disturbance gain of the closed-loop control system, respectively. $L_1(s)$ is the loop gain.

$C_1(s)$ typically has a large gain within the control bandwidth, producing a large $L_1(s)$. As a result, it can be inferred from (5) that $|G_{\text{RT1}}(s)| \approx 1$, which indicates effective reference tracking. Moreover, the feedback loop also reduces the disturbance gain by a factor of $1/(1+L_1(s))$ according to (6), mitigating the influence of the disturbances. Nonetheless, the requirement for stability limits the gain of $C_1(s)$ and thus leads to constrained disturbance rejection capability.

B. Proposed Structure With Multiple Feedback Loops

A new control structure with multiple feedback loops is proposed. First, a double-loop control system is shown in Fig. 4. Opposed to the single-loop structure in Fig. 3, the new double-loop structure feeds back the control output a second time via an additional loop. $C_2(s)$ is the controller employed to regulate the outer loop.

The characteristics of the double-loop control system can be analyzed using transfer functions. The reference-tracking gain of the system can be derived as

$$G_{\text{RT2}}(s) = \frac{L_2(s)}{1 + L_2(s)} \tag{8}$$

where

$$L_2(s) = C_2(s)G_{\text{RT1}}(s). \tag{9}$$

Equations (8) and (9) have similar forms to those of (5) and (7), with $C_2(s)$ substituting for $C_1(s)$ and $G_{\text{RT1}}(s)$ replacing $G_p(s)$. Therefore, $C_2(s)$ can be designed in a similar fashion to $C_1(s)$. Good reference-tracking performance can be achieved with a large $L_2(s)$.

The disturbance gain of the double-loop controller can be derived as

$$G_{w2}(s) = \frac{G_p(s)}{(1 + L_1(s))(1 + L_2(s))} = \frac{1}{1 + L_2(s)}G_{w1}(s). \tag{10}$$

Within the control bandwidth, $L_2(s)$ has a large gain. It means that the additional loop reduces the disturbance gain by a factor of $1/(1+L_2(s))$, further enhancing the disturbance rejection capability of the system on top of the inner loop.

The double-loop structure can be generalized to the structure with n feedback loops, as shown in Fig. 5. $C_n(s)$ is the controller to regulate the nth feedback loop. The reference-tracking gain and disturbance gain of the control system become

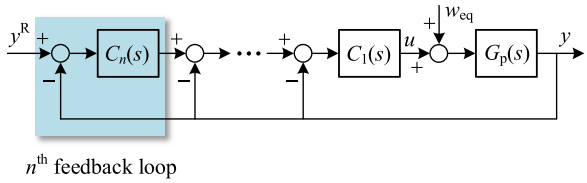

Fig. 5. Generalized control structure with n feedback loops.

$$G_{\text{RT}n}(s) = \frac{L_n(s)}{1 + L_n(s)} \tag{11}$$

$$G_{wn}(s) = \frac{1}{1 + L_n(s)}G_{w(n-1)}(s) \tag{12}$$

where

$$L_n(s) = C_n(s)G_{\text{RT}(n-1)}(s). \tag{13}$$

$C_n(s)$ should be designed according to $G_{\text{RT(n-1)}}(s)$ to achieve accurate reference tracking. In the meantime, the stability of the control system should be considered.

It can be derived from (12) that

$$G_{wn}(s) = G_p(s)\prod_{i=1}^{n}\frac{1}{1 + L_i(s)}. \tag{14}$$

It means that each additional feedback loop imposes a positive effect on disturbance rejection. This equation highlights the main advantage of the multiloop control structure.

III. Design Guideline for the Multiloop Controller

The key to designing the multiloop controller in Fig. 5 lies in the design of $C_1(s)$, $C_2(s)$, …, $C_n(s)$. As the control theory for single-loop systems has been well established, it is reasonable to assume a well-designed $C_1(s)$ that achieves stability and sufficient dynamics for the innermost loop comprised of $C_1(s)$ and $G_p(s)$. Then, the design problem becomes how to sequentially close additional loops to preserve the stability and dynamic performance of the whole control system. The method to design $C_2(s)$ in the double-loop controller will first be elaborated, followed by the discussion of the multiloop structure.

A. Design of C_2(s) in the Double-Loop Controller

For existing controllers with two nested feedback loops, the outer loop is typically designed to be much slower than the inner loop to simplify the design process. This approach is reasonable if each loop controls a different output and each output has a different requirement of the dynamics. However, it is not preferred for the double-loop controller, in which the two loops are controlling the same output. This is because the gain of enhanced robustness can be defeated by the significant compromise of control bandwidth. Thus, the objective of the following discussion is to add the outer loop without sacrificing stability and control bandwidth of the system. For simplicity, the studied plant is assumed to have minimum phase.

First, the bandwidth of the control system, which is indicated by the gain crossover frequency [20], is designed. By definition, $|L_1(j\omega_{gc1})| = 1$ with ω_{gc1} being the gain crossover frequency of the inner loop. According to (5) and (9)

$$|G_{\mathrm{RT1}}(j\omega_{\mathrm{gc1}})| = \frac{|L_1(j\omega_{\mathrm{gc1}})|}{|1+L_1(j\omega_{\mathrm{gc1}})|} = \frac{1}{|1+L_1(j\omega_{\mathrm{gc1}})|} \tag{15}$$

$$|L_2(j\omega_{\mathrm{gc1}})| = \frac{|C_2(j\omega_{\mathrm{gc1}})|}{|1+L_1(j\omega_{\mathrm{gc1}})|}. \tag{16}$$

To maintain the control bandwidth, i.e., $\omega_{\mathrm{gc2}} = \omega_{\mathrm{gc1}}$, the loop gain of the outer loop should satisfy $|L_2(j\omega_{\mathrm{gc1}})| = 1$. Substituting it into (16) gives

$$|C_2(j\omega_{\mathrm{gc1}})| = |1+L_1(j\omega_{\mathrm{gc1}})|. \tag{17}$$

It provides the requirement for $C_2(s)$ to keep the bandwidth of the double-loop system unchanged.

Next, the stability of the double-loop system is considered. In particular, the phase margin and gain margin, which are the key indicators of the system's stability, are analyzed. According to [20], a well-designed control system should achieve a phase margin of at least 30° and a gain margin of at least 6 dB. Here, it is assumed that $C_1(s)$ achieves

$$\gamma_1 \geq 30^\circ \tag{18}$$

$$K_{g1}\mathrm{dB} \geq 6\mathrm{dB}\,(\mathrm{or}K_{g1} \geq 2) \tag{19}$$

where γ_1 and K_{g1} are the phase margin and gain margin of the inner loop, respectively. γ_1 corresponds to the gain crossover frequency ω_{gc1} while K_{g1} corresponds to the phase crossover frequency ω_{pc1}. γ_1 and K_{g1} are expressed by

$$\gamma_1 = \angle L_1(j\omega_{\mathrm{gc1}}) + 180^\circ \tag{20}$$

$$K_{g1} = \frac{1}{|L_1(j\omega_{\mathrm{pc1}})|}. \tag{21}$$

It can be obtained from (5) and (9) that

$$\angle L_2\left(j\omega_{\mathrm{gc2}}\right) = \angle C_2\left(j\omega_{\mathrm{gc1}}\right) + \frac{1}{2}\angle L_1\left(j\omega_{\mathrm{gc1}}\right). \tag{22}$$

The phase margin of the outer loop is expressed by

$$\gamma_2 = \angle L_2\left(j\omega_{\mathrm{gc2}}\right) + 180^\circ. \tag{23}$$

Substituting (20) and (23) into (22) gives

$$\gamma_2 = \frac{1}{2}\gamma_1 + \angle C_2\left(j\omega_{\mathrm{gc1}}\right) + 90^\circ. \tag{24}$$

To meet the requirement on the phase margin, i.e., $\gamma_2 \geq 30^\circ$, $C_2(s)$ should satisfy

$$\angle C_2\left(j\omega_{\mathrm{gc1}}\right) \geq -\frac{1}{2}\gamma_1 - 60^\circ. \tag{25}$$

The gain margin of the outer loop K_{g2} is calculated by

$$K_{g2} = \frac{1}{|L_2(j\omega_{\mathrm{pc2}})|} = \frac{|1+L_1(j\omega_{\mathrm{pc2}})|}{|C_2(j\omega_{\mathrm{pc2}})|\,|L_1(j\omega_{\mathrm{pc2}})|} \tag{26}$$

where ω_{pc2} is the phase crossover frequency of the outer loop. To achieve $K_{g2} \geq 2$, it can be derived from (26) that

$$|C_2(j\omega_{\mathrm{pc2}})| \leq \frac{|1+L_1(j\omega_{\mathrm{pc2}})|}{2\,|L_1(j\omega_{\mathrm{pc2}})|}. \tag{27}$$

$C_2(s)$ should be designed based on (17), (25), and (27). If such a controller is found, the double-loop system will preserve both the stability and dynamics of the original single-loop system while enhanced robustness can be achieved. Otherwise, it means that the requirements on the stability margins cannot be fulfilled, and the gain of $C_2(s)$ should be reduced to boost the stability at the cost of slowed dynamics.

B. A Simple Implementation of C_2(s)

Although various control methods can be adopted to implement $C_2(s)$ in the double-loop controller, PI control is also a feasible alternative. Here, a simple implementation of $C_2(s)$ based on PI control is introduced to show the concept. A PI control-based $C_2(s)$ is expressed by

$$C_2(s) = \frac{k_{p2}(s+\omega_2)}{s} \tag{28}$$

where k_{p2} and ω_2 are the two parameters with design freedom. The magnitude and phase of $C_2(s)$ are

$$|C_2(j\omega)| = k_{p2}\sqrt{1+\frac{\omega_2^2}{\omega^2}} \tag{29}$$

$$\angle C_2(j\omega) = \arctan\left(\frac{\omega}{\omega_2}\right) - 90^\circ. \tag{30}$$

If the parameters of $C_2(s)$ are designed as

$$\begin{cases} k_{p2} = \frac{1}{2}\left|1+L_1\left(j\omega_{\mathrm{gc1}}\right)\right| = \sin\left(\frac{\gamma_1}{2}\right) \\ \omega_2 = \sqrt{3}\omega_{\mathrm{gc1}} \end{cases}. \tag{31}$$

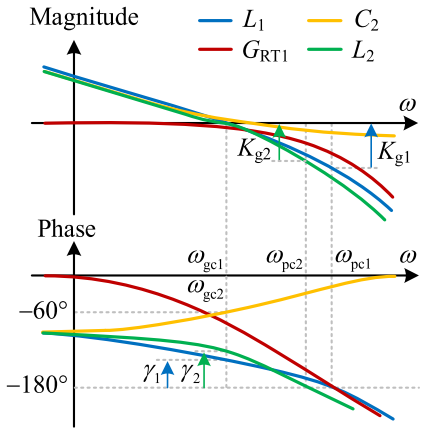

Fig. 6. Bode plots of L_1, G_{RT1}, C_2, and L_2.

It can be shown that $|C_2(j\omega_{\mathrm{gc1}})| = |1 + L_1(j\omega_{\mathrm{gc1}})|$ and $\angle C_2(j\omega_{\mathrm{gc1}}) = -60°$, and (17) and (25) are met. It means the two loops have identical bandwidths and that the phase margin of the double-loop system is sufficient.

Nonetheless, the gain margin of the system still needs to be checked. Although it is difficult to obtain an explicit condition showing when k_{p2} and ω_2 in (31) can satisfy (27) without specific knowledge of $L_1(s)$, a conservative estimation is provided below. For ease of understanding, the bode plots of L_1, G_{RT1}, C_2, and L_2 are sketched in Fig. 6.

At $\omega = \omega_{\mathrm{pc1}}$, one has $L_1(j\omega_{\mathrm{pc1}}) = -|L_1(j\omega_{\mathrm{pc1}})|$. Thus, the magnitude and phase of $L_2(j\omega)$ are

$$|L_2(j\omega_{\mathrm{pc1}})| = \frac{|C_2(j\omega_{\mathrm{pc1}})|\,|L_1(j\omega_{\mathrm{pc1}})|}{|1 + L_1(j\omega_{\mathrm{pc1}})|} = \frac{|C_2(j\omega_{\mathrm{pc1}})|}{K_{g1} - 1} \tag{32}$$

$$\angle L_2(j\omega_{\mathrm{pc1}}) = \angle C_2(j\omega_{\mathrm{pc1}}) - 180°. \tag{33}$$

Given a sufficient phase margin, ω_{pc1} is generally much higher than ω_{gc1}. It can be inferred that $\angle C_2(j\omega_{\mathrm{pc1}})$ is much larger than $\angle C_2(j\omega_{\mathrm{gc1}}) = -60°$ and thus $\angle L_2(j\omega_{\mathrm{pc1}})$ is close to –180°. As a result, ω_{pc2} is not distant from ω_{pc1}, and the requirement on $|L_2(j\omega_{\mathrm{pc2}})|$ can be reasonably projected to $|L_2(j\omega_{\mathrm{pc1}})|$ with an extra margin. The projected requirement of $K_{g2} \geq 2$ (or $|L_2(j\omega_{\mathrm{pc2}})| \leq 0.5$) can be expressed as

$$|L_2(j\omega_{\mathrm{pc1}})| \leq 0.5\lambda \tag{34}$$

$$\text{or } |C_2(j\omega_{\mathrm{pc1}})| \leq 0.5\lambda(K_{g1} - 1). \tag{35}$$

According to (32). Here $\lambda < 1$ is the margin factor. If (34) or (35) is achieved, $K_{g2} \geq 2$ is regarded to be fulfilled. In the following analysis, $\lambda = 0.71$ is selected, which corresponds to a margin of –3 dB.

Under the assumption of $\omega_{\mathrm{pc1}} > 2\omega_{\mathrm{gc1}}$, it is obtained from (29) that

$$|C_2(j\omega_{\mathrm{pc1}})| < |C_2(j2\omega_{\mathrm{gc1}})| = 1.32k_{p2} = 1.32\sin\left(\frac{\gamma_1}{2}\right). \tag{36}$$

Under the assumption of $30° \leq \gamma_2 \leq 90°$, $|C_2(j\omega_{\mathrm{pc1}})| < 0.93$ can be derived from (36). Thus, (34) or (35) is achieved

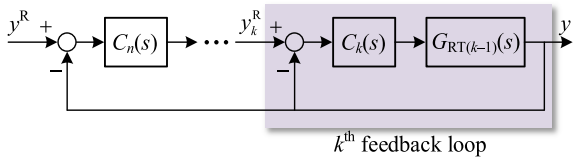

Fig. 7. Equivalent diagram of the control system.

if $K_{g1} \geq 3.62$. In other words, the confidence on K_{g2} dB $\geq$ 6 dB is high if

$$K_{g1}\text{dB} \geq 11.2 \text{ dB}. \tag{37}$$

A smaller K_{g1} leads to a lower possibility in meeting K_{g2} dB $\geq$ 6 dB. Nonetheless, it should be emphasized that the condition of (37) is highly conservative. For example, if $\gamma_1 = 45°$ and $\omega_{\mathrm{pc1}} = 2.5\omega_{\mathrm{gc1}}$, the gain margin of K_{g1} dB = 7.3 dB in the inner loop will suffice to produce K_{g2} dB $\geq$ 6 dB for the outer loop.

If K_{g2} dB $\geq$ 6 dB is not satisfied with (31), a feasible modification is to keep ω_{pc2} unchanged and reduce k_{p2} such that K_{g2} is elevated to 6 dB.

C. Design of the Multiloop Controller

The above design method for the double-loop controller is extendable to the multiloop control structure. The design of the controller $C_k(s)$ in the kth feedback loop is presented below.

The equivalent diagram of the control system for designing $C_k(s)$ is shown in Fig. 7. y_k^{R} is the equivalent reference signal of the kth loop. $G_{\mathrm{RT}(k-1)}(s)$ is the equivalent plant model expressed by

$$G_{\mathrm{RT}(k-1)}(s) = \frac{L_{k-1}(s)}{1 + L_{k-1}(s)}. \tag{38}$$

If all the k–1 inner loops are properly designed, $L_{k-1}(s)$ will satisfy $30° \leq \gamma_{k-1} \leq 90°$ and $K_{\mathrm{g}(k-1)} \geq 2$. Here, γ_{k-1} and $K_{\mathrm{g}(k-1)}$ are the stability margins of the k–1th loop. The goal is to design $C_k(s)$ such that the bandwidth of the inner k–1-loop system is retained in the kth loop and sufficient stability margins are produced.

By following the procedure of the double-loop controller design, it can be concluded that the requirements on $C_k(s)$ to reach the above goal are

$$\left|C_k(j\omega_{\mathrm{gc}(k-1)})\right| = \left|1 + L_{k-1}(j\omega_{\mathrm{gc}(k-1)})\right| \tag{39}$$

$$\angle C_k\left(j\omega_{\mathrm{gc}(k-1)}\right) \geq -\frac{1}{2}\gamma_{k-1} - 60° \tag{40}$$

$$|C_k(j\omega_{\mathrm{pc}k})| \leq \frac{|1 + L_{k-1}(j\omega_{\mathrm{pc}k})|}{2\,|L_{k-1}(j\omega_{\mathrm{pc}k})|} \tag{41}$$

where $\omega_{\mathrm{gc}(k-1)}$ and $\omega_{\mathrm{pc}k}$ are the gain crossover frequency of $L_{k-1}(s)$ and phase crossover frequency of $L_k(s)$, respectively.

$C_k(s)$ can also be realized with PI control, i.e.,

$$C_k(s) = \frac{k_{pk}(s + \omega_k)}{s}. \tag{42}$$

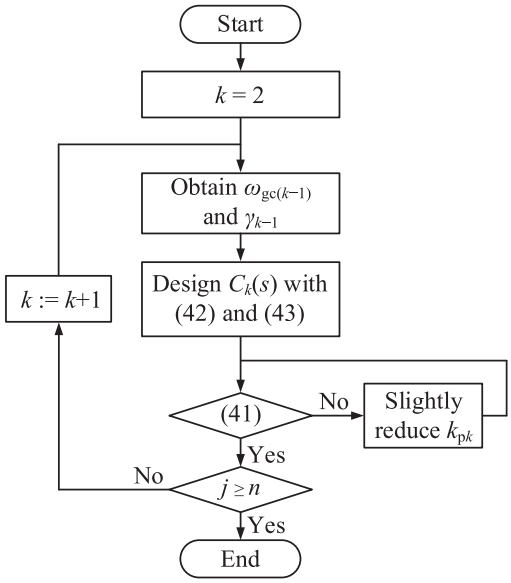

Fig. 8. Flowchart of designing a controller with n loops.

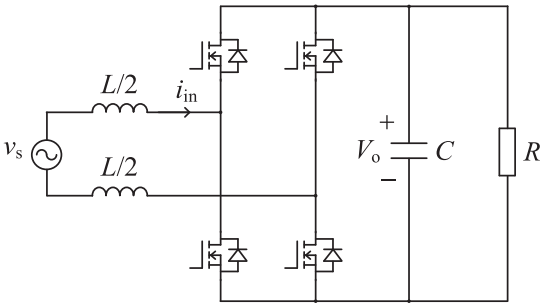

Fig. 9. Example system for illustrating the proposed multiloop controller.

If the parameters of $C_k(s)$ are designed as

$$\begin{cases} k_{pk} = \frac{1}{2}\left|1 + L_{k-1}(j\omega_{gc(k-1)})\right| = \sin\left(\frac{\gamma_{k-1}}{2}\right) \\ \omega_k = \sqrt{3}\omega_{gc(k-1)} \end{cases}. \tag{43}$$

The requirements of (39) and (40) will be satisfied. The remaining task is to check (41). If (41) is fulfilled, the parameters in (43) can be directly applied. Otherwise, the requirement of (41) can be met with reduced k_{pk}.

The flowchart of designing a controller with n loops is presented in Fig. 8. First, $C_1(s)$ is assumed to have been designed according to the design principles for conventional single-loop controllers. The gain crossover frequency ω_{gc1} and the phase margin γ_1 of the 1st loop can be obtained. Then, $C_2(s)$ can be determined according to (42) and (43) by letting $k = 2$. If (41) is met, the design of $C_2(s)$ is fixed. Otherwise, k_{p2} is reduced until (41) is fulfilled. Likewise, the remaining n–2 loops can be designed sequentially.

IV. Illustration of the Multiloop Controller With a PFC Circuit

The PFC circuit displayed in Fig. 9 is used as an example system to illustrate the proposed multiloop controller. The input of the circuit is connected to a voltage source v_s through the inductor L. The output supplies power to a resistive load R. C is the output capacitance.

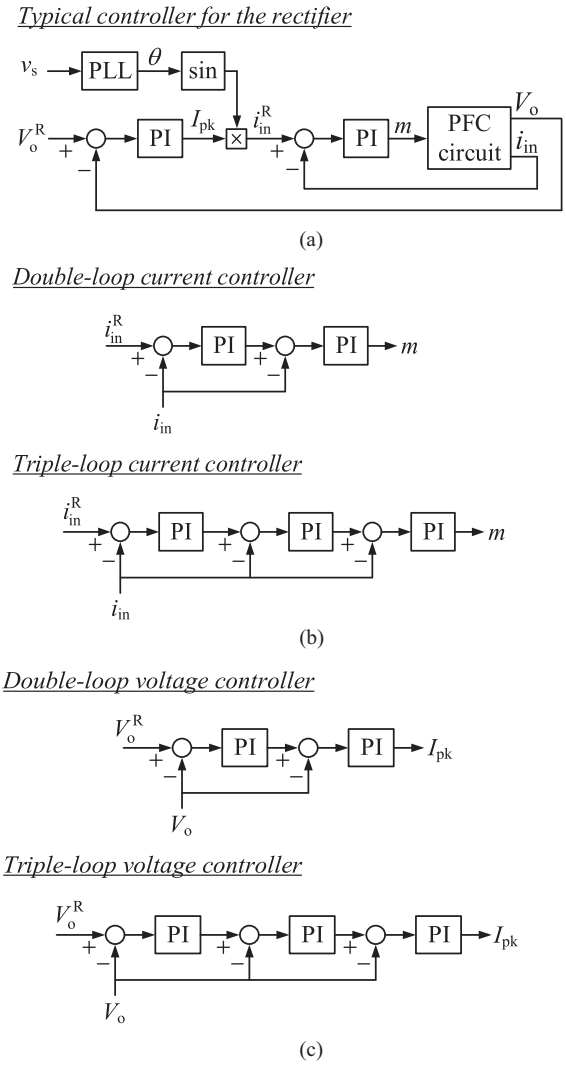

Fig. 10. Diagram of (a) a typical controller, (b) multiloop current controllers, and (c) multiloop voltage controllers.

The averaged state-space model of the rectifier is

$$\begin{cases} L\frac{di_{in}}{dt} = v_s - mV_o \\ C\frac{dV_o}{dt} = mi_{in} - \frac{V_o}{R} \end{cases} \tag{44}$$

where i_{in} is the input current; V_o is the output voltage; and m is the modulation index of the two bridge legs.

A typical controller for the rectifier is shown in Fig. 10(a), which has two nested feedback loops to respectively control the input current and output voltage [21]. It belongs to the single-loop structure in this article with respect to each control objective. The implementations of the multiloop controller for current and voltage control are displayed in Fig. 10(b) and (c), respectively. The double-loop and triple-loop structures are shown as the examples, and more feedback loops are possible for both current and voltage control. The structures of current and voltage control can be independently and flexibly selected.

TABLE I
SPECIFICATIONS OF THE RECTIFIER

Parameters	Values
Rated power	300 W
Switching frequency	20 kHz
V_s	110 Vrms / 60 Hz
V_o	200 V
L	2.6 mH
C	455 μF

It should be emphasized that the PI regulator in the single-loop controller and in the 1st loop of the multiloop controllers can be replaced by other types of regulators, such as the proportional-resonant regulator. Since this article focuses on the control structure rather than the control algorithm, PI control is used as an example to illustrate the implementation of the multiloop controllers and evaluate the performance. Fair comparison between the single-loop and multiloop controllers can be made as long as the first loop of the multiloop controllers adopts an identical regulator to the single-loop controller.

The transfer functions of the plant for current and voltage control can be derived from (44) as

$$G_{p,i}(s) = \frac{I_{\text{in}}(s)}{M(s)} = -\frac{V_o}{Ls} \tag{45}$$

$$G_{p,v}(s) = \frac{V_o(s)}{I_{pk}(s)} = \frac{RV_s}{2CRV_o s + 4V_o} \tag{46}$$

which indicate minimum-phase behaviors. Here, V_s is the peak value of the voltage source. Note that (46) only holds at frequencies much lower than the line frequency.

Given the specifications in Table I, the conventional controller employs a P controller with the gain of 0.049 for current control, while a PI controller with the P and I gains of 0.035 and 0.880 respectively is used for voltage control. The resultant loop gains of current and voltage control are depicted by the blue line in Fig. 11(a) and (b), respectively. The phase margins for the current and voltage control are 63° and 98.2°, respectively, and the gain margins are 10.5 and 52.4 dB. A slow voltage control loop is purposely designed to avoid severe distortion of the current waveform.

For the design of the multiloop current controller, the PI gains of the second loop are $k_{p2,i} = 0.522$ and $\omega_{2,i} = 6529$ rad/s according to (43). The loop gain of the second loop is displayed by the orange line in Fig. 8(a). The phase and gain margins are 61.5° and 8.34 dB, which indicate sufficient stability. The gain crossover frequency of the second loop is the same as that of the first loop, showing that the bandwidth of the controller is not compromised by the additional feedback loop.

The control parameters of the third loop according to (43) are $k_{p3,i} = 0.511$ and $\omega_{3,i} = 6529$ rad/s. However, it can be shown that the resultant gain margin is smaller than 6 dB. Therefore, $k_{p3,i}$ is modified as 0.403, while $\omega_{3,i}$ remains unchanged. The loop gain of the third loop is shown by the green line in Fig. 11(a). The phase margin and gain margin are 68.9° and 6.06 dB. The gain crossover frequency of the third loop is 441 Hz, corresponding to a reduction of 26.5% in the bandwidth.

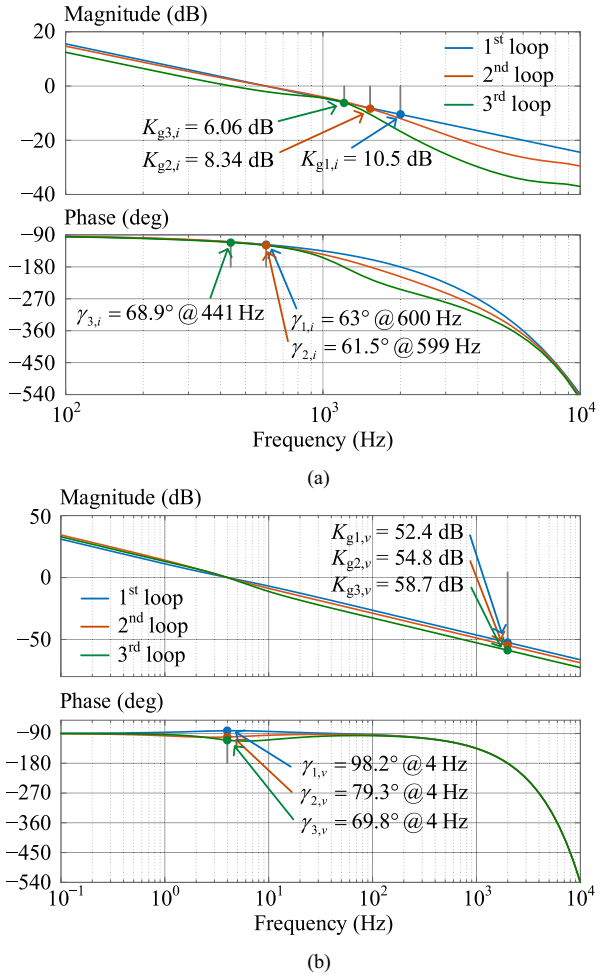

Fig. 11. Loop gain comparison of the single-loop and multiloop structures. (a) Current control; (b) Voltage control.

The multiloop voltage controller can be designed likewise. The PI gains of the second and third loops are $k_{p2,v} = 0.756$, $\omega_{2,v} = 43.53$ rad/s, and $k_{\text{p3},v} = 0.638$, $\omega_{3,v} = 43.53$ rad/s, respectively. The stability margins are 79.3° and 54.8 dB for the second loop and 69.8° and 58.7 dB for the third loop. The two additional loops retain the 4-Hz gain crossover frequency of the 1st loop.

The disturbance gains of the current and voltage controllers are displayed in Fig. 12, where the blue line, orange line, and green line represent the single-loop controller, double-loop controller, and triple-loop controller, respectively. A prominent drop of the disturbance gain can be observed with extra feedback loops. The suppression effect is stronger within the controller bandwidth, and the disturbance gain reduces with the decrease of the frequency.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

The proposed multiloop control structure and control design method are verified on the PFC circuit in Fig. 9. The

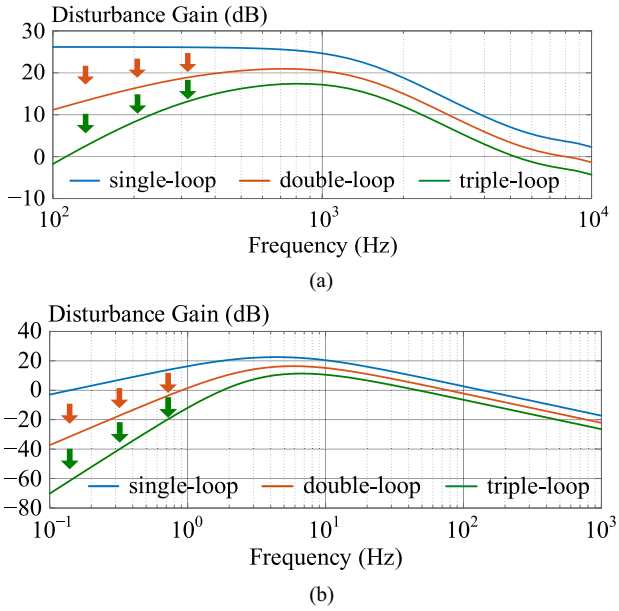

Fig. 12. Comparison of the disturbance gains of the single-loop and multiloop structures. (a) Current control. (b) Voltage control.

performances of the current and voltage controllers in Fig. 10 are examined in both simulation and experiments.

A. Simulation Results

First, three current controllers are compared in simulation.

1) Single-loop current controller.
2) Double-loop current controller.
3) Triple-loop current controller.

The voltage controller adopts the single-loop structure for a fair comparison.

The waveforms under normal and distorted grid voltage conditions are shown in Fig. 13, in which harmonics are added into the grid voltage since 0.1 s. When the grid voltage is not polluted, the input currents with the three current controllers are all sinusoidal and in phase with the grid voltage. The total harmonic distortion (THD) values with the three controllers are 6.57%, 2.53%, and 1.37%, respectively, showing that extra feedback loops improve the control performance.

When the grid voltage is polluted, the input current is obviously distorted with the single-loop controller, and the THD is increased to 9.52%. When the double-loop controller is employed, the THD is significantly reduced to 5.02%. The triple-loop controller further reduces the THD to 2.75%. The result agrees with the theoretical analysis and validates the strong disturbance rejection capability of the multiloop control structure.

Next, three voltage controllers are compared in load-change tests.

1) Single-loop voltage controller.
2) Double-loop voltage controller.
3) Triple-loop voltage controller.

In all the load-change tests, the single-loop structure is adopted for current control.

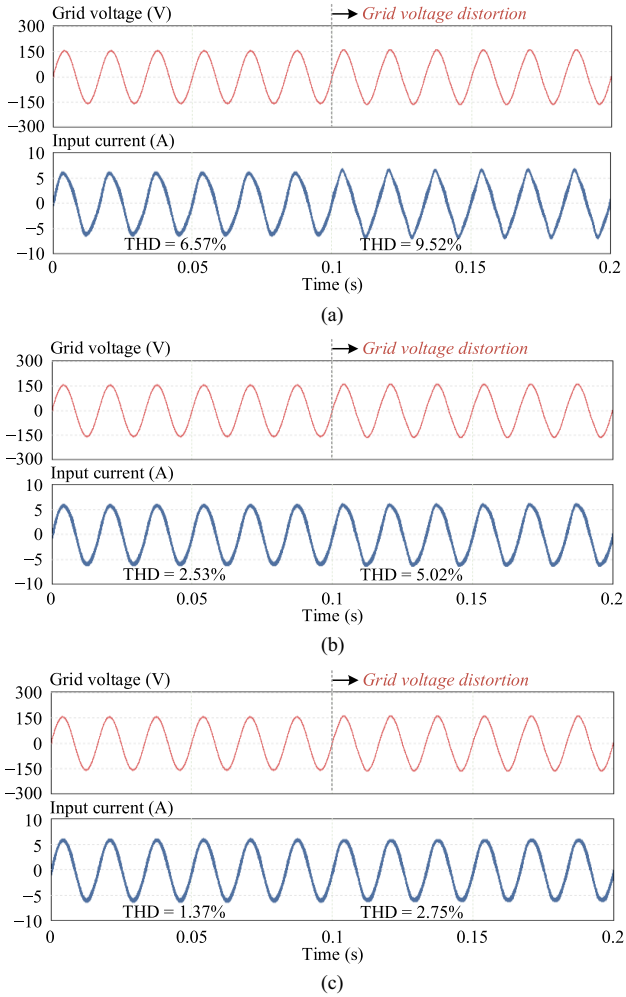

Fig. 13. Waveforms under normal and distorted grid voltage conditions. (a) Single-loop current controller. (b) Double-loop current controller. (c) Triple-loop current controller.

Fig. 14 displays the transient waveforms of the output voltage when the load is increased from 150 to 300 W. The three controllers produce similar settling times, which align with the designed control bandwidth according to Fig. 11(b).

With the single-loop voltage controller, the output voltage drops to 182 V after the load increase and is then restored to the reference level with no overshoot. The multiloop controllers cause oscillatory waveforms of the output voltage. Nonetheless, the voltage valleys with the double-loop and triple-loop controllers are lifted to 185 and 187 V, respectively. This is because the multiloop controllers suppress low-frequency voltage components more effectively, leading to voltage trajectories that move more closely around the steady-state value. Meanwhile, higher-frequency components become more dominant and exhibit oscillatory waveforms. It should be emphasized that the oscillatory behavior of the output voltage with the multiloop controllers does not mean reduced stability. The stability margins are sufficient for all the three controllers according to the design in Fig. 11(b).

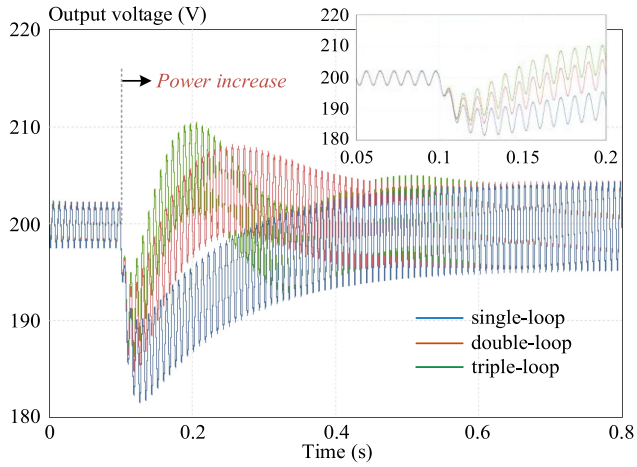

Fig. 14. Waveforms of the output voltage when the load is increased from 150 to 300 W.

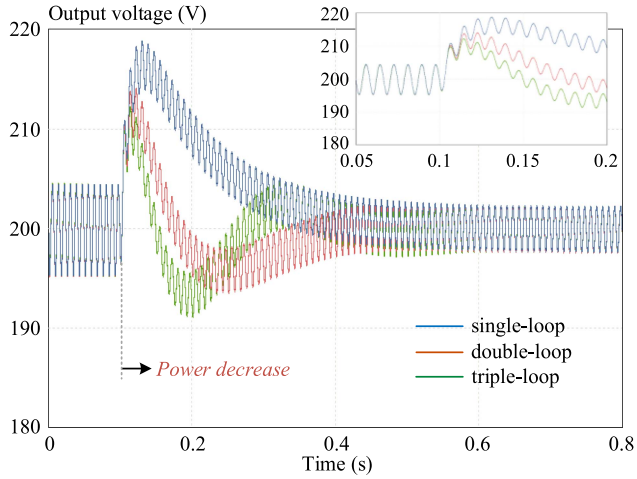

Fig. 15. Waveforms of the output voltage when the load is decreased from 300 to 150 W.

The waveforms of the output voltage in the load-decrease test are given in Fig. 15. Similar conclusions can be made from Fig. 15 as from Fig. 14. The three controllers produce similar settling times (around 0.5 s) due to identical control bandwidths, as designed in Fig. 11(b). The two multiloop controllers cause smaller deviation from the steady-state value, while the single-loop controller presents a less oscillatory waveform. In the two load transient tests, the voltage deviations with the three controllers are –9.0%/+9.5%, –7.5%/+7.0%, and –6.5%/+6.1%, respectively. The advantage of the proposed multiloop controller is again verified.

One more load variation test is conducted, where the load power is initially 200 W and starts to exhibit ±50% fluctuations with a period of 0.5 s since $t = 0.3$ s. The simulation waveforms of the output voltage with the single-loop, double-loop, and triple-loop voltage controllers are displayed in Fig. 16. The output voltage deviations with the three controllers are –8.8%/+7.5%, –4.6%/+5.0%, and –2.7%/+3.6%, respectively. The result also verifies stronger robustness of the multiloop controller against external disturbances.

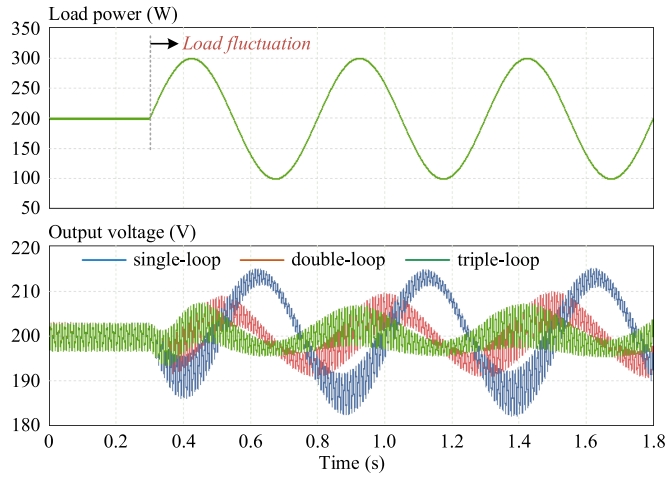

Fig. 16. Simulation waveforms of the load fluctuation test.

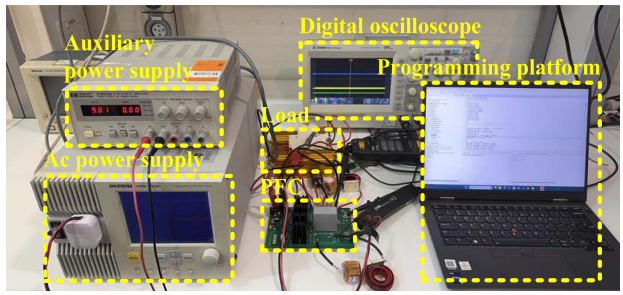

Fig. 17. Hardware prototype of the PFC circuit.

B. Experimental Results

The tests in simulation are also conducted on a hardware prototype, as displayed in Fig. 17. The ac power supplies APS-1102 and IT7909-350-90 are employed to emulate normal and distorted grid voltages, respectively. The distorted grid voltage is set to contain 3% 3rd-order harmonic and 1.5% fifth-order harmonic components. The evaluation board TDINV1000P100 is used to construct the PFC circuit. The waveforms are monitored and captured with the digital oscilloscope ZDS3024.

The results under normal and distorted grid voltage conditions are shown in Fig. 18. The single-loop, double-loop, and triple-loop current controllers are examined. The THD values with the three controllers are 7.52%, 3.18%, and 1.90% under a clean grid voltage, and become 13.34%, 9.06%, and 5.48% under grid voltage distortion. The experimental results are consistent with the simulation, and the effectiveness of the multiloop controller in different grid conditions is validated again.

The performances of the voltage controllers with different number of feedback loops are also evaluated experimentally. The waveforms in the load transient tests are presented in Fig. 19. The three controllers with one, two, and three feedback loops exhibit similar settling time, which agree with the theoretical analysis and simulation.

Similar to the waveforms in Figs. 14 and 15, the single-loop controller causes no overshoot/undershoot in the output

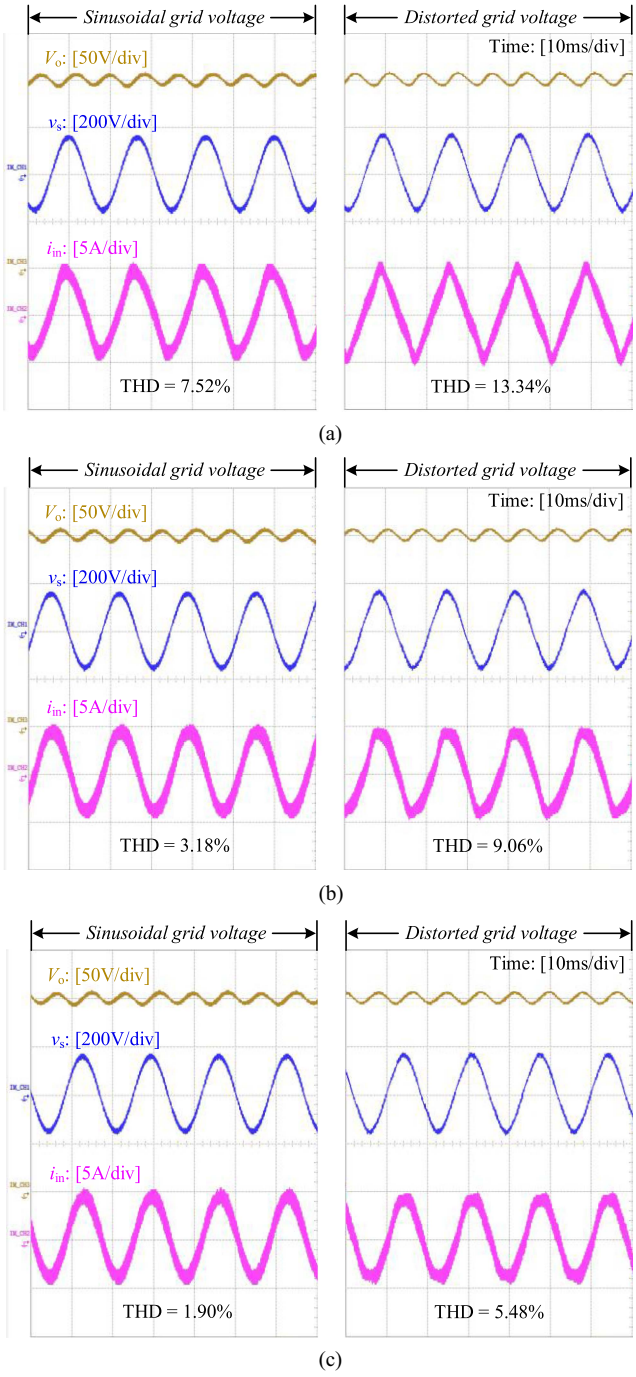

Fig. 18. Experimental waveforms under normal and distorted grid voltage conditions. (a) Single-loop current controller. (b) Double-loop current controller. (c) Triple-loop current controller.

voltage during the transient stage, while the other two yield oscillatory but asymptotically stable trajectories. In the two load transient tests, the deviations from the reference voltage with the three controllers are –10.0%/+10.0%, –9.0%/+8.0%, and –8.0%/+7.0%, respectively. The multiloop controllers perform better in the sense of avoiding overvoltage or undervoltage. The transient periods with the three controllers are all around 0.5 s, which is consistent with the simulation results in Figs. 14 and 15 and the design in Fig. 11(b).

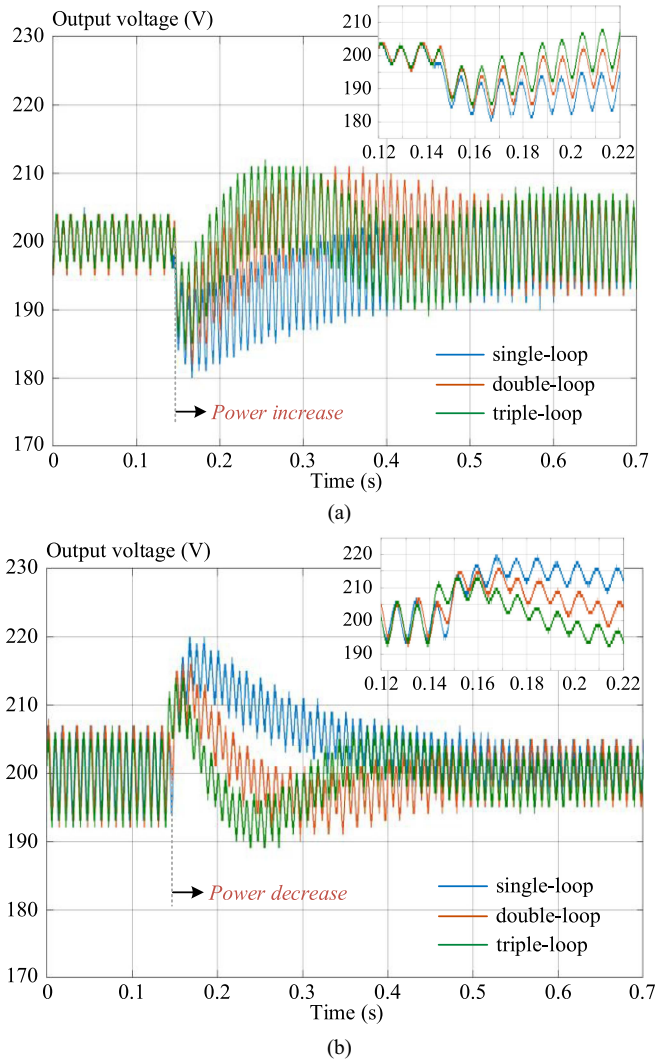

Fig. 19. Experimental waveforms of the output voltage when the load is changed (a) from 150 to 300 W, and (b) from 300 to 150 W.

VI. Conclusion

This article proposes a new multiloop control structure, which applies additional feedback loops to control each output of the control system. With the additional loops, the robustness of the control system can be boosted. It is also discovered that such an advantageous feature does not necessarily compromise the stability and bandwidth of the original system. A straightforward design guideline for the multiloop controller is provided. The proposed multiloop structure has been successfully demonstrated with simulation and practical experiments of a PFC circuit. It can potentially be combined with various existing control methods to yield enhanced performance. The optimization of the control parameters and the application of the multiloop controller can also be explored in the future.

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