A Fast and Reliable Start-up Strategy for Three-Phase DAB Power Converters

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***Abstract*—The three-phase dual active bridge (3p-DAB) converter is a promising topology for dc conversion systems, thanks to its high power density, bidirectional power flow, and soft-switching capabilities. However, how to achieve fast while reliable start-up respecting the permissible current limit remains challenging. In this work, we propose a simple and effective start-up strategy for 3p-DAB converters. First, by simply manipulating the switching positions, the initial dc-bias current is successfully eliminated. Then, the process of fast start-up under current limits is formulated as an inequality-constrained problem, for which we solve the closed-form analytical expression. This expression is then segmented via a newly proposed coordination transform, to bridge the control parameters and system states. With a simple segmental comparison, the global optimal phase-shift ratio and duty cycle to assign to the converters are obtained. Experimental results validate the effectiveness of the proposal and demonstrate its considerable improvements over the state-of-the-art techniques.**

***Index Terms*—DC bias elimination, fast start-up, reliability, three-phase dual-active bridge converters (3p-DAB).**

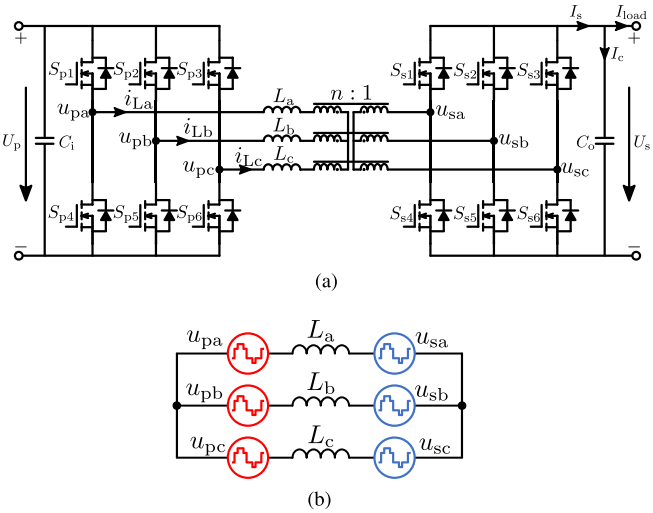

Fig. 1. 3p-DAB converter. (a) Circuit diagram. (b) Simplified equivalent circuit.

I. Introduction

GLOBAL demands for renewable energy utilization, electrified transportation, dc power transmission, dc microgrids, etc., have urged significant investigation into dc power conversion. Among the various types of dc power converters, three-phase dual active bridge (3p-DAB) converters have emerged as a promising choice due to their high power density, electrical isolation, and inherent zero-voltage switching capabilities [1]. As illustrated in Fig. 1(a), the 3p-DAB converter presents several advantages over a single-phase dual active bridge (1p-DAB) converter, e.g., enhanced power density, reduced filter size, and improved core utilization [2]. However, due to unexpected issues, the converter might fail or be shutdown for maintenance. Fast and reliable start-up is critical to enhance system stability and availability [3].

A key challenge encountered during the start-up of a DAB converter arises from the zero-voltage condition on the secondary side, which results in the direct application of the primary voltage across the leakage inductance of the transformer. As a result, an initial dc-bias occurs, which may deteriorate system stability and even damage system hardware [4].

Different techniques have been proposed to realize a reliable start-up. Currently, there are two primary categories to achieve a reliable start-up for, however, 1p-DAB converters: hardware-based solutions that involve the design of circuits, as proposed in [5] and [6], effectively suppress initial dc-bias by introducing auxiliary circuits. Meanwhile, the approaches described in [7] and [8] enhance the dc-bias capability of transformers through optimized designs, which indirectly facilitate reliable start-up. However, these hardware optimizations increase system costs and complexity. In contrast, software-based solutions focus on optimizing start-up strategies. In [9] and [10], a multistage start-up strategy is proposed, which starts the system with an open-loop control initially. However, to suppress the dc-bias, the open-loop stage gradually raises the current, which constrains the performance of converters. Several start-up strategies have been proposed to address the initial dc-bias. The authors in [11],

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[12], [13], and [14] developed control strategies tailored for single phase-shift (SPS), extended phase-shift (EPS), double phase-shift (DPS), and triple phase-shift (TPS), respectively, to suppress initial dc-bias. Although a reliable start-up is achieved, the start-up speed is sacrificed.

Several techniques to improve the start-up speed have hence been investigated and reported. In [15], a current shaping scheme based on model predictive control (MPC) is proposed, which leverages the superior control capabilities of MPC [16], [17], [18], [19], [20] to achieve a fast dynamic response to start-up. In [3], a closed-loop start-up method with soft switching capabilities is proposed, which combines EPS and TPS to initiate converter start-up at the maximum allowable precharge current. This method accelerates the start-up process while operating within the maximum allowable current; however, it limits control freedom and does not achieve maximum power. In [12], a simple and fast start-up strategy is proposed, which utilizes the Lagrange multiplier (LM) and Karush–Kuhn–Tucker (KKT) conditions to determine the optimal phase shift ratio for maximizing output power within the allowable current. However, this strategy involves continuously comparing multiple local optimal solutions, which increases computational complexity. In addition, Gong et al. [21] proposed a novel variable frequency control to achieve ultrafast start-up with a wide safety range, but the variable frequency control increases the complexity of the control system and places a heavier burden on the processor.

At present, the research on 3p-DAB mainly focuses on optimizing modulation [22], [23], [24]. Notably, Huang et al. [22] proposed a synchronous pulsewidth modulation (S-PWM), providing two degrees of freedom to control. Based on this, Sun et al. [25] proposed a simplified derivation using a segmented analytical method to obtain a minimized current stress scheme. Schulz and Bauman [26] proposed a novel closed-form minimum current stress optimization scheme. However, the report on the 3p-DAB start-up strategy is insufficient. The authors in [4] and [27] proposed strategies to suppress the start-up initial dc-bias in 3p-DAB. However, these strategies are restricted to SPS modulation and do not provide fast start-up capabilities.

In this work, we focus on 3p-DAB, propose a fast and reliable start-up strategy based on S-PWM and develop a simple method for suppressing initial dc-bias. The major contributions of this article include the following three points.

1) The current stress and transmission power of the S-PWM are described, and the current stress is divided in more detail than previously reported (see Section II).
2) A method to suppress initial dc-bias based on current trajectory control is proposed, and the influence of dead time and leakage resistance is considered (see Section IV-A).
3) A novel solution is proposed to achieve a fast and reliable start-up of the 3p-DAB converter, along with a new coordinates segmented comparison to derive the optimal control parameters (see Section IV-B).

The rest of this article is organized as follows. Section II introduces the S-PWM control. Section III elucidates the causes of the initial dc-bias and the limitations of the conventional strategy. Section IV gives a detailed explanation of the proposed strategy. Section V provides experimental results and analyses. Finally, Section VI concludes this article.

II. System Description and Modeling

In this section, the 3p-DAB converter topology, S-PWM control, current stress, and transmission power are introduced.

As shown in Fig. 1(a), the 3p-DAB consists of six half-bridges that are connected on both sides of a three-phase transformer. The turns ratio is n, L_{a}, L_{b}, and L_{c} are the leakage inductance and series external inductance of the transformer. U_{i} is the input dc voltage, C_{i} is the input filter capacitor, this side is called the primary side, U_{o} is the output side voltage, C_{o} is the output filter capacitor, and this side is called the secondary side. v_{px} and $v_{\mathrm{sx}}(\mathrm{x} \in [a, b, c])$ are the ac phase voltages, and i_{Lx} is the phase current. S_{py} and $S_{\mathrm{sy}}(\mathrm{y} \in [1, 2, 3, 4, 5, 6])$ are switching devices on the primary and secondary sides, while G_{py} and G_{sy} represent the driving signals of S_{py} and S_{sy}.

A. Simultaneous Phase-Width Modulation Control

The S-PWM control has two degrees of freedom: phase-shift ratio D and duty cycle D_c. The upper switches and lower switches conduct alternately, and the conduct time of the upper switch is D_cT_{h}. The driving signals of primary side G_{p1}, G_{p2}, and G_{p3} are 120° $(T_s/3)$ apart, and the secondary side is the same. The phase-shift between G_{py} and G_{sy} is DT_{h}, where T_{h} is half the switching period T_{s}.

To analyze the inductor current, we assume that the input voltage and output voltage are constant within a switching period and neglect the magnetizing inductance and magnetizing resistance of the transformer winding, each phase of the circuit can thus be simplified into two voltage sources and an inductor in series, as shown in Fig. 1(b).

The 3p-DAB has the ability of bidirectional power transmission. This article only analyzes the forward power transmission mode (from primary port to secondary port). According to the magnitudes between D and D_c, the S-PWM control can be divided into seven modes, as shown in Table I. The A-phase operating waveforms of the seven modes are shown in Fig. 2. Fig. 2(h) is a boundary diagram of the seven modes.

B. Current Stress and Transmission Power

Sun et al. [25] described the current stress, but the voltage level division is not detailed enough. In this article, we will rederive it. To simplify, we assume the three phases are symmetrical and take phase-A for analysis. The change of the inductor current is associated with the voltage, the equivalent voltage source on both sides of the inductor, as follows:

$$\Delta i_a = \frac{u_{\mathrm{La}}}{L_a}\Delta t = \frac{u_{\mathrm{pa}} - nu_{\mathrm{sa}}}{L_a}\Delta t. \tag{1}$$

The current stress and transmission power analysis methods of the seven working modes are similar. This section takes Mode I as an example. According to (1) and the constraint that the average inductor current value within a switching period is zero,

TABLE I
THE CONSTRAINTS AND TRANSMISSION POWER OF SEVEN OPERATING MODES

Mode	Constraints of D_c	Constraints of D	Transmission power
Mode I	$2/3 \le D_c \le 1$	$0 \le D \le D_c - 2/3$	$P_{\mathrm{N}}[2(4-3D)D]/3$
Mode II	$2/3 \le D_c \le 1$	$D_c - 2/3 \le D \le \mathrm{Min}\,[4/3 - D_c, 1/2]$	$P_{\mathrm{N}}[3(4-9D)D - 9D_c^2 + 6D_c(2+3D) - 4]/9$
Mode III	$2/3 \le D_c \le 1$	$4/3 - D_c \le D \le 1/2$	$P_{\mathrm{N}}[-4(5-9D+9D^2) - 18(-2+D_c)D_c]/9$
Mode IV	$0 \le D_c \le 2/3$	$0 \le D \le \mathrm{Min}\,[2/3 - D_c, D_c]$	$P_{\mathrm{N}}[2(2D_c - D)D]$
Mode V	$1/3 \le D_c \le 2/3$	$2/3 - D_c \le D \le \mathrm{Min}\,[D_c, 1/2]$	$P_{\mathrm{N}}[3(4-9D)D - 9D_c^2 + 6D_c(2+3D) - 4]/9$
Mode VI	$0 \le D_c \le 2/3$	$\mathrm{Max}\,[D_c, 2/3 - D_c] \le D \le 1/2$	$P_{\mathrm{N}}[-(2-3D)^2 + 9D_c^2 + 6D_c(2-3D)]/9$
Mode VII	$0 \le D_c \le 1/3$	$D_c \le D \le \mathrm{Min}\,[2/3 - D_c, 1/2]$	$P_{\mathrm{N}}(2D_c^2)$

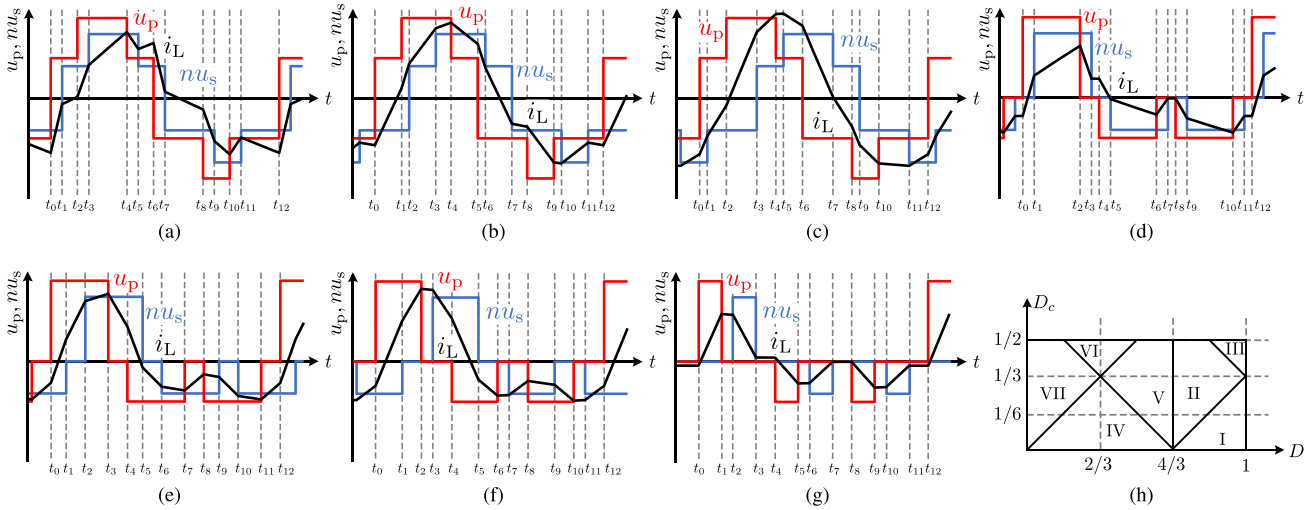

Fig. 2. Seven operating modes of S-PWM control. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Boundary of the seven operating modes.

the inductor current at each switching moment is

$$\begin{cases} i_{\mathrm{L}}(t_1) &= I_{\mathrm{N}}(-2+2k+3D) \\ i_{\mathrm{L}}(t_2) &= I_{\mathrm{N}}[-4+3D_c+k(4+3D-3D_c)] \\ i_{\mathrm{L}}(t_3) &= I_{\mathrm{N}}[-4+6D+3D_c+k(4-3D_c)] \\ i_{\mathrm{L}}(t_4) &= I_{\mathrm{N}}[4-3D_c+k(-4+6D+3D_c)] \\ i_{\mathrm{L}}(t_5) &= I_{\mathrm{N}}[4+3D-3D_c+k(-4+3D_c)] \\ i_{\mathrm{L}}(t_6) &= I_{\mathrm{N}}[2+k(-2+3D)] \\ i_{\mathrm{L}}(t_7) &= I_{\mathrm{N}}(2-2k-3D) \\ i_{\mathrm{L}}(t_8) &= I_{\mathrm{N}}[-2+3D_c+k(2-3D-3D_c)] \\ i_{\mathrm{L}}(t_9) &= I_{\mathrm{N}}[-2-6D+3D_c+k(2-3D_c)] \\ i_{\mathrm{L}}(t_{10}) &= I_{\mathrm{N}}[2-3D_c+k(-2-6D+3D_c)] \\ i_{\mathrm{L}}(t_{11}) &= I_{\mathrm{N}}[2-3D-3D_c+k(-2+3D_c)] \\ i_{\mathrm{L}}(t_{12}) &= I_{\mathrm{N}}[-2+k(2-3D)] \end{cases} \tag{2}$$

where I_{N} and k are defined as follows:

$$I_{\mathrm{N}} = \frac{U_{\mathrm{p}} T_{\mathrm{s}}}{18L}, k = \frac{nU_{\mathrm{s}}}{U_{\mathrm{p}}}. \tag{3}$$

Since the three phases are symmetrical, the transmission power of Mode I can be calculated as

$$P = P_{\mathrm{a}} + P_{\mathrm{b}} + P_{\mathrm{c}} = 3P_{\mathrm{a}} = P_{\mathrm{N}}\left[\frac{2(4-3D)D}{3}\right] \tag{4}$$

where P_{N} is defined as follows:

$$P_{\mathrm{N}} = \frac{nU_{\mathrm{p}}U_{\mathrm{s}}T_{\mathrm{s}}}{8L}. \tag{5}$$

According to different values of k, the inductor current peak value of mode I can be obtained as

$$i_{\mathrm{L,max}} = \begin{cases} i_{\mathrm{L}}(t_6) & 0 \le k < k_1 \\ i_{\mathrm{L}}(t_4) & k_1 \le k < 1 \\ i_{\mathrm{L}}(t_3) & 1 \le k < k_2 \\ i_{\mathrm{L}}(t_1) & k \ge k_2 \end{cases} \tag{6}$$

where $k_1 = \frac{-2+3D_c}{-2+3D+3D_c}$ and $k_2 = \frac{-2+3D+3D_c}{-2+3D_c}$.

Similarly, the transmission power of other modes is obtained as shown in Table II. The current stress is shown in Table III.

TABLE II
INDUCTOR STRESS CURRENT OF SEVEN MODES

Mode	Constraints	Inductor current stress
Mode I	$0 < k \leq k_1$	$I_{\mathrm{N}}[2 + k(-2 + 3D)]$
	$k_1 < k \leq 1$	$I_{\mathrm{N}}[4 - 3D_2 + k(-4 + 6D + 3D_c)]$
	$1 < k \leq k_2$	$I_{\mathrm{N}}[-4 + 6D + k(4 - 3D_c) + 3D_c]$
	$k > k_2$	$I_{\mathrm{N}}[-2 + 2k + 3D]$
Mode II	$0 < k \leq 1/2$	$I_{\mathrm{N}}[2 + k(6D - 3D_c)]$
	$1/2 < k \leq 1$	$I_{\mathrm{N}}[4 - 3D_c + k(-4 + 6D + 3D_c)]$
	$1 < k \leq 2$	$I_{\mathrm{N}}[-4 + 6D + k(4 - 3D_c) + 3D_c]$
	$k > 2$	$I_{\mathrm{N}}[2k + 6D - 3D_c]$
Mode III	$0 < k \leq 1/2$	$I_{\mathrm{N}}[2 + k(6D - 3D_c)]$
	$1/2 < k \leq 1$	$I_{\mathrm{N}}[3D + k(4 - 3D_c)]$
	$1 < k \leq 2$	$I_{\mathrm{N}}[4 + 3kD - 3xD_c]$
	$k > 2$	$I_{\mathrm{N}}[2k + 6D - 3D_c]$
Mode IV	$0 < k \leq 1$	$I_{\mathrm{N}}[k(6D - 3D_c) + 3D_c]$
	$k > 1$	$I_{\mathrm{N}}[6D - 3D_c + 3kD_c]$
Mode V	$0 < k \leq 1$	$I_{\mathrm{N}}[k(6D - 3D_c) + 3D_c]$
	$k > 1$	$I_{\mathrm{N}}[6D - 3D_c + 3kD_c]$
Mode VI	$k \geq 0$	$I_{\mathrm{N}}[3D_c + 3kD_c]$
Mode VII	$k \geq 0$	$I_{\mathrm{N}}[9D_c - 3kD_c]$

III. PROBLEMS STATEMENT

This section provides a detailed description of the issues that should be addressed during the start-up of the 3p-DAB, along with conventional solutions and shortcomings.

A. Initial DC-Bias of 3p-DAB

To simplify the analysis of initial dc-bias, the three-phase voltages are transformed into the $\alpha\beta$ coordinates using

$$\vec{u} = u_\alpha + \mathrm{j}u_\beta = \frac{2}{3}(u_{\mathrm{pa}} + e^{\mathrm{j}120^\circ}u_{\mathrm{pb}} + e^{\mathrm{j}240^\circ}u_{\mathrm{pc}}). \quad (7)$$

It is assumed that the output voltage is zero during the initial startup period, i.e., $U_{\mathrm{s}} = 0$.

According to (7), the trajectory of the three-phase currents in the initial start-up period in the $\alpha\beta$ coordinate can be obtained, as shown in Fig. 3(a) and (c), corresponding to the ranges $0 < D_c \leq 2/3$ and $2/3 < D_c \leq 1$, where $D_c = 1$ is SPS modulation. In addition, Fig. 3(b) and (d) illustrates the corresponding switch drive signal. Notably, the center of the current trajectory deviates from the origin of the coordinate axis, resulting in an initial dc-bias.

The initial dc-bias decays slowly over time, with the duration determined by the time constant L/R. A smaller time constant will reduce the efficiency of the system, while a more significant time constant will prolong the dc-bias last time, as illustrated in Fig. 4. It can be observed that, regardless of the range of D_c, the three-phase currents will exhibit a bias, with phase-A experiencing the most significant bias due to being subjected to forward voltage for a longer duration. A significant current bias may trigger the protection of the driver.

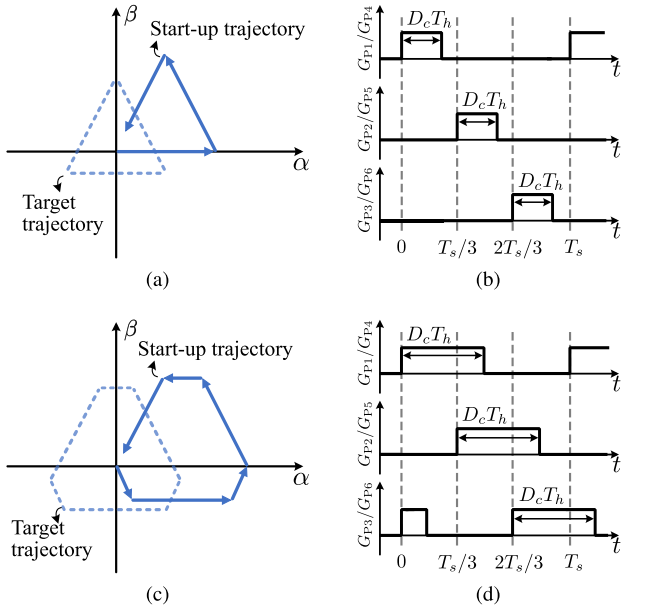

Fig. 3. Direct start-up of 3p-DAB. (a) Current trajectory with $0 < D_c \leq 2/3$. (b) Switch drive signal with $0 < D_c \leq 2/3$. (c) Current trajectory with $2/3 < D_c \leq 1$. (d) Switch drive signal with $2/3 < D_c \leq 1$.

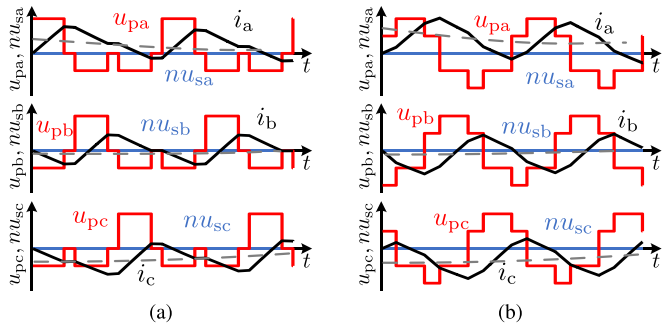

Fig. 4. Inrush current during start-up. (a) $0 < D_c \leq 2/3$. (b) $2/3 < D_c \leq 1$.

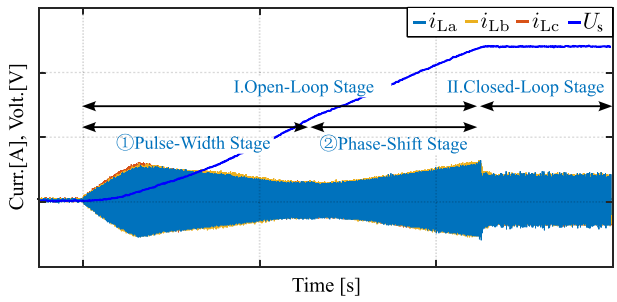

Fig. 5. Conventional start-up of three-phase DAB converter.

B. Conventional Start-up Strategy of 3p-DAB

Due to the dc-bias, the conventional start-up strategy gradually increases the current. This method produces a less significant dc-bias that dissipates quickly. The strategy is illustrated in Fig. 5, and divided into three stages.

The first stage is the pulsewidth start-up stage, during which D_c gradually increases according to the preset ramp function

TABLE III
OPTIMAL SOLUTIONS OF SEVEN OPERATING MODES IN $0 < k \leq \frac{1}{2}$

Mode	Constraints of k	Constraints of k_{i}	Local optimal solutions	Transmission power
Mode I	$0 < k \leq \frac{1}{2}$	$2-2k \leq k_{\mathrm{i}} \leq 2-k$	$D_1 = \frac{-2+k_{\mathrm{i}}+2k}{3k}$ $D_2 = 1$	$\frac{8}{9} - \frac{2(-2+k_{\mathrm{i}})^2}{9k^2}$
Mode II	$0 < k \leq \frac{1}{2}$	$2-k \leq k_{\mathrm{i}} \leq 2$	$D_1 = \frac{-2+k_i+4k}{9k}$ $D_2 = \frac{2-k_i+8k}{9k}$	$\frac{2}{27}(10 - \frac{(-2+k_{\mathrm{i}})^2}{k^2})$
Mode III	$0 < k \leq \frac{1}{2}$	$2-k \leq k_{\mathrm{i}} \leq 2$	$D_1 = \frac{-2+k_{\mathrm{i}}+3k}{6k}$ $D_2 = 1$	$\frac{7}{9} - \frac{(-2+k_{\mathrm{i}})^2}{9k^2}$
Mode IV	$0 < k \leq \frac{1}{2}$	$0 \leq k_{\mathrm{i}} \leq 1+2k-3k^2$	$D_1 = \frac{k_{\mathrm{i}}}{3(1+3k)}$ $D_2 = \frac{k_{\mathrm{i}}(1+k)}{3(1-k)(1+3k)}$	$\frac{2k_{\mathrm{i}}^2}{9+18k-27k^2}$
Mode V	$0 < k \leq \frac{1}{3}$	$1+2k-3k^2 \leq k_i \leq 2$	$D_1 = \frac{2+(1+k)k_{\mathrm{i}}-8k+6k^2}{9-6k+9k^2}$ $D_2 = \frac{(3-k)k_{\mathrm{i}}-4k+12k^2}{9-6k+9k^2}$	$\frac{8}{9} - \frac{2(-4+k_{\mathrm{i}})^2}{9(3+k(-2+3k))}$
	$\frac{1}{3} < k \leq \frac{1}{2}$	$1+2k-3k^2 \leq k_{\mathrm{i}} \leq \frac{-6+6k^2}{-3+k}$		
Mode VI	$0 < k \leq \frac{1}{2}$	$\frac{1}{2}(1+k) \leq k_{\mathrm{i}} \leq 1+k$	$D_1 = \frac{2-k_{\mathrm{i}}+2k}{3+3k}$ $D_2 = \frac{k_{\mathrm{i}}}{3+3k}$	$\frac{2k_{\mathrm{i}}^2}{9(1+k)^2}$
Mode VII	$0 < k \leq \frac{1}{2}$	$0 \leq k_{\mathrm{i}} \leq \frac{1}{2}(1+k)$	$D_1 = \frac{1}{2}$ $D_2 = \frac{k_{\mathrm{i}}}{3+3k}$	$\frac{2k_{\mathrm{i}}^2}{9(1+k)^2}$

$\mathrm{d}D_c/\mathrm{d}t$. When D_c reaches 0.5, the procedure enters the shift-phase start-up stage, where D_c remains at 0.5, and D increases according to the preset ramp function $\mathrm{d}D/\mathrm{d}t$. When the output voltage U_{s} reaches the preset value, the procedure transitions to the closed-loop stage, stabilizing the output voltage. There are two shortcomings with the conventional start-up procedure. 1) The inductor current is regulated not only by the parameters $\mathrm{d}D_c/\mathrm{d}t$ and $\mathrm{d}D/\mathrm{d}t$, but also by the load conditions and input voltage. For varying load conditions and current stress limits, parameter redesign is necessary. 2) Most of the time during the start-up procedure, the current stress remains below the maximum allowable current. This indicates that the procedure does not fully utilize the current-carrying capacity, which extends the start-up time.

IV. PROPOSED SOLUTION

In this section, we have developed a fast and highly reliable start-up strategy for the 3p-DAB converter. This strategy is divided into two key parts: (a) initial dc-bias suppression technology, and (b) maximum power start-up technology.

A. Initial DC-Bias Suppression Technology

In Section III-A, the dc-bias in 3p-DAB converter has been analyzed in detail. During the start-up, the three-phase current exhibits different degrees of bias. Studying the current suppression method for each phase separately is complicated; therefore, we transform the three-phase current into the $\alpha\beta$ coordinate system to analyze the suppression technology.

According to Fig. 3, the start-up trajectory can be divided into two categories, (a) $0 < D \leq 2/3$ and (b) $2/3 < D \leq 1$, where (a) is a triangular trajectory and (b) is a hexagonal trajectory. The direction of the current trajectory changes with the switching signal, meaning each direction's duration corresponds to the switching signal's duration. The triangle start-up trajectory has three effective switching signal states (Ignoring the magnetizing inductance and resistance; when the upper (lower) switches are in the same state, the current trajectory remains unchanged). The durations for these signals are the same, represented as $T_{\mathrm{tri}} = D_{\mathrm{c}}T_{\mathrm{h}}$. In the hexagonal startup trajectory, six switching signals correspond to the long and short sides of the hexagon trajectory. The duration are $T_{\mathrm{hexl}} = (4/3 - D_{\mathrm{c}})T_{\mathrm{h}}$ and $T_{\mathrm{hexs}} = (D_{\mathrm{c}} - 2/3)T_{\mathrm{h}}$, respectively.

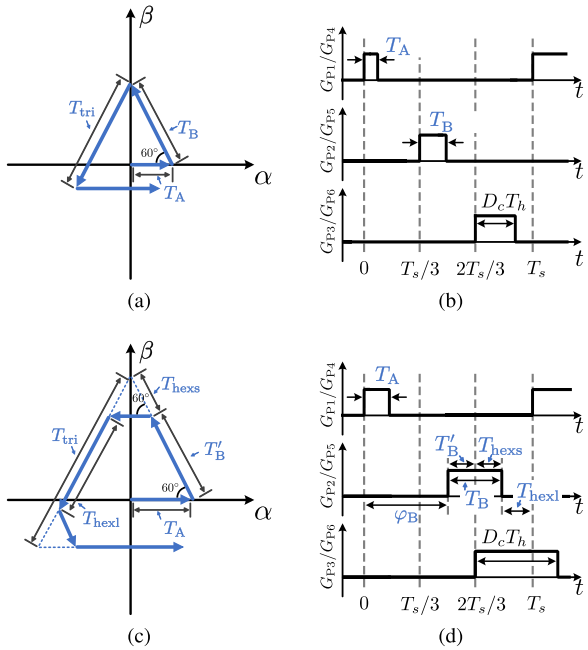

Fig. 6. Corrected start-up of 3p-DAB. (a) Current trajectory with $0 < D_c \leq 2/3$. (b) Switch drive signal with $0 < D_c \leq 2/3$. (c) Current trajectory with $2/3 < D_c \leq 1$. (d) Switch drive signal with $2/3 < D_c \leq 1$.

During the initial phase of the start-up, the current trajectory moves away from the center, so we need to adjust the switching signals to correct the trajectory. Fig. 6(a) shows the proposed corrected start-up current trajectory, with two segments of the current path being adjusted, corresponding to the switching signals of phase-A and phase-B. According to geometry, the durations of two signal segments are as follows:

$$T_{\mathrm{A}} = D_{\mathrm{c}}T_{\mathrm{h}}/3,\ T_{\mathrm{B}} = 2D_{\mathrm{c}}T_{\mathrm{h}}/3. \tag{8}$$

Similarly, Fig. 6(c) modifies two segments of the signal with the same duration as (8) and introduces a phase shift φ, ensuring that the trajectory remains unaffected after $2T_s/3$, and φ is defined as follows:

$$\varphi_{\mathrm{B}} = (2/3 + D_{\mathrm{c}}/3)T_{\mathrm{h}}. \tag{9}$$

In an ideal situation, a transformer would have zero resistance, the switch would operate without any dead time, and the current

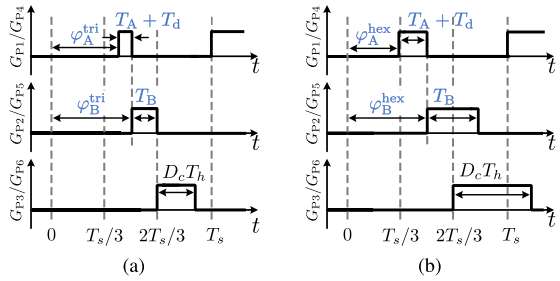

Fig. 7. Corrected start-up of 3p-DAB after compensation. (a) Switch drive signal with $0 < D_c \leq 2/3$. (b) Switch drive signal with $2/3 < D_c \leq 1$.

trajectory would accurately adhere to the corrected trajectory. However, in practical applications, it is crucial to account for and correct any deviations in the trajectory. There are two primary sources of error.

1) *Error caused by resistance:* The inductor current will remain unchanged when the upper (lower) switches are in the same state. However, due to transformer resistance, the current will gradually decay, causing the trajectory to deviate slightly from the corrected trajectory.
2) *Error caused by dead time:* The dead time reduces the actual ON-time. When there is an inductor current, the current will flow through the diode during the dead time, resulting in a voltage across the inductor. However, the inductor current is initially zero during the dead time when the switch is first turned ON. As a result, there is no voltage across the inductor, reducing the duration of the inductor voltage.

Therefore, it is necessary to compensate for current decay and dead time. The first switch adds a period of dead time compensation and phase shifts the signal to eliminate the 000 state. The compensated switching signal is shown in Fig. 7(a) and (b), where the phase shift is expressed as follows:

$$\begin{cases} \varphi_{\mathrm{A}}^{\mathrm{tri}} = (4/3 - D_{\mathrm{c}})T_{\mathrm{h}} - T_{\mathrm{d}},\ \varphi_{\mathrm{B}}^{\mathrm{tri}} = (4/3 - 2D_{\mathrm{c}}/3)T_{\mathrm{h}} \\ \varphi_{\mathrm{A}}^{\mathrm{hex}} = 2T_{\mathrm{h}}/3 - T_{\mathrm{d}},\ \varphi_{\mathrm{B}}^{\mathrm{hex}} = (2/3 + D_{\mathrm{c}}/3)T_{\mathrm{h}}. \end{cases} \tag{10}$$

B. Maximum Power Start-up Technology

In Section III-B, it is introduced that the initial dc-bias requires the start-up current to be gradually increased. In Section IV-A, we have introduced the technology of suppressing the dc-bias, allowing the start-up current to be increased to the maximum safe current at the beginning, so we do not need to consider initial dc-bias when studying the start-up technology.

Based on the output current and KCL equation, the following relationship can be obtained:

$$C_{\mathrm{o}}\frac{\mathrm{d}U_{\mathrm{s}}}{dt} = I_{\mathrm{s}} - I_{\mathrm{load}} = \frac{P}{U_{\mathrm{s}}} - \frac{U_{\mathrm{s}}}{R} = \frac{P_{\mathrm{N}}}{U_{\mathrm{s}}}p - \frac{U_{\mathrm{s}}}{R} = \frac{nU_{\mathrm{p}}T_{\mathrm{s}}}{8L}p - \frac{U_{\mathrm{s}}}{R}. \tag{11}$$

After rearranging (11), a first-order linear ordinary differential equation can be obtained. The analysis without load is the same as follows:

$$\begin{cases} \frac{\mathrm{d}U_{\mathrm{s}}}{\mathrm{d}t} + \frac{U_{\mathrm{s}}}{C_{\mathrm{o}}R} - \frac{nU_{\mathrm{p}}T_{\mathrm{s}}}{8C_{\mathrm{o}}L}p = 0 & \text{when loaded} \\ \frac{\mathrm{d}U_{\mathrm{s}}}{\mathrm{d}t} - \frac{nU_{\mathrm{p}}T_{\mathrm{s}}}{8C_{\mathrm{o}}L}p = 0 & \text{when unloaded.} \end{cases} \tag{12}$$

By solving the differential equation, the rising speed of the output voltage can be obtained

$$\begin{cases} \frac{\mathrm{d}U_{\mathrm{s}}}{\mathrm{d}t} = \frac{nU_{\mathrm{p}}T_{\mathrm{s}}}{8C_{\mathrm{o}}L}p \cdot e^{-\frac{t}{RC_{\mathrm{o}}}} & \text{when loaded} \\ \frac{\mathrm{d}U_{\mathrm{s}}}{\mathrm{d}t} = \frac{nU_{\mathrm{p}}T_{\mathrm{s}}}{8C_{\mathrm{o}}L}p & \text{when unloaded.} \end{cases} \tag{13}$$

It can be seen from (13) that in order to ensure the fastest start-up, that is, to ensure the maximum $\mathrm{d}U_{\mathrm{s}}/\mathrm{d}t$, the transmission power of 3p-DAB must be kept at the maximum value. In addition, (13) also shows the influence of other system parameters on the start-up speed. For example, the larger the output capacitance, the slower the start-up speed.

Therefore, the fast start-up is an optimization problem: Select a set of optimal quantities $(D^{\mathrm{opt}}, D_c^{\mathrm{opt}})$ to maximize the transmission power while satisfying the current limitation. Using the LM and KKT conditions, it can be expressed as

$$\begin{aligned} \min \quad & -P(D,D_c) \\ \text{s.t.} \quad & \begin{cases} i_{\mathrm{L.max}}(D,D_c) \leq I_{\mathrm{set}} \\ B_i(D,D_c) \leq 0, i = 1,\ldots,q \end{cases} \end{aligned} \tag{14}$$

where $P(D,D_c)$ is the transmission power, I_{set} is the current stress limit, $B_i(D,D_c)$ is the boundary condition of the operating mode, and q is the number of constraints.

The KKT conditions for the optimization program (14) are as follows:

$$\begin{cases} \mathcal{L}(D,D_c,\boldsymbol{\mu}) = -P(D,D_c) + \sum_{i=1}^{q}\mu_i B_i(D,D_c) \\ \left.\frac{\partial\mathcal{L}}{\partial D}\right|_{D=D^{\mathrm{opt}}} = 0, \quad \left.\frac{\partial\mathcal{L}}{\partial D_c}\right|_{D_c=D_c^{\mathrm{opt}}} = 0, \quad \mu_i \geq 0 \\ B_i(D_1,D_2) \leq 0, \quad \mu_i B_i(D_1,D_2) = 0, i = 1,\ldots,q \end{cases} \tag{15}$$

where $\mathcal{L}$ is the LM, μ_i is the KKT multiplier, and $\mu = [\mu_1,\mu_2,\ldots,\mu_q]$.

According to the value of k, we divide the start-up into four stages: 1) $0 < k \leq 1/2$, 2) $1/2 < k \leq 1$, 3) $1 < k \leq 2$, and 4) $k > 2$. We take the $0 < k \leq 1/2$ stage to analyze. By solving (15), we can get the solution illustrated in the Table III, where k_{i} is defined as follows:

$$k_{\mathrm{i}} = \frac{I_{\mathrm{set}}}{I_{\mathrm{N}}}. \tag{16}$$

The effective operating range and transmission power of each mode differ. Therefore, to obtain the global optimal solution, the transmission power for all modes is plotted in a new kk_{i} coordinate, as illustrated in Fig. 8. The mode with the largest transmission power is selected in segments, which is the global optimal solution. It is worth noting that the boundary function of the maximum power intersection of certain modes is complex, such as the boundary function between Modes I and IV (Mode V), so a linear boundary approximation is adopted, expressed as $k_{\mathrm{i}} + 3k/8 = 2$. Similarly, the global optimal solutions for other voltage ratios are determined sequentially, and all results are provided in the Table IV.

So far, the start-up procedure is as follows.

1) *Prestart stage:* Set the voltage and current limitation.

TABLE IV
GLOBAL OPTIMAL SOLUTIONS FOR FAST START-UP

Voltage range	Value range	Global optimal solutions
$0 < k \leq \frac{1}{2}$	$0 \leq k_{\rm i} \leq 1+2k-3k^2$	$D^{\rm opt} = \frac{k_{\rm i}}{3(1+3k)}, D_c^{\rm opt} = \frac{k_{\rm i}(1+k)}{3(1-k)(1+3k)}$
	$1+2k-3k^2 < k_{\rm i} \leq 2-3k/2$	$D^{\rm opt} = \frac{(1+k)k_{\rm i}+6k^2-8k+2}{3(3k^2-2k+3)}, D_c^{\rm opt} = \frac{(3-k)k_{\rm i}+12k^2-4k}{3(3k^2-2k+3)}$
	$2-3k/2 < k_{\rm i} \leq 2-k$	$D^{\rm opt} = \frac{k_{\rm i}+2(-1+k)}{3k}, D_c^{\rm opt} = 1$
	$2-2k < k_{\rm i} \leq 2$	$D^{\rm opt} = \frac{k_{\rm i}+3k-2}{6k}, D_c^{\rm opt} = 1$
$\frac{1}{2} < k \leq 1$	$0 < k_{\rm i} \leq 1+2k-3k^2$	$D^{\rm opt} = \frac{k_{\rm i}}{3(1+3k)}, D_c^{\rm opt} = \frac{k_{\rm i}(1+k)}{3(1-k)(1+3k)}$
	$1+2k-3k^2 < k_{\rm i} \leq 3-3k$	$D^{\rm opt} = \frac{k_{\rm i}+2(-1+k)}{3k}, D_c^{\rm opt} = 1$
	$3-3k < k_{\rm i} \leq 2-k$	$D^{\rm opt} = \frac{k_{\rm i}-1+k}{6k}, D_c^{\rm opt} = 1$
	$2-k < k_{\rm i} \leq 1+k$	$D^{\rm opt} = \frac{k_{\rm i}+2k-2}{3(3k-1)}, D_c^{\rm opt} = \frac{k_{\rm i}+8k-4}{3(3k-1)}$
	$1+k < k_{\rm i} \leq 2$	$D^{\rm opt} = \frac{k_{\rm i}-k}{3}, D_c^{\rm opt} = 1$
$1 < k \leq 2$	$0 < k_{\rm i} \leq -2+2k$	$D^{\rm opt} = \frac{-k_{\rm i}+2k-2}{3(1+k)}, D_c^{\rm opt} = \frac{k_{\rm i}+4}{3(1+k)}$
	$-2+2k < k_{\rm i} \leq 2$	$D^{\rm opt} = \frac{k_{\rm i}-k+1}{6}, D_c^{\rm opt} = 1$
$k > 2$	$0 < k_{\rm i} \leq 2$	$D^{\rm opt} = \frac{k_{\rm i}}{3(k-3)}, D_c^{\rm opt} = \frac{k_{\rm i}}{3(k-3)}$

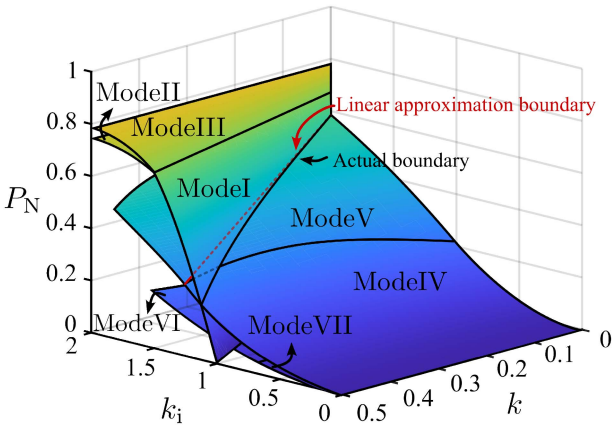

Fig. 8. Transmission power of seven modes.

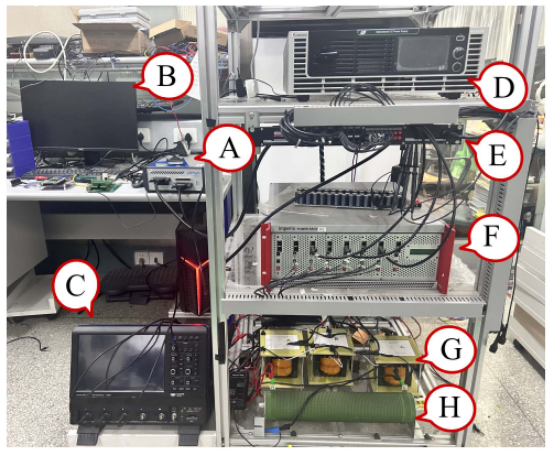

Fig. 9. Experimental setup of the laboratory prototype. A: Real-time controller, B: Monitor, C: Scope, D: dc power supply, E: Interface board, F: 3p-DAB power converters, G: High frequency three-phase transformer, and H: Load resistance.

2) *Bias suppression stage:* Calculate the optimal control solution refer to Table IV and start the dc-bias suppression.
3) *Fast start-up stage:* Repeatedly calculate the optimal control solution refer to Table IV.
4) *Steady stage:* Reach the reference voltage and switch the steady-state control strategy.

The detailed process of algorithm is shown in Algorithm 1.

V. EXPERIMENTAL VERIFICATION

In this section, we build a 3p-DAB prototype with parameters shown in Table V, and the prototype is shown in Fig. 9. The power switch used is the peb-sic-8024 half bridge power module. The MCU used is RT box rapid control system. The effectiveness of the proposed strategy is substantiated through various operations scenarios, complemented by an in-depth comparative analysis with the conventional method.

A. Initial DC-Bias Suppression Test

Figs. 10 and 11 show the experimental results of inductor current and current trajectory in the open-loop start-up experiment.

TABLE V
EXPERIMENTAL PARAMETERS

Parameter	Value
Primary-side voltage $U_{\rm p}$	60 V
Secondary-side voltage $U_{\rm s}$	80 V
Control period $T_{\rm c}$	100 μs
Switching frequency f	10 kHz
Transformer turns radio n	1
Output capacitance $C_{\rm o}$	520 μF
Inductor current limitation	6 A/4 A
Resistance load R	40 Ω/80 Ω
Total leakage inductance [$L_{\rm a}$ $L_{\rm b}$ $L_{\rm c}$]	[97.81 93.14 102.98] μH
Winding resistance [$R_{\rm a}$ $R_{\rm b}$ $R_{\rm c}$]	[0.96 0.84 0.86] Ω

Fig. 10(a)–(c) shows the results of the direct start-up experiments with $D = 0.4$, $D = 0.8$, and $D = 1$, and Fig. 11(a)–(c) shows the start-up result with the proposed initial dc-bias suppression technology.

In the conventional start-up experiments, the current trajectories of the three working conditions are seriously deviated

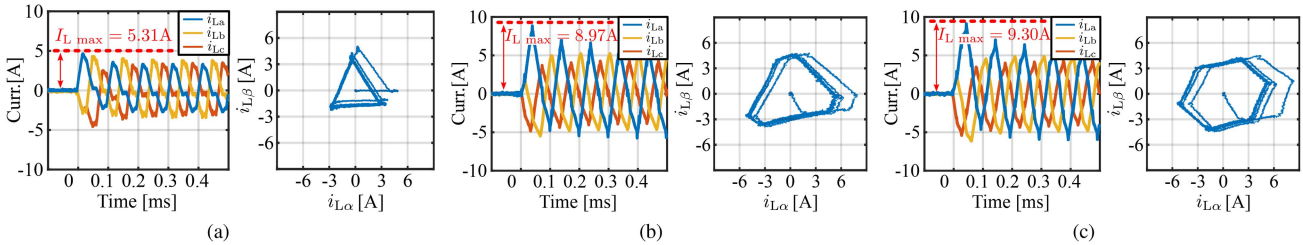

Fig. 10. Experimental waveforms of the inductor current and current trajectory in the direct start-up. (a) $D_c = 0.4$. (b) $D_c = 0.8$. (c) $D_c = 1$.

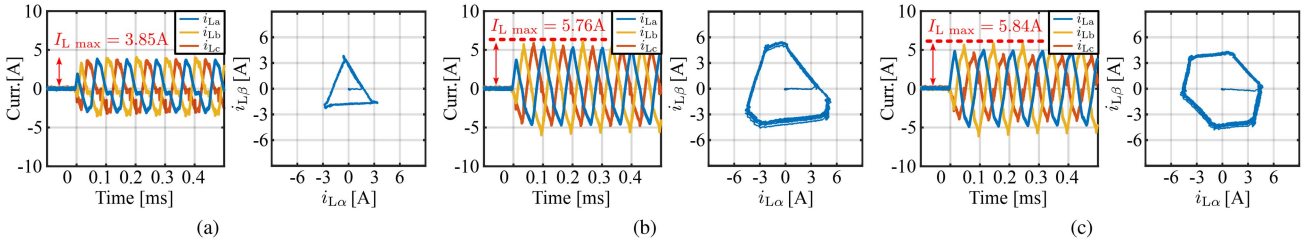

Fig. 11. Experimental waveforms of the inductor current and current trajectory in initial DC-bias suppression start. (a) $D_c = 0.4$. (b) $D_c = 0.8$. (c) $D_c = 1$.

Algorithm 1: Algorithm of Start-up.

Input: I_{set}, u_p, u_s, u_s^*
Output: D, D_A, D_B, D_C, φ_A, φ_B, φ_C

```
Initialize k_i = I_set/I_N, is_first_period = 1, is_stop = 0;
while u_s < u_s^* do
    Calculate k = u_s/u_p;
    Calculate the global optimal solutions of D and D_c using Table IV;
    if is_first_period == 1 then
        Calculate D_A, D_B, φ_A, φ_B using (8) and (10);
        D_C = D_c and φ_C = 2/3;
        is_first_period = 0;
    else
        D_A = D_B = D_C = D_c;
        φ_A = 0, φ_B = 1/3, φ_C = 2/3;
    end if
end while
while true do
    Steady control strategy (PI controller or other optimization strategies);
    if is_stop == 1 then
        Shut down;
        break;
    end if
end while
```

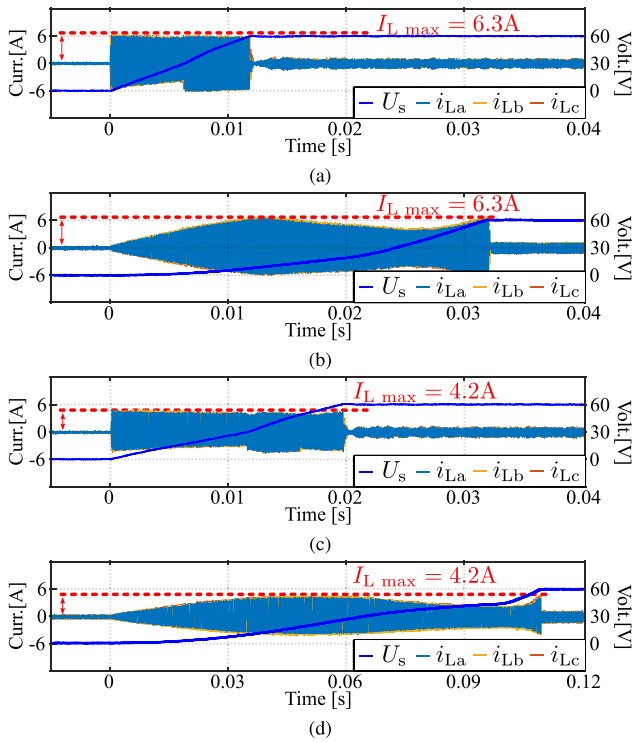

Fig. 12. Experimental waveforms of inductor current and output voltage. (a) $I_{set} = 6$ A. (b) $dD_c/dt = 0.05\ ms^{-1}$ and $dD/dt = 0.025\ ms^{-1}$. (c) $I_{set} = 4$ A. (d) $dD_c/dt = 0.01\ ms^{-1}$ and $dD/dt = 0.015\ ms^{-1}$.

from the origin. The current stress is also greater than the steady-state peak value. The current stress of the first start-up cycle is $I_{Lmax(a)} = 5.31$ A, $I_{Lmax(b)} = 8.97$ A, and $I_{Lmax(c)} = 9.30$ A, respectively. When the proposed dc-bias suppression technology is used, it can be seen that the current trajectory at start-up under the three working conditions is at the center of the origin, and the three-phase inductor current reaches the steady state value in the first cycle, which is $I_{Lmax(a)} = 3.85$ A, $I_{Lmax(b)} = 5.76$ A, and $I_{Lmax(c)} = 5.84$ A, respectively. Compared with direct start-up, the current stress is reduced by 27.5%, 35.8%, and 37.2%, respectively, proving that the proposed method can effectively suppress the dc-bias under various starting conditions.

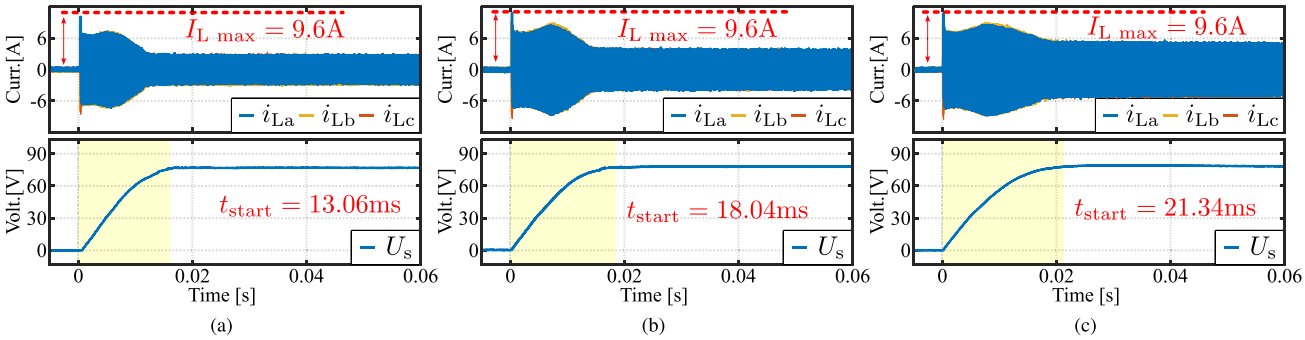

Fig. 13. Experimental waveforms of inductor current and output voltage in direct start-up. (a) No-load. (b) Half-load. (c) Full-load.

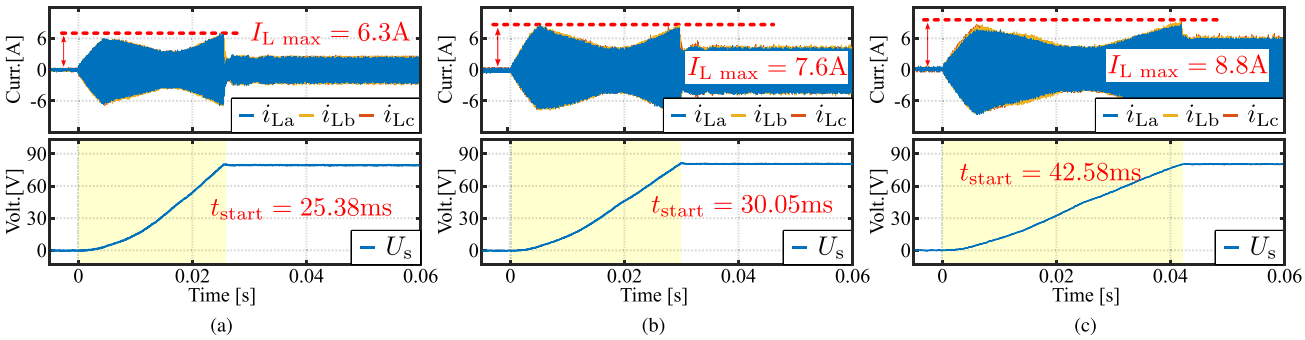

Fig. 14. Experimental waveforms of inductor current and output voltage in conventional start-up. (a) No-load. (b) Half-load. (c) Full-load.

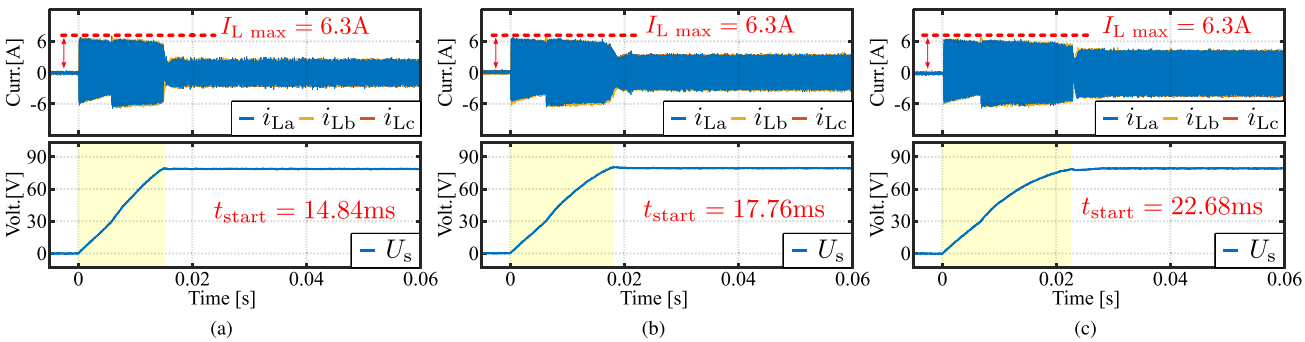

Fig. 15. Experimental waveforms of inductor current and output voltage in proposed start-up. (a) No-load. (b) Half-load. (c) Full-load.

B. Current Limitation Change Test

We configured the load at 80 Ω and set the output voltage to 60 V, changing the current limitation from 6 to 4 A. Since direct start-up cannot control the starting current, it is not included in the comparison. Fig. 12(a) and (b) shows the experimental waveforms when the current is limited to 6 A. The proposed method simply adjusts I_{set} to 6 A, and leading to a maximum three-phase current of 6.3 A due to the transformer's phase asymmetry. In contrast, the conventional method requires adjusting two parameters, $\mathrm{d}D_{\mathrm{c}}/\mathrm{dt}$ and $\mathrm{d}D/\mathrm{dt}$. However, the absence of quantitative calculation means these can only be determined through extensive trial and error, eventually setting $\mathrm{d}D_{\mathrm{c}}/\mathrm{dt} = 0.05\ \mathrm{ms}^{-1}$ and $\mathrm{d}D/\mathrm{dt} = 0.025\ \mathrm{ms}^{-1}$. Fig. 12(c) and (d) shows the start-up experimental waveforms when the current is limited to 4 A. The proposed method directly changes I_{set} to 4 A, and the maximum three-phase current reaches 4.2 A. In contrast, the conventional method requires multiple trials to finally set $\mathrm{d}D_{\mathrm{c}}/\mathrm{dt} = 0.01\ \mathrm{ms}^{-1}$ and $\mathrm{d}D/\mathrm{dt} = 0.015\ \mathrm{ms}^{-1}$. It can be observed that the proposed method is significantly simpler compared to the conventional method. Furthermore, it is evident that in the conventional method, achieving a lower current limitation condition necessitates a significant reduction in $\mathrm{d}D_{\mathrm{c}}/\mathrm{dt}$ and $\mathrm{d}D/\mathrm{dt}$, which substantially prolongs the start-up time. The start-up time of the conventional method increases from 31.77 to 108.46 ms, marking a 241.38% extension, while the proposed method only extends the start-up time from 11.82 to 19.63 ms, a mere 66.07% increase. This further underscores the superiority of the proposed method.

C. Load Condition Change Test

Fig. 13 shows the experimental results of the direct start-up and set the output voltage to 80 V, including no-load, half-load, and full-load. Under the regulation of the PI controller, full

power start-up is achieved under all three load conditions, with duty cycles of $D = 0.5$ and $D_c = 1$. The experimental results show that the direct start-up speed is fast, and its start-up times are: Fig. 13(a) no-load: 13.06 ms, Fig. 13(b) half-load: 18.04 ms, Fig. 13(c) full-load: 21.34 ms. However, the start-up current reaches 9.6 A in all cases, which limits its applicability only to situations with lower input voltages. Therefore, although direct start-up has the advantage of fast speed, its reliability is low.

Fig. 14 shows the experimental results of the conventional start-up. To thoroughly compare the start-up speed of the conventional start-up, we adjust the parameters and set the current limitation to about 6.3 A. The two parameters are set as follows: $\mathrm{d}D_c/\mathrm{dt} = 0.14\ \mathrm{ms}^{-1}$ and $\mathrm{d}D/\mathrm{dt} = 0.016\ \mathrm{ms}^{-1}$. The start-up times under the three conditions are Fig. 14(a) no-load: $t_{\mathrm{start}} = 25.38$ ms, Fig. 14(b) half-load: $t_{\mathrm{start}} = 30.05$ ms, Fig. 14(c) full-load: $t_{\mathrm{start}} = 42.58$ ms. From the experimental waveform, it can be seen that in the conventional start-up process, the current only reaches its maximum value when D_c reaches 1 or the output voltage reaches the set value. In other stages of start-up, the current is far below the limitation, which results in the power converter being unable to fully utilize its starting performance and thus becomes the main factor restricting the speed. Therefore, conventional start-up methods improve reliability, but sacrifice start-up speed.

Fig. 15 shows the experimental results of the proposed start-up. We set the current limitation to 6 A. The experimental data shows that under different load conditions, the starting current can be stably maintained near the set value (however, due to the asymmetry of the three-phase inductance, the actual current stress is 6.3 A). The proposed start-up significantly improves the reliability of the converter. In addition, this strategy fully leverages the performance advantages of the power converter and significantly accelerates the start-up speed. Specifically, the start-up times under the three conditions are: 1) Fig. 15(a) no-load: $t_{\mathrm{start}} = 14.84$ ms, 2) Fig. 15(b) half-load: $t_{\mathrm{start}} = 17.76$ ms, and 3) Fig. 15(c) full-load: $t_{\mathrm{start}} = 22.68$ ms. Compared to the direct start-up method, the proposed start-up exhibits only a minimal reduction in start-up speed. Compared to the conventional method, the start-up speed under three working conditions (no-load, half-load, and full-load) increased by 41.53%, 44.41%, and 49.97%, respectively, [corresponding to Fig. 15(a)–(c)] fully demonstrating the superiority of the proposed method.

D. Overall Comparison

Overall, a comparison of direct start-up, conventional start-up, and the proposed start-up methods is provided. Direct start-up is simple and fast, but lacks the ability to regulate the start-up current, resulting in low reliability. Conventional start-up improves reliability with current regulation but sacrifices the start-up speed. In addition, the conventional method involves complex parameter tuning and is significantly affected by load. In contrast, the proposed start-up method offers a simple and effective way to regulate the start-up current, is unaffected by load variations, and achieves both high speed and high reliability. The comparison results are shown in Table VI.

TABLE VI
COMPARISON OF METHODS

	Direct start-up	Conventional start-up	Proposed start-up
Simplicity	High	Low	High
Speed	Fast	Slow	Fast
Reliability	Low	Medium	High
Current	High	Adjustable	Adjustable

VI. CONCLUSION

The 3p-DAB converters are increasingly becoming essential components of microgrids and dc grid. Consequently, the capability to realise a fast and reliable start-up process is a critical feature. In this article, a fast and reliable start-up strategy for 3p-DAB is proposed, which maximizes the current-carrying performance of the converter and maintains the maximum power output in the safe current range during the start-up. There are three main contributions. 1) The current stress and transmission power of the S-PWM are described in detail. 2) The current trajectory is controlled to realize the reliable start-up without initial dc-bias. 3) Using coordinate transformations and segment comparison, we obtain the global maximum power output solutions under the current limit and realize a maximum power start-up. Finally, experimental results demonstrate that the proposed strategy remarkably outperforms conventional solutions across various test conditions. Our future research will concentrate on developing a steady state control strategy for the 3p-DAB converter.

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