A Cooperative Power Flow Control Strategy for Low-Voltage DC Microgrid Clusters

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***Abstract*—Hierarchical control strategies and active power flow controllers represent distinct approaches aimed at enabling flexible power distribution among different dc microgrids within a cluster. To enhance reliability and responsiveness in the face of uncertainties, particularly leveraging intermittent power flow control (IPFC), this article introduces a cooperative power flow control strategy. This method integrates an active interlinking converter featuring hysteresis control into traditional hierarchical control frameworks, activating the IPFC strategy in response to significant reference changes or uncertainties and naturally ceasing upon achieving convergence goals. This approach not only leverages the structural benefits of traditional hierarchical control but also mitigates its inherent response to uncertainties, which can be critical in dynamic operational scenarios. Importantly, it minimizes the need for large-scale, high-cost components and avoids additional switching losses typical of traditional power flow controllers. Furthermore, the proposed strategy is enhanced through the implementation of a virtual closed-loop control methodology, promising accelerated convergence rates and heightened operational reliability. Theoretical insights are validated through both simulation studies and experimental demonstrations using a hardware prototype.**

***Index Terms*—Hierarchical control, interlinking converter, low-voltage dc (LVDC) microgrid (MG) cluster, power flow control.**

I. Introduction

DC MICROGRIDS (MGs) are increasingly garnering attention due to their advantages over traditional ac MGs, including superior efficiency, cost-effectiveness, and simplified control design [1]. Furthermore, the aggregation of numerous low-voltage dc (LVDC) MGs, as exemplified in data centers, all-electric aircraft, and shipboard power distribution systems, into clusters yields substantial advantages. These include facilitating adaptable power distribution, bolstering resilience, enabling cost-effective energy allocation, reducing losses, and optimizing load responsiveness through the integration of distributed generations [2]. However, LVDC MGs incorporating renewable energy sources (RESs) are considered weak grids due to low inertia and high grid impedance, typically operating at smaller scales ranging from tens to hundreds of kilowatts [3]. Consequently, these LVDC MGs are susceptible to variations in reference points and uncertainties stemming from changes in system load capabilities and RES connections [4].

In this context, clusters of LVDC MGs can be seen as forming a "weak–weak" network, exacerbating stability issues. Thus, effective power management becomes pivotal in system control. The transmission of power through dc cables among distributed LVDC MGs plays a crucial role in ensuring stability and flexible power distribution within the cluster, contingent upon factors such as cable resistance and voltage differentials across cable ends [5]. Typically, this is managed by coordinated distributed control systems operating at higher control levels [6].

There are two ways reported in the literature that can be used to control the power flow in the cluster. The first and traditional way is to utilize hierarchical control strategies. Hierarchical control strategies [7], [8] have been proposed to fulfill the aforementioned control objectives in dc MGs. These strategies entail the deployment of a coordinated control architecture that integrates power flow control to influence the dc voltage reference within the local autonomous dc voltage control system [9]. In the event of a dc bus fault occurring in any one of the LVDC MGs, the cluster system will inevitably experience the impact before the dc breakers have an opportunity to open, despite their presence [10]. Consequently, the reliability of the LVDC MGs cluster is significantly compromised from this perspective [11]. For recent research in hierarchical control, in [12], a hierarchically coordinated control scheme for dc MG cluster under uncertainties is proposed. A distributed tertiary controller which is robust against physical (i.e., MG disconnection) and cyber (i.e., communication link) failures is proposed in [8]. A unifying hierarchical control scheme based on distributed communication is proposed where the tie-line power flow control based on a pinning control strategy is unified with the distributed optimization and average voltage regulation control loops in [13]. The advantages of these controllers are that they do not need extra hardware devices meaning less cost and no maintenance requirement. However, these control strategies have complex control structures and intensive computation, resulting in relatively long response time and convergence time.

The second approach involves interconnecting dc MGs through dc–dc converters unit. In order to increase operational reliability and enable flexible interlinking power flow control,

Received 28 August 2024; revised 21 December 2024; accepted 6 February 2025. Date of publication 20 February 2025; date of current version 14 April 2025. This work was supported by the National Science Foundation Council of China under Grant 52377194. Recommended for publication by Associate Editor A. Davoudi. *(Corresponding author: Fei Gao.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3543871.

Digital Object Identifier 10.1109/TPEL.2025.3543871

active interconnecting dc–dc converters [14] can be utilized to connect multiple LVDC MGs in the cluster. The LVDC MGs within the cluster are interconnected using a dc–dc converter to facilitate controlled power exchange through a dc tie-line. Each individual LVDC MG maintains independent voltage regulation. In addition to the interlinking tie-line and dc–dc converter, the power flow of different connected MGs is transferred to the controller of the interlinking converter through low bandwidth communication [15]. These interconnected converters are also known as power flow controllers (PFCs) [16]. However, due to its expansive design and inherent power loss, PFC is not feasible in many applications where circulation current can be avoided by redesigning tie-line placement [17]. Numerous sophisticated PFC technologies have been innovated to enhance the efficiency of power flow control [18]. Upon assessing their application range, these advanced PFC systems can be classified into two distinct categories: full-voltage compensation range PFCs and fractional voltage compensation range PFCs.

Full-voltage compensation range PFCs offer a large controllable range, which is up to the dc bus voltage, and can manage a wide range of uncertainties in dc MG cluster. In [19], a PFC is introduced, utilizing two bidirectional buck–boost converters to interlink adjacent dc clusters. This system incorporates a decentralized control strategy comprising both voltage droop control and midpoint voltage control methods to manage power exchange and minimize transmission line losses. Nonetheless, the potential stability challenges arising from the parallel connection of two bidirectional dc–dc converters on the same line are not addressed in this approach. In [20], a centralized control algorithm that consists of a fast lambda iteration and a fast voltage iteration algorithm based on a multiport converter is developed to address the power loss problem of power flow control in dc MG cluster. Similarly, in [21], a PFC utilizes a four-port dc–dc converter alongside an innovative distributed state-of-charge-based droop control algorithm aimed at minimizing power losses by reducing power flow magnitude within the dc MG cluster. In [22], a multiport interlinking converter integrating three-level neutral point clamped modules with pluggable full-bridge modules and its global power sharing strategy involving the intrinsic droop characteristics are proposed to proactively manage the power imbalance between power generation and consumption in DCMG clusters. Although full-voltage compensation range PFCs effectively handle the unbalanced power distribution resulting from diverse uncertainties and safeguard against transient faults, their inherent larger size, elevated costs, and increased energy losses inevitably restrict their applicability to more specialized scenarios.

On the other hand, fractional voltage compensation range PFCs can offer smaller sizes and lower costs. In [23], a novel coordinated power control framework involving isolated bidirectional dc–dc converters, which adopts standard proposed droop control for dc MGs and a unified control for active PFCs, is proposed for dc MG cluster. Similarly, a load flow converter that works as active PFCs in the cluster is proposed to interconnect two adjacent dc MGs and control bidirectional power flow between them to address the problems associated with uncertainty of renewable energy generation systems in [24]. In [25], a novel bidirectional hybrid dc–dc converter suitable as an interface between dc MGs, which gives the advantage of a high voltage conversion ratio without using a transformer, is proposed. The advantages of fractional voltage compensation range PFCs are that they can respond to uncertainties very fast and can make the system robust to many uncertainties which are caused by the uncertain and intermittent nature of RESs [26]. However, these aforementioned fractional voltage compensation range PFCs may face difficulties in accommodating wide voltage ranges during substantial transients and are constrained in their capacity to effectively mitigate transient faults.

This article addresses the aforementioned challenges by introducing the concept of intermittent power flow control (IPFC) derived from the full-voltage compensation range PFC concept. The term "intermittent" signifies that this control strategy actively operates as an interconnected device during transient periods induced by reference changes or uncertainties while automatically deactivating during stable conditions. This approach minimizes the switching frequency of power devices, thereby reducing switching losses within the interconnected device. Recent advancements enhance the efficacy of power flow control within LVDC MG clusters by altering the control structure or converter topologies in the power flow control. In contrast to recent research, the article proposes a PFC situated outside the traditional hierarchical controller, incorporating an interconnected dc–dc converter with a tailored control method. Its objective is to effectively manage unbalanced power flow within LVDC MG clusters. Furthermore, the article develops an enhanced strategy to improve control performance, emphasizing rapid convergence and narrow current ripple. The main contributions of this article are highlighted as follows.

1) A cooperative power flow control which contains the hysteresis control module and the hierarchical control module is developed for the LVDC MG cluster. The hysteresis control module involves an active interconnected device featuring a four-switch buck–boost converter topology with its corresponding hysteresis control.
2) A virtual closed-loop-based improvement strategy based on the basic principle of the proposed cooperative control strategy is developed to facilitate better control performance. The virtual closed-loop-based improvement strategy ensures that the fast convergence speed and small hysteresis band can be obtained at the same time.

The rest of this article is organized as follows. Section II derives the uncertainty modeling of the LVDC MG cluster under traditional hierarchical control considering reference tracking and disturbance uncertainty during operation. Section III introduces the basic control principle of the proposed IPFC, which involves a buck/boost converter with a tailored control strategy and hierarchical control along with the selection of the hardware parameters and control parameters. Section IV develops a virtual closed-loop-based improvement to obtain faster convergence speed. Validation of the analysis with simulation and experimental studies is presented in Section V. Section VI draws the conclusion.

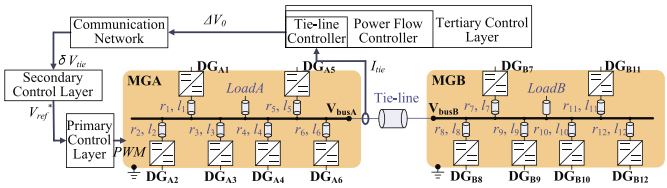

Fig. 1. Single-line diagram representation and associated radial graphs of two independently owned LVDC MG interconnected by a tie-line under hierarchical control.

II. Uncertainty Modeling in Cluster Under Hierarchical Control

This section elaborates on the operational capabilities of interconnected LVDC MGs employing tie-lines within a hierarchical control framework while also outlining the challenges encountered in managing power flow within such LVDC MG clusters. Furthermore, it tackles the complexities of uncertainty modeling, thereby ensuring a representation of real-time dynamics.

A. Hierarchical Control in LVDC MG Cluster

Power flow control utilized in the LVDC MG cluster consists of cluster control and tie-line control [27]. In cluster control, each MG runs a separate consensus control to improve the reliability of the system [28]. In tie-line control, the system voltage of MG can be adjusted to a specific level during different transients to manage the impact of uncertainties. Under such a coupled power flow control strategy, the whole MG can act as a single source. To further explain the function and characteristic of the power flow control in the LVDC MG cluster, two radial type LVDC MGs connected via a tie-line forming a cluster is analyzed in this article, as shown in Fig. 1. In this system, the tie-line current is measured and sent to the tie-line controller. From the functional perspective, the tie-line controller controls the power flow on the tie-line. From the hierarchical control scheme perspective, the tie-line controller belongs to the tertiary control layer of the hierarchical control scheme. The tie-line controller then generates the term ΔV_0 after comparing the reference current with the tie-line current and then processing the error to a PI controller. After that, δV_{tie} will be sent to the secondary control layer in each MG that contains an average voltage regulator (δV_{avr}) and current sharing regulator (δV_{csr}) through the communication network with a separate controller. The term δV is then added with the nominal value of the bus voltage (V_{ref}) to generate the reference average voltage (V_o), which is then processed to the primary control level.

Finally, the reference voltage to the primary control level can be obtained as

$$\begin{aligned} V_{\text{ref}}* &= V_{\text{ref}} + \delta V \\ \delta V &= \delta V_{\text{tie}} + \delta V_{\text{avr}} + \delta V_{\text{csr}} \end{aligned} \tag{1}$$

where

$$\delta V_{\text{tie}A} = V_{\text{bus}A} K_{p\text{tie}} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}}\right) + V_{\text{bus}A} \frac{K_{i\text{tie}}}{s} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}}\right)$$

$$\delta V_{\text{avri}A} = \left(K_{psv} + \frac{K_{isv}}{s}\right) \cdot \left(V_{\text{rated}} - V_{avi,A}\right)$$

$$\delta V_{\text{csri}A} = \left(K_{psc} + \frac{K_{isc}}{s}\right) \cdot \left(I_{avi,A} - I_{iA}\right) \tag{2}$$

where V_{rated} represents the rated voltage of MGA, I_{iA} represents the output current of converter i in MGA, $K_{p\text{tie}}$ and $K_{i\text{tie}}$, K_{psv} and K_{isv}, and K_{psc} and K_{isc} are the corresponding proportional and integral gains for the tie-line controller, average voltage regulator, and current sharing regulator, respectively. $V_{avi,A}$ and $I_{avi,A}$ represent the estimated average voltage and current of the converter i in MGA, respectively.

Although hierarchical control can control power flow in the DC MG cluster without the need for additional power electronic hardware, it may exhibit complex control process due to the communication between different control levels in hierarchical control. The bandwidth of each hierarchical control outer loop is always designed lower than the inner loop bandwidth to avoid the interaction of inner and outer control loops. When hierarchal control is used with consensus algorithm, the overall convergence rate of the control further decreases. Although there are no communication delays, the bandwidth of the consensus in the hierarchical control can be designed arbitrarily high. However, the bandwidth of the consensus control loop has upper limits due to communication delays, and, in addition to accounting for uncertainties, it is not advisable to set the bandwidth of the consensus algorithm arbitrarily large. To be modest, considering the switching frequency of several hundred kilohertz in the single dc–dc converter within the MG, the bandwidth of the inner control loop is typically in the range of tens of kilohertz. To avoid interaction with the primary control loop, the bandwidth of the secondary control loop is around a few kilohertz and when consensus is added, the bandwidth is generally reduced to less than one kilohertz. To put it briefly, fast uncertainties in one MG can adversely affect the performance of other MGs, potentially compromising the reliability of the entire cluster.

B. Uncertainty Modeling Analysis of Cluster

A comprehensive set of constraints arises from both real parametric uncertainty and disturbance uncertainty, presenting intricate challenges. These uncertainties can induce disparate response characteristics across a broad spectrum of reference tracking and disturbance scenarios during system operation. ΔZ signifies the parametric uncertainty within the Thevenin equivalent impedance, traditionally characterized by two specific conditions. The first pertains to situations where the line resistances among MGs are different from each other within a cluster. The second scenario involves nonfunctional secondary control, where local droop control assumes primary responsibility for managing the voltage and current of MGs, considered the upper limit of parametric uncertainty. ΔV_u denotes disturbance uncertainty affecting MGs within the cluster, typically stemming from control system faults, with an average value ranging from 1% to 2% (V_{rated}) [8]. By comprehensively considering these aforementioned uncertainties, one can delineate the inherent limitations of the system.

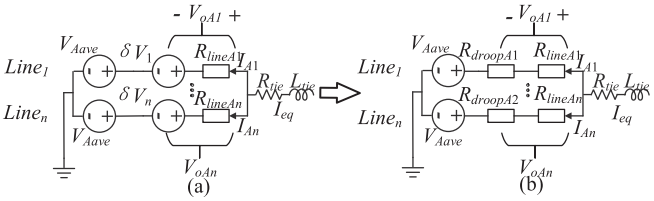

Fig. 2. Equivalent circuit of uncertainty modeling during (a) steady state and (b) communication failure.

For a deeper exploration of the cluster's uncertainty characteristics, a communication failure is considered a crucial fault scenario in this article, as depicted in Fig. 2. Assume MGA consists of *n* converters. V_{Aave} represents the average value of the dc–dc converter output voltage within MGA. V_{oAi} represents the aggregation of voltage uncertainties and voltage adjustments, as well as the impact of line resistance ($R_{\text{line}i}$) of line$_i$, while I_{Ai} denotes the current generated by the power electronics converter #*i* in MGA. δV_i represents the balancing voltage of line$_i$. To enhance local reliability, the secondary consensus within the communication network of MG is constrained to the respective MG itself. A simplified analysis of communication failures within the LVDC MG cluster and its ramifications are presented in this section. For simplicity and validity, a cluster consisting of two LVDC MGs with a tie-line is considered. When secondary control works, current sharing and voltage restoration can theoretically be attained. The steady-state model for line$_i$ and the whole MGA can be derived from the aforementioned considerations.

For the line$_i$ in MGA

$$\delta V_i + I_{Ai} \cdot R_{\text{line}Ai} = V_{oAi}. \tag{3}$$

For the whole MGA with *n* lines

$$\sum_{i=1}^{n} \delta V_i + \sum_{i=1}^{n} I_{Ai} \cdot R_{\text{line}Ai} = \sum_{i=1}^{n} V_{oAi}. \tag{4}$$

Considering that the secondary control objectives: current sharing and voltage restoration both have been achieved in MGA, the equation of the current generated by power electronics converter *i* in MGA and the balancing voltage term δV_i in line$_i$ can be obtained as

$$\begin{cases} I_{A1} = \cdots = I_{Ai} = \cdots = I_{An} = I_{Ao} \\ \sum_{i=1}^{n} \delta V_i = 0. \end{cases} \tag{5}$$

Then the voltage term and current term in (4) can be changed into

$$\begin{cases} V_{\text{eq}} = V_{oAi} = V_{oA} \\ \sum_{i=1}^{n} V_{oAi} = nV_{oA} \end{cases} \tag{6}$$

$$I_{\text{eq}} = nI_{Ao}. \tag{7}$$

Then (4) can be obtained as follows:

$$I_{Ao} \cdot \sum_{i=1}^{n} R_{\text{line}Ai} = n\Delta V_{oA}. \tag{8}$$

By combining (6)–(8) together, the equivalent Thevenin uncertainty impedance (Z_{oA}) of MGA with *n* lines equals

$$Z_{oA} = \frac{V_{\text{eq}}}{I_{\text{eq}}} = \frac{V_{oA}}{nI_{Ao}} = \frac{\frac{I_{Ao} \cdot \sum_{i=1}^{n} R_{\text{line}Ai}}{n}}{nI_{Ao}} = \frac{\sum_{i=1}^{n} R_{\text{line}Ai}}{n^2}. \tag{9}$$

As is observed in (9), the equivalent Thevenin uncertainty impedance (Z_{oA}) of the MGA during steady state is primarily influenced by line resistances of different lines in MGA and stays at a relatively small level. However, if a communication failure occurs in the secondary control layer within MGA, it becomes inoperative, preventing consensus from being achieved in the secondary control layer. This situation leads to alterations in the adjustment of voltage in hierarchical control, ultimately leading to the situation where the secondary controller fails to compensate for the voltage drop caused by the local droop control in the primary controller. The equivalent circuit is shown in Fig. 2. $R_{\text{droop}i}$ represents the droop resistance of line$_i$

$$V_{oAi} = R_{\text{line}i} \cdot I_{Ai} + V_{\text{droop}i}. \tag{10}$$

Meanwhile, the equivalent Thevenin impedance Z_{oAi} of line$_i$ can be calculated as

$$Z_{oAi} = \frac{V_{\text{eq}i}}{I_{\text{eq}i}} = R_{\text{line}i} + R_{\text{droop}i} \tag{11}$$

$$Z_{oA} = Z_{oA1} // \ldots // Z_{oAi} // \ldots // Z_{oAn}. \tag{12}$$

Upon comparing (9) and (12), it can be inferred that the occurrence of a communication failure in MGA may change the equivalent Thevenin uncertainty impedance (Z_{oA}) of the MGA, and then the power flow will be affected. The secondary controller compensates for the voltage drop caused by the droop control during steady state and slow transients when the secondary controller is working properly. However, the equivalent resistance of the droop gain is usually set several times the line resistance to achieve the accurate current sharing when secondary control is not enabled. When adding the secondary controller to work cooperatively with the primary controller, as the control bandwidth of the secondary controller is much smaller than that of the primary controller, the control process of the primary controller can be neglected. Meanwhile, the primary controller always works and the droop parameters are not changed. When the secondary controller is not working properly, the influence of the droop parameters will be revealed, resulting in much larger equivalent impedance (Z_{oA}) of MGA. Furthermore, based on the steady-state analysis of the cluster with hierarchical control, it is evident that fast transients such as communication failures, the activation/deactivation of large loads, or short-circuit faults in one MG can disrupt the steady-state model of the respective MG. This disruption may propagate to other MGs through tie-line, as shown in Fig. 2, ultimately diminishing the reliability of the entire cluster.

C. Performance of the Cluster During Different Uncertainties

The uncertainty modeling under hierarchical control during transients is formulated and scrutinized in Fig. 3. Upon considering the tie-line current influence on the reliability of the cluster system, the uncertainty model of the system under

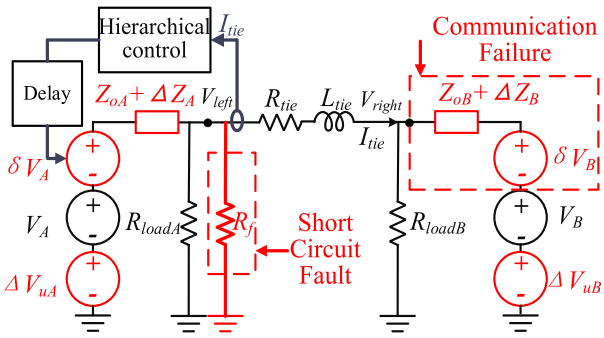

Fig. 3. Equivalent circuit of the cluster considering voltage uncertainties, communication failure, and short-circuit fault.

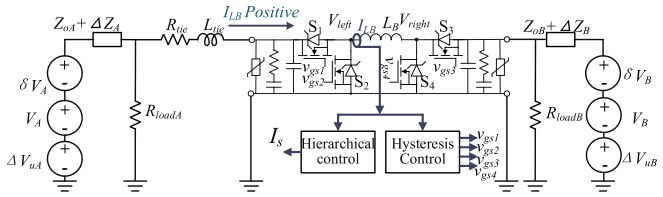

Fig. 4. Equivalent circuit of the LVDC MG cluster under the proposed cooperative power flow control considering transients.

various uncertainties can be obtained, as shown in Fig. 3, where the uncertainty parameters ΔZ, ΔV_u, and R_f in the cluster will modify according to the depth of fault and type of fault.

In the depicted equivalent uncertainty model of the LVDC MG cluster illustrated in Fig. 3, various uncertainties are considered, encompassing scenarios such as communication failures, short-circuit faults, and voltage fluctuations. When a communication failure occurs within an MG, the MG's impedance (Z_o) may exhibit an uncertainty parameter ΔZ, potentially leading to changes in the output voltage δV. Similarly, during a short-circuit event, the load resistance (R_{load}) within the MG may be subject to an uncertainty parameter (R_f), and the MG's impedance (Z_o) might also experience an uncertainty parameter ΔZ. Simultaneously, as the focus of this article is on LVDC MGs that are stabilized by a set of power electronics converters, here referred to as voltage balancing converters (VBCs). In the event of voltage disturbances within an MG, the MG's voltage could manifest an uncertainty parameter ΔV_u. Furthermore, when faced with large uncertainties, VBC within the MG may undergo a transition from its initial role as a voltage source to function as a current source. Utilizing this comprehensive uncertainty model encompassing various uncertainties, it becomes feasible to assess the transient limits governing system reliability, thereby deriving better power flow control design.

As a short summary, when uncertainties happen in clusters, MG voltage, equivalent impedance, and MG loads may undergo different depths of uncertainties. However, if the tie-line current can be controlled faster and more accurately under the abovementioned conditions, the reliability of the system can be improved. Ensuring accuracy is crucial, especially when the MG operates at its power limit and lacks sufficient capacity for transient power reserve, this need becomes even more stringent when critical loads, with tight voltage tolerance requirements, are connected to the MG.

III. Proposed IPFC Topology and Control Principle

Hierarchical control can compensate for the transient current in tie-line by initiating voltage adjustments to regulate voltages at both ends. However, the communication between different control levels in hierarchical control may make it susceptible to uncertainties in voltage and impedances along the tie-line, potentially prolonging transient processes and leading to additional power loss and struggle to address fast transients, as discussed in the previous section.

To overcome the above-mentioned challenges, a method for power flow control in the LVDC MG cluster is proposed in this section, aiming to address the limitations of both hierarchical power control and hardware-based approaches. By integrating a buck/boost converter with a tailored control strategy to work corporately with the hierarchical control, the proposed method that activates power flow control of buck/boost converter during significant transients and ceases operation once current error diminishes, resulting in a more compact, cost-effective design with enhanced transient response effectively reduces switching loss, eliminates transient time, and can compensate for many different uncertainties in the cluster.

A. Control Principle of IPFC

Fig. 4 illustrates the equivalent circuit of the proposed cooperative power control method within the simplified LVDC MG cluster. It includes the hardware-based approach and the hierarchical control. δV represents the control voltage generated by the hierarchical control. ΔV_u and ΔZ represent the uncertainty in voltage and impedance of both ends of the tie-line, respectively. V_{MGA} represents the total voltage of MGA, which contains reference command V_A and uncertainty voltage ΔV_{uA}. V_{left} and V_{right} represent the S_2 and S_4 MOSFETs drain-source voltages, respectively. The equivalent circuit of the buck/boost converter with modified current-mode hysteresis control method in the simplified LVDC MG cluster is also illustrated in Fig. 4. It includes a buck/boost converter comprising four switches (S_1, S_2, S_3, S_4) and an inductor (L_B). The ON-times of S_1 and S_2, as well as S_3 and S_4, are complementary. The hysteresis control module manages the inductor current (I_{LB}), ensuring it remains within the specified hysteresis band ΔH.

For the positive direction of I_{LB}, 0 could be used as the lower and fixed bound, while ΔH acts as the upper and controllable bound that allows a variable width of the hysteretic band. However, when the direction of I_{LB} has to be reversed, I_{LB} becomes negative and 0 has to be used as the upper and fixed bound while -ΔH is the new lower and controlled bound. Furthermore, the switching frequency of the hysteresis control can be obtained as

$$\Delta t_1 = L_B \left| \frac{\Delta H}{V_{\text{MGA}}} \right| \tag{13}$$

$$\Delta t_2 = L_B \left| \frac{\Delta H}{V_{\text{MGA}} - V_{\text{MGB}}} \right| \tag{14}$$

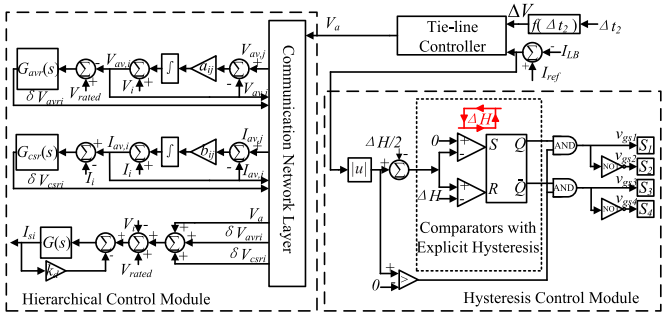

Fig. 5. Detailed control schematic of the cooperative PFC highlighting the interconnections of the control modules among it.

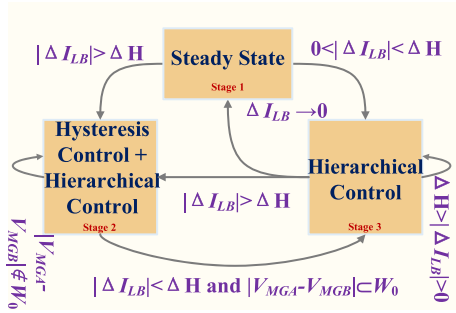

Fig. 6. Proposed cooperative power flow control procedure.

$$f_{\text{sw}} = \frac{1}{\Delta t_1 + \Delta t_2} \tag{15}$$

$$f_{\text{sw}} = \frac{1}{L_B \left| \frac{\Delta H}{V_{\text{MGA}}} \right| + L_B \left| \frac{\Delta H}{V_{\text{MGA}} - V_{\text{MGB}}} \right|} \tag{16}$$

where Δt_1 represents magnetizing time, Δt_2 represents demagnetizing time, and f_{sw} represents the variable switching frequency.

Since the hysteresis control is very fast, it can maintain the tie-line current error never exceeding the hysteresis band ΔH. Meanwhile, the average value of the tie-line current error can be maintained at the level of $\Delta H/2$ after the first hysteresis control cycle and the equation can be obtained as follows:

$$\delta V_A = V_A K_{p\text{tie}} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}} \right) + V_A \int K_{i\text{tie}} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}} \right) dt$$

$$I_{\text{tie}}^{\text{ref}} - I_{\text{tie}} = \frac{\Delta H}{2}. \tag{17}$$

$K_{p\text{tie}}$ is considered significantly small compared to $K_{i\text{tie}}$ and the high-frequency signal can be neglected; only the mean value of the tie-line current will be integrated

$$\delta V_A = V_A \int K_{i\text{tie}} \left(\frac{\Delta H}{2} \right) dt$$

$$\delta V_A = V_A K_{i\text{tie}} \left(\frac{\Delta H}{2} \right) t + \delta V_{A0} \tag{18}$$

where δV_{A0} is the initial value of the adjustment voltage of δV_A

$$V_{\text{MGA}} = \delta V_A + V_A + \Delta V_{uA}. \tag{19}$$

Fig. 5 illustrates the intricate control schematic of the proposed cooperative PFC, emphasizing the interconnections between its various control modules. These modules encompass a hierarchical control module, a hysteresis control module, and a tie-line control element. In order to control the current within the hysteresis band and allow the change of the bounds, the circuit shown in Fig. 5 is proposed.

The current-mode hysteresis control module for the buck/boost converter is implemented by using two single-threshold comparators and a latch. A linear current sensor senses the current information and generates V_{IL} signals. The inputs needed include the command I_{ref}, which can be determined arbitrarily by the users based on the application, and the command $\Delta H/2$, which can be used to control the average value of the current error at $\Delta H/2$ for positive direction or -$\Delta H/2$ for negative direction, respectively. The upper and lower values of the current error are set by clamping the current error to ΔH for positive current direction and -ΔH for negative direction, respectively. The current through the inductor is subjective to the I_{ref} and then compared with the lower and upper bounds and the latch generates two groups of complementary signals, which can be used for driving the main transistors in the power stage. In addition, a driver stage should be included to add the dead times between these signals and to properly drive the power transistors.

The control procedure of the proposed cooperative power flow control is illustrated in Fig. 6, where W_0 represents a priori given bounded set of initial conditions $W_0 \subset \mathbb{R}^N$, which will be explained in the following section. To further elaborate the basic principle of the proposed control method, a basic example of implementation is analyzed. The positive direction of the inductor current is considered here. If the tie-line current error exceeds the preset hysteresis band ΔH, the system will change from Stage 1 to Stage 2 where the system is managed by the hysteresis control module and hierarchical control module. As the current continues to converge and the voltage difference between the two ends of the tie-line decreases, the system will change from Stage 2 to Stage 3, which means the hysteresis control module will naturally stop working and the hierarchical control module will take over the power flow control of the system. On the other hand, the tie-line current error does not exceed the preset hysteresis band ΔH at the first stage. The system will change from Stage 1 into Stage 3 and back to Stage 1 after the steady state has been reached.

Finally, the switching frequency of the converter can be obtained as

$$V_{\text{MGA}} - V_{\text{MGB}} = \delta V_A + \Delta V_{uA} \tag{20}$$

$$V_A K_{i\text{tie}} \left(\frac{\Delta H}{2} \right) t + \delta V_{A0} + \Delta V_{uA} \tag{21}$$

$$f_{\text{sw}} = \frac{1}{L_B \left| \frac{\Delta H}{V_{\text{MGA}}} \right| + L_B \left| \frac{\Delta H}{V_A K_{i\text{tie}} (\frac{\Delta H}{2}) t + \delta V_{A0} + \Delta V_{uA}} \right|}. \tag{22}$$

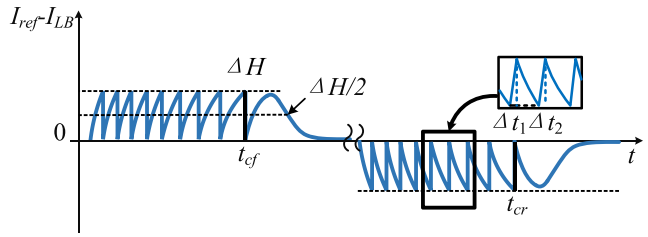

Fig. 7. Key waveforms of the current error under the proposed cooperative power flow control.

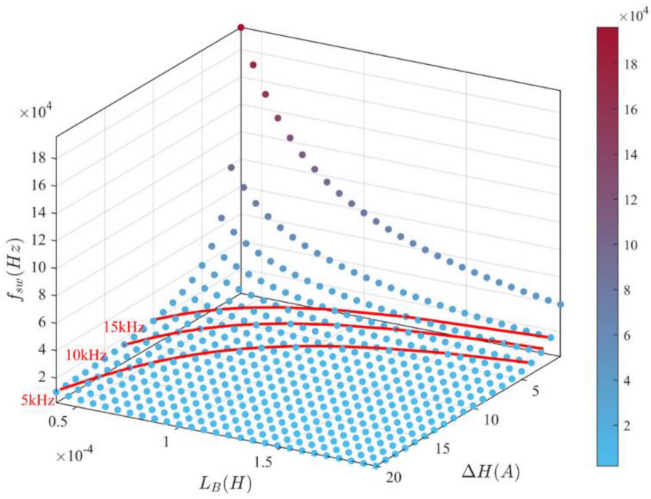

Fig. 8. Variable switching frequency with different bandwidths of hysteresis ripple under different inductances.

When the difference between V_{MGA} and V_{MGB} is becoming relatively small, the switching frequency of hysteresis control will approximately equal to zero, then the hierarchical control will start to take over. t_{cf} and t_{cr} represent the time when hierarchical control takes over in forward direction and in reverse direction, respectively

$$\delta V_A = V_A K_{p\text{tie}} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}}\right) + V_A \int_{t_{cf}}^{t} K_{i\text{tie}} \left(I_{\text{tie}}^{\text{ref}} - I_{\text{tie}}\right) dt + \delta V_c$$

$$\left|I_{\text{tie}}^{\text{ref}} - I_{\text{tie}}\right| \le \Delta H \qquad \text{for } t > t_{cf} \tag{23}$$

$$t_{cf} = \frac{|\Delta V_{uA} + \delta V_{A0}|}{V_A K_{i\text{tie}} (\Delta H/2)}. \tag{24}$$

When the current error remains in the hysteresis band and does not exceed the boundary, the hysteresis control-based converter will not be activated. Then, hierarchical control will take over until the current error finally convergences to zero.

The key waveforms of the error between the inductor current and the reference value in forward and reverse direction are shown as an analog control performance in Fig. 7 . Under the proposed control, fast and accurate power flow control can be realized. Fig. 7 is shown as an explanation of the example of analog control. For the positive direction of I_{LB}, I_{LB} is first regulated by the hysteresis control and the average value of the inductor current is controlled at $\Delta H/2$ and the current is controlled within the set upper bound (ΔH) and lower bound (0). Afterward, when the switching frequency becomes small enough which means the difference between V_{MGA} and V_{MGB} becomes relatively small, hierarchical control will take over until the inductor current has been controlled to the reference $I_{LB\text{ref}}$ accurately. Similar process happens when the direction is negative.

B. Stability of the DC MG Cluster With IPFC

The stability of the system should be guaranteed when applying the IPFC into the dc MG cluster. The hysteresis control module in the proposed cooperative power flow control acts approximately equivalent to a saturation. Then the stability analysis of the dc MG cluster with IPFC can be equivalent to the analysis of a linear system with input saturation. Adding the IPFC introduces input saturation into the linear system, preventing the tie-line current from exceeding the preset upper and lower hysteresis boundaries. From this perspective, the entire dc MG cluster must satisfy the necessary conditions for system stability when taking input saturation into account. To analyze the stability of the linear system considering input saturation, the semiglobal exponential stabilization method is utilized. This method ensures that the system remains stable within a finite, localized region of the state space, typically corresponding to the system's operating range.

The dc MG cluster system can be obtained by eliminating the intermediary and auxiliary variables and be considered a linear system as follows:

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx. \end{aligned} \tag{25}$$

When adding the IPFC into the cluster, the hysteresis control module in it can maintain the tie-line current error never becomes greater than the hysteresis band ΔH. Meanwhile, the average value of the tie-line current error can be maintained at the level of $\Delta H/2$ after the first hysteresis control cycle, which is a very short time interval as the switching frequency of the hysteresis control module is very high. Afterward, the tie-line current error is maintained within the hysteresis band. As the voltage difference across the tie-line decreases, the switching frequency of the hysteresis control module reduces. If the hierarchical tie-line current controller error converges asymptotically, the tie-line current error will not reach either the upper or lower boundary of the hysteresis band. The tie-line current error reaches zero when the control output of the hierarchical control δV approximately equals the voltage difference across the tie-line. Applying the IPFC to the tie-line is approximately equivalent to introducing input saturation into the original linear system, which can be described as

$$\begin{aligned} \dot{x} &= Ax + B\sigma_H(u) \\ y &= Cx \end{aligned} \tag{26}$$

where x ϵ $\mathbb{R}$N and u ϵ $\mathbb{R}$ are the system state and input saturation, respectively. A saturation function σ is employed in this cluster system and the control input corresponds to the tie-line current

error. Thus, $\sigma_H(s)$ is defined as a bounded function given by

$$\sigma_H(u) = \begin{cases} \zeta, \text{if } (I_{\text{ref}} - I_{LB}) \geq \zeta \\ I_{\text{ref}} - I_{LB}, \text{if } |I_{\text{ref}} - I_{LB}| < \zeta \\ -\zeta, \text{if } (I_{\text{ref}} - I_{LB}) \leq -\zeta \end{cases} \tag{27}$$

where ζ equals $\Delta H/2$ in the case proposed in this article.

The following assumptions on the system (26) can be made here: (A1) All the eigenvalues of A are located on the closed left half s-plane. (A2) The pair (A, B) is stabilizable.

Comment 1: The assumptions mentioned above can be satisfied by replacing the PI controller in the tie-line controller with a lag compensator.

Definition 1. (Semiglobal exponential stabilization via linear static state feedback): The system (26) is semiglobally exponentially stabilizable by linear static state feedback (the system consists of hierarchical controller only) if, for any a priori given bounded set of initial conditions $W \subset \mathbb{R}^N$, there exists a state feedback law $u = Kx$ such that the equilibrium $x = 0$ of the closed-loop system is locally exponentially stable and W is contained in the domain of attraction of the equilibrium $x = 0$; K represents the state feedback gain.

Comment 2: Considering tie-line current perturbation smaller than hysteresis band, a predefined range $W \subset \mathbb{R}^N$ can be provided such that there exists a state feedback law to make the system locally exponentially stable.

Theorem 1: The linear system considered here is semiglobally exponentially stabilizable via linear state feedback satisfying the assumptions A1 and A2 above. Namely, for any a priori given (arbitrarily large) bounded set W and any (arbitrarily small) ΔH, there is a linear control law $u = -Kx$ such that (a) the equilibrium $x = 0$ of the closed-loop system is locally exponentially stable and (b) W is contained in the domain of attraction of the equilibrium $x = 0$.

Comment 3: Referring to the results of [29], the dc MG cluster system is semiglobally exponentially stabilizable by linear static state feedback. Based on the initial conditions of the cluster, there exists a state feedback law $\sigma_H(u) = KCx$ such that the equilibrium $x = 0$ (I_{ref}-$I_{LB} = 0$) of the closed-loop system is locally exponentially stable and W is contained in the domain of attraction of the equilibrium $x = 0$ (I_{ref}-$I_{LB} = 0$). The proof of the Theorem 1 is shown in [29]. It should be mentioned that the value of the hysteresis band ΔH should be carefully designed and calculated to be greater than the upper error boundary of the hierarchical control tie-line current static state error.

C. Selection of Hysteresis Band and Switching Frequency

It is crucial to select an appropriate hysteresis band for IPFC to maintain the source current within a certain level during reference current change, parametric uncertainty, and disturbance voltage uncertainty. The objective of selecting the hysteresis band involves two issues. The first objective is to ensure that the power consumed by the loads of each MG connected through tie-line remains shall not overload other MGs. The second objective is to maintain the source current at a level that prevents the output currents of MGs from approaching or exceeding the saturation current. The hysteresis band should be a variable with different

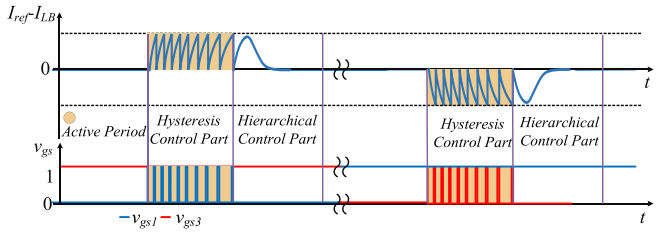

Fig. 9. Key waveforms of the tie-line current error and the control signal of IPFC during operation.

requirements. In this article, hysteresis band is considered to be set within 20% of the nominal current.

To show the relationship between switching frequency f_{sw} and the hysteresis band ΔH considering different IPFC inductor L_B more intuitively and clearly, for simplification, based on the (16) which can be used to describe the relationship between hysteresis band ΔH, IPFC inductor L_B and switching frequency f_{sw}, the boundary of the switching frequency f_{sw} when faced with a certain uncertainty is analyzed as is shown in Fig. 8. f_{sw} varies linearly with the hysteresis band, allowing determination of the appropriate hysteresis band range.

D. Power Loss Characterization of IPFC

The key waveforms of the tie-line current error ($I_{\text{ref}} - I_{LB}$) and the control signal (v_{gs}) of IPFC are shown in Fig. 9. The corresponding control signals v_{gsi} ($i = 1, 2, 3, 4$) represent the gate signals of S_i and the active period of IPFC only occurs when large uncertainties happen. To indicate the improvement of the proposed IPFC from the power loss and hardware size perspective, a comparison of the power loss between the proposed IPFC and traditional PFC is shown as follows. The power loss considered in this article involves conduction loss P_{cond} and switching loss P_{sw}.

An appropriate model for conduction loss P_{cond} is recommended as follows:

$$P_{\text{cond}} = {I_{D\text{rms}}}^2 R_{\text{on}} \tag{28}$$

where R_{on} represents the ON-resistance for the MOSFET, $I_{D\text{rms}}$ represents the MOSFET drain rms current. Meanwhile, the appropriate model for switching loss P_{sw} of MOSFET is approximately as follows:

$$P_{\text{sw}} = 0.5 V_D I_D \left(t_{\text{sw(on)}} + t_{\text{sw(off)}}\right) f_{\text{sw}} \tag{29}$$

where V_D represents the drain-to-source voltage across the MOSFET, I_D represents the drain current across the MOSFET, $t_{\text{sw(on)}}$ and $t_{\text{sw(off)}}$ are the MOSFET rise time and MOSFET fall time. The model of power loss can be obtained as

$$P_{\text{mos}} = P_{\text{cond}} + P_{\text{sw}}. \tag{30}$$

Then the power loss of the full-voltage compensation range PFC can be calculated as follows:

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} \approx \left(I_{\text{ref}}\right)^2 R_{\text{on}} + 0.5 V_D \left(I_{\text{ref}}\right) \left(t_{\text{sw(on)}} + t_{\text{sw(off)}}\right) f_{\text{sw}} \tag{31}$$

TABLE I
CHARACTERISTICS OF DIFFERENT UNCERTAINTY CATEGORIES

Uncertainty Category	Upper Limit of Occurrence Frequency	Duration of fast Uncertainty	Recovery time interval	Corresponding e_{sw}
Resources Variability	Once every minute	Tens of Milli-seconds	Tens of Milli-seconds	$20 \times 10^{-3}/60$
Load Changes	Once every minute	Tens of Milli-seconds	Tens of Milli-seconds	$20 \times 10^{-3}/60$
Commun-ication Failure	Once every day	Few seconds	Tens of Milli-seconds	$5/(60 \times 60 \times 24)$
Short Circuit Fault	Once several days	Tens of Milli-seconds	Tens of Milli-seconds	$20 \times 10^{-3}/(60 \times 60 \times 24 \times 2)$

where V_D is approximately equal to V_{MGA} or V_{MGB}. Since the current ripple is not very large, the drain current I_D will be approximately equal to I_{ref}. However, compared with full-voltage compensation range PFCs, which have continuous working operation, IPFC actively operates as a brief operation device during transient periods induced by uncertainties while automatically deactivating during steady conditions. The analysis of the effective switching loss generated by IPFC faced with different uncertainties is provided here. A coefficient e_{sw} is proposed to describe the effective characteristic of the IPFC switching loss

$$e_{\mathrm{sw}} = \frac{t_{oc}}{t_{wh}} \tag{32}$$

where t_{oc} represents the duration of the uncertainty and t_{wh} represents the mean time between the occurrence of uncertainty. Different uncertainty categories and their corresponding characteristics are listed in Table I.

As for the power loss of IPFC

$$P_{\mathrm{sw}} = 0.5 V_D I_D \left(t_{\mathrm{sw(on)}} + t_{\mathrm{sw(off)}}\right) f_{\mathrm{sw}} \cdot e_{\mathrm{sw}}. \tag{33}$$

In this way, since IPFC only works when large uncertainties happen and the coefficient term e_{sw} usually stays at a relatively low level, the IPFC switching loss will only represent a very small fraction of the power loss of IPFC. The power loss of the proposed IPFC can be obtained as follows:

$$P_{\mathrm{loss}} = P_{\mathrm{cond}} + P_{\mathrm{sw}} \approx (I_{\mathrm{ref}})^2 R_{\mathrm{on}} \tag{34}$$

which means higher switching frequency can be utilized in the IPFC design to obtain better control performance without causing too much switching loss. Furthermore, the relevant inductors and capacitors of IPFC hardware can reduce the cost and hardware size without affecting the control performance. Compared with fractional voltage compensation range PFCs, which usually have two stages and a tailored transformer in their control structure, the IPFC strategy can manage a larger control range without enlarging the hardware size or making the control structure more complex. The average power loss map of the existing PFC with a continuous working operation and IPFC with an intermittent working operation is shown in Fig. 10. Fig. 10(a) shows the power loss for the full-voltage compensation range PFC. Fig. 10(b) shows the power loss map for the proposed IPFC.

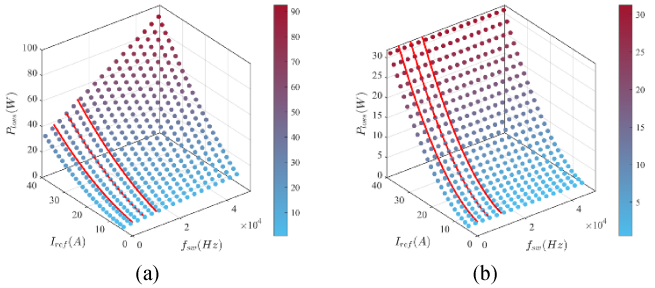

Fig. 10. Average power loss of tie-line type DC MG cluster with (a) existing PFC and (b) proposed IPFC.

TABLE II
PARAMETERS OF THE MOSFET USED IN IPFC

Parameter	Symbol	Value
Conduction Resistance	R_{on}	8mΩ
Reference Current	I_{ref}	5A-40A
Switching Frequency	f_{sw}	1kHz-50kHz
Drain-to-Source Voltage	V_D	400V
Drain Current	I_D	5A-40A
MOSFET Rise Time	$t_{sw(on)}$	41ns
MOSFET Fall Time	$t_{sw(off)}$	64ns

As shown in Fig. 10, there is a great decrease in power loss when the reference current and switching frequency stays at the same level. The result clearly demonstrates that the IPFC exhibits a relative lower power loss compared with a PFC with continuous working operation and indicates that the switching frequency can be selected relatively large by utilizing the IPFC. Furthermore, the power loss calculation parameters are listed in Table II.

To be modest, if the switching frequency can be increased to twice the existing PFCs, then according to the previously established relationship between switching frequency and inductor size, the inductance value can be reduced to half while maintaining the same control performance. This would lead to a 30% reduction in the size of the inductor. Furthermore, based on the above discussion, the proposed control strategy allows for an increase in switching frequency without causing significant switching loss. The power density of the experimental prototype developed in this article can reach 13.3 W/cm^3.

IV. IPFC CONTROLLER DESIGN IMPROVEMENT

A. *Influence of Hysteresis Band Value on Convergence for Voltage Uncertainty*

The performance of the tie-line current error and the corresponding output of the tie-line controller is shown in Fig. 11, where V_a represents the output of the tie-line controller and $I_{LB} - I_{\mathrm{ref}}$ represents the tie-line current error. The process they undergo is interconnected. The hysteresis control module directly controls the tie-line current, while the hierarchical control module controls the tie-line current through the output of tie-line controller. Since the control loop frequency of the hierarchical

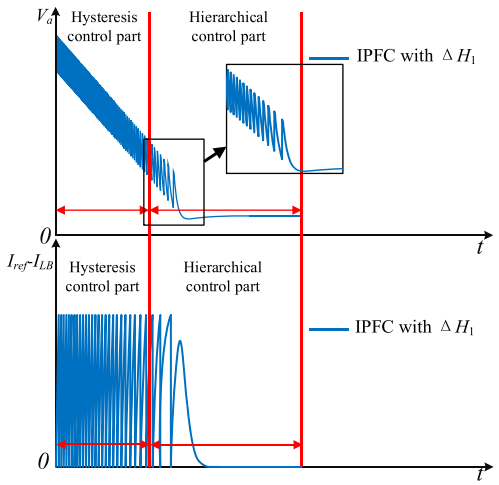

Fig. 11. Waveforms of the output of the tie-line controller under the proposed IPFC and the corresponding current error.

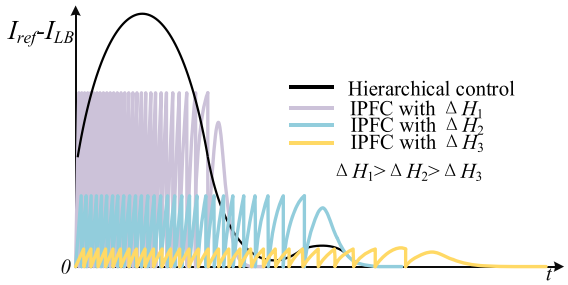

Fig. 12. Waveforms of the current error under the hierarchical control and the proposed IPFC with different hysteresis bands.

control module is relatively low while the switching frequency of the hysteresis control module is relatively high, the current error initially exhibits characteristics of hysteresis control at the first stage. After that, the subsequent control output waveform and current error will display the characteristics of classical PI control as the hysteresis control module stops working.

Fig. 12 illustrates the evolution of the current error to demonstrate the impact of different hysteresis bands ΔH_1, ΔH_2, and ΔH_3. These lines depict responses to sudden changes in voltage uncertainty with $\Delta H_1 > \Delta H_2 > \Delta H_3$. When a change occurs in the reference current, it is evident that the purple line has a shorter hysteresis process compared to the blue and yellow lines despite its larger amplitude of current error. In addition, when considering voltage disturbance uncertainty, a longer hysteresis process may occur compared to the scenario of a reference current change.

The hysteresis band influences the performance of the control process. If it is too small, although it can maintain the current within a narrow range, it will inevitably result in a longer hysteresis process, potentially leading to increased switching losses and an extended duration of the control output remaining in the transient level. Conversely, if the hysteresis band is relatively large, although the current can quickly converge to the reference,

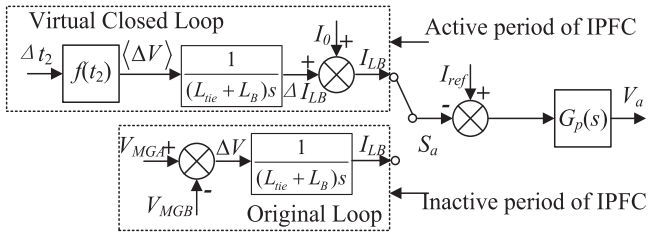

Fig. 13. Detailed control schematic of the proposed virtual closed loop for IPFC.

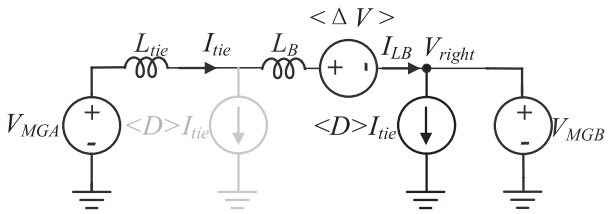

Fig. 14. Equivalent circuit of the steady-state circuit of LVDC MG cluster with IPFC.

it may fluctuate within a wider range, leading to increased power losses and increased ripple size during the active period.

B. Virtual Closed-Loop-Based Improvement

Increasing the convergence speed is the objective of the improvement. However, achieving both goals simultaneously requires more than just the appropriate selection of the hysteresis band.

During the operational phase of the IPFC, the virtual closed-loop module will be engaged, while during its inactive phase, the original loop, as depicted in Fig. 13, will take effect. To further illustrate the voltage modification logic, principle, and parameters, the equivalent circuit of the LVDC MG cluster with IPFC is shown in Fig. 14.

Upon implementation of the proposed IPFC, its operational functionality can be observed in Fig. 14, which depicts the equivalent circuit of an LVDC MG cluster featuring IPFC. Here, V_{MGA} and V_{MGB} denote the equivalent voltage sources of MGA and MGB, respectively. ΔV represents the voltage differential between MGA and MGB, with $<\Delta V>$ denoting its average value. For simplicity, the resistance of the tie-line is deemed negligible and thus excluded from consideration.

In scenarios involving uncertainties or changes in reference, the IPFC initiates action, regulating inductor current within the hysteresis band ΔH. Within a very brief period [0, Δt_a], where Δt_a denotes the cycle time derived from the subsequent equation

$$\Delta t_a = (L_B + L_{\mathrm{tie}}) \left| \frac{I_{\mathrm{ref}} - I_{LB}}{V_{\mathrm{MGA}}} \right|. \tag{35}$$

For the practical value of the tie-line inductor, Δt_a is approximately no more than hundreds of microseconds.

Considering the right arm is modulating, V_{right} and D can be expressed as

$$V_{\text{right}} = \begin{cases} 0, & t \in (0, DT) \\ (1-D)(V_{\text{MGB}}), & t \in (DT, T) \end{cases} \tag{36}$$

$$D = \frac{\Delta t_1}{\Delta t_1 + \Delta t_2}. \tag{37}$$

Given that the voltage variation ΔV changes at a much slower rate compared to the switching frequency of hysteresis control, and V_{MGA} and V_{MGB} evolve gradually during the hierarchical control process, it can reasonably be inferred that the hysteresis process operates close to its steady-state value. Consequently, the average voltage and current generated by the IPFC hardware can be expressed as follows:

$$\langle x(t) \rangle = \frac{1}{T} \int_{t-T}^{t} x(s) ds. \tag{38}$$

With the IPFC hardware maintaining the inductor current within the hysteresis band, the derivative of the average current equals 0

$$\frac{d \langle I_{LB} \rangle}{dt} = 0. \tag{39}$$

The voltage of the IPFC's inductor can be expressed as

$$L \frac{dI_{LB}}{dt} = (D) V_{\text{MGA}} + (1-D)(V_{\text{MGA}} - V_{\text{MGB}}) \tag{40}$$

and

$$L \frac{d \langle I_{LB} \rangle}{dt} = \langle D \rangle V_{\text{MGA}} + \langle 1 - D \rangle (V_{\text{MGA}} - V_{\text{MGB}}). \tag{41}$$

Consequently, the average value of duty cycle $<D>$ can be derived as follows:

$$\langle D \rangle = \frac{V_{\text{MGB}} - V_{\text{MGA}}}{V_{\text{MGB}}}. \tag{42}$$

Since the difference between V_{MGA} and V_{MGB} is relatively small as well as $<D>$, then the $<D>I_{\text{tie}}$ in Fig. 11 can be neglected and the state-space model changes from

$$V_{\text{MGA}} = \langle \Delta V \rangle + V_{\text{MGB}} + (L_{\text{tie}} + L_B) \frac{d \langle I_{LB} \rangle}{dt} \tag{43}$$

Into

$$\langle \Delta V \rangle = V_{\text{MGA}} - V_{\text{MGB}}. \tag{44}$$

Equation (44) consistently holds true following the initial cycle of hysteresis control. Moreover, leveraging (44), the difference $V_{\text{MGA}} - V_{\text{MGB}}$ can be computed using the approach elucidated later in this section. Nevertheless, the system under hierarchical control in the absence of the IPFC demonstrates stability and convergence concerning the original tie-line current, albeit amidst substantial transient conditions. Consequently, the change in inductor current without utilizing the IPFC can be evaluated by integrating the variation in $<\Delta V>$ during $[0, t_v]$, where t_v represents the time for the control process

$$\Delta I_{\text{tie}} = \frac{1}{L_{\text{tie}} + L_B} \int \langle \Delta V \rangle dt \tag{45}$$

$$I_{\text{tie}} = I_0 + \Delta I_{\text{tie}} = I_0 + \frac{1}{L_{\text{tie}} + L_B} \int \langle \Delta V \rangle dt \tag{46}$$

where I_0 is the initial value of the current before the start of IPFC. ΔI_{tie} represents the tie-line current change estimation during the transient

$$I_{\text{ref}} - I_{\text{tie}} = I_{\text{ref}} - I_0 - \frac{1}{L_{\text{tie}} + L_B} \int \langle \Delta V \rangle dt. \tag{47}$$

Therefore, by establishing a virtual closed-loop system that incorporates the information of $V_{\text{MGA}} - V_{\text{MGB}}$, the system control can progress seamlessly, treating this virtual data comparably to actual information, thus facilitating a natural evolution of control mechanisms. In this section, a virtual closed-loop control for IPFC is proposed, as shown in Fig. 13. Simultaneously, upon the establishment of known values for L_B and L_{tie}, the virtual current error can be calculated as follows:

$$\frac{1}{(L_B + L_{\text{tie}})} \int_0^{t_v} \langle \Delta V \rangle dt = \langle \Delta I_{LB} \rangle. \tag{48}$$

During the active period of IPFC, the derivative of the average inductor current is very small. Then the virtual closed loop can be used to generate this virtual current error and send the virtual error to replace the real current error to make the controller response with the same speed and behaviour as the hierarchal control. t_m represents the active period of the IPFC process

$$\langle I_{LB} \rangle = \frac{1}{(L_B + L_{\text{tie}})} \int_0^{t_v} \langle \Delta V \rangle dt + I_0. \tag{49}$$

The former control output equation can be changed into

$$V_a = G_p(s) \left(I_{\text{ref}} - I_0 - \frac{\langle \Delta V \rangle}{(L_B + L_{\text{tie}})\, s} \right). \tag{50}$$

The preservation of stability is assured through the adoption of a current-based PI control in this virtual closed-loop-based enhancement because the dynamic performance of the system when utilizing the virtual loop is approximately the same as the original system, which is tie-line impedance. Simultaneously, rapid convergence is facilitated by the capability of this enhancement to adjust the input command value. Through meticulous design and precise calibration of the virtual current error restoration, it becomes feasible to achieve both a narrow hysteresis band and swift convergence simultaneously.

The voltage difference $V_{\text{MGA}} - V_{\text{MGB}}$ can be calculated by the following equation and this computation is facilitated from the input capture unit of MCU within the hysteresis control module:

$$|V_{\text{MGA}} - V_{\text{MGB}}| = (L_B + L_{\text{tie}}) \frac{\Delta H}{\Delta t_2} \tag{51}$$

where, in this case, Δt_2 is estimated from the capture unit counter which effectively measures the interval between the turning OFF event of switch S_4 to turning ON event of switch S_4.

C. Design of Controller Parameters $K_{p\,tie}$, $K_{i\,tie}$

The convergence of MG's current and voltage can be achieved after a short time dynamics without considering time delays. However, when considering time delays, they can impact the

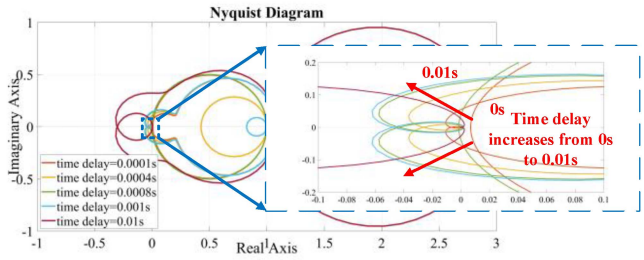

Fig. 15. Nyquist diagram of the closed-loop system with $K_{itie} = 1$ and $K_{ptie} = 0.03$, considering different time delays.

performance of the local controller, leading to tie-line inductance in combination with dc-dc converter capacitance forming a resonant pole. Meanwhile, the control system starts to suffer from higher oscillations and lower convergence speed. Therefore, to enhance the stability and robustness of the cooperation control, it is generally advisable to design K_{ptie} and K_{itie} appropriately and not to interact with any uncontrollable poles in the system. An LVDC MG cluster with the corresponding parameters has been considered and analyzed under a practical range of the time delay as 0-1 ms in this article and set the droop resistance to several times the original line resistance. In this case, the communication delay in consensus control loop and the measurement delay in sensor circuit are not considered to keep the procedure simple. Assuming the communication delay in the cooperative control loop is 0. 1 ms, the selected parameters of the PI controller in the proposed cooperative control loop have been tuned using V_a's Nyquist diagrams to keep the whole system stable within the 0-1 ms time delay. To be more specific, time delay increases from 0 to 1 ms when the selected control parameters K_{itie} and K_{ptie} are 1 and 0.03, respectively. Considering the aforementioned changes, the V_a's closed-loop Nyquist diagram is shown in Fig. 15.

It can be inferred that when $K_{itie} = 1$ and $K_{ptie} = 0.03$, the system is stable within the 0-1 ms time delay, which satisfy the stability requirement.

V. Simulations and Experimental Results

To verify the feasibility of the IPFC method, a simulation platform and an experimental platform were built, and the corresponding parameters for the simulation platform are listed in Table III. The corresponding parameters for the experimental platform are listed in Table IV.

A. Simulation Platform Details

It demonstrates that the measured dc voltage with respect to dc current agree with the simulation results and theoretical analysis under different scenarios.

B. Simulation Validations

In order to verify the effectiveness of the proposed cooperative power flow control strategy, a dc MG cluster has been modeled and tested in MATLAB/Simulink. The main system parameters

TABLE III
Parameters of the Simulation Platform

Element	Technical Parameter	Value
Hardware parameters	IPFC inductor (L_B)	0.2mH
	Tie-line resistance (R_{tie})	0.01Ω
	Tie-line inductance (L_{tie})	0.1mH
	Loads (R_{load1}, R_{load2}, R_{load3})	20Ω
	Cable resistance (R_{line1} R_{line2})	0.01Ω, 0.02Ω,0.02Ω
	RC filter	10Ω, 50μF
Control parameters	Nominal voltage (V_{rated})	400V
	Hysteresis band (ΔH)	2A
	Reference current (I_{ref})	30A-50A
	Tie-line controller (K_{itie}, K_{ptie})	1, 0.03
	Primary controller (k_p k_i)	5, 10
	Communication delay (τ)	1ms
	Droop gain ($R_{droop123}$)	0.01
	Voltage disturbance (ΔV_u)	2V-8V

TABLE IV
Parameters of the Experimental Platform

Terminals	Technical Parameter	Value
DC1	DC voltage (V_{DC1})	120 V
	DC load (R_1)	15 Ω
DC2	DC voltage (V_{DC2})	100 V
	DC load (R_2)	15 Ω
IPFC Controller	Reference current (I_{ref})	4A-8A
	IPFC inductor (L_B)	0.2mH
	Hysteresis band (ΔH)	2A
DC/DC Converter	Voltage Rating	200V
	Current Rating	20A
Cluster Environment	Total filter capacitance on each side	4700μF
	Transient test load (R_t)	4Ω

of the tested cluster and the selected control parameters of the converters and control parameters of secondary and droop control of dc MGs in the dc cluster are listed in Table III, respectively. The performance of the proposed cooperative power flow control strategy is shown in Figs. 16 –19, which shows the tie-line current applying IPFC and not applying IPFC when faced with different reference changes and disturbance uncertainties, respectively. Control Strategy 1 represents the proposed cooperative power flow control. Control Strategy 2 represents Control Strategy 1 adding the virtual closed-loop control module. The existing PFC represents the existing power flow control strategy (a load flow converter to control power flow between the dc MGs), which can also be considered as a full-voltage compensation range PFC. The comparison between traditional hierarchical control and the proposed cooperative power flow control is proposed in Figs. 16(a), 17, and 19. Meanwhile, the comparison between existing PFC and the proposed cooperative power flow control is proposed in Figs. 16(b) and 18. Fractional voltage compensation range PFC is not considered as a comparison because this type of PFC face difficulties in accommodating wide voltage ranges during substantial uncertainties and are constrained in their capacity to effectively mitigate uncertainties effects. While the proposed IPFC method belongs to the full-voltage compensation range PFC concept, they have similar characteristics but different control ranges.

1) Performance of Reference Tracking: This scenario involves two comparisons. The first one is the comparison between

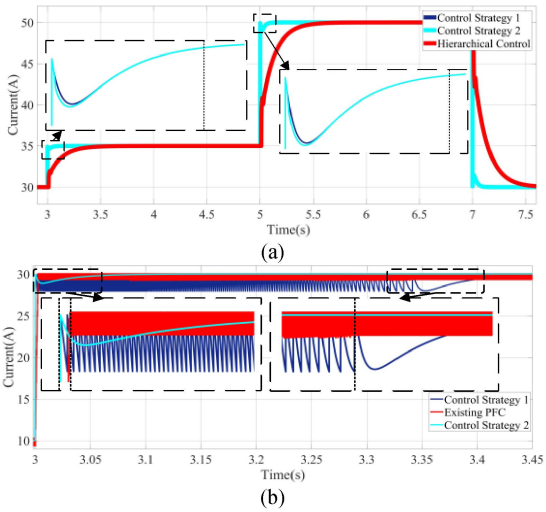

Fig. 16. (a) Waveforms of the inductor current when the reference value changes from 30 to 35 A at $t = 3.0$ s, from 35 to 50 A at $t = 5.0$ s, and from 50 A back to 30 A at $t = 7.0$ s under control strategy 1, control strategy 2, and hierarchical control, respectively. (b) Waveforms of the inductor current when the reference value of current changes from 10 to 30 A at 3.0 s under control strategy 1, control strategy 2, and existing PFC.

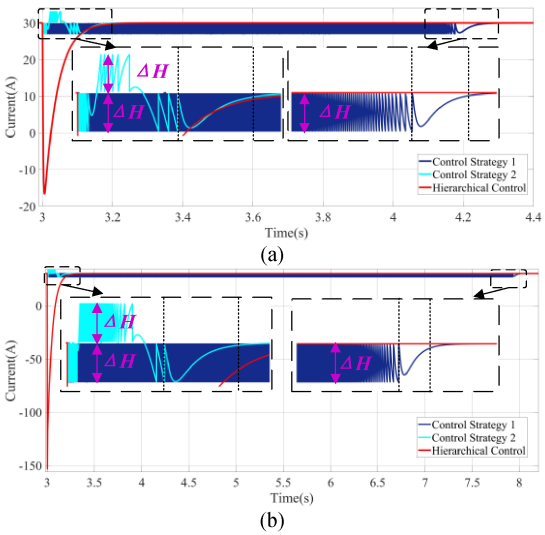

Fig. 17. Waveforms of the inductor current when different voltage disturbance uncertainties happen under control strategy 1, control strategy 2, and hierarchical control considering tie-line inductor. (a) Disturbance uncertainty in voltage (400–398 V) happens at $t = 3.0$ s. (b) Disturbance uncertainty in voltage (400–392 V) happens at $t = 3.0$ s.

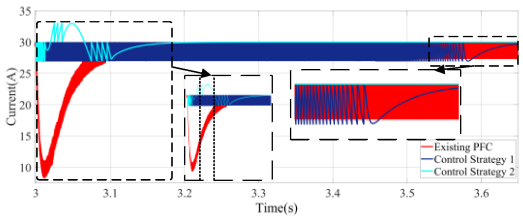

Fig. 18. Waveforms of the inductor current when disturbance uncertainties in voltage happen at $t = 3.0$ s under control strategy 1, control strategy 2, and existing PFC.

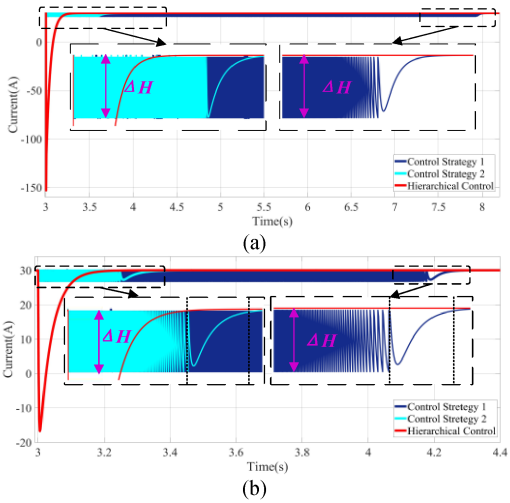

Fig. 19. Waveforms of the inductor current when different voltage disturbance uncertainties happen under control strategy 1, control strategy 2, and hierarchical control without considering the tie-line inductor. (a) Disturbance uncertainty in voltage (400–398 V) happens at $t = 3.0$ s. (b) Disturbance uncertainty in voltage (400–392 V) happens at $t = 3.0$ s.

traditional hierarchical control and the proposed cooperative power flow control, as shown in Fig. 16(a). Fig. 16(a) shows the waveforms of the inductor current when the reference value changes from 30 to 35 A at $t = 3.0$ s, from 35 to 50 A at $t = 5.0$ s, and from 50 back to 30 A at $t = 7.0$ s. Before the reference change, the system is working at its nominal state with the value of the reference current being 30 A; during this process, the performance of the current under the hierarchical control, control strategy 1 and control strategy 2, is the same. The value of the reference current changes from 30 to 35 A at $t = 3.0$ s. It can be observed from Fig. 16(a) that when only applying hierarchical control, the current will undergo a larger and longer transient process which involves a 0.01 s time delay and finally convergence to the new reference at $t = 3.45$ s. However, when applying Control Strategy 1, the current can be controlled within the first hysteresis control cycle initially when the reference current changes at $t = 3.0$ s and convergences to 35 A at $t = 3.02$ s without involving a 0.01 s time delay. Furthermore, under Control Strategy 2, a faster convergence speed can be obtained. The value of the reference current changes from 35 to 50 A at $t = 5.0$ s, which is a relatively bigger change compared with 30–35 A. Therefore, the convergence time is longer and the current convergences to the new reference at 5.15 s under Control Strategies 1 and 2. When only applying hierarchical control, current convergences to 50 A at $t = 5.5$ s. Finally, the value of the reference current changes from 50 to 35 A at $t = 7.0$ s. The current will undergo a similar transient process. Since the change in reference current will not have a big effect on the voltage of MGs, then the inductor current can be controlled within the first hysteresis control cycle. Meanwhile, the hysteresis control and the virtual closed-loop control module will be active only for a very short time and then the hierarchical control takes over before the inductor current finally converges to the new reference value.

The second one is the comparison between the existing PFC and the proposed cooperative power flow control, as shown in Fig. 16(b). The figure shows the waveforms of the inductor current when the reference value of current changes from 10 to 30 A at 3.0 s. Before the reference change, the system is working at its nominal state with the reference being 10 A, and the performance of the current under the Control Strategy 1 and Control Strategy 2 is the same. However, when applying the existing full-voltage compensation range PFC, the current will demonstrate the typical characteristics of pulsewidth modulation (PWM) control. In this way, the current will experience a process with the amplitude being 0.7 A and switching frequency being 5 kHz. The reference changes from 10 to 30 A at $t = 3.0$ s. It can be observed from Fig. 14 that when applying the full-voltage compensation range PFC, the current can be controlled initially and convergences to the new reference 30 A within 5 ms. However, the control process will also show the typical characteristics of PWM control with a larger amplitude being 0.85 A. Since the control process with PWM characteristics is continuous, it will cause relatively large switching losses. When applying the Control Strategy 1, the control process is the dark blue line shown in Fig. 16(b). When the reference changes at $t = 3.0$ s, the current can be controlled around the new reference value within the first hysteresis control cycle. Then the current can be controlled within the predesigned hysteresis process. This process will last about 34 ms, after that the hierarchical control will take over and the IPFC will spontaneously stop working. Finally, the current will converge to 30 A at $t = 3.4$ s. IPFC in Control Strategy 1 can work intermittently without causing a continuous control process possessing PWM signal characteristics. Compared with the aforementioned two power flow control strategies, when applying Control Strategy 2, a smaller hysteresis control process can be obtained. The current can be controlled around the new reference within the first hysteresis control cycle and convergence to 30 A at $t = 3.03$ s, which is a great improvement in the speed.

2) Performance of Voltage Disturbance Uncertainties: This scenario involves two comparisons. The first one is the comparison between traditional hierarchical control and the proposed cooperative power flow control, as shown in Fig. 17(a), and (b). Fig. 17(a) and (b) shows the waveforms of the inductor current when disturbance uncertainties in voltage happen. Before the disturbance uncertainties happen at $t = 3.0$ s, the system is working at its nominal state with the 30 A inductor current. During this process, the performance of the current under these three control strategies is the same. When a disturbance uncertainty in voltage (400—398 V) happens at $t = 3.0$ s in MGA, when only applying hierarchical control, the current drops to -16 A initially and undergoes a large and long transient process containing a 0.01 s time delay, before converging to the nominal value 30 A at $t = 3.2$ s. On the other hand, when applying Control Strategy 1, the inductor current can be controlled within a 2 A hysteresis band initially when the disturbance happens at $t = 3.0$ s without having a time delay, as shown in Fig. 17(a). The hysteresis control module stops working at $t = 4.17$ s and then the hierarchical control takes over before the current convergences to 30 A at $t = 4.3$ s. Although the current does not undergo large transient, it will inevitably have a relatively long hysteresis process causing extra switching loss. Furthermore, when applying Control Strategy 2, the virtual closed-loop control module can be activated initially at $t = 3.0$ s. It can be observed in Fig. 17(a) that the hysteresis control and the virtual closed-loop control module both stop working at $t = 3.10$ s, and after that, hierarchical control takes over until the current convergences to 30 A at $t = 3.17$ s, which is a relatively small convergence time compared with Control Strategy 1. Meanwhile, a larger disturbance uncertainty in voltage (400–392 V) occurs at $t = 3.0$ s in MGA. For only applying hierarchical control, a larger and longer transient process will happen, potentially causing overload protection of the cluster. As shown in Fig. 17(b), the current drops to -152 A at $t = 3.0$ s and finally convergences to 30 A at $t = 3.4$ s, involving a 0.01 s time delay. Meanwhile, for Control Strategy 1, the hysteresis process is relatively longer as the hysteresis control stops working at $t = 7.94$ s potentially causing extra switching loss and then the hierarchical control will take over until the current convergences to the reference value at $t = 8.0$ s, which is a relatively longer process compared with the former disturbance uncertainty (400–398 V). However, when applying Control Strategy 2, the virtual closed-loop module can be activated initially when the hysteresis control is activated at $t = 3.0$ s and becomes inactivated when the hysteresis control is not working at $t = 3.125$ s, and then the hierarchical control takes over until the current convergences to the reference value at $t = 3.2$ s, which is a great improvement. As a short summary, although Control Strategy 1 prevents overcurrent, it results in a prolonged hysteresis process. After applying Control Strategy 2, the current not only be controlled within a small hysteresis band but can also achieve a fast convergence speed.

The second one is the comparison between the existing PFC and the proposed cooperative power flow control, as shown in Fig. 18. Fig. 18 shows the waveforms of the inductor current when disturbance uncertainties in voltage happen at $t = 3.0$ s. When a disturbance uncertainty in voltage (400–398 V) happens at $t = 3.0$ s in MGA, the current drops to 8.5 A initially and undergoes a larger and longer transient process before converging to the nominal value 30 A at $t = 3.1$ s applying the full-voltage compensation range PFC. After that, the current will experience a process with the amplitude being 2.75 A and switching frequency being 5 kHz, which will have a continuous working process. On the other hand, when applying Control Strategy 1, the current can be controlled within a 2 A hysteresis band initially when the disturbance happens at $t = 3.0$ s. The hysteresis control process stops working at $t = 3.57$ s and then the hierarchical control module takes over before the current finally convergences to 30 A at $t = 3.65$ s. Although the convergence time for Control Strategy 1 is relatively longer than the full-voltage compensation range PFC, Control Strategy 1 has the intermittent working process and only works when the large uncertainties happen. Furthermore, when applying Control Strategy 2, the virtual closed-loop control module can also be activated initially at $t = 3.0$ s. The hysteresis control and the virtual closed-loop control module both stop working at $t = 3.10$ s, and after that, the hierarchical control takes over until the current convergences to 30 A at $t = 3.14$ s, which is a relatively small convergence time compared with Control Strategy 1.

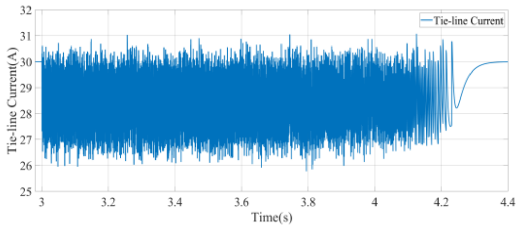

Fig. 20. Waveforms of the inductor current considering a 2 V voltage disturbance uncertainty under the proposed cooperative power flow control adding a noise signal whose variance is 0.15 A and the sample time is 0.001 s.

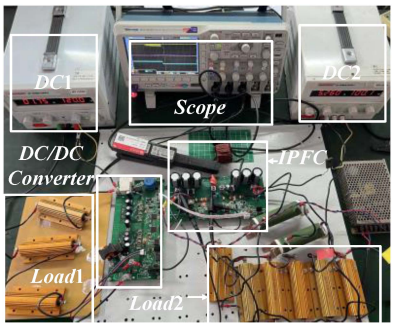

Fig. 21. Experimental setup.

Nevertheless, in the majority of LVDC MG clusters, the tie-line inductors are notably diminutive in comparison to the proposed IPFC's inductor. Consequently, the waveforms of the inductor current exhibit variations when voltage disturbance uncertainties are present in Fig. 19(a) and (b), differing from scenarios where the tie-line inductor is accounted for. It becomes apparent that under conditions where the tie-line inductor is significantly smaller than the IPFC inductor, the convergence process of the current does not penetrate the hysteresis band in the opposite direction.

3) Performance Considering Measurement Noise: In this scenario, a voltage uncertainty is considered and the waveforms of the tie-line current are shown in Fig. 20. A noise signal whose variance is 0.15 A and the sample time is 0.001 s is considered and is added into hysteresis control module of the proposed cooperative power flow control. Although the tie-line current exhibits waveform characteristics affected by noise during the hysteresis control process, the tie-line current remains within the preset hysteresis band ΔH throughout the entire hysteresis control process. Furthermore, the time required for convergence is not significantly impacted.

C. Experimental Setup

In order to further verify and test the proposed coordinated power flow control, an experimental LVDC cluster with two dc MGs and one tie-line prototype had been set up, as well as our proposed IPFC controller, for simplification and the discussion in Section VI. The tie-line inductor is neglected as shown in Fig. 21 and the equivalent circuit of it is shown in Fig. 22 with

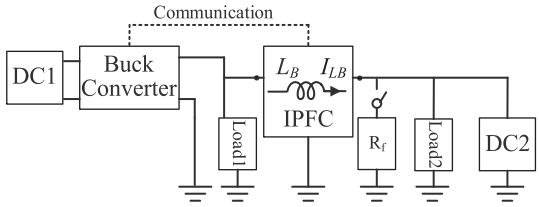

Fig. 22. Equivalent circuit of the experimental setup.

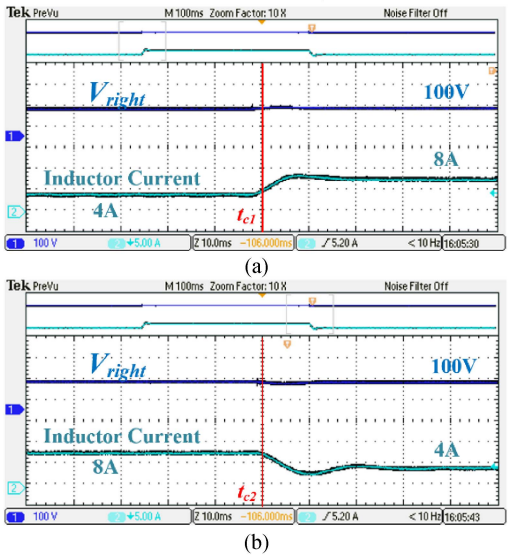

Fig. 23. V_{right} (channel 1) and inductor current in tie-line (channel 2) waveforms of the cluster under only hierarchical control considering reference changes (a) from 4 to 8 A at t_{c1} and (b) from 8 to 4 A at t_{c2}.

the corresponding parameters being listed in Table IV. The components DSP (DSPIC33EJ64MC506), CPLD (EPM3064ATI44-10N), and MOSFET (IRFZ48N) are embedded into the carefully designed IPFC circuit to realize the aforementioned capacities.

D. Experimental Validation

1) Performance of Reference Tracking: When exclusively employing hierarchical control without the incorporation of additional active PFCs, the behavior of the converter's V_{right} and the inductor current during a transient in reference current is depicted in Fig. 23. Examination of Fig. 23(a) indicates that when the reference value of the inductor current shifts from 4 to 8 A at time (t_{c1}), the current initially fails to promptly adjust to the new reference value, exhibiting significant transient behavior. A comparable operational pattern is observed at (t_{c2}) when transitioning the reference value back from 8 to 4 A, as illustrated in Fig. 23(b), showcasing notable transient effects on the inductor current. Nonetheless, the absence of active PFCs and reliance solely on hierarchical control can lead to unforeseen transient behaviors within the system.

In contrast, utilizing solely the hysteresis control module, without integrating hierarchical control, results in the initial control of the inductor current when transitioning the reference value from 4 to 8 A at (t_{c1}). However, the hysteresis process

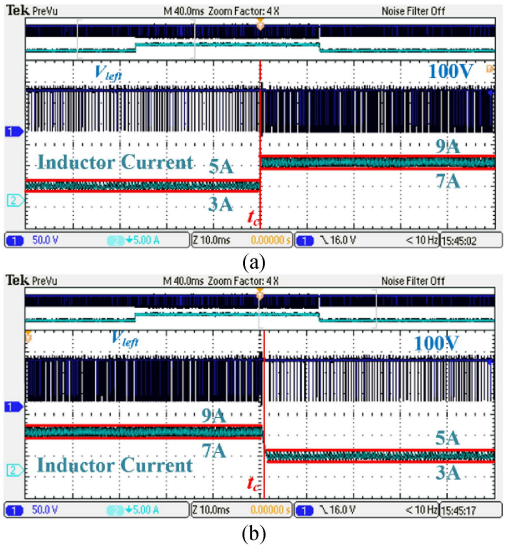

Fig. 24. V_{right} (channel 1) and inductor current in tie-line (channel 2) waveforms of the cluster under only hysteresis control considering reference changes (a) from 4 to 8 A at t_{c1} and (b) from 8 to 4 A at t_{c2}.

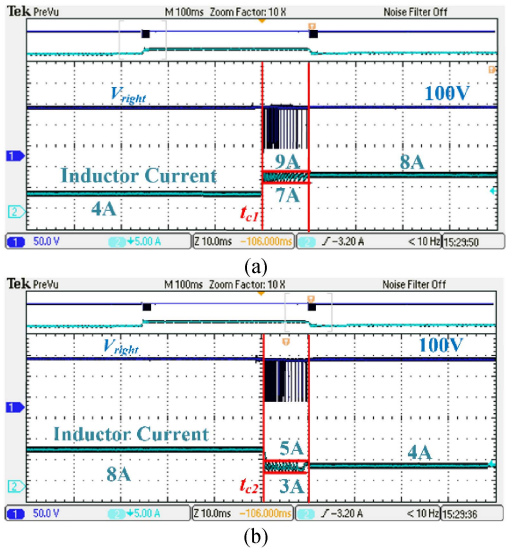

Fig. 25. V_{right} (channel 1) and inductor current in tie-line (channel 2) waveforms of the cluster under the proposed cooperative power flow control considering reference changes (a) from 4 to 8 A at t_{c1} and (b) from 8 to 4 A at t_{c2}.

continues unabated at a consistent switching frequency without cessation. A similar operational pattern is evident at (t_{c2}) when reverting the reference value from 8 back to 4 A. As illustrated in Fig. 24, the inductor current is effectively constrained within a 2A hysteresis band for both reference values. Nevertheless, lacking hierarchical control within the proposed PFC prevents the natural termination of the hysteresis process, potentially leading to additional switching losses akin to those encountered with traditional PFCs.

Upon the application of the proposed IPFC method, the operational characteristics of the converter's V_{right} and the inductor current are depicted in Fig. 25 during a transition in reference current. Analysis of Fig. 25(a) reveals that when the reference value of the inductor current shifts from 4 to 8 A at time (t_{c1}), the controller effectively maintains the inductor current within the designated hysteresis band initially at (t_{c1}). Moreover, employing this IPFC method facilitates the rapid convergence of the inductor current to the new reference value within a single hysteresis cycle as the discrepancies between V_{MG1} and V_{MG2} diminish, consistent with the aforementioned simulation outcomes. Similar operational efficacy is observed in Fig. 25(b) when the reference value reverts from 8 to 4 A at (t_{c2}), demonstrating the inductor current's swift adjustment to the revised reference within one hysteresis cycle. Consequently, the operation of the IPFC method is characterized by intermittent behavior, allowing the hysteresis process to naturally cease.

2) Performance of Adding Virtual Closed-Loop Module Improvement and Performance of Different Voltage Uncertainties: When employing the proposed IPFC method, the performance metrics of V_{right}, MG2 bus voltage, and inductor current under a 4 V voltage fluctuation are detailed in Fig. 26(a). Analysis reveals that with the introduction of the IPFC method, upon the occurrence of a voltage uncertainty at $t = 20.0$ ms, the controller promptly activates, ensuring that the inductor current remains within a predefined hysteresis band of 2 A. The hysteresis

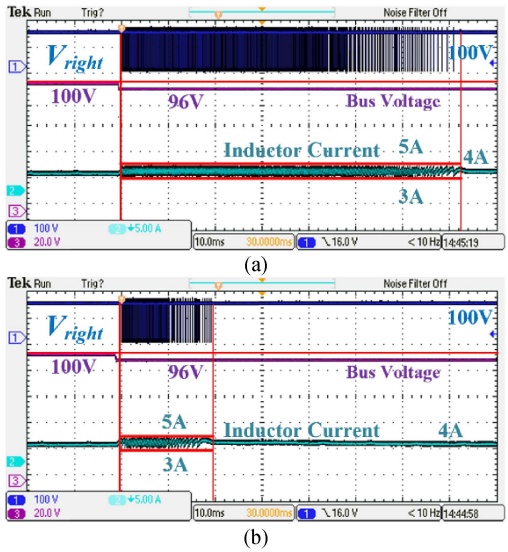

Fig. 26. V_{right} (channel 1), inductor current in tie-line (channel 2) and bus voltage (channel 3) waveforms of the cluster considering a 4 V voltage disturbance uncertainty. (a) Basic principle of proposed IPFC. (b) Adding virtual closed-loop control module to the proposed IPFC. .

mechanism persists for approximately 72.0 ms, ceasing naturally as the voltage mismatch between V_{MG1} and V_{MG2} diminishes, thereby transitioning control hierarchically. However, the duration of 72.0 ms represents a notably extended process. To enhance control efficiency, a virtual closed-loop control module is incorporated into the IPFC method. The implementation of this enhancement is depicted in Fig. 26(b), demonstrating improved V_{right} and inductor current performance during a 4 V voltage uncertainty. Upon the onset of uncertainty at $t = 20.0$ ms with the enhanced module, the controller activates promptly, maintaining the inductor current within the 2 A hysteresis band. Remarkably, the hysteresis process now lasts only 19.5 ms, a

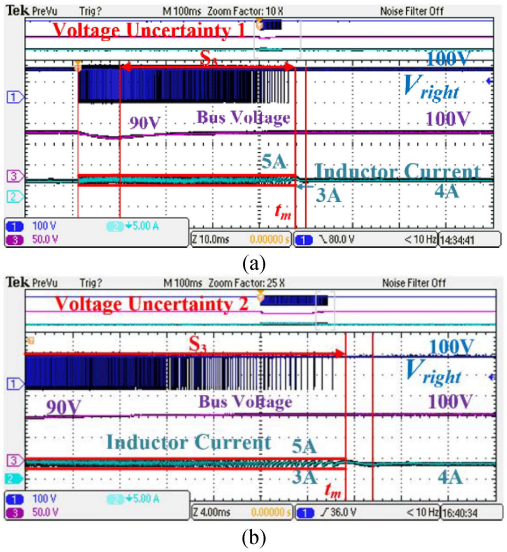

Fig. 27. V_{right} (channel 1), inductor current in tie-line (channel 2), and bus voltage (channel 3) waveforms of the cluster under the proposed IPFC adding a virtual closed-loop module considering (a) 10 V voltage disturbance uncertainty lasting 5.0 ms. (b) 10 V voltage disturbance uncertainty lasting 10.0 ms.

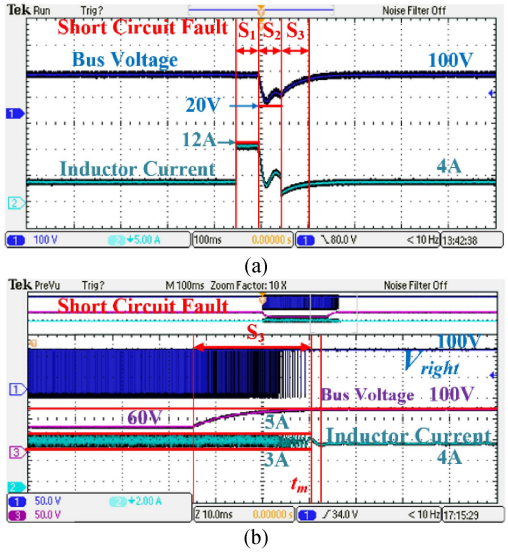

Fig. 28. V_{right} (channel 1), inductor current in tie-line (channel 2), and bus voltage (channel 3) waveforms of the cluster considering a short-circuit fault of 4 Ω. (a) Under only hierarchical control. (b) Under the proposed IPFC adding a virtual closed-loop module.

substantial improvement compared to the basic control method's 72.0 ms. As V_{MG1} and V_{MG2} disparities lessen, the hysteresis control's switching frequency approaches zero by $t = 36.0$ ms, effectively transitioning to hierarchical control methods. These experimental findings corroborate simulation results, affirming the practicality and efficacy of the proposed enhancement method.

When employing the enhanced IPFC method, the behavior of V_{right}, MG2 bus voltage, and inductor current amidst a 10 V voltage uncertainty, characterized by a 5.0 ms onset and a 10.0 ms duration, is illustrated in Fig. 27(a) and (b). The asymmetrical power flow induced by varying durations of 10 V voltage uncertainties can potentially be alleviated through the application of the refined IPFC approach. In the case of voltage uncertainty 1, Fig. 27(a) demonstrates that the enhanced controller promptly activates upon the onset of uncertainty, effectively maintaining the inductor current within a predefined hysteresis band of 2 A. A comparable performance is observed for voltage uncertainty 2.

3) Performance of Short-Circuit Fault Protection: To substantiate the efficacy of the proposed IPFC method in safeguarding against short-circuit faults, the performance of MG2's bus voltage and inductor current is analyzed across three distinct stages—initial charging (S1), fault occurrence (S2), and recovery (S3)—as illustrated in Fig. 28(a) and (b). Fig. 28(a) demonstrates that without utilizing the proposed IPFC method, a 4 Ω short-circuit fault in MG2 causes the bus voltage to plummet to 20 V, accompanied by an initial surge in inductor current to 12 A, followed by a transient process before stabilizing at the reference value of 4 A. In contrast, Fig. 28(b) showcases the implementation of the enhanced control strategy, ensuring that the bus voltage is maintained at a secure 60 V. Concurrently, the inductor current is regulated within a predefined hysteresis band of 2 A, with upper and lower limits set at 5 A and 3 A, respectively, averaging around 4 A. Moreover, as the voltage mismatch between V_{MG1} and V_{MG2} diminishes, the switching frequency of the hysteresis control approaches zero, as evidenced by the performance of V_{right} and inductor current, thereby facilitating the convergence of inductor current toward the targeted reference of 4 A.

In summary, the integration of an intermittent controller introduces a control mechanism characterized by reduced switching frequency and intermittent operation. Moreover, by incorporating a virtual closed-loop control module into the strategy, rapid convergence can be achieved, resulting in minimized switching losses. Experimental findings corroborate the simulation results across scenarios such as reference changes, short-circuit faults, and voltage uncertainties. Throughout these conditions, the inductor current consistently adheres to the predetermined hysteresis band, avoiding severe transient behaviors. Concurrently, the MG voltage remains stably maintained even amidst short-circuit faults.

E. Large-Scale DC MG Cluster Experiment

In this section, a larger-scale LVDC MG cluster consisting of two 100-V nonidentical DC MGs was developed using the OPAL-RT simulator, which has the same structure as Fig. 1 containing MGA and MGB, and the experimental setup is shown in Fig. 29. Both MGA and MGB consist of six independent dc sources and six buck converters and both of them are governed by hierarchical control, with dynamic consensus-based distributed secondary control applied to each of them individually. The corresponding parameters of the cluster system considered here are based on the parameters used in Table IV. The performance of the dc MG cluster is shown in Figs. 30 and 31, which show the inductor current applying IPFC and not applying IPFC when faced with different uncertainties, respectively.

1) Communication Failure: This scenario involves the comparison between the traditional hierarchical control and the proposed cooperative power flow control strategy when the

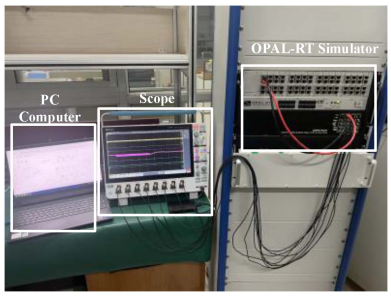

Fig. 29. Experimental setup.

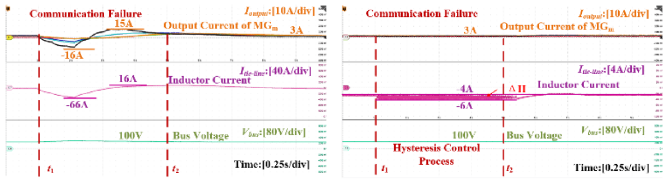

Fig. 30. Waveforms of the output currents of the MGA are shown in Ch1&2&3&4&5&6. The tie-line current of the cluster is shown in Ch7. The output voltage of MGA is shown in Ch8, considering a communication failure happening in MGB. (a) Without IPFC. (b) With IPFC.

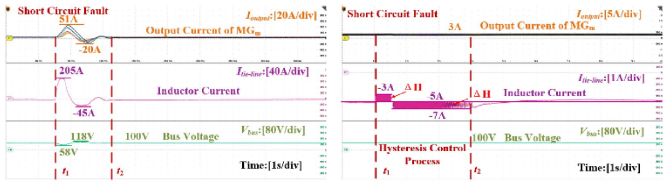

Fig. 31. Waveforms of the output currents of the MGA are shown in Ch1&2&3&4&5&6. The tie-line current of the cluster is shown in Ch7. The output voltage of MGA is shown in Ch8, considering a short-circuit fault happening in MGB. (a) Without IPFC. (b) With IPFC.

dc cluster is faced with a communication failure. Consider a communication failure happening in MGB at $t = t_1$s. The output currents of the MGA are shown in Ch1&2&3&4&5&6. The tie-line current of the cluster is shown in Ch7. The output voltage of MGA is shown in Ch8. As is shown in Fig. 30, before the communication failure happens, the cluster system is working at its nominal state with the MGA and MGB reaching the consensus, where they both achieve their respective secondary control objectives: current sharing and voltage recovery. When a communication failure happens at $t = t_1 s$ in MGB, under traditional hierarchical control, the output currents of MGA are not able to maintain the consensus, and encounter oscillation. The output currents return to the former consensus and achieve the current sharing again at $t = t_2$s. Meanwhile, as for the tie-line current, it also experiences a transient. As has been discussed in Section II-B, uncertainty such as communication failure may not cause voltage source uncertainty and the bus voltage of MGA is not affected and stays at its nominal level. On the other hand, when applying the proposed cooperative power flow control strategy, the output currents of MGA are able to maintain the consensus and the inductor current on the tie-line can be controlled within the preset hysteresis band initially when the communication failure happens at $t = t_1$s. The hysteresis control process ends at $t = t_2$s and then the hierarchical control module takes over before the current finally convergences to the current reference value. These experimental results are consistent with those in Section V-C.

2) Big Load Change: This scenario involves the comparison between the traditional hierarchical control and the proposed cooperative power flow control strategy when the dc cluster is faced with a big load change. Consider a big load change happening in MGB at $t = t_1$s. The output currents of the MGA are shown in Ch1&2&3&4&5&6. The tie-line current of the cluster is shown in Ch7. The output voltage of MGA is shown in Ch8. As is shown in Fig. 31, under the traditional hierarchical control, before the short-circuit fault happen at $t = t_1$s, the system operates in its nominal state, with MGA and MGB reaching consensus. When a short-circuit fault occurs at $t = t_1$s in MGB, the output currents of MGA are not able to maintain the consensus. Meanwhile, the output currents of the MGA surge to a relatively high level initially and encounter oscillation with large amplitude. The inductor current undergoes a similar process. Furthermore, the output voltage of MGA also witnesses oscillation with large amplitude. Finally, the consensus can be reached again after the short-circuit fault has been cleared. On the other hand, when applying the proposed cooperative power flow control strategy, the output currents of MGA are able to maintain the consensus and the inductor current can be controlled within the preset hysteresis band initially when the short-circuit fault happens at $t = t_1$s. The hysteresis control process ends at $t = t_2$s and then the hierarchical control module in the cooperative power flow control takes over before the inductor current finally convergences to the current reference value. Furthermore, the bus voltage of MGA cannot be affected and can stay at its nominal level. These experimental results are also consistent with those in Section V-C.

As a summary, the efficacy of power flow control within a larger-scale LVDC MG cluster faced with different uncertainties can be significantly enhanced through the application of the proposed cooperative power flow control strategy. By measuring the waveforms of the output currents and voltages of the individual converters within the respective dc MG, as well as the inductor current on the tie-line when faced with communication failures and big load change, new experimental results have been added and the effectiveness of the proposed cooperative power flow control can also be verified. The experimental results are consistent with those obtained from the simple LVDC MG cluster discussed above. This further validates the effectiveness of the proposed cooperative power flow control strategy.

VI. Conclusion

For the application of a dc cluster with multiple distributed LVDC MGs, a cooperative power flow control framework to improve the system efficiency and reliability has been proposed

in this article. Furthermore, a virtual closed-loop control strategy has been added to the basic principle of the proposed control which could improve the response speed and control performance. The main findings of this article can be highlighted as follows.

1) Hierarchical control alone is not enough for appropriate and flexible power flow control in the LVDC MG cluster during different uncertainties. Meanwhile, continuous operation and constant switching frequency caused by active PFCs could cause extra switching loss and these devices always have a large size and high cost.
2) A cooperative power flow control strategy is introduced to enhance the transient performance of the LVDC MG cluster. This strategy pioneers a novel approach by introducing the concept of IPFC. It includes a configuration of an intermittent PFC that integrates hysteresis control in conjunction with hierarchical control. This innovative configuration opens up a new paradigm for power flow control within LVDC MG clusters.
3) In light of the foundational operation principles of the proposed control strategy, this article also introduces an enhanced strategy aimed at augmenting the control performance. This refined approach achieves significantly accelerated convergence speeds, resulting in a reduction of convergence time by approximately two-thirds.
4) With the proposed method, flexible power flow control with an intermittent working period in the LVDC MG cluster can be realized when faced with reference tracking or disturbance uncertainties.

It is important to emphasize that the aforementioned objectives have been achieved through a cohesive coordinated control strategy that operates without the need for switching between control schemes. The efficacy of this proposed approach was validated through comprehensive means, including theoretical analysis, simulation, and experimental testing.

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