A Constant Switching Frequency Real-Time Digital Control for ZVS Four-Switch-Buck-Boost Converter

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***Abstract*—In this article, a constant switching frequency real-time digital control scheme is proposed for the four-switch buck-boost converter. With this control scheme, all the power switches can realize zero-voltage-switching, and the ripple and root-mean-square value of the inductor current can be minimized in the whole voltage and load ranges. Since all the control variables in any operation mode are obtained in real-time with one closed-loop PI controller and simple calculations, the inductor current in each switching cycle is optimized, and smooth operation mode transition and high dynamic response in the step change of load or input voltage is achieved. The effectiveness of the proposed control scheme is verified with a 300 W prototype.**

***Index Terms*—Constant switching frequency, digital control, four-switch buck-boost converter (FSBB), zero voltage switching (ZVS).**

I. Introduction

FOR the applications such as distributed power supply systems with energy storage batteries for uninterrupted power supply, or aerospace power processing units powered by solar panel, a dc–dc converter, featuring voltage step-up and step-down, is necessary to realize a constant output voltage from a variable input voltage. The four-switch buck-boost (FSBB) converter, as shown in Fig. 1, has attracted more and more attention due to its advantages of a low voltage stress on power switches and few passive components [1], [2]. Various control schemes for the FSBB converter have been proposed, such as the two-mode control [3], [4], [5], [6], [7] and the three-mode control [8], [9], [10]. To increase the switching frequency, the switching loss, especially the turn-ON loss of the wide bandgap power devices, becomes a major issue. Therefore, a quadrilateral inductor current modulation for the FSBB converter [11], [12], which can achieve zero-voltage-switching (ZVS) for all the power switches, has been widely investigated.

Received 14 September 2024; revised 9 January 2025; accepted 21 February 2025. Date of publication 6 March 2025; date of current version 14 April 2025. This work was supported by the National Natural Science Foundation of China under Grant 52237009 and in part by the Naturel Science Foundation of Jiangsu Province under Grant BK20221489. Recommended for publication by Associate Editor L. Corradini. *(Corresponding author: Fei Yang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3547755.

Digital Object Identifier 10.1109/TPEL.2025.3547755

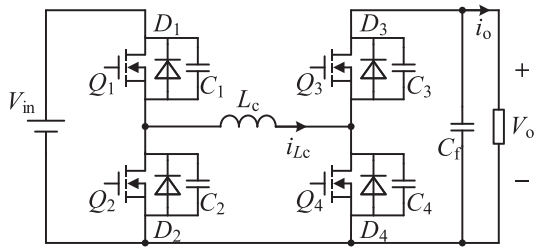

Fig. 1. Topology of FSBB converter.

In order to realize ZVS for the power switches and minimize the ripple and root mean square (RMS) value of the inductor current, the FSBB converter with the quadrilateral inductor current modulation has two optimal operation modes, namely, pseudo discontinuous current mode (PDCM) and pseudo critical continuous current mode (PCRM), as shown in Fig. 2. The inductor current at points C and O (O') should be controlled at $-I_{ZVS}$ in both PDCM and PCRM, and the inductor current under PDCM should be controlled at I_{ZVS} at point A for $V_{in} \geq V_o$ or point B for $V_{in} < V_o$ [13], [14], [15].

As shown in Fig. 2, D_{T1}, D_{T2}, D_{T3}, and D_{T4} are the duty cycles of four switching modes, and the sum of them equals to 1. So, there are three control variables for regulating the output voltage, while realize ZVS for the power switches and minimize the inductor current ripple [16].

Since D_{T1} for $V_{in} \geq V_o$ and D_{T3} for $V_{in} < V_o$ should be constant in PDCM, and D_{T4} is 0 in PCRM, D_{T2} or variables containing D_{T2}, which have a closed relationship with the load in both PDCM and PCRM and any voltage conversions, are widely used as the independent control variable. Given that the direct computation of D_{T2} is complex, a closed-loop PI controller is often employed to determine D_{T2} or its associated variables.

However, as the load increases, D_{T2} increases in PDCM and decreases in PCRM, as shown in Fig. 2. Thus, the closed-loop PI controller with a monotonically increasing control logic is only applicable to PDCM rather than PCRM, and a change in the control strategy or control variable is required when the operation mode transitions, leading to a complex control.

For the analog control, a pulsewidth modulation (PWM) plus a phase-shift control scheme with a constant switching frequency is proposed, and a phase-shift regulator and an output voltage regulator work together in PCRM [13]. However, the two closed-loops are coupled, which affects the converter stability

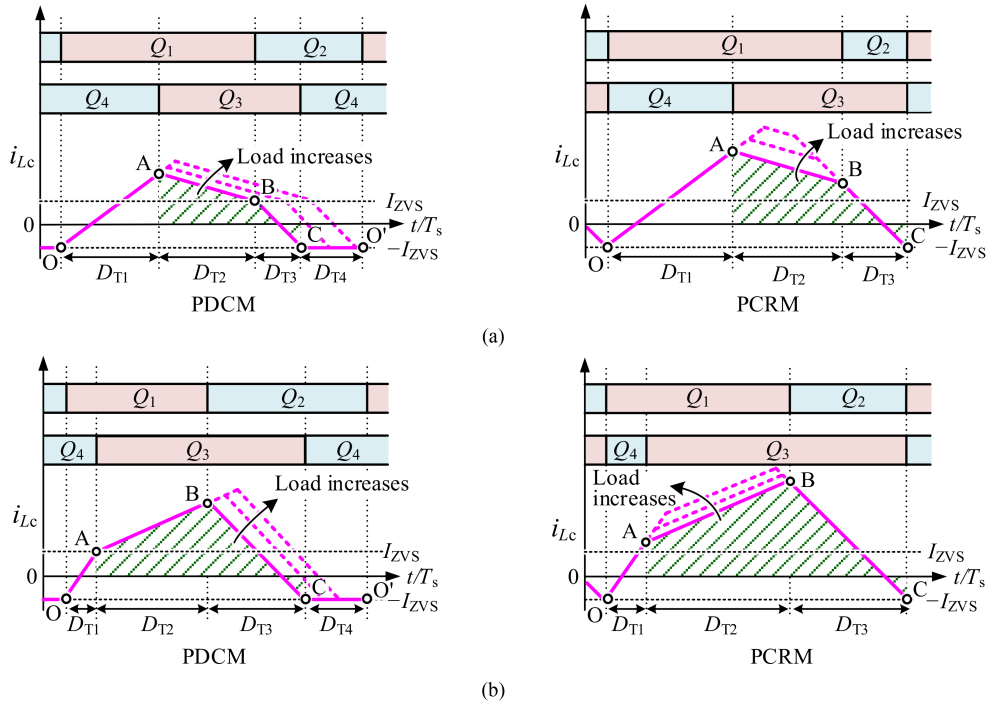

Fig. 2. Quadrilateral inductor current control for (a) $V_{\text{in}} < V_o$ and (b) $V_{\text{in}} \geq V_o$.

and dynamic response when the operation mode changes [14]. An approximate phase-shift duty cycle is proposed to replace the phase-shift duty cycle closed-loop, which improves the dynamic performance, at the expense of slightly increased inductor current RMS value [15].

For the digital control, the three-dimensional (3D) look up table (LUT) is used to avoid the operation mode transition and complicated calculations. However, a large size of data is needed in the LUT to achieve a high steady-state accuracy and better dynamic response [16], [17]. A pseudo discontinuous conduction mode with a 2D LUT is proposed to keep the converter in PDCM with different ZVS current control methods, which eliminate the modulation mode transition in the whole working conditions [18]. Some variable switching frequency control methods with real-time calculations are also proposed to keep the converter operating in one operation mode under all working conditions, most in PDCM, while additional frequency control and careful magnetic component design are needed [19], [20], [21]. A constant switching frequency control strategy based on a control variable of $(D_{T1} + D_{T3})/2$ is proposed, which is implemented with a closed-loop controller and some real-time calculations. However, when the input and output voltages are the same, the converter keeps working in PCRM in the whole load range, and the power switches may lose ZVS at light load [22].

In order to control the FSBB converter in PDCM or PCRM for any working condition without the aspects such as LUT, complex calculations, variable switching frequency and multi closed-loop control interactions, a constant switching frequency digital control scheme is proposed in this article. The main contributions are as follows.

1) The boundary conditions of D_{T2} in PDCM and PCRM with constant switching frequency are derived for the operating mode identification and the control variable
2) A control algorithm is proposed to determine the needed D_{T2} in PDCM or PCRM by one closed-loop controller and simple calculations, and the converter can be regulated under any working condition in real-time.

The rest of this article is organized as follows. In Section II, based on the optimal inductor current waveform, the steady-state D_{T2}, which varies with the load current, as well as the boundary conditions of D_{T2} between PDCM and PCRM, are provided. In Section III, the relationship between D_{T2} and the output of the output voltage regulator in any operation mode is established, and a constant switching frequency real-time digital ZVS control scheme for the FSBB converter is proposed. In Section IV, the experimental verification is presented.

II. Relationship of D_{T2} and Load Current

The FSBB converter has been given in Fig. 1, where $Q_1 \sim Q_4$ are the power switches, V_{in} and V_o are the input and output voltages, and L_c is the inductor. The duty cycles of the four switching modes in the quadrilateral inductor current modulation are D_{T1}, D_{T2}, D_{T3}, and D_{T4}. At steady-state, the voltage gain of the FSBB converter and the duty cycles satisfy

$$\begin{cases} \dfrac{V_o}{V_{\text{in}}} = \dfrac{D_{T1} + D_{T2}}{D_{T2} + D_{T3}} \\ D_{T1} + D_{T2} + D_{T3} + D_{T4} = 1 \end{cases}. \tag{1}$$

A. Relationship Between Load Current and D_{T2}

From Fig. 2, the inductor current values at points A and B, I_{LcA} and I_{LcB}, can be expressed as

$$I_{LcA} = -I_{\text{ZVS}} + \frac{V_{\text{in}}}{L_c} D_{T1} T_s \tag{2}$$

$$\underline{V_{\text{in}} - V_o}$$

where I_{ZVS} is the current required to realize ZVS, and T_s is the switching period.

The inductor current i_{Lc} flows into the load when Q_3 is ON, and the load current I_o can be expressed as

$$I_o = \frac{I_{LcA} + I_{LcB}}{2} D_{T2} + \frac{I_{LcB} - I_{\mathrm{ZVS}}}{2} D_{T3}. \tag{4}$$

When the converter operates in PDCM, to realize the switch ZVS and minimize the inductor current ripple and the RMS value, I_{LcA} and I_{LcB} should satisfy

$$\begin{cases} I_{LcB} = I_{\mathrm{ZVS}} & V_{\mathrm{in}} < V_o \\ I_{LcA} = I_{\mathrm{ZVS}} & V_{\mathrm{in}} \geq V_o \end{cases}. \tag{5}$$

According to Fig. 2 and (1)–(5), the load current provided in PDCM with respect to D_{T2} can be expressed as

$$I_{o\_\mathrm{PDCM}} = \begin{cases} \dfrac{V_o - V_{\mathrm{in}}}{2L_c} T_s D_{T2}^2 + I_{\mathrm{ZVS}} D_{T2} & V_{\mathrm{in}} < V_o \\ \dfrac{V_{\mathrm{in}}}{V_o} \left(\dfrac{V_o - V_{\mathrm{in}}}{2L_c} T_s D_{T2}^2 + I_{\mathrm{ZVS}} D_{T2} \right) & V_{\mathrm{in}} \geq V_o \end{cases}. \tag{6}$$

When the converter enters PCRM, $D_{T4} = 0$. From (1)–(4), the load provided in PCRM with respect to D_{T2} is expressed as

$$I_{o\_\mathrm{PCRM}} = \frac{V_{\mathrm{in}}}{2L_c (V_{\mathrm{in}} + V_o)^2} \cdot \begin{Bmatrix} -\left(V_{\mathrm{in}}^2 + V_o^2 + V_{\mathrm{in}} V_o\right) T_s D_{T2}^2 \\ +\left[2V_{\mathrm{in}} V_o T_s - 2L_c I_{\mathrm{ZVS}} \left(V_{\mathrm{in}} + V_o\right)\right] D_{T2} \\ +V_{\mathrm{in}} V_o T_{\mathrm{s}} - 2L_c I_{\mathrm{ZVS}} \left(V_{\mathrm{in}} + V_o\right) \end{Bmatrix}. \tag{7}$$

From (6) and (7), for given I_{o_PDCM} and I_{o_PCRM}, a positive value of D_{T2} can be solved and respectively expressed as

$$D_{T2} = \begin{cases} \dfrac{\sqrt{\left(L_c I_{\mathrm{ZVS}}\right)^2 + 2\left(V_o - V_{\mathrm{in}}\right) L_c I_{o\_\mathrm{PDCM}} T_s} - L_c I_{\mathrm{ZVS}}}{\left(V_o - V_{\mathrm{in}}\right) T_s} & V_{\mathrm{in}} < V_o \\ \dfrac{\sqrt{\left(L_c I_{\mathrm{ZVS}}\right)^2 + 2\dfrac{\left(V_{\mathrm{in}} - V_o\right) V_o}{V_{\mathrm{in}}} L_{\mathrm{c}} I_{\mathrm{o\_PDCM}} T_{\mathrm{s}}} - L_c I_{\mathrm{ZVS}}}{\left(V_{\mathrm{in}} - V_o\right) T_s} & V_{\mathrm{in}} \geq V_o \end{cases}. \tag{8}$$

$$D_{T2} = \frac{V_{\mathrm{in}} V_o T_s - L_c I_{\mathrm{zvs}} \left(V_{\mathrm{in}} + V_o\right)}{\left(V_{\mathrm{in}}^2 + V_o^2 + V_{\mathrm{in}} V_o\right) T_s} \pm \frac{\left(V_{\mathrm{in}} + V_o\right) \sqrt{\begin{matrix} \left(L_c I_{\mathrm{ZVS}}\right)^2 - 2L_c I_{\mathrm{ZVS}} \left(V_{\mathrm{in}} + V_o\right) T_s + V_{\mathrm{in}} V_o T_{\mathrm{s}}^2 \\ -2L_c I_{o\_\mathrm{PCRM}} \left(V_{\mathrm{in}}^2 + V_o^2 + V_{\mathrm{in}} V_o\right) T_s / V_{\mathrm{in}} \end{matrix}}}{\left(V_{\mathrm{in}}^2 + V_o^2 + V_{\mathrm{in}} V_o\right) T_s}. \tag{9}$$

When L_c, I_{ZVS}, and T_s are given, a schematic diagram of the steady-state D_{T2} as the function of I_o are depicted in Fig. 3. As seen, D_{T2} in PDCM increases from 0 to the defined maximum value D_{T2_b} as I_{o_PDCM} increases, and D_{T2} in PCRM decreases as I_{o_PCRM} varies. The variation trends of the curves of D_{T2} with respect to I_o in any voltage conversion are similar.

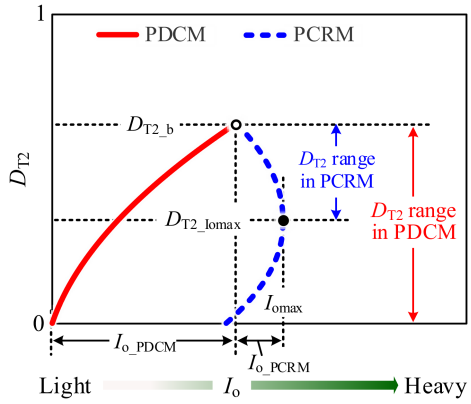

Fig. 3. Schematic diagram of steady-state D_{T2} as the function of I_o.

B. Boundary Conditions of D

In PDCM, from (1)–(3) and (5), D_{T4} as the function of D_{T2} can be represented as

$$D_{T4} = \begin{cases} 1 - \dfrac{2L_c I_{\mathrm{ZVS}}}{V_o T_s} - \dfrac{2L_c I_{\mathrm{ZVS}}}{V_{\mathrm{in}} T_s} - \dfrac{V_o}{V_{\mathrm{in}}} D_{T2} & V_{\mathrm{in}} < V_o \\ 1 - \dfrac{2L_c I_{\mathrm{ZVS}}}{V_{\mathrm{in}} T_s} - \dfrac{2L_c I_{\mathrm{ZVS}}}{V_o T_s} - \dfrac{V_{\mathrm{in}}}{V_o} D_{T2} & V_{\mathrm{in}} \geq V_o \end{cases}. \tag{10}$$

When $D_{T4} = 0$, the boundary D_{T2} of PDCM and PCRM, D_{T2_b}, which is also the maximum D_{T2}, is derived from (10) as

$$D_{T2\_b} = \begin{cases} \dfrac{V_{\mathrm{in}}}{V_o} - \dfrac{2L_c I_{\mathrm{ZVS}} \left(V_{\mathrm{in}} + V_o\right)}{V_o^2 T_s} & V_{\mathrm{in}} < V_o \\ \dfrac{V_o}{V_{\mathrm{in}}} - \dfrac{2L_c I_{\mathrm{ZVS}} \left(V_{\mathrm{in}} + V_o\right)}{V_{\mathrm{in}}^2 T_s} & V_{\mathrm{in}} \geq V_o \end{cases}. \tag{11}$$

As shown in Fig. 3, for a given I_{o_PDCM}, the converter works in PDCM and the variation range of D_{T2} within $[0,\ D_{T2\_b}]$.

For a given I_{o_PCRM}, the converter works in PCRM, and there are two solutions of D_{T2} from (9). When the value inside the square root of (9) is 0, a maximum load $I_{o\max}$ the converter can provide in PCRM is obtained, and its corresponding D_{T2} is

$$D_{T2\_\mathrm{Iomax}} = \frac{V_o V_{\mathrm{in}} T_s - L_c I_{\mathrm{zvs}} \left(V_o + V_{\mathrm{in}}\right)}{\left(V_{\mathrm{in}}^2 + V_o^2 + V_o V_{\mathrm{in}}\right) T_s}. \tag{12}$$

As D_{T2} decreases, I_{o_PCRM} increases when $D_{T2\_\mathrm{Iomax}} \leq D_{T2} \leq D_{T2\_b}$ and decreases when $D_{T2} < D_{T2\_\mathrm{Iomax}}$. Since the inductor current in a switching cycle when $D_{T2} < D_{T2\_\mathrm{Iomax}}$ tends to be triangular, which means a higher inductor current ripple and RMS value, it is favorable to keep the converter under PCRM working with $D_{T2\_\mathrm{Iomax}} \leq D_{T2} \leq D_{T2\_b}$ [13].

From (11) and (12), with the known L_c, I_{ZVS}, and T_s, after the input and output voltages are obtained, the corresponding D_{T2_b} and D_{T2_Iomax} can be calculated, and the variation ranges of D_{T2} in PDCM and PCRM are obtained. Then, if the value of D_{T2} for a working condition is attained, the proper operation mode can be determined. Then, based on the inductor volt-second balance or the ZVS requirements, the other control variables can be successively derived from D_{T2}.

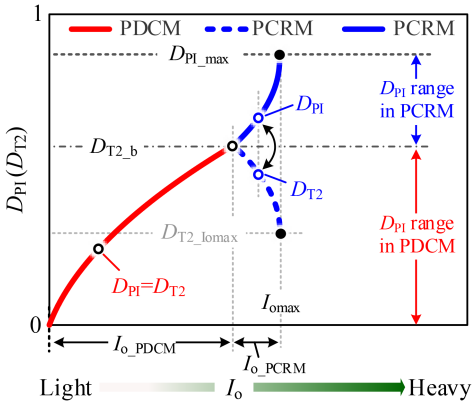

Fig. 4. Schematic diagram of required $D_{\rm PI}$ in steady-state as the function of I_o.

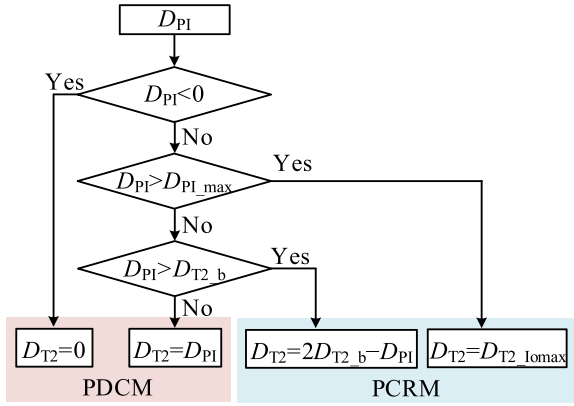

Fig. 5. Process of converting $D_{\rm PI}$ to D_{T2}.

III. Real-Time Control Scheme Based on D_{T2}

A. Acquisition of D_{T2} From Closed-loop PI Controller

To regulate the output voltage, a closed-loop PI controller is often adopted to obtain the D_{T2}. Based on the negative feedback mechanism, the output of the closed-loop PI controller, $D_{\rm PI}$, keeps increasing as the load current increases.

When the converter works in PDCM, D_{T2} also increases as $I_{o\_\rm PDCM}$ increases, and the steady-state D_{T2} can be treated as the required $D_{\rm PI}$, as shown by the solid red line in Fig. 4. In practice, when $D_{\rm PI} < D_{T2\_b}$, we have $D_{T2} = D_{\rm PI}$ [19].

When the converter works in PCRM, as $I_{o\_\rm PCRM}$ increases, $D_{\rm PI}$ increases from D_{T2_b} to a higher value, while D_{T2} decreases from D_{T2_b} to $D_{T2\_\rm Iomax}$, as shown in Fig. 4. So, $D_{\rm PI}$ cannot be used as D_{T2} directly in PCRM. Since D_{T2_b} can be calculated, if the cure of D_{T2} shown by the dashed blue line is flipped up horizontally on the axis of D_{T2_b}, the solid blue line, which increases as $I_{o\_\rm PCRM}$ increases, can be treated as the required $D_{\rm PI}$. In practice, when $D_{\rm PI} \geq D_{T2\_b}$, D_{T2} can be calculated as

$$D_{T2} = 2D_{T2\_b} - D_{\rm PI}. \tag{13}$$

The maximum $D_{\rm PI}$ corresponding to $D_{T2\_\rm Iomax}$ can be obtained from (13), expressed as

$$D_{\rm PI\_max} = 2D_{T2\_b} - D_{T2\_\rm Iomax}. \tag{14}$$

In this way, the required $D_{\rm PI}$ for PDCM and PCRM, as well as the boundary conditions of $D_{\rm PI}$, are established based on D_{T2}, as shown in Fig. 4, and the acquisition process of D_{T2} from $D_{\rm PI}$ is shown in Fig. 5. For any input and output voltage, the D_{T2_b} and $D_{\rm PI\_max}$ are obtained initially. When a $D_{\rm PI}$ is provided by the closed-loop PI controller: if $D_{\rm PI} < D_{T2\_b}$, the converter will be controlled in PDCM, and $D_{T2} = D_{\rm PI}$ and if $D_{T2\_b} \leq D_{\rm PI} \leq D_{\rm PI\_max}$, the converter will be controlled in PCRM, and $D_{T2} = 2D_{T2\_b} - D_{\rm PI}$. For any working condition with the given load and output voltage, the regulation of $D_{\rm PI}$ is carried out by the closed-loop PI controller, and the steady-state D_{T2} will be obtained at last.

B. Variable I_{ZVS} Control

Fig. 6 shows the implementation of the proposed control scheme for the FSBB converter, where $V_{\rm in}$ and V_o are sampled by ADCs, and the inductor current is sensed and compared to a reference value with analog circuits.

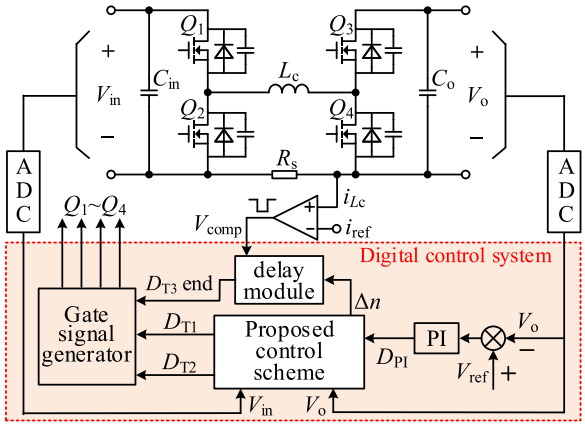

Fig. 6. Block diagram of the proposed control scheme.

Normally, a constant $I_{\rm ZVS}$ with an enough margin is used to realize ZVS for all the power switches under all working conditions. Assuming that the power switches are identical with an output capacitance $C_{\rm oss}$, the dead time between the driver signals of Q_1 (Q_3) and Q_2 (Q_4) is denoted as $t_{\rm dead}$, the minimum $I_{\rm ZVS}$ for the ZVS of all the switches in a switching cycle is

$$I_{\rm ZVS} = \begin{cases} 2C_{\rm oss}V_o/t_{\rm dead} & V_{\rm in} < V_o \\ 2C_{\rm oss}V_{\rm in}/t_{\rm dead} & V_{\rm in} \geq V_o \end{cases}. \tag{15}$$

If a variable $I_{\rm ZVS}$ is used based on (15), the boundary conditions of D_{T2} can be further simplified by substituting (15) into (11) and (12), respectively, expressed as

$$D_{\rm T2\_b} = \begin{cases} \left(1 - \dfrac{4C_{\rm oss}L_c}{T_s t_{\rm dead}}\right) \cdot \dfrac{V_{\rm in}}{V_o} - \dfrac{4C_{\rm oss}L_c}{T_s t_{\rm dead}} & V_{\rm in} < V_o \\ \left(1 - \dfrac{4C_{\rm oss}L_c}{T_s t_{\rm dead}}\right) \cdot \dfrac{V_o}{V_{\rm in}} - \dfrac{4C_{\rm oss}L_c}{T_s t_{\rm dead}} & V_{\rm in} \geq V_o \end{cases} \tag{16}$$

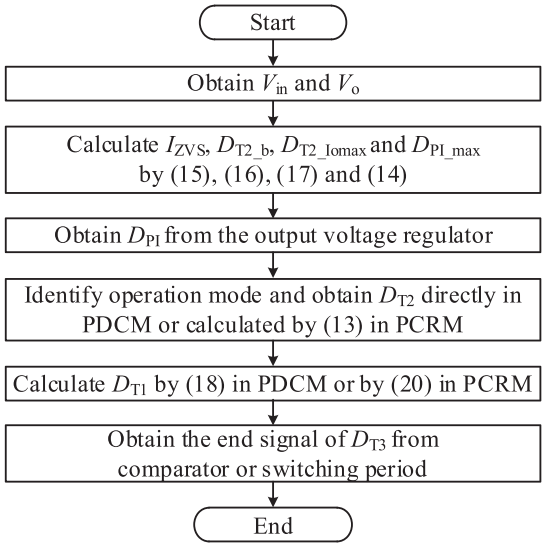

Fig. 7. Flowchart of the proposed control strategy in a switching cycle.

$$D_{T2\_Iomax} = \begin{cases} \dfrac{V_{in}V_o + \dfrac{2V_{in}^2 L_c C_{oss}}{T_s t_{dead}}}{V_{in}^2 + V_o^2 + V_{in}V_o} - \dfrac{2C_{oss}L_c}{T_s t_{dead}} & V_{in} < V_o \\ \dfrac{V_{in}V_o + \frac{2V_o^2 L_c C_{oss}}{T_s t_{dead}}}{V_{in}^2 + V_o^2 + V_{in}V_o} - \dfrac{2C_{oss}L_c}{T_s t_{dead}} & V_{in} \geq V_o \end{cases}. \quad (17)$$

Once C_{oss}, L_c, T_s, and t_{dead} are determined, some terms in (16) and (17), such as $(C_{oss}\, L_c/T_s\, t_{dead})$, are constant values, and the boundary conditions are mainly related with V_{in} and V_o. Since V_{in} and V_o can be easily obtained in digital control, a variable I_{ZVS} is used in this article to optimize the real-time calculations.

C. Control Process in One Switching Cycle

The overall operating process of the proposed control scheme in one switching cycle is shown in Fig. 7. Initially, some terms related with the given parameters are obtained as constant values. When V_{in} and V_o are sampled, I_{ZVS}, D_{T2_b}, D_{T2_Iomax} and D_{PI_max} are calculated by (15), (16), (17) and (14), which are used to determine the variation range of D_{PI} for different operation modes. Then, when D_{PI} is provided by the closed-loop PI controller, the proper operation mode is confirmed, and D_{T2} is obtained directly in PDCM or calculated by (13) in PCRM. Based on D_{T2}, D_{T1} for different operation modes can be obtained.

When the converter works in PDCM, I_{LcA} and I_{LcB} satisfy (5). According to (1)–(3), (5) and (15), D_{T1} is derived as

$$D_{T1} = \begin{cases} \left(\dfrac{V_o}{V_{in}} - 1\right) D_{T2} + \dfrac{4L_c C_{oss}}{T_s t_{dead}} \dfrac{V_o}{V_{in}} & V_{in} < V_o \\ \dfrac{4L_c C_{oss}}{T_s t_{dead}} & V_{in} \geq V_o \end{cases}. \quad (18)$$

Thus, the converter can be controlled in switching modes 1 and 2, successively.

When the converter enters switching mode 3, a $-I_{ZVS}$ cross detection is used to generate the turn-OFF signal of Q_3. The

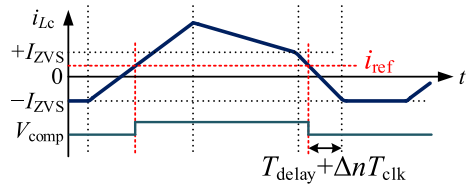

Fig. 8. Key waveforms for $-I_{ZVS}$ cross detection considering circuit delays.

represents a reference current i_{ref} through an analog comparator. When i_{Lc} drops to i_{ref}, the output signal of the comparator V_{comp} changes to a low level. At this moment, i_{Lc} does not reach $-I_{ZVS}$, and the turn-OFF signal for Q_3 is not provided until several controller clock cycles later, as shown in Fig. 8. The delay number of clock cycles, Δn, can be derived as

$$\Delta n = \frac{1}{T_{clk}}\left[\frac{L_c}{V_o}\left(i_{ref} + I_{ZVS}\right) - T_{delay}\right] \quad (19)$$

where T_{clk} is the period of the FPGA operation clock, and T_{delay} represents the total delay time caused by other factors, such as the comparator circuit, drive circuit, signal processing and switching time. In practice, T_{delay} can be measured with the experimental circuits, i_{ref} is set slightly higher than 0 considering the signal processing time, and Δn is calculated when V_o and the variable I_{ZVS} value are obtained.

When the converter works in PCRM, with $D_{T4} = 0$ and (1)–(3), D_{T1} varied with D_{T2} is derived as

$$D_{T1} = \frac{V_o - V_{in}D_{T2}}{V_{in} + V_o}. \quad (20)$$

Then, the converter is successively controlled in three switching modes.

In summary, since D_{T2} and D_{T1} in any operation mode can be obtained with a closed-loop PI controller and some simple calculations, the whole control scheme can be carried out in real-time based on digital controllers, and any operation mode transition caused by a change of load or input voltage can be smoothly regulated. As the inductor current is controlled in a proper operation mode in each switching cycle, an optimized load current is provided in any transient-state and steady-state.

IV. Experimental Verification

In order to verify the universality and control performance of the proposed control scheme, a 300 W prototype of FSBB converter is built in the lab. The switching frequency is set as 500 kHz. The main parameters and the main components of the prototype are listed in Tables I and II, respectively, and the photo of the prototype is shown in Fig. 9(a). Four 650-V GaN HEMTs (NV6128 from Navitas) are used as the power switches. The output capacitor of the MOSFETs, C_{oss}, is highly nonlinear, and it is replaced by a fixed equivalent value in calculations. For the input voltage range of 100-300 V, the maximum C_{oss} of the GaN HEMTs is about 120 pF. In order to achieve ZVS of all the switches in the whole input voltage range, $C_{oss} =$ 150 pF is used in calculations. The comparator is MAX9203 from Analog Devices. The total measured circuit delay of the designed converter is 146 ns, i_{ref} is set as 1 A to provide enough

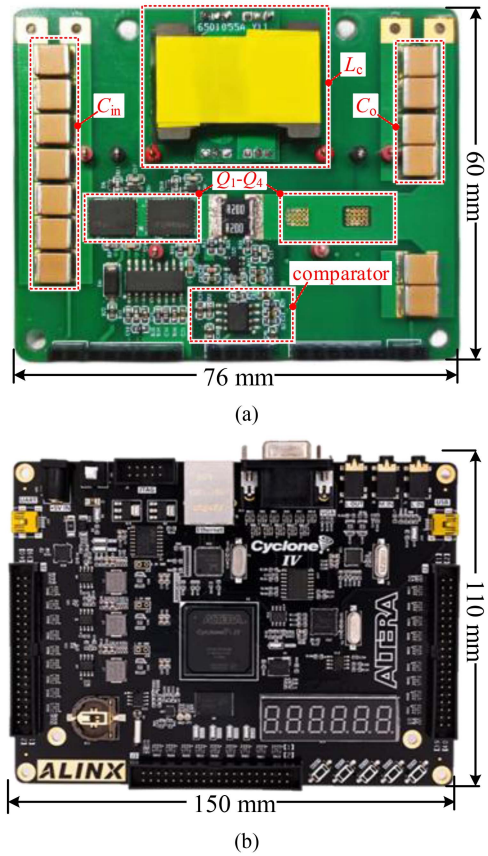

Fig. 9. Photograph of the (a) prototype and (b) FPGA control board.

TABLE I
MAIN PARAMETERS OF THE PROTOTYPE

Parameter	Value	Parameter	Value
Input Voltage V_{in}	100~300 V	Switching Frequency f_s	500 kHz
Rated Output Voltage V_o	200 V	Inductor L_c	12 μH
Rated Load current I_o	1.5 A	Output Capacitor C_o	10 μF
C_{oss}	150 pF	t_{dead}	60 ns

TABLE II
MAIN COMPONENTS OF THE PROTOTYPE

Components	Specification	Components	Specification
Switches Q_1~Q_4	GaN NV6128 650 V, 20A	FPGA	EP4CE15F23C8
Driver	SKYWORKS Si8274AB1-IS1	Comparator	Analog Devices MAX9203
Inductor L_c	TDK, PQI26/12 12 μH	Output Capacitor C_o	10*1μF, 250V MLCC, 10 μF

A 12 μH inductor is designed for providing the rated power in the whole input voltage range. A PQI-shaped core with PC95 material and a PCB winding is used to fabricate the inductor. By substituting (16) and (17) into (6) and (7), respectively, the load boundaries of the operation modes under different input voltages can be calculated, as shown in Fig. 10.

The deviation of the inductance has a major impact on the control accuracy, which should be considered in the control. In

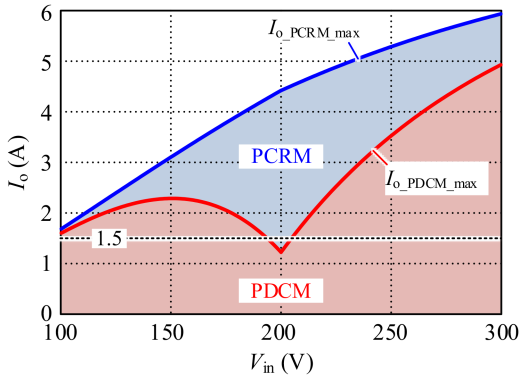

Fig. 10. Operation mode variation range in different V_{in}.

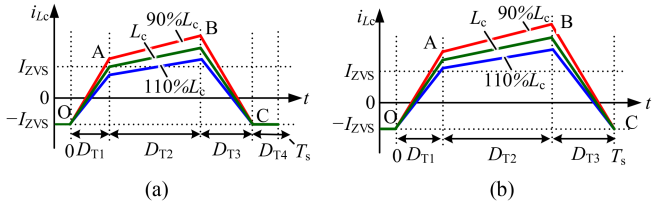

Fig. 11. Inductor current waveforms with different inductances for (a) pseudo discontinuous current mode and (b) pseudo critical continuous current mode.

the proposed control scheme, D_{T2} is provided by the closed-loop PI controller, and D_{T3} is determined by a comparator. Only D_{T1} is calculated by the controller based on (18) in PDCM or (20) in PCRM.

Taking the step-down conversion as an example, when D_{T2} and D_{T1} are obtained, the inductor current waveform for different inductances is shown in Fig. 11. As seen, if the actual inductance is lower than the designed one, the inductor current at point A will be higher than I_{ZVS}, and the power switches can still achieve ZVS. On the contrary, a larger actual inductance, will result in an inductor current lower than I_{ZVS} at point A, and the ZVS for Q_3 may be lost, especially in PDCM. In practice, considering the ZVS realization, a larger inductance or a larger I_{ZVS} can be used in the calculations, which will lead to a large D_{T1} and a high inductor current at point A. In this article, the calculated I_{ZVS} is multiplied by a coefficient of 1.5 to ensure ZVS.

Although the inductance deviation affects the inductor current and the output current, the closed-loop PI controller will adjust D_{PI} automatically to regulate the output voltage, and D_{T2} and D_{T1} will be regulated to proper values.

The digital control system adopts a general development FPGA control board AX515 from ALINX Company, as shown in Fig. 9(b), which uses an Altera's Cyclone IV series chip EP4CE15F23C8. The devices used in the FPGA for the proposed control scheme are given in Table III, which are used to execute all the variable calculations, clock process, digital filtering of the sampled input and output voltage, operating mode judgement, PWM output and so on. The whole control process for each switching cycle requires at least 30 clock cycles, and all the calculations can be completed in about 150 ns for an FPGA operation clock of 200 MHz.

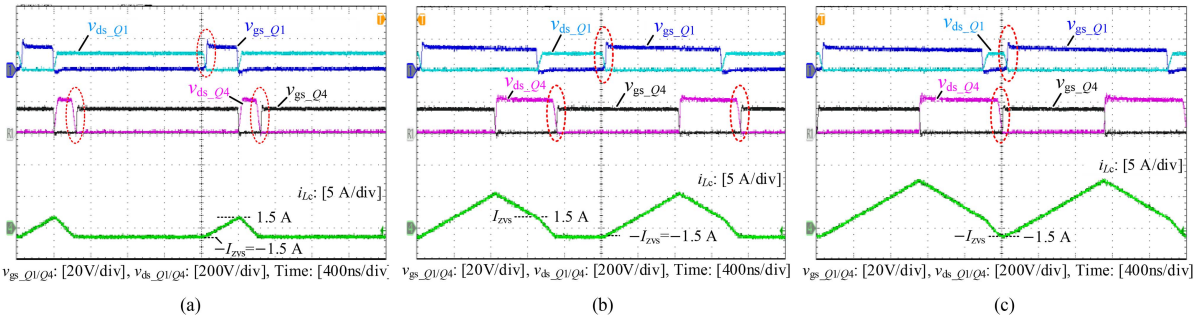

Fig. 12. Steady-state waveforms of the FSBB converter for $V_{\text{in}} = 100\,\text{V}$ at (a) no load, (b) half load, and (c) full load.

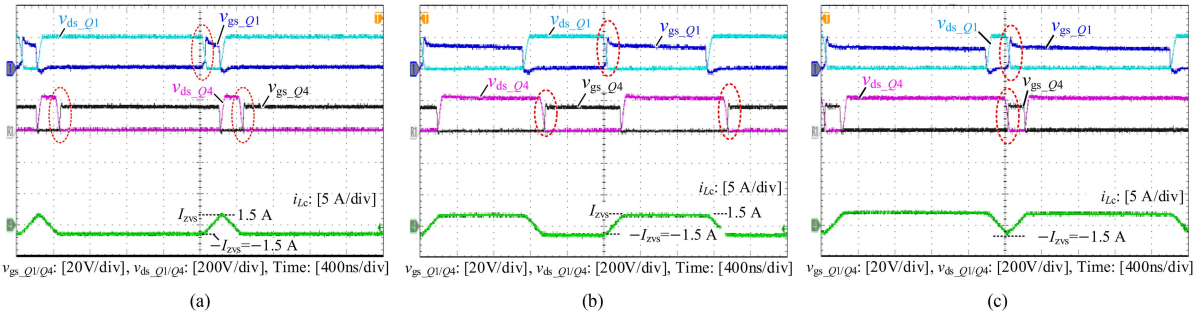

Fig. 13. Steady-state waveforms of the FSBB converter for $V_{\text{in}} = 200\,\text{V}$ at (a) no load, (b) half load, and (c) full load.

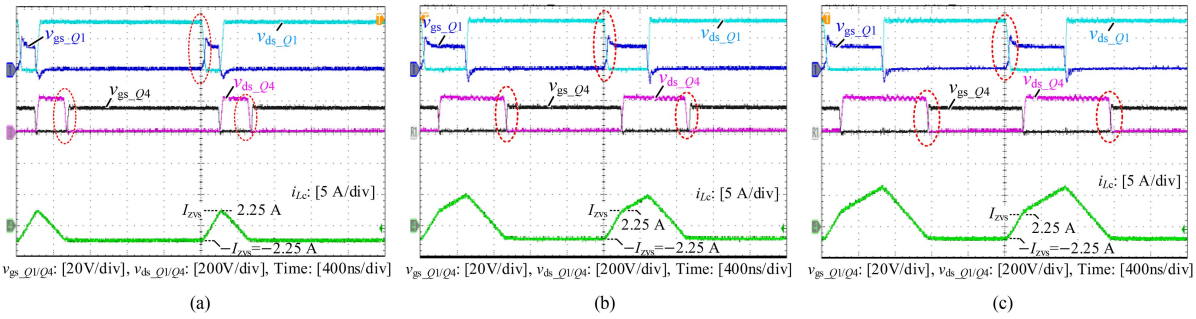

Fig. 14. Steady-state waveforms of the FSBB converter for $V_{\text{in}} = 300\,\text{V}$ at (a) no load, (b) half load, and (c) full load.

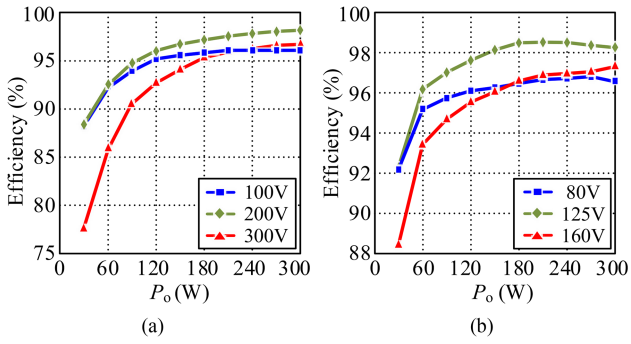

Fig. 15. Conversion efficiency of the FSBB converter in (a) a wide input voltage range, and (b) a narrow input voltage range.

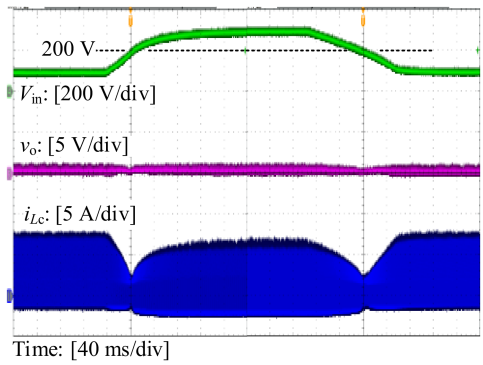

Fig. 16. Dynamic waveforms at full-load when the input voltage changes between 100 V and 300 V.

Since the calculations of the proposed control scheme are greatly simplified, which only involve addition, subtraction, multiplication and division, the proposed control scheme can also be implemented with low-cost digital controllers.

Figs. 12, 13, and 14 show the steady-state experimental waveforms of the FSBB converter at no-load, half-load and full-load conditions under different input voltages. $V_{\text{gs\_}Q1}$ and $v_{\text{gs\_}Q4}$

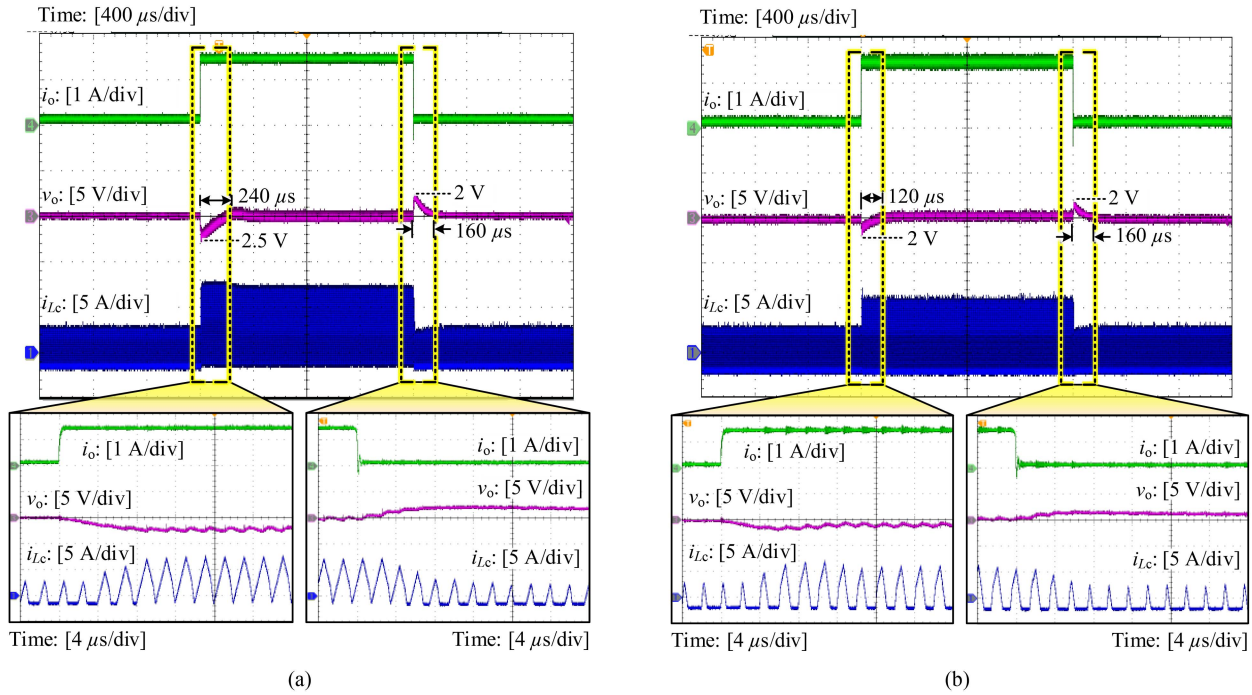

Fig. 17. Dynamic waveforms of the FSBB converter between 10% and 100% full-load at (a) $V_{\text{in}} = 100\,\text{V}$ and (b) $V_{\text{in}} = 300\,\text{V}$.

TABLE III
DEVICE USED IN THE FPGA FOR THE PROPOSED CONTROL

Parameter	Value	Parameter	Value
Total logic elements	7164	Total pins	32
Total combination of functions	6127	Embedded multiplier 9-bit elements	17
Dedicated logic registers	3845	Total PLLs	1

are the drive signals of power switches Q_1 and Q_4, and $v_{\text{ds\_}Q1}$ and $v_{\text{ds\_}Q4}$ are their drain-source voltages. i_{Lc} is the inductor current. As seen, the ZVS is achieved for Q_1 and Q_4. Likewise, Q_2 and Q_3 also realize ZVS. The inductor current ripple and RMS value are minimized in any operation mode. Since the variable I_{ZVS} is applied based on the higher value between the input and output voltages, I_{ZVS} is a constant value of 1.5 A when $V_{\text{in}} < V_o$, and increases to 2.25 A for $V_{\text{in}} = 300\,\text{V}$.

Fig. 15(a) shows the converter efficiency under different loads and input voltages. The converter operates in PDCM for most working conditions due to the wide input voltage range, as shown in Fig. 10. The maximum efficiency is 98.12% at $V_{\text{in}} = 200\,\text{V}$ and $I_o = 1.5\,\text{A}$. A 300 W prototype for the application with an narrow input voltage of 80–160 V and output voltage of 125 V is built, and the converter efficiency which is higher than that of the wide input voltage range is shown in Fig. 15(b).

Fig. 16 shows the dynamic waveform at full-load when the input voltage is changing between 100 V and 300 V, where v_o is the output voltage (ac coupled). As V_{in} changes, the converter has a smooth transition between PDCM and PCRM without any output voltage fluctuations, and also a smooth step-up and step-down conversions, meanwhile the switch ZVS with varied I_{ZVS} is achieved in the variation process.

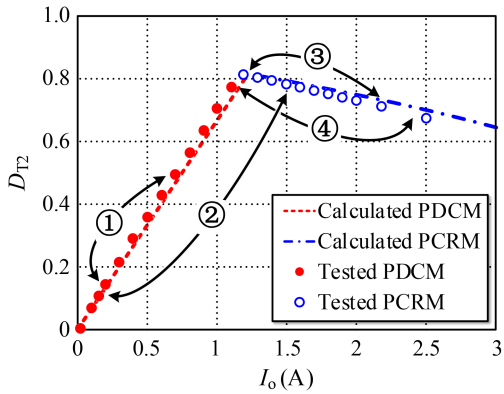

Fig. 18. D_{T2} varied with the load current when $V_{\text{in}} = V_o = 200\,\text{V}$.

Fig. 17 shows the dynamic waveform with step change between 10% and 100% load under different input voltages. When $V_{\text{in}} = 100\,\text{V}$, the converter operates in PDCM at 10% load and PCRM at full-load, and the transition process between PDCM and PCRM is smooth. The converter keeps in PDCM when $V_{\text{in}} = 300\,\text{V}$. In general, due to the real-time regulation, the inductor current changes to the steady state within limited regulation time, and the overshoot/undershoot of the output voltage is quite low. The switch ZVS is achieved in all the transit states and steady states.

Fig. 18 shows the steady-state D_{T2} that varies with the load current I_o when $V_{\text{in}} = V_o = 200\,\text{V}$, which has an operation mode changing in the whole load range, as shown in Fig. 10. The relationship between D_{T2} and I_o is positively correlated in PDCM and negatively correlated in PCRM. The variation trend of the experimental tests is in well agreement with the

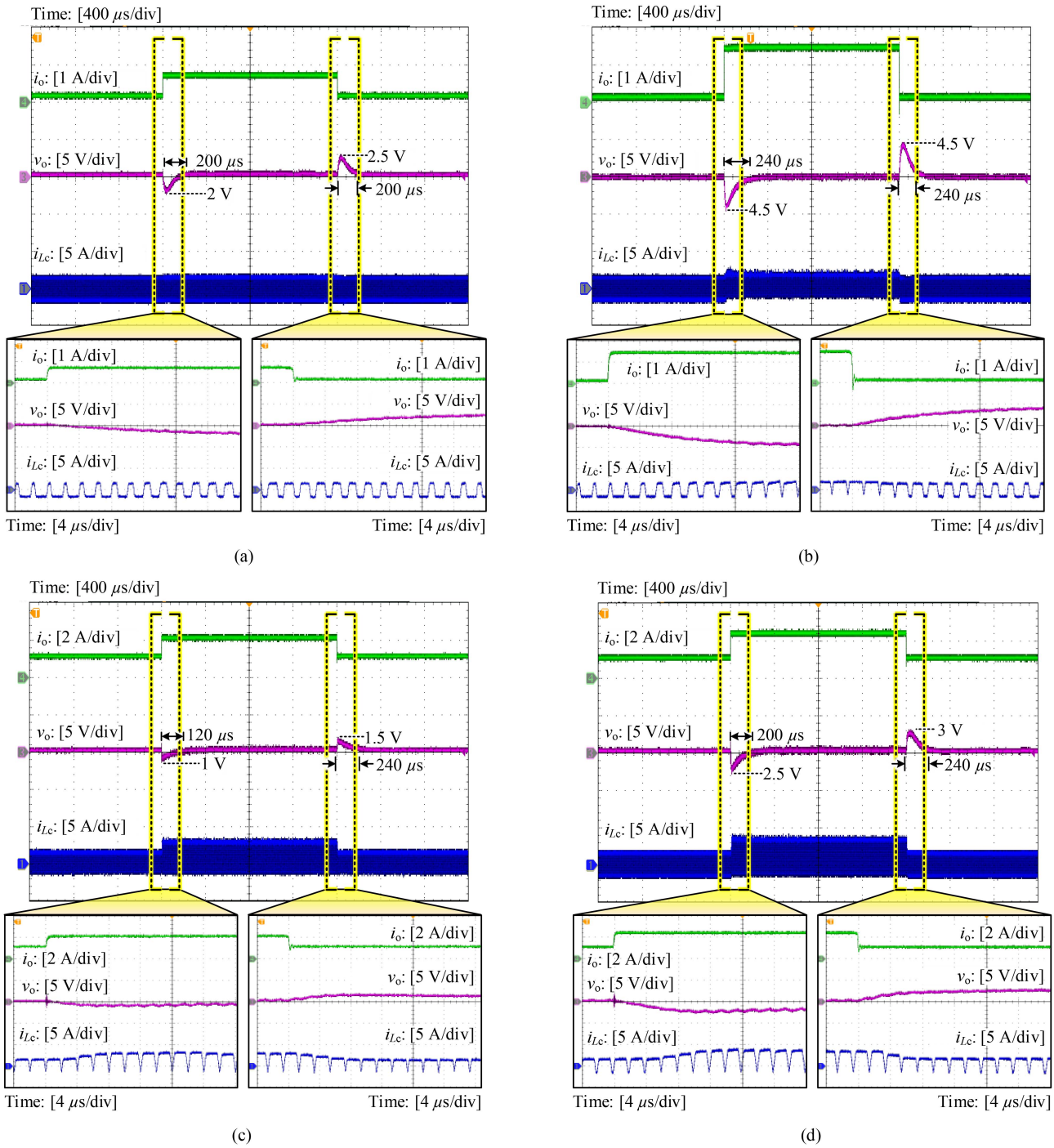

Fig. 19. Dynamic waveforms of the FSBB converter for $V_{\text{in}} = V_o = 200$ V under (a) condition change ①, (b) condition change ②, (c) condition change ③, and (d) condition change ④.

theoretical calculation curve. Since the power losses are ignored in the calculation, the experimental values of D_{T2} are higher in PDCM and lower in PCRM, which leads to a higher input power than the theoretical values.

Fig. 19 shows the dynamic waveform in different step changes in load current as presented in Fig. 18. For the load variation only in PDCM (marked ①) and the load change between a light load in PDCM and a heavy load in PCRM (marked ②), D_{T2} increases as the load current increases. For the load change in PCRM (marked ③) and between the heavy load in PDCM and a heavier load in PCRM (marked ④), D_{T2} decreases as the load current increases. Since the inductor current in each switching cycle is regulated to realize the switch ZVS and achieve minimum RMS value of inductor current, the converter can work smoothly when there is any variation of operation modes and working conditions.

V. Conclusion

In this article, a constant switching frequency real-time quadrilateral inductor current ZVS control scheme for the FSBB converter is proposed. According to the input and output voltages and given parameters of the converter, the proper operation mode in each switching cycle can be identified in real-time, and the needed D_{T2} in PDCM or PCRM, as well as other control variables, are attained from an output voltage regulator and simple calculations. As a result, the ZVS of each switch and the minimum RMS value of the inductor current in a wide input voltage and load range are achieved at any steady-state and transient-state, and a fast and smooth transition is achieved in any step change in the input voltage or load current.

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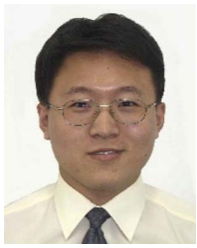

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