The Influence and Optimization Constraints of SiC Power Module Layout on High-Frequency Conducted CM Current During Switching Transients

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***Abstract*—The penetration rate of SiC MOSFETs is gradually increasing due to their excellent electrical and thermal characteristics. However, the wide-bandgap devices exhibit faster di/dt, dv/dt and are more sensitive to parasitic inductances of power module during switching transients. Meanwhile, the influence of parasitic inductances on the propagation path of electromagnetic interference cannot be ignored either. The coupling between the switching transient waveforms and the propagation paths is formed through parasitic inductances. This article elucidates the impact of parasitic inductances and capacitances of power modules at different positions on common mode (CM) current during switching transients and provide constraints for the optimal range of parasitic parameters by establishing a conducted time-domain CM mathematical model considering power modules's parasitic parameters. The switching waveforms are divided into CM noise sources and differential mode (DM) noise sources. So the CM current is not only related to the CM noise source, but also to the DM noise source due to the asymmetric parasitic parameters of the power module. Based on the analysis, this article can identify the impact of parasitic parameters at different positions of power modules on CM current at different switching stages and guide the selection and redesign of the commercial power modules to reduce CM current and switching losses based on the switching characteristics. In the experiment, the double pulse test with power module BSM120D12P2C005 is established, and the influence of different layouts of power modules on CM current is verified and compared.**

***Index Terms*—Common mode (CM) current, electromagnetic interference (EMI) model, parasitic parameters, power module, SiC MOSFETs.**

NOMENCLATURE

C_{13}	Sum of C_1 and C_3.
C_{23}	Sum of C_2 and C_3.
C_{123}	Sum of C_1, C_2, and C_3.
L_{12}	Sum of L_1, L_2.
L_{sum}	Sum of L_1, L_2, L_{s1}, and L_{s2}.
p_1	L_1 divided by L_{s1}.
p_2	L_2 divided by L_{s1}.
p_3	L_{s2} divided by L_{s1}.
n	C_2 divided by C_3.
q	C_1 divided by C_3.
SN-HF	Soft turn-ON and hard turn-OFF.
HN-HF	Hard turn-ON and hard turn-OFF.
CRM	Critical conduction mode.
CCM	Continuous conduction mode.

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I. Introduction

THE power devices are the core of converters. Compared with Si IGBTs and diodes, SiC MOSFETs have the advantages of higher operating temperature, higher breakdown voltage, and faster switching speed. In addition, the body diode of SiC MOSFETs or SiC SBDs can reduce the reverse recovery current. By increasing the switching speed and frequency, the efficiency and power density of the converter based on wide-bandgap devices can be significantly improved. However, faster dv/dt and higher switching frequency will cause more serious electromagnetic interference (EMI) noise [1].

The factors affecting conducted EMI include noise sources, propagation paths, and disturbed equipment. The line impedance stabilization network (LISN) can be used for disturbed equipment because it provides three functions: preventing noise from flowing from the power supply to the equipment under test (EUT) and vice versa, allowing noise from the EUT to be conducted to the measurement equipment, and providing a standard impedance to ensure consistent and repeatable test conditions. [2]. Therefore, only the noise source and propagation path need to be researched and analyzed in the EMI model.

A. Noise Sources

The switching devices, such as IGBTs, MOSFETs, or Diodes, are the noise sources of EMI during switching process. According to the substitution theorem, the switching devices can be substituted by voltage sources or current sources [3], [4].

In traditional EMI models, the trapezoidal waveform is often used for switching equivalent voltage waveform. Fig. 1 shows the common mode (CM) circuit model based on a double

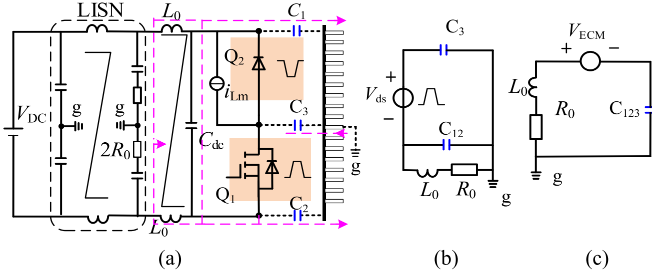

Fig. 1. Traditional CM circuit model without considering parasitic inductance. (a) CM current test circuit based on DPT. (b) Simplified ECM circuit. (c) ECM circuit.

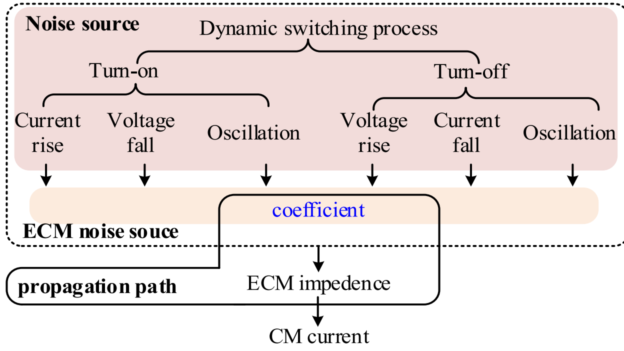

Fig. 2. CM current analysis flow chart.

pulse testing (DPT) circuit. The high-side and low-side devices can be replaced with trapezoidal waveform respectively. The voltage waveforms of the high-side and low-side devices are complementary because their sum is equal to the dc bus voltage. Therefore, the voltage waveforms of both the high-side and low-side devices form a CM noise source. Han et al. [5] used trapezoidal waveform to analyze the influence of switching frequency and switching speed on the conducted EMI spectrum. The influence of driving parameters on the conducted EMI of IGBT modules was analyzed in [6].

However, due to the faster switching speed of SiC MOSFETs, the loop parasitic inductance can no longer be ignored during the switching process [7], [8]. The parasitic inductances worsen the switching waveforms and cause switching oscillations during the switching process [9]. Even it can change the switching trajectory [10], [11], [12]. The voltage waveforms of both high-side and low-side devices not only form CM noise sources but also DM noise sources. The traditional noise source without considering parasitic inductances was inaccurate, especially high-frequency[13]. Therefore, the ideal trapezoidal waveform can no longer replace the switching waveform of SiC MOSFETs.

The voltage waveform of SiC MOSFETs is related to the dynamic switching process, including current slew rate, voltage slew rate, and oscillation, as shown in Fig. 2. Many papers have analyzed the switching process in detail [14], [15]. The detailed EMI spectrum envelope analytic expressions were derived considering Miller platform, reverse conduction, and ringing effects in [16]. The frequency spectrum of the switching voltage waveform is calculated and analyzed in [13]. However, these more accurate switching voltage waveforms are not further used for EMI models. In this article, the switching waveforms are further decoupled into CM noise and DM noise.

B. Propagation Path

The propagation paths are related to CM filter and the parasitic parameters of power module. The CM capacitances of power module play an important role in the propagation paths [17], [18]. Fig. 1 shows the equivalent CM (ECM) conduction model without considering parasitic inductances of power module. The C_1, C_2, and C_3 are the parasitic capacitances from dc+, dc−, and AC to the baseplate, respectively. The C_{12} is the sum of C_1 and C_2. The C_{123} is the sum of C_{12} and C_3. The sum of the high-side and low-side device voltages without considering parasitic inductances is equal to the dc bus voltage. So the voltage of power devices based on half-bridge structure has only one degree of freedom. The low-side device can be equivalent to a voltage noise source. The ECM noise source and ECM impedance are expressed in [19] as

$$\begin{cases} V_{\mathrm{ECM}} = -\frac{C_3}{C_{123}} V_{\mathrm{ds}} = -k V_{\mathrm{ds}} \\ Z_{\mathrm{ECM}} = sL_0 + R_0 + 1/sC_{123} \end{cases}. \tag{1}$$

The coefficient k establishes the connection between noise source and ECM noise source without considering parasitic inductances.

Due to the faster switching speed of SiC MOSFETs, the parasitic inductances cannot be ignored either in the propagation paths. The traditional CM current propagation path without considering parasitic inductances is inaccurate, especially high-frequency [20]. In order to obtain a more accurate CM propagation path, the nonideal parasitic parameters need to be considered in the CM model. The CM current caused by differential mode (DM) voltage is analyzed due to the unbalance of dc bus parasitic capacitances C_{ug} and C_{lg} [21]. However, the DM voltage is equivalent to the DC CM voltage noise source, ignoring the changes in the drain voltage of high-side device and source voltage of low-side device caused by parasitic inductances [21]. The propagation path considering all parasitic parameters is given [22], [23], [24], [25], [26]. However, only the simulation and experiment are compared. The impact of parasitic parameters on CM current has not been analyzed.

C. CM Model

The CM current depends on the noise sources and the propagation paths simultaneously. Both of these are related to parasitic inductances. Therefore, the traditional model that does not consider parasitic inductances is inaccurate [19]. In addition, the CM models where parasitic inductances are only considered in noise sources or propagation paths are also inaccurate [21], [23]. To obtain a more accurate CM model, parasitic inductances need to be considered simultaneously in both the noise sources and propagation paths. The DM and CM models considering all parasitic parameters have been established and solved using MATLAB [23], [27], [28]. And the effect of parasitic parameters on propagation paths and noise sources is analyzed separately.

Although numerical solutions can be obtained through simulation software, analytical expressions cannot be obtained and the effect of parasitic inductances cannot be further understood. The coupling formed by parasitic inductances between the noise sources and the propagation paths has not been analyzed either. So, the phenomenon of different CM currents during the turn-ON and turn-OFF processes cannot be explained in [17].

The parasitic inductances cause coupling between noise sources and propagation paths. In order to establish the analytical expression for the CM model considering parasitic inductances, each stage during the switching process needs to be analyzed. This article presents a conducted CM mathematical model considering parasitic inductances, establishing the relationship between the noise source and ECM noise source. The model connects the CM current with the dynamic switching process. The transient time domain CM current can be obtained during the switching process, which is more intuitive than the CM current spectrum. Based on the model, the impact of parasitic inductances and capacitances of power modules at different positions on CM current is analyzed.

D. CM Current Suppression Method

Generally, reducing noise source and increasing propagation path impedance are two ways to suppress EMI noise.

The noise source indexes include switching frequency, voltage slew rate, and oscillation [5], [13]. The voltage slew rate often compromises between switching losses and EMI based on the DPT circuit [1]. The methods of suppressing high-frequency oscillation mainly focus on the new packaging structure by reducing parasitic inductance, adding a snubber circuit. and decoupling capacitances [29], [30], [31], [32], [33], [34].

Increasing the propagation path impedance or changing the CM current propagation path can also suppress the CM current. For example, stacking two direct bonded coppers (DBCs) and connecting the shielding layer to a static potential [35], [36], [37]. The capacitances between the shielded node and ground are reduced due to the increased dielectric thickness. Therefore, the propagation path impedance is increased. However, the stacking DBCs increase the thermal resistance of the power module.

This article aims to establish a conducted CM model considering parasitic parameters to identify the impact of parasitic parameters on CM current at different switching stages and guide the selection and redesign of power modules to reduce the amplitude of CM current in the time domain and frequency domain.

The main contributions are given as follows.

1) The CM mathematical model considering parasitic parameters of the power module is derived, including ECM impedance and ECM voltage. That reveals the difference between the traditional model and the proposed model.
2) The relationship between ECM noise sources and switching waveforms is derived. The switching waveforms are divided into three parts. Each part is related to the stage of switching process and has a clear meaning.

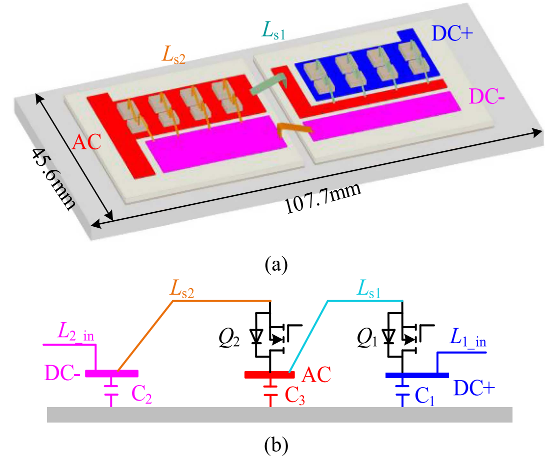

Fig. 3. Internal structure layout of power module BSM120D12P2C005. (a) Physical structure. (b) Equivalent circuit diagram.

TABLE I
PARASITIC PARAMETERS OF POWER MODULE BSM120D12P2C005

L_{1_in}	L_{2_in}	L_{s1}	L_{s2}	C_1	C_2	C_3
3nH	3nH	6.6nH	9.7nH	56pF	80pF	102pF

3) The effect of power module's parasitic parameters at different positions on CM current is analyzed during the turn-ON and turn-OFF, respectively. According to the switching characteristics, power modules with different layouts can be selected and redesigned to reduce CM current.

The rest of the article is organized as follows. Section II establishes the conducted ECM mathematical model. The ECM noise voltages are derived with respect to the high-side and low-side device voltages during switching process in Section III. Section IV analyzes the effect of parasitic parameters on the ECM noise voltages and gives the constraints of the optimal region. The model and the effect of different parasitic parameters on the CM current are verified by experiments in Section V. Section V also verifies the model based on different switching characteristics and power module layouts. Section VI provides conclusions.

II. CONDUCTED CM MODELING CONSIDERING PARASITIC PARAMETERS

A. High-Frequency CM Circuit Modeling

Fig. 3 shows the internal physical structure layout and equivalent circuit of the power module BSM120D12P2C005 from ROHM. The power module, consisting of eight bare dies on the high-side and on the low-side, respectively, forms a half-bridge structure. The L_{s1} is the sum of parasitic inductance from the source of high-side dies to ac. The L_{s2} is the sum of parasitic inductance from the source of low-side dies to dc-. L_{1_in} and L_{2_in} are the parasitic inductance of the dc+ and dc- terminal inside the power module, respectively. Table I shows the parasitic parameters of power module BSM120D12P2C005 extracted by ANSYS Q3D.

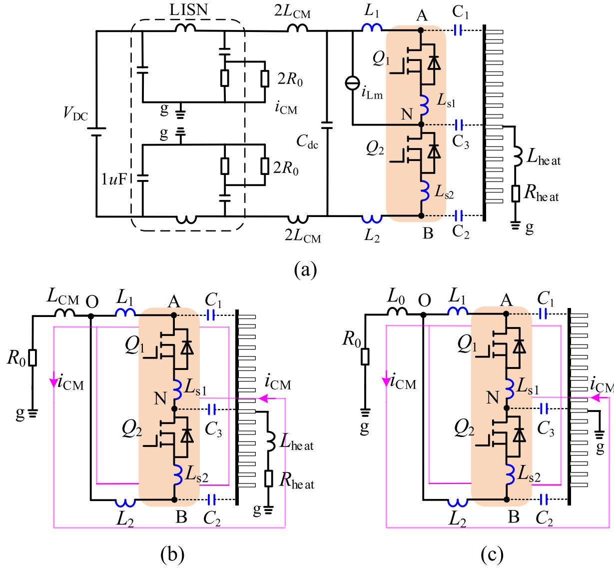

Fig. 4. Conducted CM circuit modeling considering parasitic parameters of power module. (a) EMI modeling. (b) High-frequency CM modeling. (c) Simplified high-frequency CM modeling.

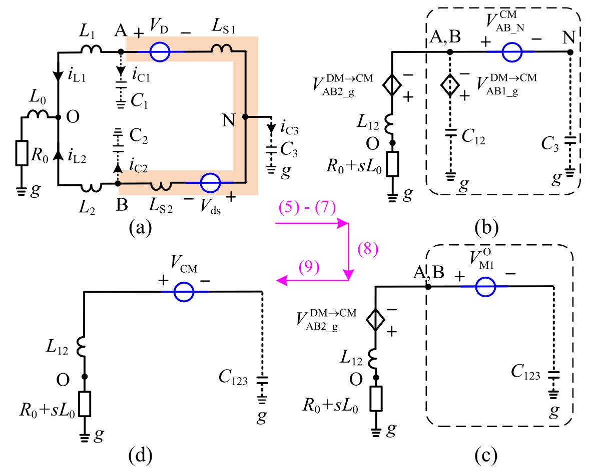

Fig. 5. Conducted equivalent CM modeling considering parasitic parameters of power module. (a) Original circuit. (b) Equivalent circuit after decoupling of noise sources. (c) Equivalent circuit in (b) derived using Thevenin's theorem. (d) Final equivalent model.

Fig. 4(a) shows the EMI circuit diagram based on the power module in Fig. 3. The parasitic inductances L_1 and L_2 also include Busbar parasitic inductances in the test circuit: $L_1 = L_{1_in}+L_{1_ext}$, $L_2 = L_{2_in}+L_{2_ext}$. The L_{1_ext} and L_{2_ext} are the Busbar parasitic inductances, also known as external parasitic inductances of power modules. The L_{heat} and R_{heat} are the inductance and resistance of the connection wires between the heat sink and the LISN. The C_{dc} is a decoupling capacitance with low parasitic inductance. The $2R_0$ is the 50 Ω internal resistance of the measuring equipment or terminal. The LISN is a simplified circuit diagram, and its main function is to provide a stable impedance and CM current path in this article. The L_{CM} can be considered as either line inductance or CM inductance, which does not affect the analysis process. The i_{CM} is the CM current flowing from LISN to the heat sink caused by power device switching. The V_{DC} is the dc bus voltage. The i_{Lm} is the inductive load current, which is almost constant during switching transients due to the large inductance value.

The voltage V_{DC}, current i_{Lm} and high-side device Q_1 and low-side device Q_2 of the power module are noise sources of CM current. When only considering high-frequency CM current, the V_{DC} and low impedance capacitance C_{dc} can be regarded as short circuit and the current i_{Lm} can be regarded as open circuit. The LISN and measuring equipment/terminal can be regarded as resistance $2R_0$. The impact of parasitic parameters of the decoupling capacitor and LISN on the high-frequency equivalent circuit is discussed separately in Appendix B and C. Therefore, the high-frequency ECM circuit can be obtained from Fig. 4(a), as shown in Fig. 4(b).

The components L_{heat}, R_{heat}, and L_{CM} are on the same branch. Within the conducted EMI frequency range, the inductive reactance is much greater than the resistance. Therefore, the effect of resistance on CM current can be ignored. Then, these components can be combined into a single component L_0. In other words, the impedance of the heatsink can be considered as part of the CM filter, as shown in Fig. 4(c). In Fig. 4(c), the CM current is caused by the high-side device Q_1 and low-side device Q_2 of the power module. The purpose of the following derivation process is to obtain the CM current generated by the high-side device Q_1 voltage and low-side device Q_2 voltages during switching transients.

B. ECM Mathematical Modeling

Fig. 5 shows the equivalent process of the high-frequency EMI model. When considering parasitic inductances, the sum of the high-side device and low-side device voltages in Fig. 4(b) is not equal to the dc voltage. Therefore, the voltage of the high-side device and low-side device can be regarded as two independent noise voltage sources, V_D and V_{ds}, as shown in Fig. 5(a). The i_{C1}, $i_{C2,}$ and i_{C3} are the currents of parasitic capacitances C_1, C_2, and C_3, and the i_{L1} and i_{L2} are the currents of parasitic inductance L_1 and L_2. respectively.

The CM noise voltage and DM noise voltage with nodes N and g as the reference are defined as

$$\begin{cases} V_{AB_N}^{CM} = (V_{AN} + V_{BN})/2 \\ V_{AB_g}^{CM} = (V_{Ag} + V_{Bg})/2 = V_{AB_N}^{CM} + V_{Ng} \\ V_{AB_N}^{DM} = V_{AB_g}^{DM} = V_{AN} - V_{BN} = V_{Ag} - V_{Bg} \end{cases} \tag{2}$$

where V_{AN}, V_{BN}, V_{Ag}, $V_{Bg,}$ and V_{Ng} are the voltage between two subscript nodes, for example, V_{AN} represents the voltage between nodes A and N. The CM current and DM current of parasitic capacitances C_1, $C_{2,}$ and parasitic inductance L_1 and L_2 are defined as

$$\begin{cases} i_{C12_g}^{CM} = i_{C1}+i_{C2} \\ i_{C12_g}^{DM} = (i_{C1} - i_{C2})/2 \end{cases} \tag{3}$$

$$\begin{cases} i_{\mathrm{L12_g}}^{\mathrm{CM}} = i_{\mathrm{L1}} + i_{\mathrm{L2}} \\ i_{\mathrm{L12_g}}^{\mathrm{DM}} = (i_{\mathrm{L1}} - i_{\mathrm{L2}})/2 \end{cases}. \tag{4}$$

The relationship between the CM current of parasitic capacitances and CM noise voltage and DM noise voltage is derived in Appendix A

$$i_{\mathrm{C12_g}}^{\mathrm{CM}} = \frac{Z_{\mathrm{C_1}} + Z_{\mathrm{C_2}}}{Z_{\mathrm{C_1}} Z_{\mathrm{C_2}}} V_{\mathrm{AB_g}}^{\mathrm{CM}} + \frac{Z_{\mathrm{C_2}} - Z_{\mathrm{C_1}}}{Z_{\mathrm{C_1}} Z_{\mathrm{C_2}}} \frac{V_{\mathrm{AB_g}}^{\mathrm{DM}}}{2} \tag{5}$$

where Z_{C1} and Z_{C2} are the impedance of parasitic capacitances C_1 and C_2. The CM current of parasitic capacitances consists of two parts, one is generated by the CM noise voltage, and the other is caused by the DM noise voltage due to the asymmetry of the CM capacitance C_1, C_2. The CM noise voltage can be obtained by rearranging (5)

$$\begin{cases} V_{\mathrm{AB_g}}^{\mathrm{CM}} = \frac{1}{sC_{12}} i_{\mathrm{C12_g}}^{\mathrm{CM}} - V_{\mathrm{AB1_g}}^{\mathrm{DM\to CM}} \\ V_{\mathrm{AB1_g}}^{\mathrm{DM\to CM}} = \frac{C_1 - C_2}{C_{12}} \frac{V_{\mathrm{AB_g}}^{\mathrm{DM}}}{2} \end{cases} \tag{6}$$

where C_{12} is the sum of parasitic capacitances C_1 and C_2. The CM noise voltage also includes the DM noise voltage due to the asymmetry of CM capacitances C_1 and C_2 as expressed in (6). When CM capacitance C_1 equals C_2, $V_{\mathrm{AB1_g}}^{\mathrm{DM\to CM}}$ equals 0. Similarly, the CM noise voltage of parasitic inductances L_1 and L_2 branches can also be obtained

$$\begin{cases} V_{\mathrm{AB_g}}^{\mathrm{CM}} = s\frac{L_1 L_2}{L_{12}} i_{\mathrm{L12_g}}^{\mathrm{CM}} - V_{\mathrm{AB2_g}}^{\mathrm{DM\to CM}} + V_{\mathrm{Og}} \\ V_{\mathrm{AB2_g}}^{\mathrm{DM\to CM}} = \frac{L_2 - L_1}{L_{12}} \frac{V_{\mathrm{AB_g}}^{\mathrm{DM}}}{2} \end{cases} \tag{7}$$

where L_{12} is the sum of parasitic inductances L_1 and L_2. When CM inductance L_1 equals L_2, $V_{\mathrm{AB2_g}}^{\mathrm{DM\to CM}}$ equals 0. Fig. 5(a) can be simplified to Fig. 5(b) by using (2)–(7). Fig. 5(b) can be simplified to Fig. 5(c) using (8) and Thevenin theorem

$$V_{\mathrm{M1}}^{\mathrm{O}} = \frac{C_3}{C_{123}} \left(V_{\mathrm{AB_N}}^{\mathrm{CM}} + V_{\mathrm{AB1_g}}^{\mathrm{DM\to CM}} \right) - V_{\mathrm{AB1_g}}^{\mathrm{DM\to CM}} \tag{8}$$

where C_{123} is the sum of parasitic capacitances C_1, C_2, and C_3. The final CM high-frequency equivalent model can be obtained, as shown in Fig. 5(d). In order to distinguish from the traditional model without considering parasitic inductance, it is called the modified model. The ECM noise voltage and impedance of the modified model can be expressed as

$$\begin{cases} V_{\mathrm{ECM}} = V_{\mathrm{M1}}^{\mathrm{O}} + V_{\mathrm{AB2_g}}^{\mathrm{DM\to CM}} \\ Z_{\mathrm{ECM}} = \frac{sL_1 L_2}{L_{12}} + sL_0 + R_0 + \frac{1}{sC_{123}} \end{cases}. \tag{9}$$

The effect of parasitic inductance of the decoupling capacitances on the model is discussed in Appendix B.

The Bode diagram of the ECM impedance of the traditional model (1) and the modified model (9) with different parasitic inductances L_1 and L_2 can be obtained as shown in Fig. 6. The ECM impedance is almost independent of the parasitic inductances L_1, L_2.

However, the phase and amplitude of CM current are not only related to ECM impedance but also related to ECM noise source. The ECM noise voltage related to parasitic parameters can be obtained according to (2)–(9)

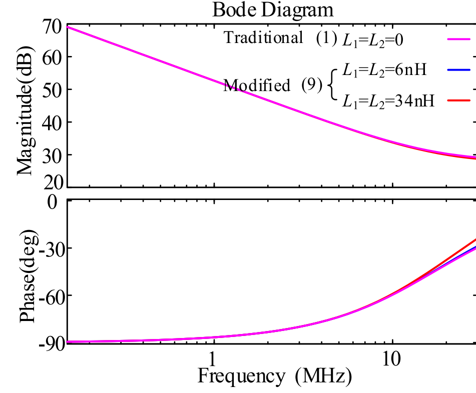

Fig. 6. Bode diagram of the ECM impedance of the traditional model and modified model with different parasitic inductance L_1, L_2.

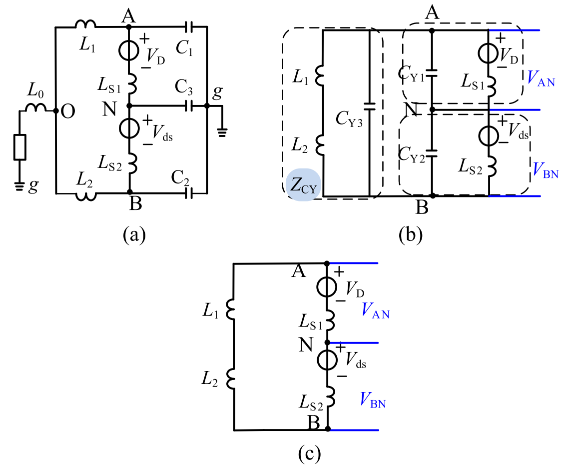

Fig. 7. The simplified process of noise voltage. (a) Original circuit. (b) Equivalent circuit after ignoring LISN. (c) Final simplified circuit.

$$V_{\mathrm{ECM}} = \frac{(L_2 C_{23} - L_1 C_1) V_{\mathrm{AN}} + (L_1 C_{13} - L_2 C_2) V_{\mathrm{BN}}}{L_{12} C_{123}}. \tag{10}$$

The relationship between V_{AN}, V_{BN}, and V_{D}, V_{ds} will be introduced in Section III.

Therefore, in the proposed mathematical model, the ECM propagation path impedance is the same as the traditional impedance. However, the influence of power module's parasitic parameters is represented by ECM noise voltage V_{ECM}. The ECM noise voltage at each stage of the switching process is analyzed in Section III.

III. ECM Noise Voltage During Switching Process

A. *Relationship Between* V_{AN}, V_{BN} *and* V_{D}, V_{ds}

Generally, the influence of CM current on noise sources can be ignored because their orders of magnitude are different. Therefore, compared with the noise source, the voltage drop of high-frequency CM noise voltage on LISN can be ignored. Fig. 7(a) can be simplified to Fig. 7(b). The impedance C_{Y1},

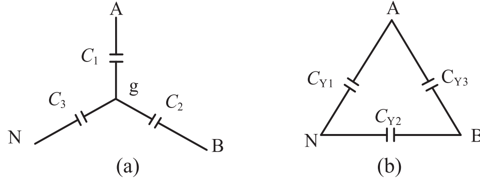

Fig. 8. Y-△ impedance transformation. (a) Y impedance. (b) △ impedance.

$C_{Y2,}$ and C_{Y3} as shown in Fig. 7(b) can be obtained by Y-Δ transformation, as shown in Fig. 8

$$\begin{cases} Z_{C_{Y1}} = (Z_{C_1}Z_{C_2} + Z_{C_2}Z_{C_3} + Z_{C_3}Z_{C_1})/Z_{C_2} \\ Z_{C_{Y2}} = (Z_{C_1}Z_{C_2} + Z_{C_2}Z_{C_3} + Z_{C_3}Z_{C_1})/Z_{C1} \\ Z_{C_{Y3}} = (Z_{C_1}Z_{C_2} + Z_{C_2}Z_{C_3} + Z_{C_3}Z_{C_1})/Z_{C_3} \end{cases}. \quad (11)$$

Generally, the parasitic capacitances C_1, C_2, and C_3 are less than the output capacitances of the power devices. At the same time, the capacitances C_{Y1}, C_{Y2}, and C_{Y3} are smaller than capacitances C_1, C_2, and C_3 due to Y-Δ transformation. Therefore, the influence of parasitic capacitances C_1, C_2, and C_3 on the noise source can be ignored below the resonant frequency of the noise source[38]. Fig. 7(b) can be simplified to Fig. 7(c).

We can get the relationship between voltages V_{AN}, V_{BN} and V_{D}, V_{ds} according to Fig. 7(c)

$$\begin{cases} V_{\mathrm{AN}} = \frac{L_{12}+L_{s2}}{L_{\mathrm{sum}}}(V_{\mathrm{D}} + V_{\mathrm{ds}}) - V_{\mathrm{ds}} \\ V_{\mathrm{BN}} = \frac{L_{s2}}{L_{\mathrm{sum}}}(V_{\mathrm{D}} + V_{\mathrm{ds}}) - V_{\mathrm{ds}} \end{cases} \quad (12)$$

where L_{sum} is the sum of parasitic inductances L_1, L_2, L_{s1}, and L_{s2}. Due to the commutation parasitic inductance, the voltage and current waveforms are asymmetric during turn-ON and turn-OFF process. Therefore, it is necessary to analyze different stages during switching process in detail.

B. CM Noise Voltage During Turn-ON Process

According to Kirchhoff's voltage law, the state equation in Fig. 7(c) can be expressed as

$$V_{\mathrm{D}}^{\mathrm{on}}(t) + V_{\mathrm{ds}}^{\mathrm{on}}(t) + L_{\mathrm{sum}}\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} = 0. \quad (13)$$

The superscript "on" of V_{D} and V_{ds} represents the turn-ON process. According to the superposition theorem, high-side and low-side noise voltage can be divided into two parts: voltage exchange $V_{\mathrm{D}}^{\mathrm{on}}(\mathrm{tri})$, $V_{\mathrm{ds}}^{\mathrm{on}}(\mathrm{tri})$, and voltage oscillation $V_{\mathrm{D}}^{\mathrm{on}}(\mathrm{osci})$, $V_{\mathrm{ds}}^{\mathrm{on}}(\mathrm{osci})$.

$$\begin{cases} V_{\mathrm{D}}^{\mathrm{on}}(t) = V_{\mathrm{D}}^{\mathrm{on}}(\mathrm{tri}) + V_{\mathrm{D}}^{\mathrm{on}}(\mathrm{osci}) \\ V_{\mathrm{ds}}^{\mathrm{on}}(t) = V_{\mathrm{ds}}^{\mathrm{on}}(\mathrm{tri}) + V_{\mathrm{ds}}^{\mathrm{on}}(\mathrm{osci}) \end{cases} \quad (14)$$

Fig. 9 shows equivalent circuit diagram during turn-ON process, and Fig. 10 shows the noise voltage source V_{D}, V_{ds} and current i_{d} switching waveform. The C_{D} and C_{ds} are the output capacitances of the high-side and low-side devices, respectively. The i_{d} is the power loop current. The i_{ch} and i_{ds} are the channel current and output capacitance current of the low-side device, respectively. The power loop remains unchanged until the gate voltage reaches the threshold voltage. The low-side device is the active device.

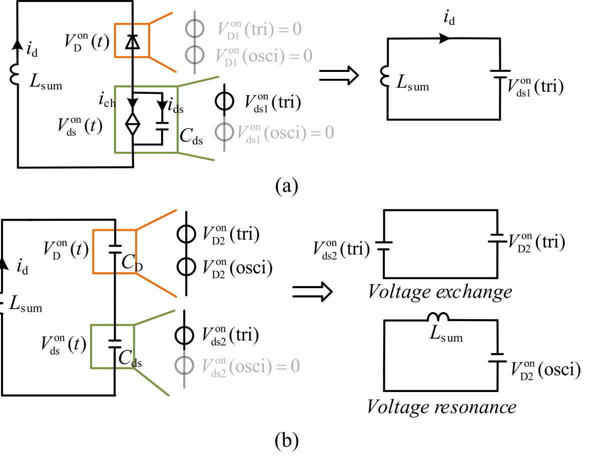

Fig. 9. Equivalent circuit diagram during turn-ON process. (a) Current rise stage (b). Voltage fall stage.

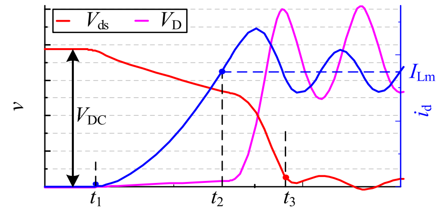

Fig. 10. Piecewise transition waveforms during turn-ON process.

1) Current Rise Stage (t_1–t_2): The high-side voltage V_{D} remains unchanged during current rise stage. So the high-side noise voltage and low-side noise voltage can be expressed as

$$V_{\mathrm{D}}^{\mathrm{on}}(t) = 0; V_{\mathrm{ds}}^{\mathrm{on}}(t) = -L_{\mathrm{sum}}\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}. \quad (15)$$

According to (13)–(15), the exchange and oscillation voltage of the high-side and low-side devices can be defined as

$$\begin{cases} V_{\mathrm{D1}}^{\mathrm{on}}(\mathrm{tri}) = V_{\mathrm{D1}}^{\mathrm{on}}(\mathrm{osci}) = 0 \\ V_{\mathrm{ds1}}^{\mathrm{on}}(\mathrm{tri}) = 0; V_{\mathrm{ds1}}^{\mathrm{on}}(\mathrm{osci}) = -L_{\mathrm{sum}}\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases}. \quad (16)$$

Take (15) into (12), the voltage V_{AN} and V_{BN} can be obtained

$$\begin{cases} V_{\mathrm{AN}} = L_{s1}\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ V_{\mathrm{BN}} = (L_{12} + L_{s1})\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases}. \quad (17)$$

Take (17) into (10), the ECM noise voltage can be obtained

$$\begin{cases} V_{\mathrm{ECM}} = -k_{\mathrm{O_off}}L_{\mathrm{sum}}\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ k_{\mathrm{O_off}} = -\frac{L_{s1}C_3+L_1C_{13}-L_2C_2}{L_{\mathrm{sum}}C_{123}} \end{cases}. \quad (18)$$

2) Voltage Fall Stage (t_2–t_3): When the loop current i_{d} is equal to the load current I_{Lm}, the high-side device voltage V_{D} begins to rise and the low-side device voltage V_{ds} begins to fall. In addition, there is L_{sum} C_{D} oscillation circuit in the power circuit, as shown in Fig. 9(b). The voltage of the high-side and

low-side devices can be expressed as

$$\begin{cases} V_{\rm ds}^{\rm on}(t) = V_{\rm ds}(t_2) + \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \\ V_{\rm D}^{\rm on}(t) = -V_{\rm ds}(t_2) - \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t - L_{\rm sum}\frac{{\rm d}i_{\rm d}}{{\rm d}t} \end{cases}. \tag{19}$$

According to (13), (14), (19), the exchange and oscillation voltage of the high-side and low-side devices can be defined as

$$\begin{cases} V_{\rm ds2}^{\rm on}({\rm tri}) = V_{\rm ds}(t_2) + \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \\ V_{\rm D2}^{\rm on}({\rm tri}) = -V_{\rm ds}(t_2) - \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \end{cases} \tag{20}$$

$$\begin{cases} V_{\rm ds2}^{\rm on}({\rm osci}) = 0; \\ V_{\rm D2}^{\rm on}({\rm osci}) = -L_{\rm sum}\frac{{\rm d}i_{\rm d}}{{\rm d}t} \end{cases}. \tag{21}$$

Therefore, the circuit can be divided into two parts according to the superposition theorem, as shown in Fig. 9(b).

Voltage exchange part:

Take (20) into (12), the voltage $V_{\rm AN}$, $V_{\rm BN}$ can be obtained

$$V_{\rm AN} = V_{\rm BN} = -V_{\rm ds2}^{\rm on}({\rm tri}). \tag{22}$$

Take (22) into (10), the ECM noise voltage can be obtained

$$V_{\rm ECM}({\rm tri}) = -\frac{C_3}{C_{123}}V_{\rm ds2}^{\rm on}({\rm tri}). \tag{23}$$

Voltage oscillation part:

Similarly, by bringing (21) into (12), the voltage $V_{\rm AN}$ and $V_{\rm BN}$ can be obtained

$$\begin{cases} V_{\rm AN} = \frac{L_{12}+L_{\rm s2}}{L_{\rm sum}}V_{\rm D2}^{\rm on}({\rm osci}) \\ V_{\rm BN} = \frac{L_{\rm s2}}{L_{\rm sum}}V_{\rm D2}^{\rm on}({\rm osci}) \end{cases}. \tag{24}$$

Take (24) into (10), the ECM noise voltage can be obtained

$$\begin{cases} V_{\rm ECM}({\rm osci}) = k_{\rm O_on}V_{\rm D2}^{\rm on}({\rm osci}) \\ k_{\rm O_on} = \frac{L_{\rm s2}C_3+L_2C_{23}-L_1C_1}{L_{\rm sum}C_{123}} \end{cases}. \tag{25}$$

Therefore, the ECM noise voltage can be obtained by adding (23) and (25) during voltage fall stage

$$\begin{aligned} V_{\rm ECM} &= V_{\rm ECM}({\rm tri}) + V_{\rm ECM}({\rm osci}) \\ &= -\frac{C_3}{C_{123}}V_{\rm ds2}^{\rm on}({\rm tri}) + k_{\rm O_on}V_{\rm D2}^{\rm on}({\rm osci}). \end{aligned} \tag{26}$$

3) Oscillation Stage (t_3–t_4): The power loop enters the oscillation stage when the low-side device voltage equals 0. The ECM noise voltage is the same as in (25).

According to (18) and (25), the relationship between $k_{\rm O_on}$ and $k_{\rm O_off}$ can be established, which will be used to discuss the optimization constraints of the power module's parasitic parameters in Section IV

$$k_{\rm O_on} = k_{\rm O_off} + \frac{C_3}{C_{123}}. \tag{27}$$

C. CM Noise Voltage During Turn-OFF Process

The state equation is the same as the turn-ON process (13) during turn-OFF process. The high-side and low-side noise voltage can also be divided into two parts: voltage exchange $V_{\rm D}^{\rm off}({\rm tri})$, $V_{\rm ds}^{\rm off}({\rm tri})$, and voltage oscillation $V_{\rm D}^{\rm off}({\rm osci})$, $V_{\rm ds}^{\rm off}({\rm osci})$.

$$\begin{cases} V_{\rm D}^{\rm off}(t) = V_{\rm D}^{\rm off}({\rm tri}) + V_{\rm D}^{\rm off}({\rm osci}) \\ V_{\rm ds}^{\rm off}(t) = V_{\rm ds}^{\rm off}({\rm tri}) + V_{\rm ds}^{\rm off}({\rm osci}) \end{cases}. \tag{28}$$

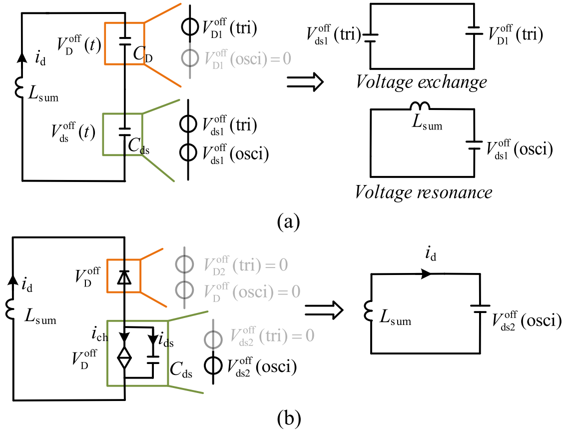

Fig. 11. Equivalent circuit diagram during turn-OFF process. (a) Voltage rise stage. (b). Current fall stage.

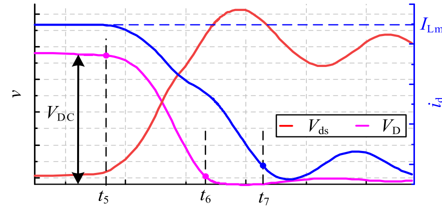

Fig. 12. Piecewise transition waveforms during turn-OFF process.

The superscript "off" of $V_{\rm D}$ and $V_{\rm ds}$ represents the turn-OFF process. Fig. 11 shows equivalent circuit diagram during turn-OFF process and Fig. 12 shows the noise voltage $V_{\rm D}$, $V_{\rm ds,}$ and current $i_{\rm d}$ waveforms. The power loop remains unchanged until the gate voltage drops to the Miller platform.

1) Voltage Fall Stage (t_5–t_6): When the gate voltage drops to the Miller platform, the low-side device voltage $V_{\rm ds}$ begins to rise and the high-side device voltage $V_{\rm D}$ begins to fall. The voltage of the high-side and low-side device can be expressed as (19)

$$\begin{cases} V_{\rm ds}^{\rm off}(t) = \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t - L_{\rm sum}\frac{{\rm d}i_{\rm d}}{{\rm d}t} \\ V_{\rm D}^{\rm off}(t) = -\frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \end{cases}. \tag{29}$$

According to (13), (28), and (29), the exchange and oscillation voltage of the high-side and low-side device can be defined as

$$\begin{cases} V_{\rm ds1}^{\rm off}({\rm tri}) = \frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \\ V_{\rm D1}^{\rm off}({\rm tri}) = -\frac{{\rm d}V_{\rm ds}}{{\rm d}t}t \end{cases} \tag{30}$$

$$\begin{cases} V_{\rm ds1}^{\rm off}({\rm osci}) = -L_{\rm sum}\frac{{\rm d}i_{\rm d}}{{\rm d}t} \\ V_{\rm D1}^{\rm off}({\rm osci}) = 0 \end{cases}. \tag{31}$$

Similar to the voltage fall stage during turn-ON process, the circuit can also be divided into two parts, as shown in Fig. 11(a).

Voltage exchange part:
Take (30) into (12), the voltage V_{AN} and V_{BN} can be obtained

$$V_{\mathrm{AN}} = V_{\mathrm{BN}} = -V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{tri}). \tag{32}$$

Take (31) into (10), the ECM noise voltage can be obtained

$$V_{\mathrm{ECM}}(\mathrm{tri}) = -\frac{C_3}{C_{123}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{tri}). \tag{33}$$

Voltage oscillation part:
Take (31) into (12), the voltage V_{AN} and V_{BN} can be obtained

$$\begin{cases} V_{\mathrm{AN}} = -\frac{L_{\mathrm{s1}}}{L_{\mathrm{sum}}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{osci}) \\ V_{\mathrm{BN}} = -\frac{L_{12}+L_{\mathrm{s1}}}{L_{\mathrm{sum}}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{osci}) \end{cases}. \tag{34}$$

Take (34) into (10), the ECM noise voltage can be obtained

$$V_{\mathrm{ECM}}(\mathrm{osci}) = k_{\mathrm{O_off}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{osci}). \tag{35}$$

Therefore, the ECM noise voltage can be obtained by adding (33) and (35) during voltage rise stage

$$\begin{aligned} V_{\mathrm{ECM}} &= V_{\mathrm{ECM}}(\mathrm{tri}) + V_{\mathrm{ECM}}(\mathrm{osci}) \\ &= -\frac{C_3}{C_{123}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{tri}) + k_{\mathrm{O_off}} V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{osci}). \end{aligned} \tag{36}$$

2) Current Fall Stage: (t_6–t_7): The circuit enters the current fall stage when the high-side device voltage drops to approximately 0. The voltage of the high-side and low-side devices can be expressed as

$$V_{\mathrm{D}}^{\mathrm{off}}(t) = 0; V_{\mathrm{ds}}^{\mathrm{off}}(t) = -L_{\mathrm{sum}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}. \tag{37}$$

According to (13), (28), and (37), the exchange and oscillation voltage of the high-side and low-side device can be defined as

$$\begin{cases} V_{\mathrm{D2}}^{\mathrm{off}}(\mathrm{tri}) = V_{\mathrm{D2}}^{\mathrm{off}}(\mathrm{osci}) = 0 \\ V_{\mathrm{ds2}}^{\mathrm{off}}(\mathrm{tri}) = 0; V_{\mathrm{ds2}}^{\mathrm{off}}(\mathrm{osci}) = -L_{\mathrm{sum}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases}. \tag{38}$$

The circuit can also be divided into two parts, as shown in Fig. 11(b). Take (38) and (12) into (10), the ECM noise voltage can be obtained

$$V_{\mathrm{ECM}} = k_{\mathrm{O_off}} V_{\mathrm{ds2}}^{\mathrm{off}}(\mathrm{osci}). \tag{39}$$

3) Oscillation Stage (t_7–t_8): When the channel current drops to 0, the circuit enters the oscillation stage. The ECM noise voltage is the same as (39).

D. Comparison of ECM Noise Source During Turn-ON Process and Turn-OFF Process

According to the analysis above, the voltage waveforms of high-side and low-side devices are divided into three parts: Part I, Part II, and Part III as shown in Fig. 13. Therefore, the proposed model is decomposed into a traditional model and two additional models, which have the following advantages.

1) In Part I, the propagation path is the same as the traditional model, as introduced in (1). The noise source $V_{\mathrm{ds}}(\mathrm{tri})$ is the CM noise source. Where symbol $V_{\mathrm{ds}}(\mathrm{tri})$ represents $V_{\mathrm{ds2}}^{\mathrm{on}}(\mathrm{tri})$ during the turn-ON process or $V_{\mathrm{ds1}}^{\mathrm{off}}(\mathrm{tri})$ during the turn-OFF process.

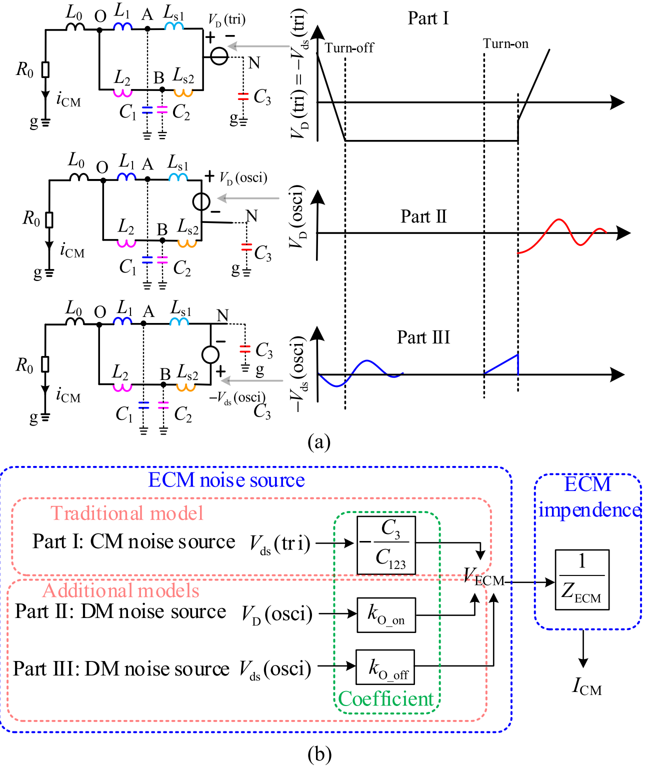

Fig. 13. Summary of CM current and noise sources. (a) Noise sources and CM circuit model. (b) Relationship between CM current and noise sources.

2) In Part II and Part III, the propagation paths are different from traditional model. The noise sources $V_{\mathrm{D}}(\mathrm{osci})$ and $V_{\mathrm{ds}}(\mathrm{osci})$ are called DM noise sources. They are related to each stage of the switching process and have a clear meaning.
3) The two DM noise sources are distinguished due to different propagation paths according to the turn-ON and turn-OFF. Therefore, the CM current generated by turn-ON and turn-OFF can be controlled separately.
4) All noise sources have the same ECM impedance. Therefore, the only difference in the effect of the noise sources on the CM current is the coefficients between the noise sources and the ECM noise sources. The coefficients are only related to the parasitic parameters of the power module.

Table II compares the ECM noise voltage during turn-ON and turn-OFF process. The ECM noise source consists of the noise source and the coefficient related to power module's parasitic parameters. Therefore, the effect of parasitic parameters on the ECM noise voltage can be divided into two parts. One is the effect on coefficient $k_{\mathrm{O_on}}$, $k_{\mathrm{O_off}}$, and the other is the effect on noise source (dynamic switching process). These two parts can be analyzed independently. The coefficients will be discussed in Section IV. The dynamic switching process is compared during turn-ON and turn-OFF in this section.

The voltage slew rate is divided into two stages due to parasitic inductance during turn-ON as shown in Fig. 10, current rise stage $\mathrm{d}v_{\mathrm{ds1}}^{\mathrm{on}}/\mathrm{d}t$ and voltage fall stage $\mathrm{d}v_{\mathrm{ds2}}^{\mathrm{on}}/\mathrm{d}t$. The first voltage slew

TABLE II
COMPARISON OF ECM NOISE VOLTAGE DURING TURN-ON AND TURN-OFF PROCESS

Stage	Turn-on	Stage	Turn-off
Current rise	$k_{\text{O_off}}V_{\text{ds1}}^{\text{on}}(\text{osci})$	Voltage rise	$k_{\text{O_off}}V_{\text{ds1}}^{\text{off}}(\text{osci})-\frac{C_3}{C_{123}}V_{\text{ds1}}^{\text{off}}(\text{tri})$
Voltage fall	$k_{\text{O_on}}V_{\text{D2}}^{\text{on}}(\text{osci})-\frac{C_3}{C_{123}}V_{\text{ds2}}^{\text{on}}(\text{tri}))$	Current fall	$k_{\text{O_off}}V_{\text{ds2}}^{\text{off}}(\text{osci})$
Oscillation	$k_{\text{O_on}}V_{\text{D2}}^{\text{on}}(\text{osci})$	Oscillation	$k_{\text{O_off}}V_{\text{ds2}}^{\text{off}}(\text{osci})$

rate of low-side devices is related to the current slew rate as expressed in (15), and the second voltage slew rate is related to the Miller platform voltage

$$\frac{\mathrm{d}V_{\text{ds2}}^{\text{on}}(\text{tri})}{\mathrm{d}t} = -\frac{V_{\text{GG}} - V_{\text{miller}}}{R_{\text{g}}C_{\text{gd}}} \tag{40}$$

where V_{GG} and R_{g} is the driving voltage and resistance. The V_{miller} is the Miller platform voltage. The C_{gd} is the Miller capacitor of the low-side device. Generally, the first voltage slew rate is relatively small, and the second voltage slew rate is relatively large during turn-ON process. In addition, the ECM noise source is also related to the high-side device voltage $V_{\text{D2}}^{\text{on}}(\text{osci})$ in the modified model. The voltage slew rate of the high-side device is very large compared with the low-side device, as shown in Fig. 10.

Different from the turn-ON, the voltage slew rate only occurs in the voltage rise stage during turn-OFF process, as shown in Fig. 12. Due to the charging of the parasitic capacitance of the low-side device and the discharging of the parasitic capacitance of the high-side device, so the low-side device voltage V_{ds} rise and the high-side device voltage V_{D} fall at the same time. Therefore, it has advantages in switching loss and low voltage slew rate during turn-OFF process.

IV. EFFECT AND OPTIMIZATION CONSTRAINTS OF PARASITIC PARAMETERS ON CM CURRENT

The CM current is equal to the ECM noise voltage divided by the ECM impedance.

Part I: The CM current generated by Part I can be obtained

$$I_{\text{CM1}} = \frac{C_3}{C_{123}}\frac{V_{\text{ds}}(\text{tri})}{Z_{\text{ECM}}} = \frac{C_3 V_{\text{ds}}(\text{tri})}{C_{123}\left(\frac{sL_1L_2}{L_{12}} + sL_0 + R_0 + \frac{1}{sC_{123}}\right)} \tag{41}$$

where symbol $V_{\text{ds}}(\text{tri})$ represents $V_{\text{ds2}}^{\text{on}}(\text{tri})$ during the turn-ON process or $V_{\text{ds1}}^{\text{off}}(\text{tri})$ during the turn-OFF process. The CM current generated by Part I is positively correlated with the parasitic capacitance C_3 and negatively correlated with C_{123}. Therefore, the parasitic capacitance C_3 is as small as possible and C_{123} is as large as possible in the power module design.

Part II & Part III: The ECM voltage and the voltage of high-side and low-side devices are linked by $k_{\text{O_on}}$, $k_{\text{O_off}}$ in Part II and Part III, as discussed in Section V-D.

The average CM current generated by Part II and Part III can be obtained

$$\frac{1}{I_{\text{CM2}}} = \frac{2Z_{\text{ECM}}}{|k_{\text{O_on}}||V_{\text{D}}^{\text{on}}(\text{osci})| + |k_{\text{O_off}}||V_{\text{ds}}^{\text{off}}(\text{osci})|}. \tag{42}$$

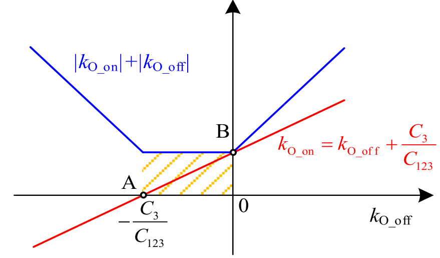

Fig. 14. $k_{\text{O_on}}$ and the sum of absolute values of $k_{\text{O_on}}$ and $k_{\text{O_off}}$ with $k_{\text{O_off}}$.

In general, the oscillation voltage of the high-side and low-side device voltage is not equal during the turn-ON and turn-OFF process. There are three cases

$$\begin{cases} V_{\text{D}}^{\text{on}}(\text{osci}) = kV_{\text{ds}}^{\text{off}}(\text{osci}) & V_{\text{D}}^{\text{on}}(\text{osci}) > V_{\text{ds}}^{\text{off}}(\text{osci}) \\ V_{\text{D}}^{\text{on}}(\text{osci}) = V_{\text{ds}}^{\text{off}}(\text{osci}) & \\ V_{\text{ds}}^{\text{off}}(\text{osci}) = kV_{\text{D}}^{\text{on}}(\text{osci}) & V_{\text{D}}^{\text{on}}(\text{osci}) < V_{\text{ds}}^{\text{off}}(\text{osci}) \end{cases}. \tag{43}$$

Take (43) into (42), the CM current, which is only related to the smaller noise voltage on the high and low sides, can be obtained

$$\begin{cases} \frac{1}{I_{\text{CM2}}} = \frac{2Z_{\text{ECM}}}{(|k_{\text{O_on}}|+|k_{\text{O_off}}|+(k-1)|k_{\text{O_on}}|)V_{\text{ds}}^{\text{off}}(\text{osci})} \\ \frac{1}{I_{\text{CM2}}} = \frac{2Z_{\text{ECM}}}{(|k_{\text{O_off}}|+|k_{\text{O_off}}|)V_{\text{D}}^{\text{on}}(\text{osci})} \\ \frac{1}{I_{\text{CM2}}} = \frac{2Z_{\text{ECM}}}{(|k_{\text{O_on}}|+|k_{\text{O_off}}|+(k-1)|k_{\text{O_off}}|)V_{\text{D}}^{\text{on}}(\text{osci})} \end{cases}. \tag{44}$$

The smaller the sum of the absolute values of $k_{\text{O_on}}$ and $k_{\text{O_off}}$, the smaller the ECM noise voltage is. Fig. 14 shows the curve of the coefficient $k_{\text{O_on}}$ and the sum of the absolute values of $k_{\text{O_on}}$ and $k_{\text{O_off}}$ with $k_{\text{O_off}}$. Therefore, the optimal area of the coefficient is the shaded area, as shown in Fig. 14.

The optimal area contains two pieces of information. One is that $k_{\text{O_on}}$ is a non-negative value and $k_{\text{O_off}}$ is a nonpositive value. The other is that the sum of the absolute values of $k_{\text{O_on}}$ and $k_{\text{O_off}}$ is equal to C_3/C_{123}. According to (18) and (25), the relationship between $k_{\text{O_on}}$ and $k_{\text{O_off}}$ can also be established, so the constraints of the optimal region can be obtained

$$k_{\text{O_on}} = k_{\text{O_off}} + \frac{C_3}{C_{123}}(k_{\text{O_on}} \geq 0\,\&\,k_{\text{O_off}} \leq 0). \tag{45}$$

When the turn-ON and turn-OFF oscillation noise sources are equal, the working points within the optimization area can be arbitrarily selected. The power module layout that satisfies the optimization area is referred to as layout B, characterized by $k_{\text{O_on}}$ being greater than 0 and $k_{\text{O_off}}$ being less than 0. When the

TABLE III
COMPARISON OF ECM NOISE VOLTAGE BETWEEN LAYOUT A AND LAYOUT C OF POWER MODULE DURING TURN-ON PROCESS

Stage	Layout A	Layout C
Current rise	$-\frac{C_3}{C_{123}}V_{\text{ds}}^{\text{on}}(t)$	0
Voltage fall	$-\frac{C_3}{C_{123}}V_{\text{ds}}^{\text{on}}(t)$	$\frac{C_3}{C_{123}}V_{\text{D}}^{\text{on}}(t)$
Oscillation	0	$\frac{C_3}{C_{123}}V_{\text{D}}^{\text{on}}(t)$

TABLE IV
COMPARISON OF ECM NOISE VOLTAGE BETWEEN LAYOUT A AND LAYOUT C OF POWER MODULE DURING TURN-OFF PROCESS

Stage	Layout A	Layout C
Voltage rise	$-\frac{C_3}{C_{123}}V_{\text{ds}}^{\text{off}}(t)$	$-\frac{C_3}{C_{123}}V_{\text{D}}^{\text{off}}(t)$
Current fall	$-\frac{C_3}{C_{123}}V_{\text{ds}}^{\text{off}}(t)$	0
Oscillation	$-\frac{C_3}{C_{123}}V_{\text{ds}}^{\text{off}}(t)$	0

oscillation noise sources of turn-ON are greater than turn-OFF, the minimum CM current can be obtained at point A in Fig. 14. The power module layout that satisfies point A is referred to as layout A, characterized by $k_{\text{O_on}}$ equaling 0. When the oscillation noise source of turn-ON is smaller than turn-OFF, the minimum CM current can be obtained at point B in Fig. 14. The power module layout that satisfies point B is referred to as layout A, characterized by $k_{\text{O_off}}$ equaling 0. Therefore, Layout A and C are the two boundaries of the optimization area for Layout B, respectively.

The ECM noise source of Layout B has been listed in Table II. Tables III and IV compare the ECM noise source of Layout A and Layout C during turn-ON and turn-OFF process. The ECM noise source based on Layout A is only related to the low-side device voltage. The ECM noise source based on Layout B is related to both the high-side and low-side device voltages. The ECM noise source based on Layout C is only related to the high-side device voltage. Due to the different noise voltages of the high-side and the low-side during switching process, the impact of power module with different layouts on the ECM noise source also varies. Therefore, the parasitic inductance of the power module plays an important role in the high-frequency range.

The CM capacitance C_3 and parasitic inductance L_{s1} are selected as reference values. The coefficient $k_{\text{O_on}}$, $k_{\text{O_off}}$ of ECM noise voltage can be obtained according to (18) and (25)

$$\begin{cases} k_{\text{O_on}} = \frac{p_3+p_2+np_2-qp_1}{(1+n+q)(1+p_1+p_2+p_3)} \\ k_{\text{O_off}} = -\frac{1+p_1(1+q)-p_2 n}{(1+n+q)(1+p_1+p_2+p_3)} \end{cases} \quad (46)$$

where the p_1 is L_1 divided by L_{s1}, the p_2 is L_2 divided by L_{s1}, the p_3 is L_{s2} divided by L_{s1}, the n is C_2 divided by C_3, and the q is C_1 divided by C_3.

There are many aspects to be considered in power module design, and it is impossible to fully meet the expected parasitic

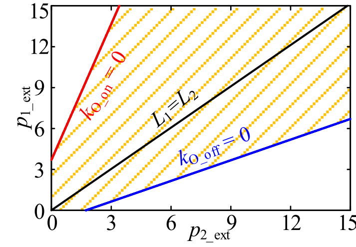

Fig. 15. Constraints for optimal region of parasitic inductance L_1, L_2.of power module BSM120D12P2C005.

TABLE V
PARASITIC PARAMETERS OF POWER MODULE CAS300M12BM2

L_{1_in}	L_{2_in}	L_{s1}	L_{s2}	C_1	C_2	C_3
6nH	6nH	2.7nH	0.5nH	154pF	36pF	183pF

parameters. However, there are many combinations. Taking power module BSM120D12P2C005 as an example, the parasitic parameters are known. So the parasitic inductance L_1 and L_2 are the only two free variables by Busbar design. The L_1 and L_2 include the parasitic inductance of the power module itself L_{1_in}, L_{2_in}, and the Busbar L_{1_ext}, L_{2_ext} as expressed in (47) by taking L_{s1} as the per unit

$$\begin{cases} p_1 = p_{1_\text{ext}} + p_{1_\text{in}} \\ p_2 = p_{2_\text{ext}} + p_{2_\text{in}} \end{cases} . \quad (47)$$

According to (45), the optimal constraints (48) can be obtained by bringing (47) and parameters from Table I into (46). Fig. 15 shows the constraints for the optimal region of parasitic inductances L_{1_ext} and L_{2_ext}

$$\begin{cases} p_{1_\text{ext}} \leq 3.32p_{2_\text{ext}} + 3.7 \\ p_{1_\text{ext}} \geq 0.505p_{2_\text{ext}} - 0.869 \end{cases} . \quad (48)$$

V. EXPERIMENTAL VERIFICATION AND COMPARISON OF CM CURRENT WITH DIFFERENT POWER MODULE LAYOUTS

A. Experimental Setup

The DPT circuit and conducted CM EMI test platform are established as shown in Fig. 16. The L_m is an air inductance of 300 uH. The parasitic parameters of power modules BSM120D12P2C005 and CAS300M12BM2 have been extracted by Q3D as listed in Table I and Table V. The driver chip UCC5390SC, from TI, is selected, which has split output during switching process. Therefore, the driving resistance R_g can be divided into turn-ON driving resistance $R_{\text{g_on}}$ and turn-OFF driving resistance $R_{\text{g_off}}$. The capacitors of the snubber circuit are composed of three 22 nF multilayer ceramic chip capacitors in parallel. The diode C4D20120A of the snubber circuit, from ROHM, is selected.

The positions of the four test waveforms are marked in the schematic diagram. Due to the parasitic inductance of the power module itself, the test voltage is different from the actual voltage.

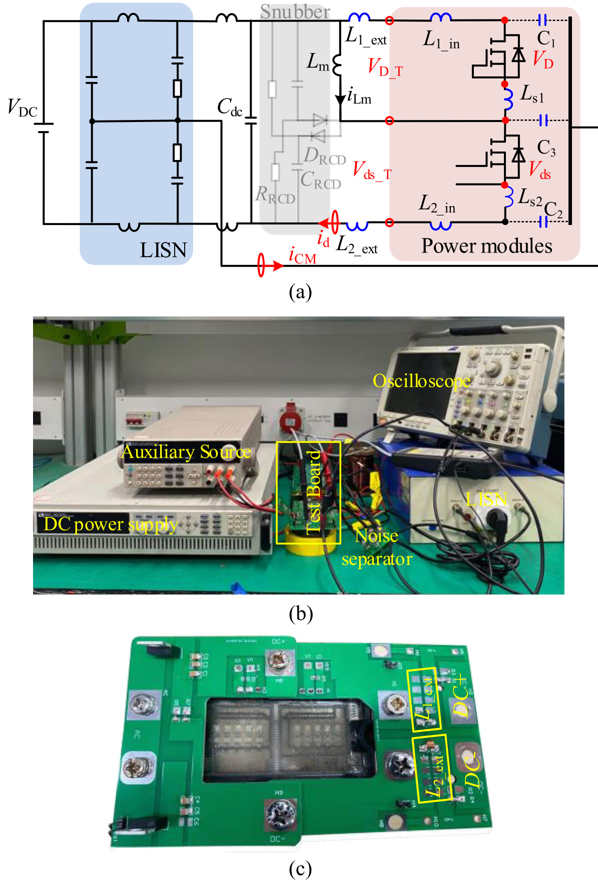

Fig. 16. Experimental test. (a) Schematic diagram of DPT circuit. (b) Test platform. (c) Testing circuit board.

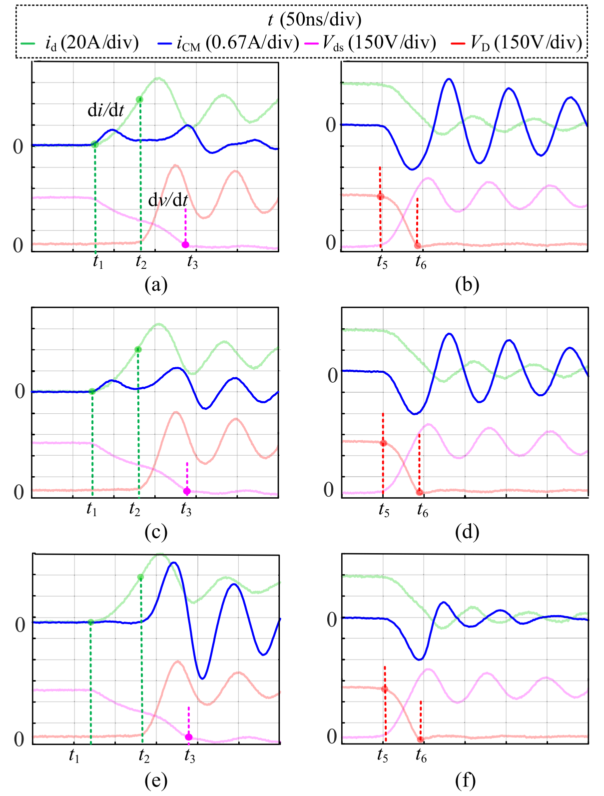

Fig. 17. Current i_d, i_{CM} and voltage V_{ds}, V_D waveforms of power module BSM120D12P2C005 with driving resistance $R_{g_on} = 3.3\ \Omega$, $R_{g_off} = 1.3\ \Omega$. (a) and (b) Layout A, $k_{on} = 0$: Turn-ON and Turn-OFF. (c) and (d) Layout B, $k_{on} \neq 0$ and $k_{off} \neq 0$: Turn-ON and Turn-OFF. (e) and (f) Layout C, $k_{off} = 0$. Turn-ON and Turn-OFF.

The relationship between them can be expressed approximately

$$\begin{cases} V_D = V_{D_T} - (L_{1_in} + L_{s1})\mathrm{d}i_d/\mathrm{d}t \\ V_{ds} = V_{ds_T} - (L_{2_in} + L_{s2})\mathrm{d}i_d/\mathrm{d}t \end{cases}. \quad (49)$$

The test voltage will be processed to get the actual voltage by MATLAB. So the voltage waveforms are the actual voltage waveforms in the following.

B. Model Validation With Different Power Modules

The CM current is related to ECM impedance and ECM noise source. The ECM impedance of the traditional and proposed model is the same. However, the proposed ECM noise source related to the parasitic parameters of the power module is different from the traditional model. Therefore, the influence of the parasitic parameters of the power module on the ECM noise source is verified in this section. The ECM noise includes noise sources and coefficients. The noise sources are a dynamic switching process, which can be measured by oscilloscope. So the ECM noise source coefficients can be verified by comparing the noise sources and CM current.

To validate the model, two constraints need to be verified: $k_{O_on} = 0$ and $k_{O_off} = 0$. Figs. 17 and 18 show the waveforms of the turn-ON and turn-OFF processes of the power modules BSM120D12P2C005 and CAS300M12BM2, respectively. By comparing the noise sources and CM current at each stage of the switching process, the models in Tables II, III, and IV can be validated.

In Fig. 17, the total parasitic inductances of the busbar for power module BSM120D12P2C005 are the same. Consequently, the noise sources during the switching process are the same for two different constraints. However, the CM current is different due to different power module layouts. For example, compared to Fig. 17(c), (e), the CM current in Fig. 17(a) is smaller during turn-ON oscillation when $k_{O_on} = 0$, which validates the models in Table II and III. Similarly, compared to Fig. 17(b), (f), the CM current in Fig. 17(d) is smaller during turn-OFF oscillation when $k_{O_off} = 0$, thus validating the model in Table II and IV.

In addition, the model is also validated for the other power module CAS300M12BM2, as shown in Fig. 18. To ensure the same noise sources during switching process for two different constraints, the sum of the parasitic inductances for power module busbar is also the same. By comparing the CM currents at each stage in Fig. 18(a), (c), (e), the models in Table II and III can also be validated. Furthermore, by comparing the CM currents in Fig. 18(d), (d), (f), the models in Table II and IV can likewise be validated.

Consequently, the models are applicable to all power modules as long as the equivalent circuit of the power module can be

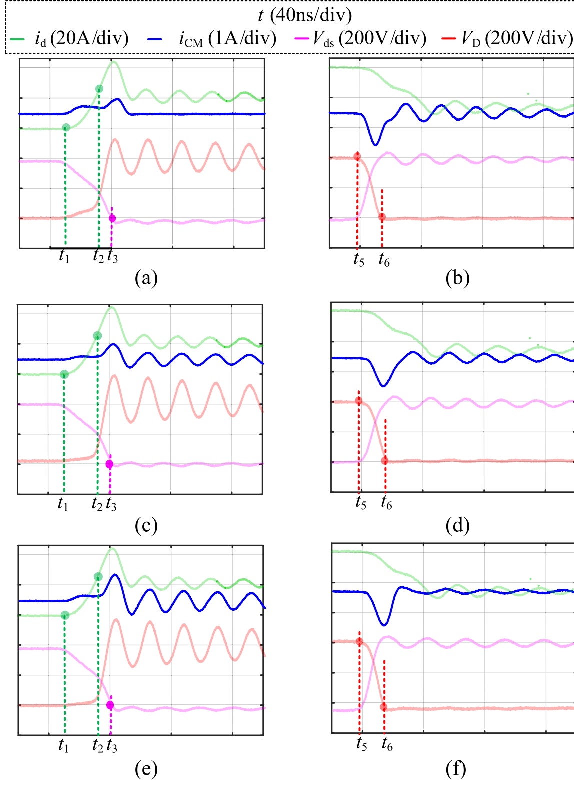

Fig. 18. CM current i_d, i_{CM} and voltage V_{ds}, V_D waveforms of power module CAS300M12BM2 with driving resistance $R_{g_on} = 9.1\ \Omega$, $R_{g_off} = 9.1\ \Omega$. (a) and (b) Layout A, $k_{on} = 0$: Turn-ON and Turn-OFF. (c) and (d) Layout B, $k_{on} \neq 0$ and $k_{off} \neq 0$: Turn-ON and Turn-OFF. (e) and (f) Layout C, $k_{off} = 0$. Turn-ON and Turn-OFF.

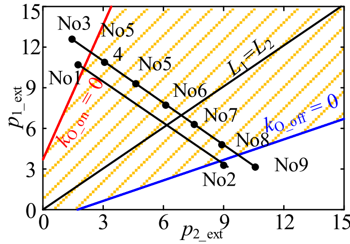

Fig. 19. Experimental conditions and numbers of power module BSM120D12P2C005.

simplified to that shown in Fig. 3(b). The next step is to further validate the impact of different layouts on the CM current and to examine various application cases, utilizing power module BSM120D12P2C005.

C. Comparison of CM Currents With Different Power Module Layouts

Fig. 19 shows the experimental numbers with different combinations of Busbar parasitic inductors L_{1_ext}, L_{2_ext} that can verify the influence of parasitic inductors at different positions on CM current.

In order to decouple noise sources V_{ds} and V_D between t_2 and t_3, the voltage V_{ds} can be reduced to almost zero by reducing the turn-ON drive resistance as shown in Fig. 20. There is no CM current between t_2 and t_3 for layout A. However, there is a large CM current between t_2 and t_3 for layout C. Therefore, the CM model in Tables III–IV can be fully verified in Fig. 20.

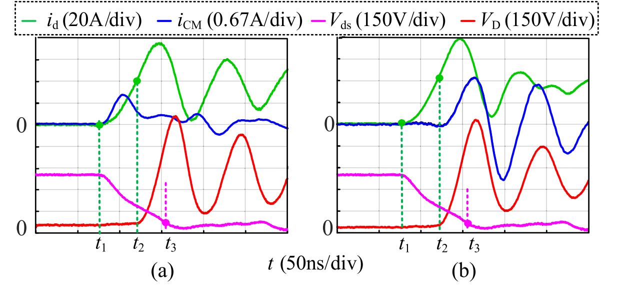

Fig. 20. Current i_d, i_{CM} and voltage V_{ds}, V_D waveform with driving resistance $R_{g_on} = R_{g_off} = 1.3\ \Omega$ at No1 and No3 during turn-ON. (a) No1 (Layout A). (b) No2 (Layout C).

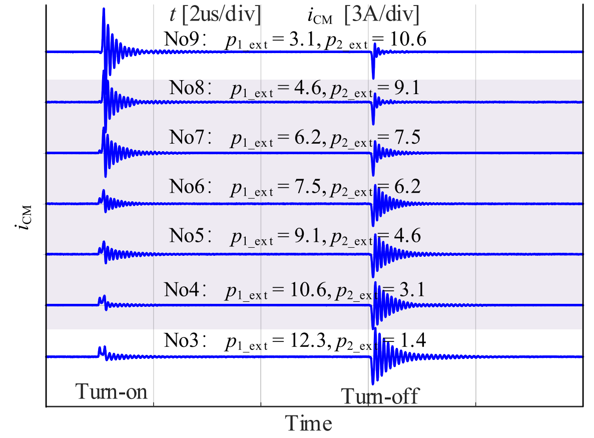

Fig. 21. CM current comparison with different combinations of Busbar parasitic inductance L_{1_ext}, L_{2_ext} from No3 to No9.

The constraint of the optimal region is verified by scanning different combinations of Busbar parasitic inductance L_{1_ext}, L_{2_ext} from No3 to No9 as shown in Fig. 21. The CM current increases during turn-ON and decreases during turn-OFF from No4 to No9. However, the CM current increases during turn-ON and almost unchanged or increases slightly during turn-OFF from No8 to No9. The CM current is almost unchanged or increases slightly during turn-ON and increases during turn-OFF from No4 to No3. Therefore, the combinations of Busbar parasitic inductance L_{1_ext}, L_{2_ext} from No4 to No8 are optimal, which is consistent with Fig. 19.

D. Case Application

The noise source includes the slew rate and oscillation of the noise source during the switching process according to the proposed model. According to the switching characteristics, the converters based on half-bridge structure mainly include SN-HF and HN-HF. The CRM of Buck or Boost converters is typical SN-HF. The CCM of Buck or Boost converters is typical HN-HF.

Case for SN-HF: For SN-HF, the current rising stage does not exist during turn-ON, so the switching loss and oscillation can

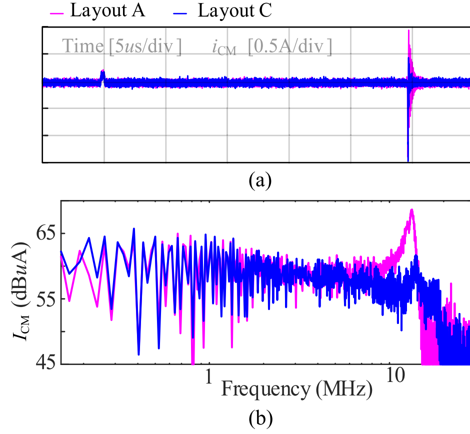

Fig. 22. CM current comparison of layout A and layout C for SN-HF. (a) Time domain CM current. (b) Frequency domain CM current.

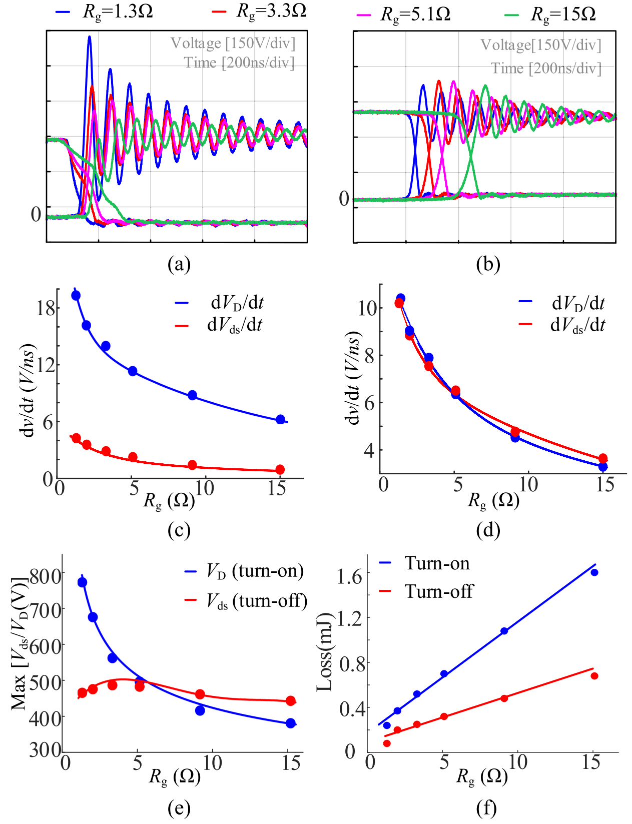

Fig. 23. Comparison of switching loss and noise source with driving resistance during turn-ON and turn-OFF. (a) Time domain voltage waveform during turn-ON. (b) Time domain voltage waveform during turn-OFF. (c) Voltage slew rate during turn-ON. (d) Voltage slew rate during turn-OFF. (e) Peak voltage (noise source of oscillating). (d) Switching loss.

be ignored. The voltage slew rate can be reduced by increasing the turn-ON driving resistance. Compared with the turn-ON, the influence of noise source on CM current is greater during turn-OFF. Layout C is more suitable for SN-HF compared with layout A according to Table III and IV.

Fig. 22 compares the CM current of layout A and layout C based on SN-HF. Layout C has a smaller CM current in time domain and frequency domain than layout A.

Case for HN-HF without oscillations: For HN-HF, the current rise stage and voltage fall stage are separated during turn-ON, which leads to greater switching loss. However, the current rise stage and voltage fall stage coincide during turn-OFF, which can achieve lower loss. The switching losses can be reduced by smaller driving resistors, but the noise sources, including voltage slew rate and oscillation are increased. Fig. 23 compares switching losses and noise sources with different driving resistances during turn-ON and turn-OFF.

The voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ is much greater than $\mathrm{d}V_\mathrm{ds}/\mathrm{d}t$ during turn-ON, as shown in Fig. 23(c). But the voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ is almost the same as that of $\mathrm{d}V_\mathrm{ds}/\mathrm{d}t$ during turn-OFF, as shown in Fig. 23(d). So the ECM noise source is more sensitive to power module layout during turn-ON. According to Tables IV and V, layout A is only related to voltage slew rate $\mathrm{d}V_\mathrm{ds}/\mathrm{d}t$, and layout C is only related to voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ during turn-ON. If the voltage slew rate $\mathrm{d}V_\mathrm{ds}/\mathrm{d}t$ of layout A is equal to the voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ of layout C, the driving resistance of layout A is much smaller than that of layout C. So layout A is more suitable for reducing switching loss and EMI caused by voltage slew rate.

The nondischarge RCD snubber circuit can suppress switching oscillation without affecting the voltage slew rate [39]. Fig. 24 shows time domain switching waveforms and CM current spectrum of layout A and layout C. The CM current spectrum of the two layouts is almost the same below 3 MHz. However, the layout A has a smaller CM current spectrum than layout C above 3 MHz.

Case for HN-HF with oscillations: The overvoltage V_D decreases gradually during turn-ON and the overvoltage V_ds first increases and then decreases during turn-OFF with the increase of driving resistance, as shown in Fig. 23(e). When the overvoltage V_ds is greater than V_D, layout C is more appropriate to reduce CM current caused by the overvoltage V_ds. However, a large turn-ON driving resistance is required, which will cause a larger turn-ON loss, such as 15 Ω in Fig. 23(e). The slope of the turn-ON loss increasing with the driving resistance is larger than the turn-OFF loss. So the lower overvoltage V_ds can also be achieved by increasing the turn-OFF driving resistance, which may not increase the overall loss.

Further, we take the noise source as the design goal and the switching loss as the evaluation standard to illustrate that layout A is more suitable for HN-HF with oscillation than layout C.

1) The voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ during turn-OFF is larger than the voltage slew rate $\mathrm{d}V_\mathrm{ds}/\mathrm{d}t$ during turn-ON, so the voltage slew rate $\mathrm{d}V_\mathrm{D}/\mathrm{d}t$ is the first factor to limit the turn-OFF driving resistance for layout A.
2) The oscillation of voltage V_ds is the second factor to limit the turn-ON driving resistance for layout A. The oscillation of voltage V_D does not affect the CM current during turn-ON for layout A.

Therefore, the turn-ON driving resistance does not need to compromise between EMI and turn-ON loss for layout A. Although the turn-OFF driving resistance needs to make a compromise between turn-OFF loss and EMI, the slope of switching

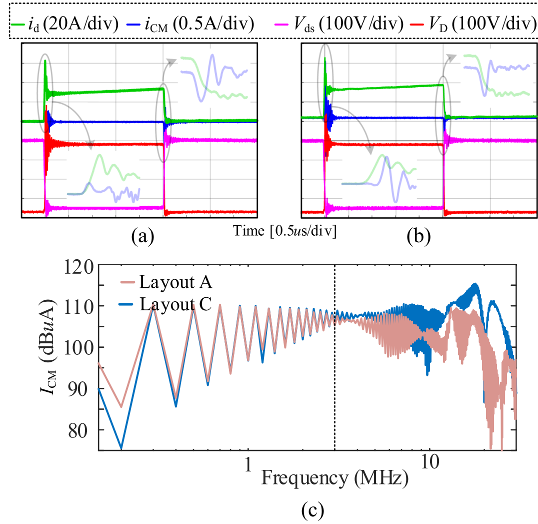

Fig. 24. CM current comparison of layout A and layout C for HN-HF with RCD snubber circuit. (a) Time domain switching waveform of layout A. (b) Time domain switching waveform of layout C. (c) Comparison of CM current spectrum of layout A and layout C.

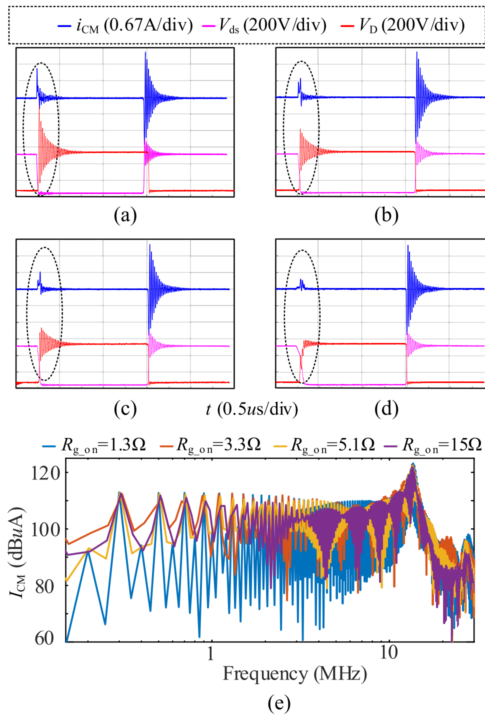

Fig. 25. CM current comparison with different turn-ON driving resistors of layout A for HN-HF. (a) $R_{g_on} = 1.3\ \Omega$. (b) $R_{g_on} = 3.3\ \Omega$. (c) $R_{g_on} = 5.1\ \Omega$. (d) $R_{g_on} = 15\ \Omega$. (e) Comparison of CM current spectrum with different turn-ON driving resistors.

loss increasing with the turn-OFF driving resistance is relatively small.

Fig. 25 compares the CM current with different turn-ON drive resistors of layout A. Although the noise sources increase with the decrease of the turn-ON driving resistors, the CM current spectrum is almost unchanged. Therefore, the CM current is almost independent of the turn-ON driving resistors for layout A.

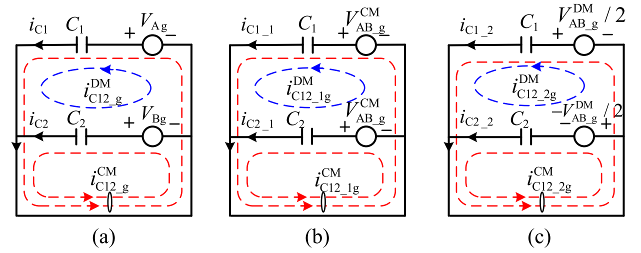

Fig. 26. CM and DM coupling principle due to impedance asymmetry. (a) Sum of CM and DM noise excitation. (b) CM noise excitation. (c) DM noise excitation.

VI. Conclusion

This article establishes a conducted CM model based on DPT circuit considering parasitic parameters of power module and Busbar. The transient CM current during switching process can be obtained.

Based on the model, the switching waveforms are divided into one CM noise source and two DM noise sources. The CM current generated by the CM noise source is the same as the traditional model, mainly affecting the mid-frequency spectrum. The propagation paths exhibit weak dependency on the parasitic inductances of the power module in comparison to the parasitic capacitances. However, the two DM noise sources have different CM circuit model, mainly affecting high-frequency spectrum. Their propagation paths are related to both the parasitic inductances and capacitances of the power module. The influence of parasitic parameters at different positions of power modules on CM current is analyzed. According to the coefficients between two DM noise sources and ECM noise sources, three different power module layouts are defined.

For SN-HF, layout C is more suitable than layout A. If the power module meets layout C, the CM current can be significantly reduced during turn-OFF. For HN-HF, layout A is more suitable than layout C. If the power module meets layout A, the turn-ON driving resistance does not need to compromise between EMI and turn-ON loss. So the model can guide the selection and redesign of power module layout and driver to reduce CM current and switching losses according to switching characteristics.

Appendix

A. Relationship Between the CM Current of Parasitic Capacitances and CM Noise Voltage and DM Noise Voltage

In Fig. 5(a), the parasitic inductances and capacitances are in parallel, so their current is only related to the voltage at point A. To obtain the CM current of parasitic capacitances, Fig. 5(a) can be simplified as Fig. 26(a) when ignoring parasitic inductance and LISN.

According to the definitions of CM and DM noise voltage, the noise source can be expressed as

$$\begin{cases} V_{Ag} = V_{AB_g}^{CM} + V_{AB_g}^{DM}/2 \\ V_{Bg} = V_{AB_g}^{CM} - V_{AB_g}^{DM}/2 \end{cases} . \tag{50}$$

Therefore, Fig. 26(a) can be decomposed into Fig. 26(b) and (c) according to the superposition theorem. Similarly, according to the formula (3), the parasitic capacitance currents can be represented by CM current and DM current

$$\begin{cases} i_{\rm C1} = i_{\rm C12_g}^{\rm CM}/2 + i_{\rm C12_g}^{\rm DM} \\ i_{\rm C2} = i_{\rm C12_g}^{\rm CM}/2 - i_{\rm C12_g}^{\rm DM} \end{cases} . \tag{51}$$

In Fig. 26(b), the CM current and DM current generated by the CM noise voltage can be obtained. Due to the asymmetry of the circuit impedance, the CM noise voltage also produces a DM current

$$\begin{cases} i_{\rm C12_1g}^{\rm CM} = i_{\rm C1_1} + i_{\rm C2_1} = \frac{V_{\rm AB_g}^{\rm CM}}{Z_{C_1}} + \frac{V_{\rm AB_g}^{\rm CM}}{Z_{C_2}} = \frac{Z_{C_1}+Z_{C_2}}{Z_{C_1}Z_{C_2}} V_{\rm AB_g}^{\rm CM} \\ i_{\rm C12_1g}^{\rm DM} = \frac{i_{\rm C1_1}-i_{\rm C2_1}}{2} = \frac{V_{\rm CM}}{2Z_{C_1}} - \frac{V_{\rm CM}}{2Z_{C_2}} = \frac{Z_{C_2}-Z_{C_1}}{2Z_{C_1}Z_{C_2}} V_{\rm AB_g}^{\rm CM} \end{cases} . \tag{52}$$

Similarly, in Fig. 26(c), the CM current and DM current generated by the DM noise voltage can be obtained. The DM noise voltage also produces a CM current due to the asymmetry of the circuit impedance

$$\begin{cases} i_{\rm C12_2g}^{\rm CM} = i_{\rm C1_2} + i_{\rm C2_2} = \frac{V_{\rm AB_g}^{\rm DM}}{2Z_{C_1}} - \frac{V_{\rm AB_g}^{\rm DM}}{2Z_{C_2}} = \frac{Z_{C_2}-Z_{C_1}}{2Z_{C_1}Z_{C_2}} V_{\rm AB_g}^{\rm DM} \\ i_{\rm C12_2g}^{\rm DM} = \frac{i_{\rm C1_2}-i_{\rm C2_2}}{2} = \frac{V_{\rm AB_g}^{\rm DM}}{4Z_{C_1}} + \frac{V_{\rm AB_g}^{\rm DM}}{4Z_{C_2}} = \frac{Z_{C_1}+Z_{C_2}}{4Z_{C_1}Z_{C_2}} V_{\rm AB_g}^{\rm DM} \end{cases} . \tag{53}$$

According to formulas (52) and (53), the sum of parasitic capacitances CM currents generated by CM noise voltage and DM noise voltage can be obtained

$$\begin{aligned} i_{\rm C12_g}^{\rm CM} &= i_{\rm C12_1g}^{\rm CM} + i_{\rm C12_2g}^{\rm CM} \\ &= \frac{Z_{\rm C_1}+Z_{\rm C_2}}{Z_{\rm C_1}Z_{\rm C_2}} V_{\rm AB_g}^{\rm CM} + \frac{Z_{\rm C_2}-Z_{\rm C_1}}{Z_{\rm C_1}Z_{\rm C_2}} \frac{V_{\rm AB_g}^{\rm DM}}{2}. \end{aligned} \tag{54}$$

B. Discussion on Model Error Due to Decoupling Capacitance

The error of the proposed model without considering the parasitic inductance of the decoupling capacitance is discussed in this section. The influence of asymmetric parasitic parameters on CM current has been analyzed in [40]. However, this analysis process is different due to different objectives.

The new equivalent circuit considering the parasitic inductance of the decoupling capacitance from Fig. 5(a) can be obtained, as shown in Fig. 27(a).

The difference and average of the impedances of parasitic inductors L_1, L_2 are defined [40]

$$\begin{cases} Z_{\rm s} = (Z_{L_1} + Z_{L_2})/2 \\ \Delta Z_{\rm s} = (Z_{L_1} - Z_{L_2})/2 \end{cases} . \tag{55}$$

The CM voltage resulting from the asymmetry of parasitic capacitances in the power module is not affected by the parasitic inductance of the decoupling capacitance, as expressed in (6). The new impedance and CM voltage, caused by the asymmetry of the parasitic inductance in the power module, is expressed in (56), shown at the top of the next page, and (57), shown at the top of the next page, Fig. 27(a) can be simplified to Fig. 27(b) by using (56) and Fig. 27(b) can be simplified to Fig. 27(c) by using (8). The ECM noise source (58), shown at the top of the next page, can be obtained according to Fig. 27(c), (d). The relationship between voltages $V_{\rm AN}$, $V_{\rm BN}$, and $V_{\rm D}$, $V_{\rm ds}$ can be obtained as expressed in (59).

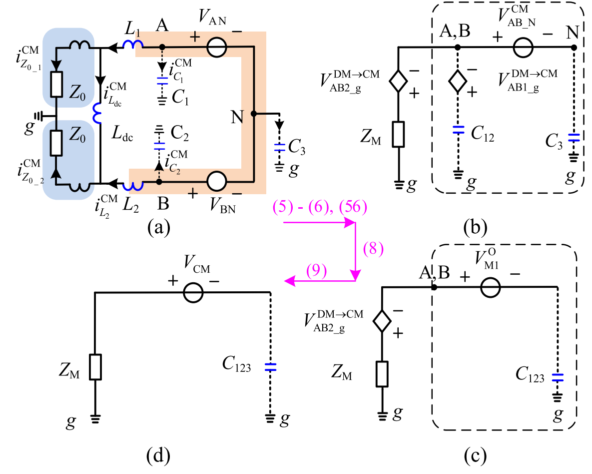

Fig. 27. New conducted CM equivalent modeling considering the parasitic inductances of power module and decoupling capacitances at same time.

$$\begin{cases} V_{\rm AN} = \frac{L_{12}+L_{s2}+L_{\rm dc}}{L_{\rm sum}+L_{\rm dc}}(V_{\rm D} + V_{\rm ds}) - V_{\rm ds} \\ V_{\rm BN} = \frac{L_{s2}}{L_{\rm sum}+L_{\rm dc}}(V_{\rm D} + V_{\rm ds}) - V_{\rm ds} \end{cases} . \tag{59}$$

The new coefficients $k_{\rm O_on}$ and $k_{\rm O_off}$ can be obtained by bringing (59) into (58) when the voltages $V_{\rm ds}$ and $V_{\rm D}$ equal to 0, respectively. The parasitic inductance of the decoupling capacitance is equally distributed to the parasitic inductors L_1 and L_2 as

$$\begin{cases} k_{\rm O_on} = \frac{L_{s2}C_3+(L_2+0.5L_{\rm dc})C_{23}-(L_1+0.5L_{\rm dc})C_1}{C_{123}(L_{\rm sum}+L_{\rm dc})} \\ k_{\rm O_off} = -\frac{L_{s1}C_3+(L_1+0.5L_{\rm dc})C_{13}-(L_2+0.5L_{\rm dc})C_2}{C_{123}(L_{\rm sum}+L_{\rm dc})} \\ k_{\rm O_on} = k_{\rm O_off} + \frac{C_3}{C_{123}} \end{cases} . \tag{60}$$

Although the constraints considering the parasitic inductance of the decoupling capacitance are changed, the ECM noise source of layout A and layout C remains unchanged according to Table III and IV.

C. High-Frequency Models of the LISN and the Measuring Equipment or Terminal

Fig. 28 shows the simplified schematic of the LISN and the measurement equipment, which can be referenced from various EMC standards, such as MIL-STD-461[2]. The LISN is inserted between the power source and EUT and provides an interface to the measurement equipment or terminal. The measurement device or terminal can provide a stable 50 Ω impedance over a certain frequency range according to different EMC standards.

The LISN consists of the inductances, capacitances, and resistances. The inductances present a high impedance at the test frequency range, preventing noise from the power supply to the EUT and vice versa. The capacitors provide a low impedance

$$V_{\mathrm{AB_g}}^{\mathrm{CM}} = \left(\frac{Z_s^2 - \Delta Z_s^2}{Z_{\mathrm{dc}} + 2Z_{\mathrm{s}} + \frac{Z_{\mathrm{dc}} Z_{\mathrm{s}}}{Z_0}} + \frac{Z_s^2 - \Delta Z_s^2}{2Z_0 + 2Z_{\mathrm{s}} + \frac{4Z_0 Z_{\mathrm{s}}}{Z_{\mathrm{dc}}}} + \frac{\Delta Z_{\mathrm{s}}}{\frac{2}{Z_0} + \frac{2}{Z_{\mathrm{s}}} + \frac{4}{Z_{\mathrm{dc}}}} + \frac{Z_0}{2} \right) i_{\mathrm{L12_g}}^{\mathrm{CM}} + \left(\frac{\Delta Z_{\mathrm{s}}}{Z_{\mathrm{dc}} + 2Z_{\mathrm{s}} + \frac{R_{\mathrm{dc}} Z_{\mathrm{s}}}{Z_0}} + \frac{\Delta Z_{\mathrm{s}}}{2Z_0 + 2Z_{\mathrm{s}} + \frac{4Z_0 Z_{\mathrm{s}}}{Z_{\mathrm{dc}}}} \right) V_{\mathrm{DM}} = Z_{\mathrm{M}} i_{Z_{\mathrm{M_g}}}^{\mathrm{CM}} + V_{\mathrm{AB2_g}}^{\mathrm{DM}\to\mathrm{CM}} \quad (56)$$

$$V_{\mathrm{AB2_g}}^{\mathrm{DM}\to\mathrm{CM}} \approx \frac{\Delta Z_{\mathrm{s}}}{Z_{\mathrm{dc}} + 2Z_{\mathrm{s}}} V_{\mathrm{DM}} = \frac{L_1 - L_2}{L_{\mathrm{dc}} + L_1 + L_2} \frac{V_{\mathrm{DM}}}{2} \quad (Z_0 >> Z_{\mathrm{s}} \& Z_0 >> Z_{\mathrm{dc}}) \quad (57)$$

$$V_{\mathrm{CM}} = \frac{L_2 C_2 + L_2 C_3 - L_1 C_1 + 0.5 L_{\mathrm{dc}}(C_{23} - C_1)}{(L_{12} + L_{\mathrm{dc}}) C_{123}} V_{\mathrm{AN}} + \frac{L_1 C_{12} - L_2 C_3 + 0.5 L_{\mathrm{dc}}(C_{12} - C_3)}{(L_{12} + L_{\mathrm{dc}}) C_{123}} V_{\mathrm{BN}} \quad (58)$$

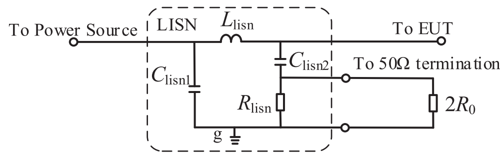

Fig. 28. Simplified schematic diagram of the LISN and the terminal.

path at the test frequency range, allowing noise from the EUT to be conducted to the measurement equipment. The resistors provide a standard impedance to ensure consistent and repeatable test conditions.

The performance of the LISN is also related to the parasitic parameters of the components. However, EMC testing standards stipulate that the LISN must not resonate within the conducted EMI testing frequency range. This means that the resonant frequency resulting from the parasitic parameters inside the LISN should be significantly higher than the conducted EMI testing frequencies. Consequently, the impact of these parasitic parameters can be considered negligible.

Therefore, at the test frequency range, the inductors of the LISN can be considered as open circuit, and the capacitors of the LISN can be considered as short circuit. Meanwhile, the resistances of the LISN are significantly greater than the terminal resistance. So the parallel resistance of the LISN and terminal can be simplified to a 50 Ω resistor.

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