Multi Module Parallel MHz Power Amplifier with Hybrid Structure and Optimized Control Strategy

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***Abstract*—Megahertz power amplifiers typically modulate power by paralleled-architectures and outphasing methods. However, when power drops in a large ratio, the effective admittances of modules are always not within the high-efficiency range. This article optimizes four-paralleled-module system through two operation modes: four modules turn-ON at high power and two modules turn-ON at low power to reduce the effective susceptance range at low power. In addition, a combining network consisting of four independently optimized T-networks is proposed to provide ideal load conditions for each module during phase variation. With the help of new networks and hybrid modes, the system is optimized to ensure that the effective admittance trajectory of each module is within the minimum loss range. A 13.56 MHz prototype consisting of four Class E modules is constructed, which maintains an efficiency of 76%–89% with output power of 20–200 W, with an average improvement of 9.5% compared to asymmetric Chireix methods.**

***Index Terms*—High frequency, multimodule inverter, parallel network.**

I. Introduction

THE RF power supplies with 13.56 MHz frequency are widely used in semiconductor etching systems, such as inductively coupled plasma etching and capacitively coupled plasma etching. An accurate and efficient control of power is always the key issue in RF power supply applications [1], [2], [3], [4]. Since the traditional RF amplifier works in linear amplification mode, its power is often controlled by the input signal or dc voltage. As the switch mode amplifiers with higher efficiencies are gradually being followed, the nonlinear characteristics of their power and input signals bring challenges for accurate power control, while the pursuit of higher power density makes an extra dc/dc converter no longer preferred.

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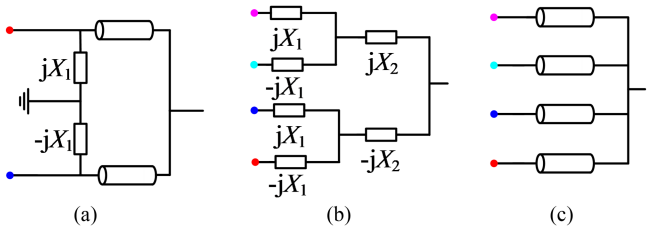

Fig. 1. Circuit structure of power modulated RF power sources. (a) Chireix. (b) Four-way. (c) ON/OFF.

Driven by the above demands, researchers attempt to exploit the voltage source/current source characteristics of some switch mode amplifiers by connecting them in parallel or series in order to find an optimized solution for power control [5], [6], [7], [8], [9].

An outphasing method for controlling power is proposed as shown in Fig. 1(a), which controls the power by phase differences between two parallel voltage sources [10], [11]. The two voltage-source amplifiers are connected to the load through an intermediate Chireix network, which consists of one-fourth-wavelength transmission lines and parallel inductor/capacitor. When the phase is varied, the effective admittances of two amplifiers move in a circular trajectory, and their projection on the horizontal G-axis (conductance) relates to the output power of the module. The method provides an effective way to indirectly control the power through phases. However, the radius of the circle trajectory of admittance is often designed to be very large in order to cover as wide range of power as possible, which in turn leads to a large variation of not only the conductance, but also the susceptance that related to loss. Although the asymmetric selection of shunt inductance and capacitance mitigates the excessively deviation of susceptance, the efficiencies under dynamic power is still difficult to improve.

On the basis of Chireix, a four-way combining network is further proposed to expand the variation of conductance G while limiting the variation of susceptance B [12], [14]. As shown in Fig. 1(b), six inductors and capacitors form a parallel network, and by the precise design of the resonant elements together with tuning the phases of four input voltages, the input admittance Y_1-Y_4 of the network can be varied in the minimum $\Delta B/\Delta G$ manner. The benefit of this method is that for most switch mode amplifiers, a large G range with a small B range represents wide output power and low average loss. However, not only does the system require a network of six components, but all four

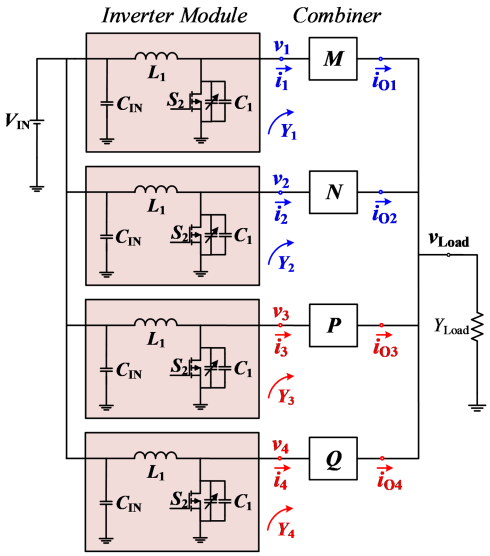

Fig. 2. Circuit structure of proposed inverter system.

amplifier modules need to be loaded with a high-quality factor filter to provide clean resonant current to the network, resulting in a system with at least seven inductors. Not only is the power density challenged, but the tuning difficulties caused by errors of elements also affect the practical application.

In addition to the above scheme, an ON/OFF system is proposed, as shown in Fig. 1(c), the core of which still utilizes phase to control the power [15], [16], [17]. However, when the desired power is high, all modules are in the ON state, and the drive signals of each module are applied with a fixed duty cycle and different phases, and when the desired power is low, some of the modules are in the OFF state, and their drive signals are set to 0. All the power amplifier modules are connected in parallel through a T-type power combining network. This approach further increases the flexibility of the power modulation, in which the designing of admittances no longer gives way to full power range, but rather splits the power into different levels in order to ensure small variations in the susceptance B. However, there are still some problems that need to be solved, such as the OFF amplifier modules are still coupled in the system, which affects other modules, and its switch still has the risk of reverse conduction, leading to some amount of power flowing back to the dc side.

To synthesize the above background, this article combines the idea of multiple operating modes in ON/OFF systems with the idea of using network to design admittance trajectories in outphasing systems, and improves the efficiency of the system under dynamic power through a combination of hybrid amplifier module, hybrid parallel network and hybrid control parameters of phases and ON/OFF states. These hybrid approach not only bring margins for designing combining networks to reduce elements, but also avoid the couple between OFF module and the system.

The proposed inverter is shown in Fig. 2, where four switch type class E power amplifiers are connected in parallel through a power synthesis network composed of M, N, P, and Q matrices. All modules are driven with signals of the same duty cycle and different phases v_{GS1}-v_{GS4}. Since the four inverter modules share the input voltage V_{IN}, their output voltages v_1, v_2, v_3, v_4 have the same amplitude, while the phases of v_1, v_2, v_3, v_4 follow the phases of the drive signals. The fundamental component of voltages v_1-v_4 can be expressed as $V\mathrm{e}^{\mathrm{j}\varphi 1}$-$V\mathrm{e}^{\ \mathrm{j}\varphi 4}$, where V is the amplitude of voltages, which is proportional to the dc input voltage V_{IN}, and φ_1-φ_4 are the phases of drive signals v_{GS1}-v_{GS4}.

Taking module i as example, there are two operation modes. When $v_{\mathrm{GS}i}$ is a square wave with duty cycle D and frequency f, the module operates in an ON mode, the power is amplified from the dc end to the ac end. The relationship between the load conductance Y_i and the loss $P_{\mathrm{Loss}i}$ is as binary cubic function as

$$\begin{aligned} P_{Lossi}(G_i, B_i) = {} & ls_{00} + ls_{10}G_i + ls_{01}B_i + ls_{20}{G_i}^2 \\ & + ls_{11}G_iB_i + ls_{02}{B_i}^2 + ls_{21}{G_i}^2B_i \\ & + ls_{12}G_i{B_i}^2 + ls_{03}{B_i}^3. \end{aligned} \tag{1}$$

ls_{00}-ls_{03} are the fitting coefficients in (1), where the first number represents the exponent of G_i and the second number represents the exponent of B_i. For example, ls_{mn} is the coefficient for ${G_i}^m{B_i}^n$. Similarly, a power model for module i is as

$$P_i(G_i, B_i) = p_{00} + p_{10}G_i + p_{01}B_i + p_{11}G_iB_i + p_{02}{B_i}^2. \tag{2}$$

p_{00}-p_{03} are the fitting coefficients in (2), where the first number represents the exponent of G_i and the second number represents the exponent of B_i. For example, p_{mn} is the coefficient for ${G_i}^m{B_i}^n$. When $v_{\mathrm{GS}i}$ is always 0 V, the module operates in an OFF mode, the switch behaves as a diode. When the current amplitude at the ac side I_i is large, the reverse diode conducts, and the power is rectified from the ac side to the dc side. When I_i is small, the reverse diode no longer conducts, and the power only circulates between passive components. The threshold value of I_{i} occurs just when the diode is not turned on, where the lowest point of oscillation voltage v_{DSi} is just 0 V. Therefore, the amplitude of output current i_{i} can be limited as

$$I_i < V_{IN}Y_{OFF} \tag{3}$$

where Y_{OFF} is the equivalent impedance of the circuit when the diode is not turned ON, and Y_{OFF} is expressed as

$$Y_{OFF} = \frac{-j\omega C_{IN} + j\omega^3 L_1 C_1 C_{IN}}{\omega^2 L_1 C_{IN} + \omega^2 L_1 C_1 + 1}. \tag{4}$$

The four two-port passive networks M, N, P, Q consist of inductors and capacitors which are connected in parallel to further form a five-port complex passive matrix A as

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \end{bmatrix} = A(M, N, P, Q) \begin{bmatrix} Ve^{i\varphi_1} \\ Ve^{i\varphi_2} \\ Ve^{i\varphi_3} \\ Ve^{i\varphi_4} \\ Y_{Load} \end{bmatrix}. \tag{5}$$

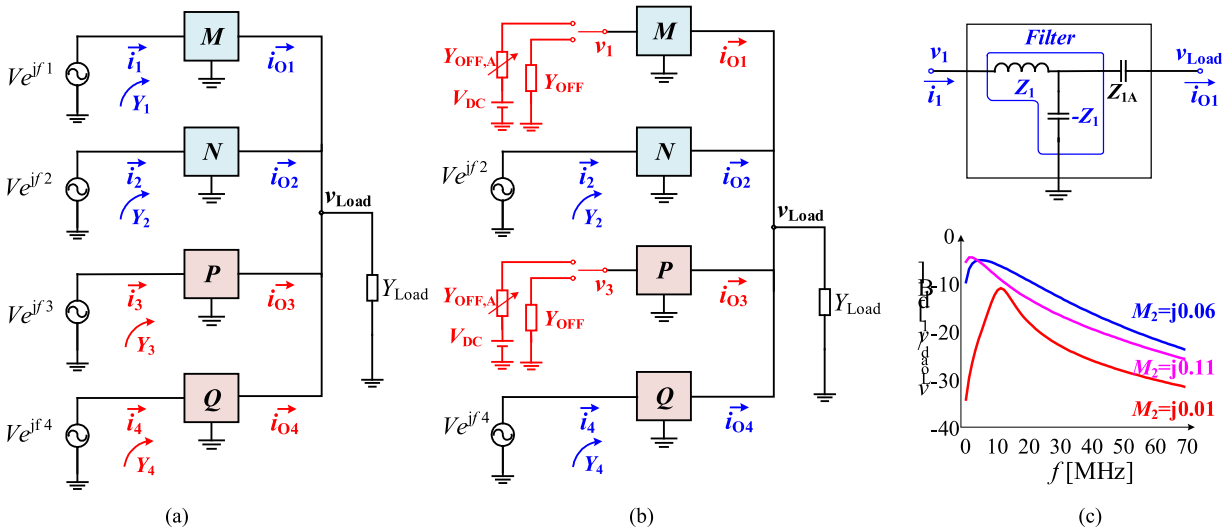

Fig. 3. Circuit of proposed inverter system under different operation modes. (a) Four-ON mode. (b) Two-ON mode. (c) Structure of combiner.

When v_1-v_4 are modulated, the input effective conductance Y_1-Y_4 are varied as functions of $A(M, N, P, Q)$. The benefits brought by matrix A can be concluded as follows.

1) Through φ_1-φ_4, Y_1-Y_4 can be varied to control the output power according to $P_{\text{Load}} = \Sigma P(G_i, B_i)$.
2) While regulating power, the parameter of matrix A can be utilized to further limit the variation range of Y_1-Y_4, thus reducing system loss according to $P_{\text{Loss}} = \Sigma P_{\text{Lossi}}(G_i, B_i)$.
3) When the output power is low, the drive signals v_{GS1}, v_{GS3} can be set to 0 to turn off the module, thus limiting the deviation of Y_i to reduce P_{Loss}.

II. Operation Modes of Proposed System

A. Operation Modes of System

As analyzed above, when $v_{\text{GS}i}$ is a square wave, the class E amplifier module is in ON mode, operating as a voltage source with output voltage expressed as $Ve^{j\varphi i}$. and when $v_{\text{GS}i}$ is 0 V, the amplifier module is in OFF mode, either behaving as a static load Y_{OFF} or as a rectifier. As shown in Fig. 3(a) and (b), the operating state of system can be categorized into two modes: When the output power is high, all four modules are in ON mode. When the output power is low, two modules 2, 4 are in ON mode and two modules 1, 3 are in OFF mode. M, N, P, Q are used to adjust the trajectories Y_1, Y_2, Y_3, Y_4 in the ON state, and limit the amplitudes of i_1 and i_3 in the OFF state.

The four power synthesis networks M, N, P, Q can be represented as matrix of two port networks, as follows:

$$\begin{bmatrix} i_1 \\ i_{O1} \end{bmatrix} = \begin{bmatrix} M_1 & M_2 \\ -M_2 & M_3 \end{bmatrix} \begin{bmatrix} Ve^{i\varphi_1} \\ v_{Load} \end{bmatrix}$$

$$\begin{bmatrix} i_2 \\ i_{O2} \end{bmatrix} = \begin{bmatrix} N_1 & N_2 \\ -N_2 & N_3 \end{bmatrix} \begin{bmatrix} Ve^{i\varphi_2} \\ v_{Load} \end{bmatrix}$$

$$\begin{bmatrix} i_3 \\ i_{O3} \end{bmatrix} = \begin{bmatrix} P_1 & P_2 \\ -P_2 & P_3 \end{bmatrix} \begin{bmatrix} Ve^{i\varphi_3} \\ v_{Load} \end{bmatrix}$$

$$\begin{bmatrix} i_4 \\ i_{O4} \end{bmatrix} = \begin{bmatrix} Q_1 & Q_2 \\ -Q_2 & Q_3 \end{bmatrix} \begin{bmatrix} Ve^{i\varphi_4} \\ v_{Load} \end{bmatrix} \tag{6}$$

where M_1, N_1, P_1, Q_1 and M_2, N_2, P_2 and Q_2 are the coefficients of the matrix in (6). Physically, M_1, N_1, P_1, Q_1 and M_2, N_2, P_2, Q_2 are related to the resonant elements, and their values determine the inductance and capacitance in the M, N, P, Q networks.

It is worth noting that there is no filtering structure in the amplifier modules, in order to provide low-harmonic currents i_i for amplifiers as in part A, networks M, N, P and Q must have sufficient low-pass filtering characteristics. There are several kinds of circuit structures for the networks, such as T-type, Π-type, or even *LCLC* structure, among which, T network is adopted for all four networks to optimize filtering effect. Based on the T-network structure, a low-pass filter can be formed by making $M_3 = N_3 = P_3 = Q_3 = 0$, and resonant parameters Z_1 and Z_{1A} can be calculated from (7), the frequency response is shown in Fig. 3(c)

$$\begin{cases} Z_1 = -\frac{1}{M_2} \\ Z_{1A} = -\frac{M_1 + M_2}{{M_2}^2} \end{cases}. \tag{7}$$

1) Four-ON Mode: The first operating state of the system is shown in Fig. 3(a), and the driving signals $v_{\text{GS}i}$ of the four modules are all provided with duty cycle D and phase φ_1-φ_4, respectively. Then, all four modules operate in ON state, and their output voltages can be expressed as $Ve^{j\varphi 1}$-$Ve^{j\varphi 4}$, respectively. From (6), Y_1, Y_2, Y_3, Y_4 can be calculated as

$$\begin{cases} Y_1 = c_1 + R_{11}e^{i(\varphi_2-\varphi_1)} + R_{12}e^{i(\varphi_3-\varphi_1)} + R_{13}e^{i(\varphi_4-\varphi_1)} \\ Y_2 = c_2 + R_{21}e^{i(\varphi_1-\varphi_2)} + R_{22}e^{i(\varphi_3-\varphi_2)} + R_{23}e^{i(\varphi_4-\varphi_2)} \\ Y_3 = c_3 + R_{31}e^{i(\varphi_1-\varphi_3)} + R_{32}e^{i(\varphi_2-\varphi_3)} + R_{33}e^{i(\varphi_4-\varphi_3)} \\ Y_4 = c_4 + R_{41}e^{i(\varphi_1-\varphi_4)} + R_{42}e^{i(\varphi_2-\varphi_4)} + R_{43}e^{i(\varphi_3-\varphi_4)} \end{cases}. \tag{8}$$

From (8), the trajectory variation rules of Y_1, Y_2, Y_3, Y_4 can be obtained. Taking module 2 as an example, Y_2 is plotted in Fig. 4(a). It can be seen from Fig. 4(a) that Y_2 is determined by

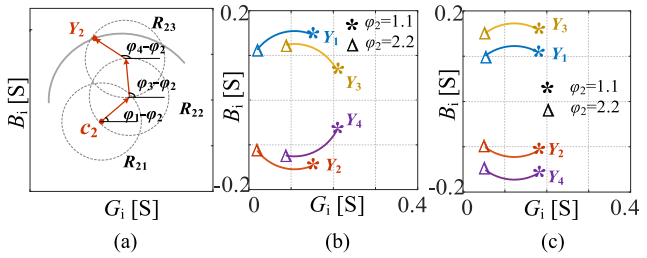

Fig. 4. Admittance trajectory and variation pattern of Y_1, Y_2, Y_3, Y_4. (a) Trajectory of Y_2. (b) Y_1-Y_4 with $\varphi_3 = 0.8$. (c) Y_1-Y_4 with $\varphi_3 = 0$.

TABLE I
GEOMETRIC PARAMETERS OF Y TRAJECTORY

c_1	R_{11}	R_{12}	R_{13}
$\left[-M_2^2/Y_{Load}, -jM_1\right]$	$-M_2N_2/Y_{Load}$	$-M_2P_2/Y_{Load}$	$-M_2Q_2/Y_{Load}$
c_2	R_{21}	R_{22}	R_{23}
$\left[-N_2^2/Y_{Load}, -jN_1\right]$	$-M_2N_2/Y_{Load}$	$-P_2N_2/Y_{Load}$	$-N_2Q_2/Y_{Load}$
c_3	R_{31}	R_{32}	R_{33}
$\left[-P_2^2/Y_{Load}, -jP_1\right]$	$-M_2P_2/Y_{Load}$	$-N_2P_2/Y_{Load}$	$-P_2Q_2/Y_{Load}$
c_4	R_{41}	R_{42}	R_{43}
$\left[-Q_2^2/Y_{Load}, -jQ_1\right]$	$-M_2Q_2/Y_{Load}$	$-N_2Q_2/Y_{Load}$	$-P_2Q_2/Y_{Load}$

an initial point c_2, three vectors with modulus lengths R_{21}, R_{22}, R_{23}, and phases φ_1-φ_2, φ_3-φ_2, and φ_4-φ_2. c_2, R_{21}, R_{22} are as in Table I.

For the values of P_2 and Q_2, it is found that same optimization effect can be achieved with a minimum number of variables when designing M_2, N_2 and P_2, Q_2 as exactly the same two pairs. Therefore, considering the simplicity of the optimization process, this method reduces the number of variables in the circuit by making P_2 and Q_2 equal. Parameters M_2, N_2, P_2, Q_2 and phase φ_1-φ_4 of the network are simplified, as in (9), where φ_4 and φ_2 varies in a difference of φ_3. K is the ratio of M_2, N_2 and P_2, Q_2

$$\begin{cases} M_2 = N_2 = K \cdot P_2 = K \cdot Q_2 \\ \varphi_1 = 0, \quad \varphi_4 = \varphi_2 - \varphi_3 \end{cases}. \tag{9}$$

Then, Y_1-Y_4 in (8) can be simplified as in (10).

$$\begin{cases} Y_1 = M_1 - KP_2^2 \\ \left[K + Ke^{i(\varphi_2)} + e^{i(\varphi_3)} + e^{i(\varphi_2-\varphi_3)}\right]/Y_{Load} \\ Y_2 = N_1 - KP_2^2 \\ \left[K + Ke^{i(-\varphi_2)} + e^{i(-\varphi_3)} + e^{i(\varphi_3-\varphi_2)}\right]/Y_{Load} \\ Y_3 = P_1 - P_2^2 \\ \left[1 + Ke^{i(-\varphi_3)} + Ke^{i(\varphi_2-\varphi_3)} + e^{i(\varphi_2-2\varphi_3)}\right]/Y_{Load} \\ Y_4 = Q_1 - P_2^2 \\ \left[1 + Ke^{i(\varphi_3)} + Ke^{i(\varphi_3-\varphi_2)} + e^{i(2\varphi_3-\varphi_2)}\right]/Y_{Load} \end{cases}. \tag{10}$$

Fig. 4(b) and (c) shows Y_1, Y_2, Y_3, Y_4 trajectories with different φ_2 and φ_3. φ_2 determines the length and extension direction of the Y_1-Y_4 trajectories, and φ_3 further determines the distributional relationship of these trajectories.

2) Two-on Mode: The second operating state of the system is shown in Fig. 3(b). Module 2 and module 4 are operating in the ON state. In the case where only two modules are activated, only the phase difference between φ_2 and φ_4 affects the system behavior. Therefore, to simplify the following analysis, the phase φ_4 of module 4 is set to zero($\varphi_4 = 0$), and the phase φ_2 of module 2 is varied to adjust Y_2 and Y_4 and thus adjusting power, and their output voltages can be expressed as $Ve^{j\varphi 2}$ and Ve^{j0}, respectively. The module 1 and module 3 are operating in the OFF state, and their drive signals are 0V. When amplitudes of i_1 and i_3 are less than the current threshold, module 1 and module 3 can be equivalent to Y_{OFF}. When i_1 and i_3 are greater than the current threshold, the module 1 and module 3 are operating in a non-ideal state. From (6), i_1 and i_3 can be calculated as

$$\begin{aligned} i_1 &= \frac{{M_2}^2}{-Y_{OFF} - M_1} v_{Load} \\ i_3 &= \frac{{P_2}^2}{-Y_{OFF} - P_1} v_{Load}. \end{aligned} \tag{11}$$

Combining (11) and (3), M_2, P_2 can be designed according to (12), which help to prevent diode from conducting in an OFF module

$$\begin{aligned} M_2 &< \frac{V_{IN}}{v_{Load}} \left| Y_{OFF} - M_1 \right| \\ P_2 &< \frac{V_{IN}}{v_{Load}} \left| Y_{OFF} - P_1 \right|. \end{aligned} \tag{12}$$

When the currents of modules 1 and 3 are both limited and their body diodes cannot conduct, the equivalent impedance of modules 1 and 3 is Y_{OFF}, as deduced in (4). The effective admittance Y_2 and Y_4 of modules 2 and 4 can be calculated as

$$\begin{aligned} Y_2 &= N_1 - \left({N_2}^2 + N_2Q_2e^{i\varphi_2}\right) \\ &\quad \Big/ \left(Y_{Load} - \frac{{P_2}^2}{Y_{OFF} + P_1} - \frac{{M_2}^2}{Y_{OFF} + M_1}\right) \\ Y_4 &= Q_1 - \left({Q_2}^2 + N_2Q_2e^{i(-\varphi_2)}\right) \\ &\quad \Big/ \left(Y_{Load} - \frac{{P_2}^2}{Y_{OFF} + P_1} - \frac{{M_2}^2}{Y_{OFF} + M_1}\right) \end{aligned} \tag{13}$$

where $\varphi_4 = 0$, φ_2 is adjusted to modulate Y_2 and Y_4.

3) Optimization Principles for Proposed System: For class E power amplifiers, the output power P_{i} has an almost linear relationship with G_i, but a weak correlation with B_{i}. This means that a wide range of ΔG_i brings a larger power range ΔP_i. Similarly, the loss of a single module is strongly correlated with B_{i}, which means that larger ΔB_i leads to larger loss $\Delta P_{\mathrm{Loss}i}$. In order to minimize losses while adjusting power, output power and total loss of system P_{Load} and P_{Loss} are utilized to demonstrate the output power range and loss range as

$$P_{\mathrm{Loss}} = \begin{cases} \sum_{i=1}^{4} P_{Lossi}\left(G_i, B_i\right), & \text{Four-ON-Mode} \\ P_{\mathrm{Loss2}}\left(G_2, B_2\right) + P_{\mathrm{Loss4}}\left(G_4, B_4\right), & \text{Two-ON-Mode} \end{cases}$$

$$P_{\mathrm{Load}} = \begin{cases} \sum_{i=1}^{4} P_i\left(G_i, B_i\right), & \text{Four-ON-Mode} \\ P_2\left(G_2, B_2\right) + P_4\left(G_4, B_4\right), & \text{Two-ON-Mode} \end{cases}. \tag{14}$$

Similarly, in order to ensure that the output power P_i of each module is positive, i.e., the module is in the inverted rather than rectified state, G_i of ON modules must be greater than zero

$$G_i \geq 0. \tag{15}$$

From above analysis, the operation modes and design considerations of proposed system can be summarized as follows.

1) *Four-ON Mode*: All four modules are in ON mode, and their admittance Y_1-Y_4 are expressed as (10).
2) *Two-ON Mode*: 24 modules are in ON mode, with their admittance Y_2,Y_4 expressions as in (13). A total of 13 modules are in OFF mode, to make module 13 nonrectified, the matrices M_2, P_2 need to satisfy (12).
3) To optimize system by controlling power while reducing loss, Y_1-Y_4 in (10) and (13) need to be designed to make the system power P_{Load} in (14) in accordance with the corresponding power ranges, while P_{Loss} as small as possible, and the G_i of each module should be in accordance with (15) in order to ensure a stable inverting state.

III. Design of Network and Phases

A Calculation of M_1, N_1, P_1, Q_1

According to the analysis in Session II, the design process for M, N, P, and Q under multiple constraints are introduced as follows. The calculation process of the evaluation coefficients M_1, N_1, P_1, Q_1 is shown in Fig. 5.

First, in four-ON mode, $P_{\text{Load,Max}}$, $P_{\text{Load,4Min}}$ are defined as maximum and minimum output power for four-ON mode operation. $B_{\text{Ei,4ON}}$ is calculated as the average effective susceptance when the system power P_{Load} is in the range of [$P_{\text{Load,4Min}}$, $P_{\text{Load,Max}}$].

Second, in two-ON Mode, $P_{\text{Load,4Min}}$, $P_{\text{Load,Min}}$ are defined as maximum and minimum output power for two-ON mode operation. $B_{Ei,2\text{ON}}$ is calculated as the average effective susceptance when the system output power P_{Load} is in the range of [$P_{\text{Load,Min}}$, $P_{\text{Load,4Min}}$].

Then, M_1, N_1, P_1, Q_1 are adjusted step by step according to the difference between $B_{Ei,4\text{ON}}$, $B_{Ei,2\text{ON}}$ and $B_{i,\text{opt}}$, where N_1, Q_1, $M1$, P_1 are iterated in order to make the susceptance of 1–4 modules in 4-ON mode, $B_{1,4\text{ON}}$, $B_{2,4\text{ON}}$, $B_{3,4\text{ON}}$, $B_{4,4\text{ON}}$ and the susceptacne of 2–4 modules in two-ON mode $B_{2,2\text{ON}}$, $B_{4,2\text{ON}}$ converge to a certain ideal value of $B_{1,\text{opt}}$, $B_{2,\text{opt}}$, $B_{3,\text{opt}}$, $B_{4,\text{opt}}$. $B_{\text{i,opt}}$ are the optimal average susceptance that minimize loss of module i within the range of $G_i = [j0\text{S}, j0.05\text{S}]$.

With proposed process, the admittance of the modules can be adjusted to the target range step by step, and one case is as shown in Fig. 6, where the ideal susceptances $B_{1,\text{opt}}$, $B_{2,\text{opt}}$ of modules 1, 2 are -j0.24S, and that of modules 3, 4 are -j0.13S. Fig. 6(a) shows the trajectories of Y_1, Y_2, and Fig. 6(b) shows the trajectories of Y_3, Y_4, from which it can be seen that the adjustment of M, N, P, Q matrixes brings a significant improve on the admittance trajectories.

B. Optimization of φ_3

With certain M_2, N_2, P_2, Q_2 and optimal [M_1, N_1, P_1, Q_1], the system loss P_{Loss} with system output power P_{Load} under four-ON mode is calculated using (14), where relationships of phase φ_1-φ_4 declared in (9). A calculation result of P_{Loss} versus P_{Load} with different φ_3 is as shown in Fig. 7.

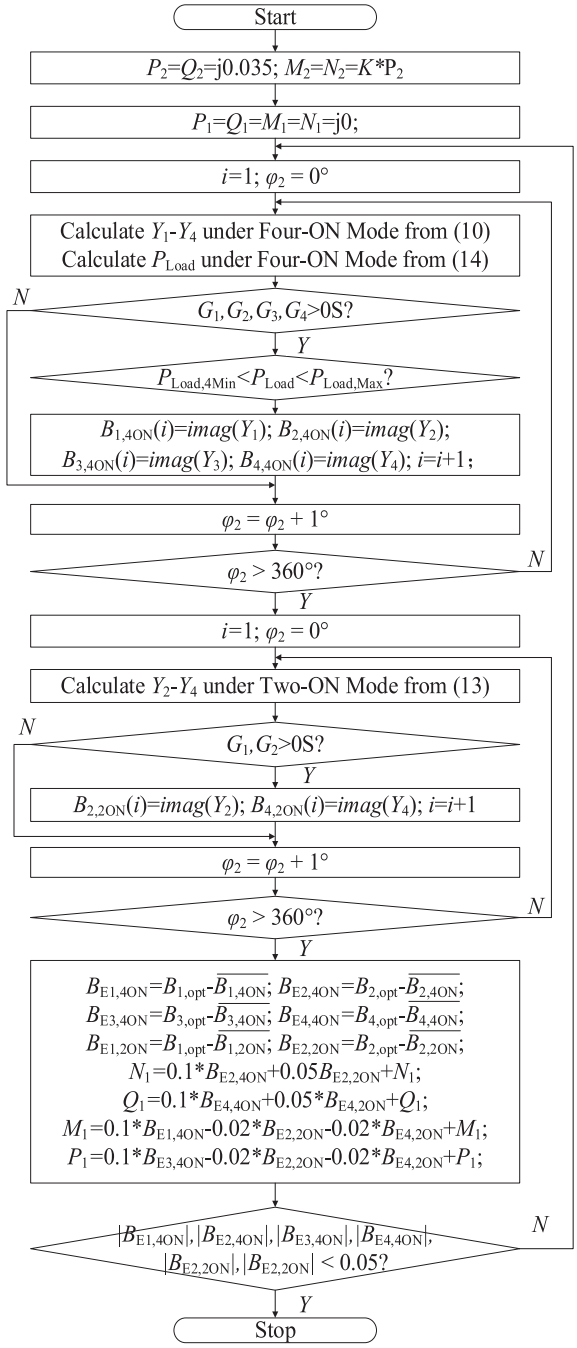

Fig. 5. Calculation process of P_{Loss} and P_{Load} for certain M_2, N_2, P_2, Q_2.

When the system output power is assumed to vary between [$P_{\text{Load,4Min}} = 60$ W, $P_{\text{Load,Max}} = 200$ W] in four-ON mode, $\varphi_3 = 0.4$ (purple line) and $\varphi_3 = -0.8$ (bule line) ensures that the loss is minimized within 20 W. In four-ON Mode, the maximum loss difference between the two lines occurs at an output power of 150 W, where the blue line is 0.5 W lower than the purple line, which means that the blue line has less than a 0.8% improvement on efficiency in four-ON mode. In two-ON mode, the maximum loss difference between the two lines occurs at an output power

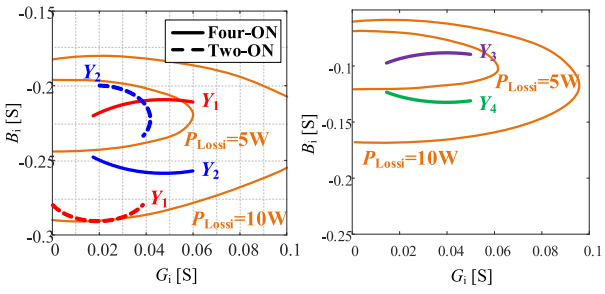

Fig. 6. Trajectories of Y_1-Y_4 with $M_2 = N_2 = j0.023$S, $P_2 = Q_2 = j0.019$S, $M_1 = -j0.257$S, $N_1 = -j0.211$S, $P_1 = -j0.128$S, and $M_1 = -j0.092$S. (a) Y_1, Y_2. (b) Y_3, Y_4.

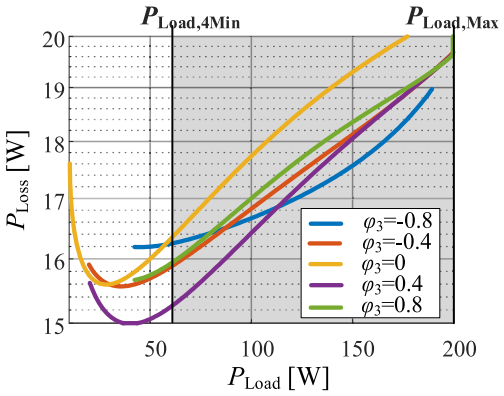

Fig. 7. P_{Loss} versus P_{Load} for $M_2 = N_2 = P_2 = Q_2 = j0.035$S, and $Y_{Load} = 0.02$S.

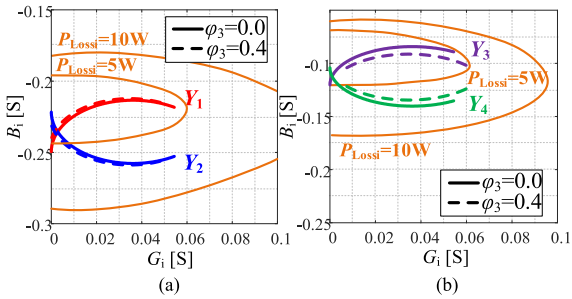

Fig. 8. Trajectory of admittances for $M_2 = N_2 = P_2 = Q_2 = j0.035$S, $Y_{Load} = 0.02$S, $P_{Load,4Min} = 50$ W, and $P_{Load,Max} = 200$ W. (a) Y_1-Y_2. (b) Y_3-Y_4.

of 40 W, where the purple line is 1.2 W lower than the blue line, which means that the purple line has an improvement of up to 3% on efficiency in two-ON mode. Summarizing the above comparison results, the system efficiency is optimized with φ_3 being 0.4.

The effective conductance Y_1-Y_4 of each module with $\varphi_3 = 0.4$ and $\varphi_3 = 0$ is shown in Fig. 8. It can be seen that while controlling the output power of each ON module, their admittance is adjusted to a low-loss region with the help of phase φ_3.

C. *Optimization of* K

With a calculation process in Figs. 5 and 7, optimal values of M_1, N_1, P_1, Q_1, φ_3 according to M_2, N_2, P_2, Q_2 can be found.

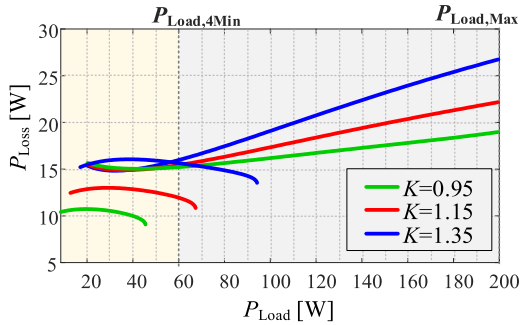

Fig. 9. P_{Loss} versus P_{Load} for $P_2 = Q_2 = j0.035$S, $Y_{Load} = 0.02$S, and $\varphi_3 = 0.4$.

Subsequently, in order to further cover a lower power range, the two-ON mode is adopted, with the system power range being defined as $P_{Load} < P_{Load,4Min}$. At this time, only modules 2 and 4 are turned ON, and φ_2 is used to regulate power. The system needs to meet the following conditions simultaneously: the currents of OFF branches are limited with the help of (12) and the effective admittance Y_2, Y_4 covers power range while ensuring a lower overall loss.

The coefficient K ($K = M_2/P_2 = N_2/Q_2$) can be used to balance the output power range and loss range, as shown in Fig. 9. When K is small ($K = 0.95$, green line), the output power in two-ON mode may not reach $P_{Load,4Min}$, resulting in an intermittent output power regulation. When K is large ($K = 1.35$, blue line), the system loss increase significantly. Therefore, it is necessary to find a moderate value of K so that P_{Load} varies continually from $P_{LoadMin}$ to $P_{Load,4Max}$, at the same time, the average P_{Loss} is kept small.

In two-ON mode, for the green line in Fig. 9, the maximum output power cannot reach 60W due to the insufficient conductance G_2 and G_4 caused by the small K ($K = 0.95$). For the red and blue lines in Fig. 9, higher K($K>1$) leads to higher maximum values of conductance G_2 and G_4, which leads to maximum value of P_{Load} more than 60 W. For the red line, with $K = 1.1$, maximum G_2 is 0.03S, maximum G_4 is 0.055S, a total conductance $\Sigma G = 0.085$S lead to a maximum power of $P_{Load} = 65$ W. For the blue line, with $K = 1.35$, maximum G_2 is 0.042S, maximum G_4 is 0.06S, a total conductance $\Sigma G = 0.102$S lead to a maximum power of $P_{Load} = 95$ W. The effective conductance Y_1-Y_4 with $K = 1.1$ and $K = 1.35$ is shown in Fig. 10. The selection of $K = 1.1$ ensures that the trajectories of Y_1 and Y_2 are within the low loss boundaries, while not affecting the variation of Y_3 and Y_4.

As can be seen in Fig. 10, the trajectory of ZVS is a line that varies laterally along the G-axis. However, Y_1-Y_4 vary on both the G-axis and the B-axis. The phase shifting and network parameters have limited control relative to the admittance. Therefore, with limited control variables, only most of Y_1-Y_4 can be designed to conform to the ZVS trajectories, and at some extreme powers, ZVS cannot be accommodated.

The above provides a method for selecting K using a class E circuit and 0–200 W output power as an example. When other options are considered, the value of K can be evaluated by following design flow in Fig. 11.

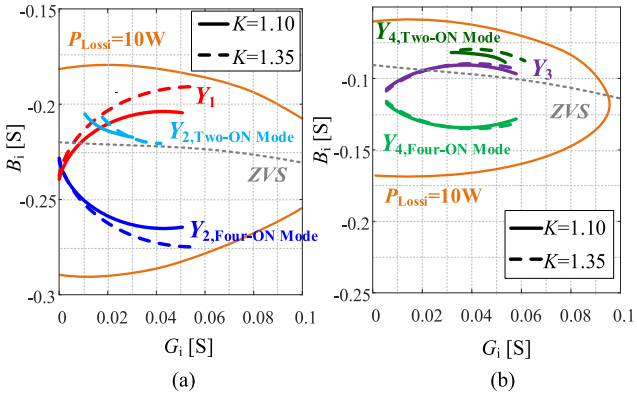

Fig. 10. Trajectory of admittances Y_1-Y_4 for $P_2 = Q_2 = j0.035$S, $Y_{\text{Load}} = 0.02$S, $P_{\text{Load,4Min}} = 60$ W, $P_{\text{Load,Max}} = 200$ W, and $\varphi_3 = 0.4$. (a) Y_1-Y_2. (b) Y_3-Y_4.

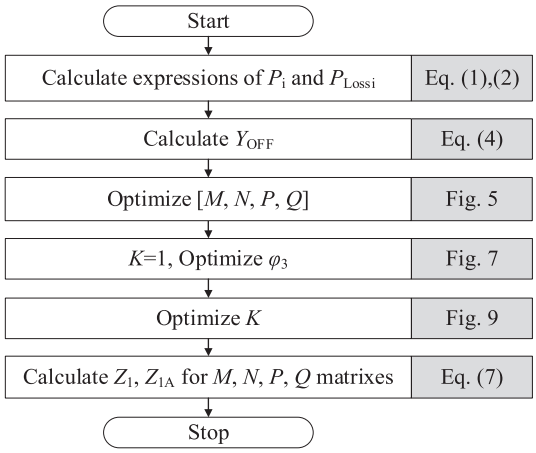

Fig. 11. Design process for proposed paralleled inverter system.

IV. Experiment Result

The above analysis provides a comprehensive design method for controlling power using multiple parallel power amplifier modules, which is divided into four main steps as shown in Fig. 11.

The first step is to use load-pull method to obtain the relationship between load admittance and loss and output power for amplifier modules. The second step is to design matrices M, N, P, Q in power combining network to help the effective admittance Y_1-Y_4 fall within the lowest loss range while covering desired power. The third step is to further reduce the system loss by correcting the phase φ_3 and the coefficient K ($K = M_2/P_2 = N_2/Q_2$). The final step is to calculate resonate parameters in M, N, P, Q matrices.

Based on the above steps, a four-module paralleled-system with a frequency of 13.56 MHz, a rated load of 50 Ω, and an output power of 20–200 W is proposed. The circuit structure is shown in Fig. 12, with four Class E amplifiers with input voltage $V_{\text{IN}} = 30$ V, and with drive signals square waves with duty cycles $D = 0.3$ and phases of φ_1-φ_4. The output terminals of modules are connected to the load through four T-type networks.

For modules 2 and 4 with larger resonant capacitors C_2, C_4, and modules 1 and 3 with smaller resonant capacitors C_1 and C_3,

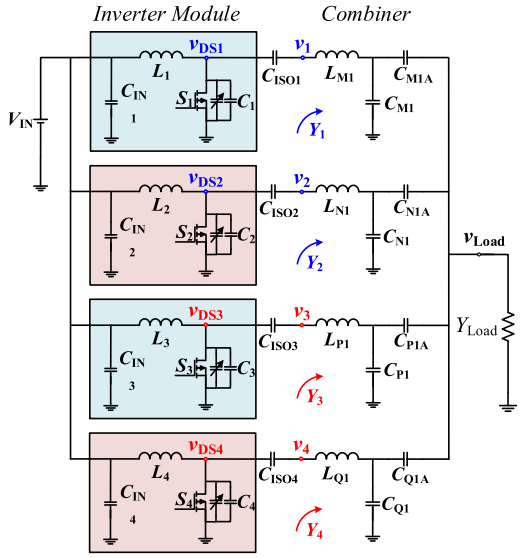

Fig. 12. Circuit structure of proposed inverter system.

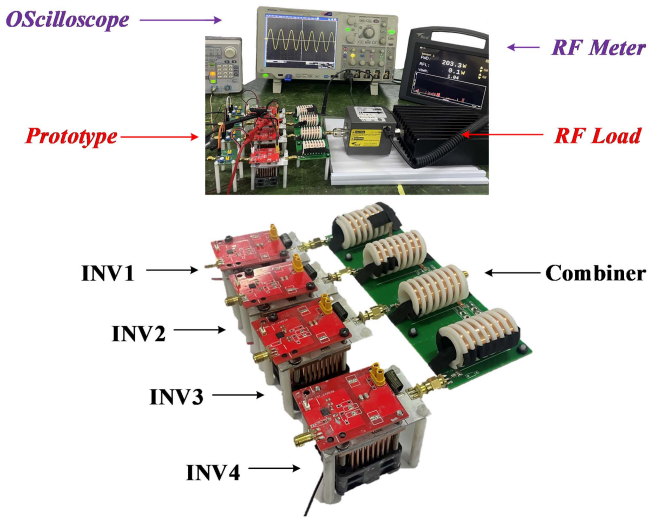

Fig. 13. Prototype and test environment.

the coefficients in (1) and (2) are given in Table IV. With similar losses and power distributions, the small resonant capacitors of modules 1 and 3 ensure a smaller Y_{OFF}, thereby improving the system power range in two ON mode.

With above modules and network parameters, the output power of system P_{Load} can be adjusted from 20 to 200 W, $P_{\text{Load,4Min}}$ is selected as 60 W. When 20 W $< P_{\text{Load}} <$ 60 W, two-ON mode is adopted, while when $P_{\text{Load}} >$ 60 W, four-ON mode is adopted. A prototype is built as Fig. 13 shows.

According to Table II and Fig. 11, parameters of M, N, P, Q are optimized, K is selected as 1.10, and φ_3 is optimized as 0.4. Then relevant parameters of the circuit are given in Table III, waveforms, output power and input power are captured using oscilloscope MSO5204B, voltage probe P6139B, RF Meter Bird 4421A and dc Source Chroma 62150H.

The efficiency of proposed system at full power (20–200 W, 10:1) are shown in Fig. 14 , in comparison, the other lines

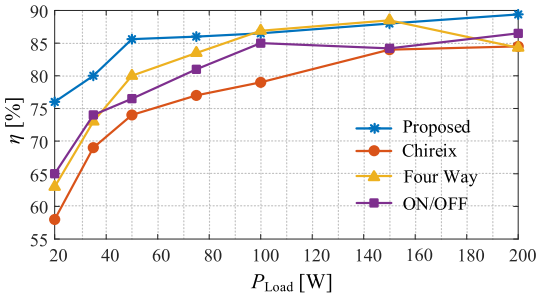

Fig. 14. Efficiency of proposed prototype at full power.

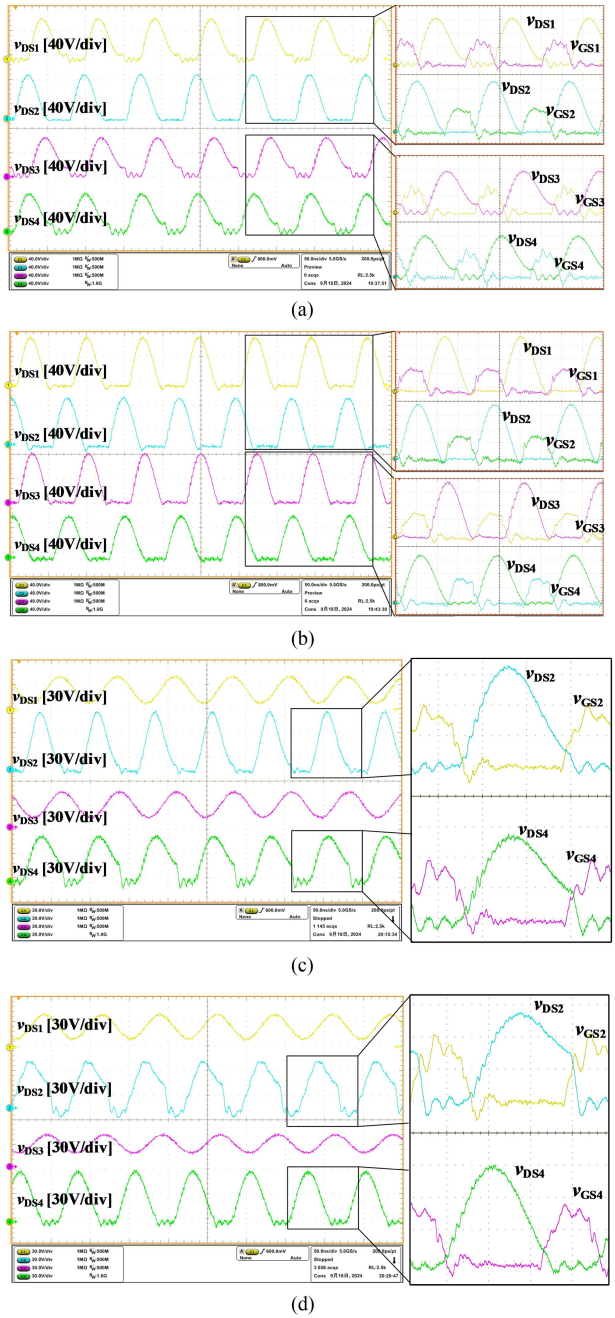

Fig. 15. Drain-source waveforms of modules at full power. (a) $P_{\mathrm{Load}} = 200$ W, four-ON mode. (b) $P_{\mathrm{Load}} = 100$ W, Four-ON mode. (c) $P_{\mathrm{Load}} = 50$ W, two-ON mode. (d) $P_{\mathrm{Load}} = 20$ W, two-ON mode.

TABLE II
FACTORS IN (1) AND (2)

Factors	*Module* 2,4	*Module* 1,3	*Factors*	*Module* 2,4	*Module* 1,3
ls_{00}	348.6	46.62	ls_{12}	-5776	1905
ls_{10}	-549.0	-79.37	ls_{03}	16160	11300
ls_{01}	3850	909.5	p_{00}	-0.649	-7.829
ls_{20}	2164	2165	p_{10}	238.1	436.7
ls_{11}	-3521	452.2	p_{01}	-6.911	-189.9
ls_{02}	13930	6048	p_{11}	-2648	-3957
ls_{21}	5161	3157	p_{02}	-19.74	-647.9

TABLE III
PARAMETERS IN PROPOSED INVERTER SYSTEM

Label	*Value*
C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4}	100nF, 100V, C0G
C_{ISO1}, C_{ISO2}, C_{ISO3}, C_{ISO4}	100nF, 100V, C0G
S_1, S_2, S_3, S_4	GS61004B, GaN Systems
L_1, L_2, L_3, L_4	500nH, 270mΩ, Coil Craft
C_1, C_2	2000pF, ATC 700A
C_3, C_4	800pF, ATC 700A
L_{M1}, L_{P1}	420nH, 143mΩ
L_{N1}, L_{Q1}	395nH, 115mΩ
C_{M1}, C_{P1}	240pF, 10pF, ATC 700A
C_{N1}, C_{Q1}	270pF, 10pF, ATC 700A
C_{M1A}	56pF, ATC 700A
C_{N1A}	220pF, ATC 700A
C_{P1A}	27pF, 22pF, ATC 700A
C_{Q1A}	240pF, ATC 700A
Driver	LM5113
Z_{Load}	50Ω

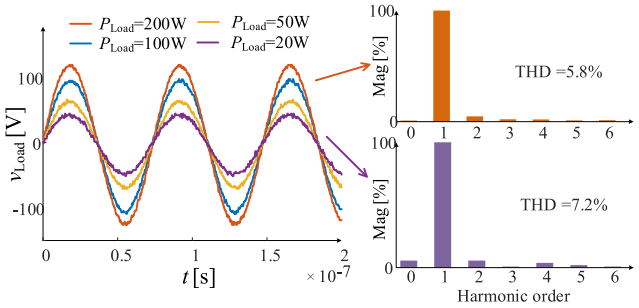

Fig. 16. Output voltage waveforms of prototype at full power.

represent the efficiency measured using same Class E modules, inductors with same quality and networks with control methods optimized at rated power (200 W).

Since the asymmetric Chireix network can only modulate power through circular admittance trajectories, its efficiency at low power is significantly reduced compared to the two-ON mode of this article. Similarly, the four-way combining network provides an admittance trajectory with a small change in susceptance B and a large change in conductance G, which leads to an increase in efficiency over Chireix at full power. However, the Four-way combining network does not have filtering characteristic, which means that each inverter module needs to be filtered by a resonant tank with high quality factor, which limits the efficiency considering the loss of the filtering inductors.

TABLE IV
EFFICIENCIES AND INDUCTORS OF RELATED WORKS

Parameters	*This Work*	*Chireix* [10]	*Four-way* [12]	*ON/OFF* [15]
Power [W]	20-200	20-200	20-200	20-200
Efficiency[%]	76-89	59-84	63-88.5	65-86.5
Inductors	4	6	7	8
Capacitors	8	8	7	12

ON/OFF mode avoid excessive deviation of susceptance B at low power by ordering three modules to turn on at 100 W and two modules to turn ON at 45 W. However, due to the lack of targeted design of the combining network, the basic structure remains similar to Chireix, and the variation of conductance B within each power level remains to be extreme, which introduces additional switching losses.

The drain-source voltage of proposed system at full power (20–200 W, 10:1) are shown in Fig. 15. At four-ON mode, as shown in Fig. 15(a) and (b), modules 1–4 are nearly zero-voltage-switched, which represents modules working in a low loss region. At two-ON mode, as shown in Fig. 15(c) and (d), module 13 are kept away from reverse conducting, which represents ON modules working in a low loss region and OFF modules decoupling from system. These waveforms demonstrate the effectiveness of the proposed method, where admittances are designed according to criteria to ensure a wide power coverage while maintaining high overall efficiency. Through above design flow, two ways are adopted to address the problem: make Y_1-Y_4 coincide with the ZVS trajectory as much as possible, and sacrifice ZVS at certain power points to ensure the relative balance of efficiency at full power. These two steps are maximal effort to increase efficiency for a streamlined system. To ensure ZVS operation over the full power range, it may be necessary to make Y_1-Y_4 track the ZVS trajectory, and the system will need to introduce more variables.

The output voltage v_{Load} of proposed system at full power (20–200 W, 10:1) are shown in Fig. 16. As shown in the waveform, the proposed network composed of M, N, P, and Q matrices not only plays a role in adjusting admittance, but also has good low-pass filtering effect. Therefore, the system and modules do not require additional filters to ensure sinusoidal resonance currents in each branch and output terminal.

As conclusion, with design and control criteria proposed in different papers, the efficiencies and resonant element quantities of systems built with same power range (20–200 W, 1:10) and same class E inverter modules are given in Table IV, where the adopted approach utilizes fewer inductors to maintain a higher efficiency.

V. CONCLUSION

To avoid efficiency drop of megahertz amplifiers during high to low power regulation, this article proposes a novel parallel system architecture which is composed by four inverter modules connecting in parallel through four matrices. The system is divided into high power level and low power level by four-ON mode and two-ON mode, avoiding deviation of effective admittance at low power. Combining network of four matrices is further optimized to limit effective input admittance into low-loss region, which helps improve the average efficiency of system at full power. As a result, a 13.56 MHz, 20–200 W prototype consisting of four class E modules with independent control of ON/OFF status and phases, and power combining network with four matrices independently designed is proposed. The adoption of two-ON mode increases the efficiency at low power from 55% to 77%. The optimized matrix and phase ensure that all modules are under optimized load conditions, where switches in ON modules are turned on with minimized zero drain-source voltages, while OFF modules are clamped with positive drain-source voltages to avoid rectification. The average efficiency of the system is increased from 75.1% to 84.5%. The adopted network balances filtering and admittance modulation, reducing the inductors in the system from 8 to 4, significantly reducing volume and AC Resistance (ACR) losses.

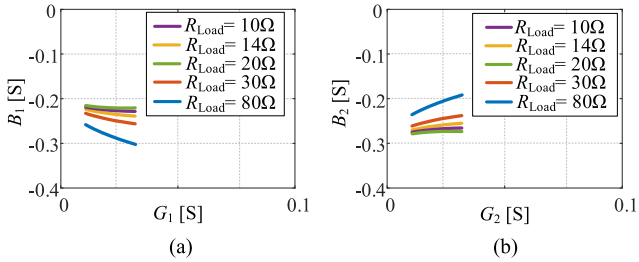

Fig. 17. Trajectory of admittances Y_1-Y_2 under four-ON mode. (a) Y_1. (b) Y_2.

APPENDIX

In this article, the multimodule operation is carried out for a rated load of 50 Ω, and variable load operation is considered as follows.

Taking four-ON mode as example, parameters of networks M, N, P, Q are already optimized in Section V for a rated load of 50 Ω. To analyze the system performance under variable load, the load of system is set to vary from 10 to 80 Ω. Then by bringing M_1, N_1, P_1, Q_1, M_2, N_2, P_2, Q_2, and Y_{Load} into (8), Y_1-Y_4 trajectories with output power varying from 60 to 200 W can be obtained, as Fig. 17 shows. As seen in Fig. 17, an increase in load resistance R_{Load} leads to a longitudinal downward shift of the Y_1 trajectory and a longitudinal upward shift of the Y_2 trajectory, and vice versa. When R_{Load} is greater than 80 Ω, the Y_1 and Y_2 trajectories will be outside the region where inverter modules can operate properly.

Further, substituting Y_1-Y_4 into the loss prediction (14), the system loss P_{Loss} corresponding to the inverter output power P_{Load} is shown in Fig. 18. The results show that the overall system loss increases with the increase of load R_{Load}. However, in the analyzed range of $10\ \Omega < R_{\mathrm{Load}} < 80\ \Omega$, total loss is kept under 25 W. The calculation result of phase φ_2 with different load is as Fig. 19 shows, where indicates that different φ_2 are required to control power with different loads.

When the load exceeds certain ranges, adjusting phases cannot fully correct admittance, where additional impedance matching

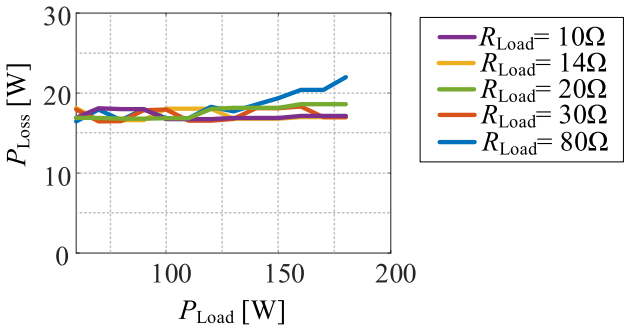

Fig. 18. P_{Loss} versus P_{Load} under four-ON mode.

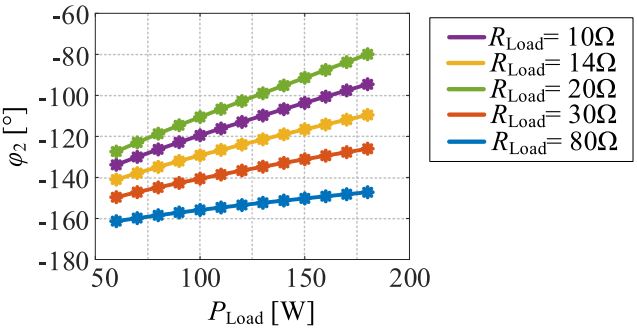

Fig. 19. φ_2 versus P_{Load} under four-ON mode.

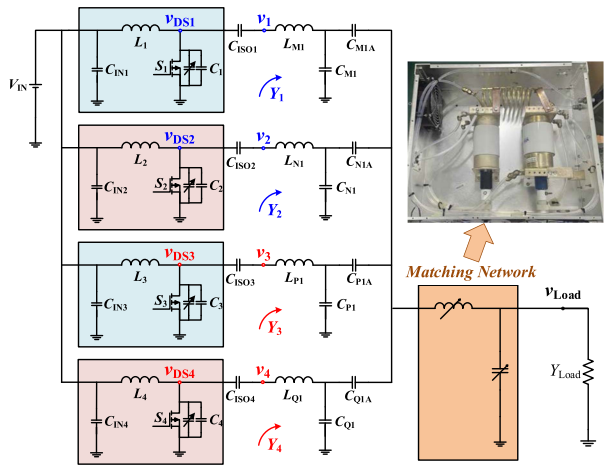

Fig. 20. Inverter system with varying load.

networks may be required to correct the load as Fig. 20 shows, where the capacitance and inductance of the vacuum capacitor and the tap inductor are adjusted by stepper motors to match the load impedance Z_{LOAD} to 50 Ω, therefore providing a constant load for inverter system.

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