Implementation of SOLM as an Extended SVPWM for Variable Six Pulse DC-Bus Electrolytic Capacitor-Less VSI Based Constant V/f Induction Motor Drive

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***Abstract*—Synchronous one-leg modulation (SOLM) technique has been used for six-pulse dc-bus electrolytic capacitor-less voltage source inverter (VSI) considering reduced switching loss compared to space vector pulsewidth modulation (SVPWM). The existing method for generating the modulating signal in SOLM technique utilizes a sector identification-based approach. This work demonstrates, through both mathematical analysis and hardware results, that despite differences in the dc-bus voltage, modulating signal and instantaneous pole voltage waveforms between SVPWM and SOLM techniques, their average pole voltages are identical. Based on this understanding, this work proposes implementing the SOLM technique as an extension of SVPWM technique without requiring sector identification. A comparison between the proposed and the existing implementations of SOLM shows reduction in computational effort. A 1.25-kVA hardware prototype was developed for open-loop V/f control of a 1-hp induction motor. A comparison has been made between SVPWM with fixed dc-bus voltage, SVPWM with variable dc-bus voltage and SOLM with variable six-pulse dc-bus voltage. VSI efficiency with SOLM was in the range of 98.4%–99.1% at different operating conditions. Operation of the converter was successfully demonstrated under motor acceleration, steady-state operation as well as during deceleration.**

***Index Terms*—Electrolytic capacitor-less, induction motor (IM) drive, single active bridge (SAB), six-pulse modulation, space vector pulsewidth modulation (SVPWM), V/f control and voltage source inverter (VSI).**

I. Introduction

VOLTAGE source inverters (VSIs) that utilize minimal or no capacitance in the dc-bus, rather than relying on a sizeable electrolytic capacitor, may be termed dc-bus electrolytic capacitor-less VSI [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. They have the advantage of increased reliability, efficiency, and power density over conventional VSIs, which use large electrolytic capacitors in the dc-bus [2], [7]. The dc-bus voltage in these converters can either maintain a constant dc profile [1], [2], [3] or exhibit a six-pulse varying dc profile [4], [5], [6], [7], [8], [9], [10], [11], [12], depending on the application and the VSI control scheme employed. In [1], [2], and [3], space vector pulsewidth modulation (SVPWM) is implemented with a constant dc-bus voltage profile. In contrast, the three-phase two-level VSIs discussed in [4], [5], [6], [7], [8], [9], and [10] exhibit a six-pulse dc-bus voltage profile and employ a modulation scheme in which only one leg's switches alternate between ON and OFF states for one-third of the fundamental period, which leads to a reduction in switching loss by 66% compared to the sinusoidal pulsewidth modulation (SPWM) technique, as noted in [7]. This modulation scheme has been referred to as synchronous one-leg modulation (SOLM) [9]. Similar PWM schemes have also been implemented in different forms, such as 1/3-PWM in [11] and 240-CPWM in [12]. One of the methods of implementing SVPWM uses the calculation of dwell times for the voltage vector to be applied in a particular sector [4], [5], [6], [7], [8], [9], [10]. In this method, sector identification for the space phasor of voltage is required. As per the available literature, the existing method of implementing SOLM also requires sector identification. Another method of implementing SVPWM is the carrier and modulating signal-based approach, which eliminates the need for sector identification. This method is inherently suitable for implementation via digital controllers [13] for SVPWM as well as other PWM methods. However, this second method of implementation is not yet reported for SOLM.

The use of a small value dc-bus capacitor in the converters reported in [4], [5], [6], [7], [8], [9], and [10] allows the voltage at the dc-bus to be varied at a faster rate under closed-loop control. This flexibility of the dc-bus voltage can be used for variable voltage variable frequency (VVVF) control of induction motor (IM) drives. The variation of dc-bus voltage as per the drive operating conditions can provide better utilization of the dc-bus voltage along with an increase in efficiency especially at lower speeds [14]. Research works presented in [9], [12], and [14], show the use of a variable dc-bus voltage for IM drive. In [9], SOLM with V/f control of IM drive with a dc-bus electrolytic capacitor-less VSI has been proposed but the V/f control is limited to a minimum voltage and frequency value below which SPWM is used. In [12], a variable dc-bus voltage control with 240-CPWM for three-phase two-level VSI is shown using R-L load as an emulation of IM drive. The use of an interleaved boost converter in [12] limits the minimum value of the dc-bus voltage that can be achieved. In [14], a variable dc-bus voltage fed

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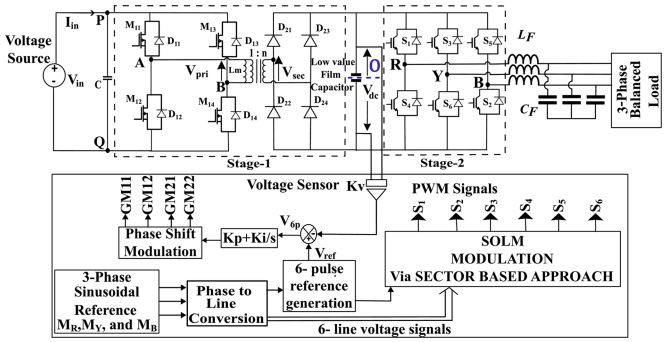


Fig. 1. Schematic of DC-bus electrolytic capacitor less VSI.

SVPWM based VSI for IM control is reported. In [15], a variable dc-bus voltage-based IM drive for improving performance at low motor speeds is reported. Sridharan and Krein [14] and Kwon and Kim [15] use a SVPWM-based control of VSI for IM, which can be replaced by SOLM to achieve increased efficiency.

The V/f control of IM drive for a wide range of speed variation, using the converter shown in Fig. 1 based on [16], with SOLM technique and a variable dc-bus voltage has not yet been reported in literature. Considering these aspects the following contributions are made through this work.

1) It is shown using mathematical equations, simulations as well as hardware results that the averaged output pole voltages are the same for both SVPWM and SOLM even though their modulating signals, instantaneous values of pole voltages and instantaneous dc-bus voltages are different. Based on this understanding, it is shown that SOLM can be implemented as an extension of the SVPWM technique, which does not require sector identification unlike the existing method. The proposed implementation of SOLM as an extended SVPWM technique requires fewer computational resources and is simpler to implement compared to the existing sector identification-based approach.
2) SOLM with V/f control of an IM drive with variable dc-bus voltage for a wide range of speed variation has been demonstrated through hardware results. Existing literature on variable dc-bus voltage either concentrates on a restricted low-speed region or utilizes alternate modulation techniques at lower speeds, potentially resulting in lower efficiency. In this work, no such limitation on V/f implementation is present.
3) A detailed comparison considering V/f operation of an IM drive using the power converter shown in Fig. 1 is provided between the following:
   a) SVPWM with fixed dc-bus voltage and a variable modulation index;
   b) SVPWM with a variable dc-bus voltage and fixed modulation index; and
   c) SOLM with a variable dc-bus voltage and fixed modulation index. Enhanced efficiency with SOLM technique compared to the other two techniques is shown using experimental data.

The above-mentioned points were verified using theoretical, simulation, and hardware results. Hardware results were obtained using a laboratory-made power converter prototype with a power rating of 1.25 kVA, whose schematic is shown in Fig. 1.

The article is organized as follows. Section I provides a brief introduction to the state-of-the-art and outlines the contributions of this work. Section II provides a mathematical analysis demonstrating the equivalence of averaged pole voltages between the SVPWM and SOLM techniques. Section III discusses the proposed implementation of SOLM as an extension of the SVPWM technique. Section IV discusses the simulation and hardware results obtained in this work. Section V concludes this article.

II. DC-Bus Electrolytic Capacitor Less Inverter: SOLM and SVPWM Techniques

The circuit diagram of dc-bus electrolytic capacitor less VSI shown in Fig. 1 uses a single active bridge [17] at the input side and a three phase two level VSI at the output side. If the output side VSI is operated using SVPWM then dc-bus voltage $V_{\rm dc}$ needs to be constant and if it is operated in SOLM, the dc-bus needs to have six-pulse waveform. In this section, similarities and dissimilarities between SVPWM and SOLM are discussed. Further, this understanding is utilized to implement SOLM as an extended version of SVPWM, which retains the benefit of reduced switching loss.

Conventional SVPWM technique: In carrier and modulating signal-based implementation of SVPWM technique, the modulating signal is generated by adding a common mode signal to the three phase sinusoidal reference signals [13]. Considering a three-phase balanced set of sinusoidal voltages as given by $V_R = V_m \times \sin(\omega t)$, $V_Y = V_m \times \sin(\omega t - 2\pi/3)$, and $V_B = V_m \times \sin(\omega t + 2\pi/3)$, the space phasor of voltage ($\overrightarrow{V_{\rm ref}}$), as defined in [18], can be represented by the following equation:

$$\overrightarrow{V_{\rm ref}} = \frac{3}{2} \times V_m \times e^{j\left(\omega t - \frac{\pi}{2}\right)}. \tag{1}$$

Here, V_m is the maximum value of the fundamental frequency component of phase voltage to be produced at the inverter terminals. Using the dc-bus voltage $V_{\rm dc}$ and available switching states, $\overrightarrow{V_{\rm ref}}$ is created such that balanced set of output voltage is generated at the inverter terminals. There are eight switching states (100, 110, 010, 011, 001, 101, 000, and 111 for phases R, Y, and B, respectively), as shown in Fig. 2(a). Here, 1 represents top switch is ON and bottom switch is OFF and 0 represents bottom switch is ON and top switch is OFF, in any given phase.

Switching states of SVPWM and SOLM: In the SVPWM technique, the reference vector $\overrightarrow{V_{\rm ref}}$ is generated using two active voltage vectors and two zero voltage vectors. For example, in Sector-I, the active vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ along with the zero voltage vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ are used to create $\overrightarrow{V_{\rm ref}}$, as shown in Fig. 2(a). In case of SOLM technique only active voltage vectors are used to generate $\overrightarrow{V_{\rm ref}}$ and no zero voltage vectors are used. For example, in Sector-I only the active voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ are used as shown in Fig. 2(b). In SVPWM, the six active voltage vectors are of constant magnitude $V_{\rm dc}$, because the dc-bus voltage is constant. However, in SOLM the dc-bus is of six-pulse nature so the magnitude of dc-bus voltage keeps changing within one sector. The peak value of this six-pulse waveform is $V_{\rm dc}^{\rm max} = V_{\rm dc}^{\rm peak}$ and the minimum value is $V_{\rm dc}^{\rm min} = \sqrt{3}/2 \times V_{\rm dc}^{\rm peak}$. This upper bound and lower bound are shown as $V_1^{\rm max}$ and $V_1^{\rm min}$ for voltage vector $\overrightarrow{V_1}$ in Fig. 2(b). From Fig. 2(a), it can be observed that Sector-I is bounded by voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_0}$, and $\overrightarrow{V_7}$. Here, $\overrightarrow{V_{\rm ref}}$ is aligned with voltage vector $\overrightarrow{V_1}$ when $\omega t = \pi/2$, $\overrightarrow{V_{\rm ref}}$ is aligned with $\overrightarrow{V_2}$, when $\omega t = (5\pi/6)$. Equations of the averaged pole

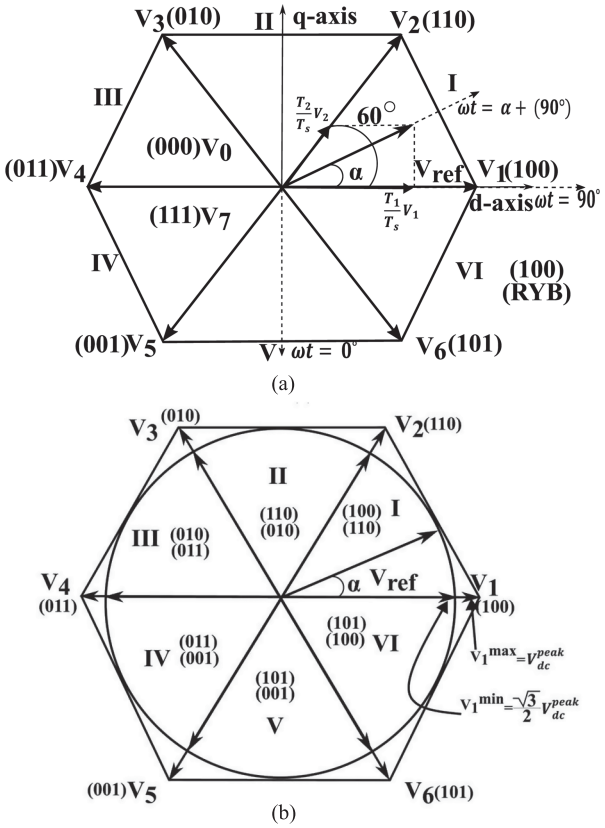


Fig. 2. Switching states of (a) SVPWM and (b) SOLM techniques.

voltages for both SVPWM and SOLM techniques are derived below when $\overrightarrow{V_{\text{ref}}}$, is in Sector-I.

Averaged pole voltage for SVPWM: The pole voltages of each phase are defined as the difference of potential between the respective mid-points of the VSI leg (R, Y, or B) and the dc-bus (O) as shown in Fig. 1. For example: The pole voltage V_{RO} is defined as the potential of "R" with respect to the potential of "O" [18]. The averaged pole voltage equation can be derived by considering the dwell times of applied voltage vectors within one switching cycle [9]. The reference voltage ($\overrightarrow{V_{\text{ref}}}$) phasor [19] is given by the following equation:

$$\overrightarrow{V_{\text{ref}}} = \overrightarrow{V_1} \times \frac{T_1}{T_s} + \overrightarrow{V_2} \times \frac{T_2}{T_s} + \overrightarrow{V_0} \times \frac{T_0}{T_s} + \overrightarrow{V_7} \times \frac{T_7}{T_s}. \quad (2)$$

Here, dwell times T_1, T_2, T_0, and T_7, for voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_0}$, and $\overrightarrow{V_7}$ are used to calculate $\overrightarrow{V_{\text{ref}}}$. Here, T_s is half of the carrier time period (T_c). The maximum magnitude of $\overrightarrow{V_{\text{ref}}}$ [20] is $\sqrt{3}/2 \times V_{\text{dc}}$.

When $\overrightarrow{V_{\text{ref}}}$ is having maximum magnitude then after taking projection on stationary d-axis, shown in Fig. 2(a), the following equation can be written as

$$\sqrt{3}/2 \times V_{\text{dc}} (\cos\alpha) \times T_s = V_{\text{dc}} \times T_1 + V_{\text{dc}} \times T_2 \times \cos(\pi/3). \quad (3)$$

Here, V_{dc} is the dc link voltage, and α is the angle between $\overrightarrow{V_{\text{ref}}}$ and d-axis. Now by projecting the reference voltage to q-axis, we obtain

$$\sqrt{3}/2 \times V_{\text{dc}} (\sin\alpha) \times T_s = V_{\text{dc}} \times \sin(\pi/3) \times T_2. \quad (4)$$

It is to be noted here $\alpha = \omega t - (\pi/2)$. On solving (3) and (4), T_1, and T_2 can be evaluated as

$$T_1 = T_s \times (\sin(\pi/3 - \alpha)) \quad (5)$$

$$T_2 = T_s \times (\sin\alpha). \quad (6)$$

The dwell times of T_0 and T_7 are equally distributed within one switching cycle considering the total zero vector period as T_Z.

Here, T_0=$T_7 = T_Z/2$ and $T_1 + T_2 + T_Z = T_s$. Averaged pole voltages ($V_{\text{RO}}^{\text{avg}}$, $V_{\text{YO}}^{\text{avg}}$, and $V_{\text{BO}}^{\text{avg}}$) within one switching cycle [9] are given by (7)–(9) as

$$V_{\text{RO}}^{\text{avg}} = \left[\frac{V_{\text{dc}}}{2}\left[\frac{T_1 + T_2}{T_s}\right]\right] \quad (7)$$

$$V_{\text{YO}}^{\text{avg}} = \left[\frac{V_{\text{dc}}}{2}\left[\frac{T_2 - T_1}{T_s}\right]\right] \quad (8)$$

$$V_{\text{BO}}^{\text{avg}} = -\left[\frac{V_{\text{dc}}}{2}\left[\frac{T_1 + T_2}{T_s}\right]\right]. \quad (9)$$

Pole voltages: Equation of averaged pole voltages for $\pi/2 < \omega t \leq 5\pi/6$ are calculated from (5)–(9). Also using $\alpha = \omega t - \pi/2$, the result can be represented as shown in the following equation:

$$\left.\begin{aligned} V_{\text{RO}}^{\text{avg}} &= \left(\tfrac{V_{\text{dc}}}{2}\right) \times \sin\left(\left(\tfrac{\pi}{3}\right) + \alpha\right) \\ V_{\text{YO}}^{\text{avg}} &= \left(\tfrac{\sqrt{3}}{2}\right) V_{\text{dc}} \times \sin\left(\alpha - \left(\tfrac{\pi}{6}\right)\right) \\ V_{\text{BO}}^{\text{avg}} &= -\left(\tfrac{V_{\text{dc}}}{2}\right) \times \sin\left(\left(\tfrac{\pi}{3}\right) + \alpha\right) \end{aligned}\right\}. \quad (10)$$

Line Voltages: Average pole voltages in (10) are used to calculate the line voltages ($V_{\text{RY}}^{\text{avg}}$, $V_{\text{YB}}^{\text{avg}}$, and $V_{\text{BR}}^{\text{avg}}$) as shown in the following equation:

For $\pi/2 < \omega t \leq 5\pi/6$

$$\left.\begin{aligned} V_{\text{RY}}^{\text{avg}} &= V_{\text{RO}}^{\text{avg}} - V_{\text{YO}}^{\text{avg}} = (V_{\text{dc}}) \times \sin\left(\left(\tfrac{\pi}{3}\right) - \alpha\right) \\ V_{\text{YB}}^{\text{avg}} &= V_{\text{YO}}^{\text{avg}} - V_{\text{BO}}^{\text{avg}} = (V_{\text{dc}}) \times (\sin(\alpha)) \\ V_{\text{BR}}^{\text{avg}} &= V_{\text{BO}}^{\text{avg}} - V_{\text{RO}}^{\text{avg}} = -(V_{\text{dc}}) \times \sin\left(\left(\tfrac{\pi}{3}\right) + \alpha\right) \end{aligned}\right\}. \quad (11)$$

Phase Voltages: The fundamental component of the averaged pole voltages and the three-phase load voltages are balanced individually and no low frequency common mode current is flowing. Hence, from the point-of-view of the fundamental component it can be said that the dc-bus mid-point, O and the three-phase load neutral-point, N are at the same potential**.** Therefore, using the line voltages in (11), load phase voltages ($V_{\text{RN}}^{\text{avg}}$, $V_{\text{YN}}^{\text{avg}}$, and $V_{\text{BN}}^{\text{avg}}$) can be expressed as shown in the following equation:

For $\pi/2 < \omega t \leq 5\pi/6$

$$\left.\begin{aligned} V_{\text{RN}}^{\text{avg}} &= \frac{\left(V_{\text{RY}}^{\text{avg}} - V_{\text{BR}}^{\text{avg}}\right)}{3} = \left(\tfrac{V_{\text{dc}}}{\sqrt{3}}\right) \times \sin\left(\tfrac{\pi}{2} + \alpha\right) \\ V_{\text{YN}}^{\text{avg}} &= \frac{\left(V_{\text{YB}}^{\text{avg}} - V_{\text{RY}}^{\text{avg}}\right)}{3} = \left(\tfrac{V_{\text{dc}}}{\sqrt{3}}\right) \times \sin\left(\alpha - \left(\tfrac{\pi}{6}\right)\right) \\ V_{\text{BN}}^{\text{avg}} &= \left(V_{\text{BR}}^{\text{avg}} - V_{\text{YB}}^{\text{avg}}\right)/3 = -\left(\tfrac{V_{\text{dc}}}{\sqrt{3}}\right) \times \sin\left(\left(\tfrac{\pi}{6}\right) + \alpha\right) \end{aligned}\right\}. \quad (12)$$

Averaged pole voltage for SOLM: In case of SVPWM the dc-bus voltage is constant and in SOLM dc-bus voltage changes within a sector, therefore equation for V_{dc} is necessary to find expression for average value of pole voltage. While using SOLM in Sector-I, R-phase top switch and B-phase bottom switch remain ON continuously, which can be understood from Fig. 2(b). In Sector-I, switching happens only in Y-phase. As R and B phase switches are clamped so dc-bus voltage $V_{\text{dc}} = V_{\text{RB}}$, in

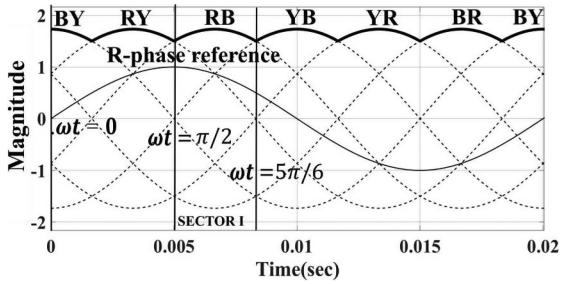


Fig. 3. Position of Sector-I with respect to six-pulse reference waveform.

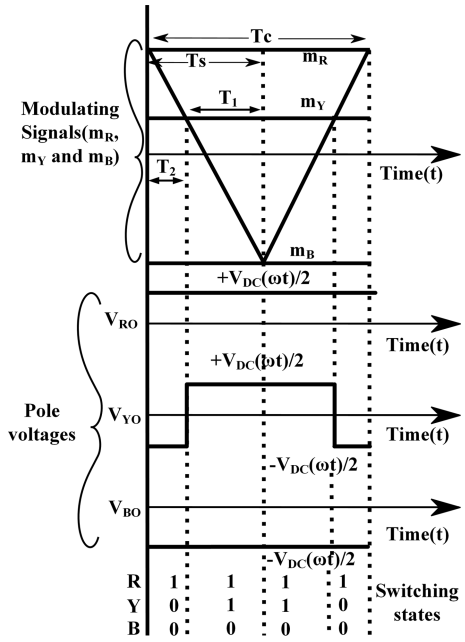


Fig. 4. Switching states and pole voltages for SOLM technique in Sector-I.

Sector-I. Now, the six-pulse reference for the dc-bus is generated from the three balanced unit magnitude sinusoidal references. Subsequently corresponding line signals are produced from these three reference signals. At a given instant the maximum among all possible six-line reference signals is chosen as the six-pulse dc-bus reference waveform. These key waveforms are shown in Fig. 3 and the six-pulse reference is traced in bold. This reference waveform is used for closed-loop control of the dc-bus voltage via Stage-1 of the power converter shown in Fig. 1. From Fig. 3, it can also be observed that for $\pi/2 < \omega t \leq 5\pi/6$, that is in Sector-I, dc-bus reference is the line reference RB. If unit magnitude R-phase reference follows $\sin(\omega t)$, then the line voltage, $V_{\mathrm{RB}} = \sqrt{3} \times V_m \times \sin(\omega t - \pi/6)$. Considering $\sqrt{3} \times V_m = V_{\mathrm{dc}}^{\mathrm{peak}}$ and $\alpha = \omega t - (\pi/2)$ in Sector-I, the expression for dc-bus voltage can be written as

$$V_{\mathrm{dc}}(\omega t) = V_{\mathrm{dc}}^{\mathrm{peak}} \times \sin(\alpha + (\pi/3)) \tag{13}$$

where V_m is the Maximum value of the required phase voltage $= \sqrt{2} \times V_p$ and V_p =RMS value of the required phase voltage.

Pole voltages: Averaged pole voltages can now be calculated using dwell times from Fig. 4. The dwell time for $\overrightarrow{V_1}$ is T_1, and for $\overrightarrow{V_2}$ it is T_2. Here, no zero vectors are present and $T_1 + T_2 = T_s$. Therefore, for $\pi/2 < \omega t \leq 5\pi/6$, the averaged pole voltages ($V_{\mathrm{RO}}^{\mathrm{avg}}$, $V_{\mathrm{YO}}^{\mathrm{avg}}$, and $V_{\mathrm{BO}}^{\mathrm{avg}}$) can be written as shown in the following equation:

$$\left.\begin{aligned} V_{\mathrm{RO}}^{\mathrm{avg}} &= \frac{V_{\mathrm{dc}}(\omega t)}{2} = \frac{V_{\mathrm{dc}}^{\mathrm{peak}}}{2} \times \sin(\alpha + (\tfrac{\pi}{3})) \\ V_{\mathrm{YO}}^{\mathrm{avg}} &= \frac{V_{\mathrm{dc}}(\omega t)}{2} \left[\frac{T_2 - T_1}{T_s}\right] = \frac{\sqrt{3} V_{\mathrm{dc}}^{\mathrm{peak}}}{2} \times \sin(\alpha - (\tfrac{\pi}{6})) \\ V_{\mathrm{BO}}^{\mathrm{avg}} &= \frac{-V_{\mathrm{dc}}(\omega t)}{2} = -\frac{V_{\mathrm{dc}}^{\mathrm{peak}}}{2} \times \sin(\alpha + (\tfrac{\pi}{3})) \end{aligned}\right\}. \tag{14}$$

Line voltage: Averaged line voltages ($V_{\mathrm{RY}}^{\mathrm{avg}}$, $V_{\mathrm{YB}}^{\mathrm{avg}}$, and $V_{\mathrm{BR}}^{\mathrm{avg}}$) across the loads are calculated by the averaged pole voltages using (14) as follows:

For $\pi/2 < \omega t \leq 5\pi/6$

$$\left.\begin{aligned} V_{\mathrm{RY}}^{\mathrm{avg}} &= V_{\mathrm{RO}}^{\mathrm{avg}} - V_{\mathrm{YO}}^{\mathrm{avg}} = V_{\mathrm{dc}}^{\mathrm{peak}} \times \sin((\tfrac{\pi}{3}) - \alpha) \\ V_{\mathrm{YB}}^{\mathrm{avg}} &= V_{\mathrm{YO}}^{\mathrm{avg}} - V_{\mathrm{BO}}^{\mathrm{avg}} = V_{\mathrm{dc}}^{\mathrm{peak}} \times \sin(\alpha) \\ V_{\mathrm{BR}}^{\mathrm{avg}} &= V_{\mathrm{BO}}^{\mathrm{avg}} - V_{\mathrm{RO}}^{\mathrm{avg}} = -V_{\mathrm{dc}}^{\mathrm{peak}} \times \sin((\tfrac{\pi}{3}) + \alpha) \end{aligned}\right\}. \tag{15}$$

Phase voltage: The averaged load phase voltages can be calculated from the averaged line voltages using (15), based on the logic provided for the derivation of (12) from (11)

For $\pi/2 < \omega t \leq 5\pi/6$

$$\left.\begin{aligned} V_{\mathrm{RN}}^{\mathrm{avg}} &= \frac{V_{\mathrm{RY}}^{\mathrm{avg}} - V_{\mathrm{BR}}^{\mathrm{avg}}}{3} = \frac{V_{\mathrm{dc}}^{\mathrm{peak}}}{\sqrt{3}} \times \sin(\tfrac{\pi}{2} + \alpha) \\ V_{\mathrm{YN}}^{\mathrm{avg}} &= \frac{V_{\mathrm{YB}}^{\mathrm{avg}} - V_{\mathrm{RY}}^{\mathrm{avg}}}{3} = \frac{V_{\mathrm{dc}}^{\mathrm{peak}}}{\sqrt{3}} \times \sin(\alpha - (\tfrac{\pi}{6})) \\ V_{\mathrm{BN}}^{\mathrm{avg}} &= \frac{V_{\mathrm{BR}}^{\mathrm{avg}} - V_{\mathrm{YB}}^{\mathrm{avg}}}{3} = -\frac{V_{\mathrm{dc}}^{\mathrm{peak}}}{\sqrt{3}} \times \sin(\alpha + (\tfrac{\pi}{6})) \end{aligned}\right\}. \tag{16}$$

It can be observed that (10) and (14) are similar, indicating that the averaged pole voltages are the same for SVPWM and SOLM in Sector-I. Same analysis can be extended for all six sectors. So, the low frequency content in the pole voltages is the same for SOLM and SVPWM in a fundamental cycle. Therefore, the line voltages and load phase voltages are also same, which can be understood from (11), (12), (15), and (16). However, the low-frequency content in line and phase voltages are comprised of only the fundamental frequency component.

For SVPWM technique the dc-bus (V_{dc}) voltage required to produce the desired line voltage can be calculated by considering maximum value of $\overrightarrow{V_{\mathrm{ref}}}$, which is $|\overrightarrow{V_{\mathrm{ref}}}| = \sqrt{3}/2 \times (V_{\mathrm{dc}}) = 3/2 \times (V_m)$ [21]. Therefore, ideally required value of dc-bus voltage for SVPWM is $V_{\mathrm{dc}} = \sqrt{3} \times V_m$, which is equal to peak of the voltage. For SOLM technique, peak of 6-pulse dc-bus voltage ($V_{\mathrm{dc}}^{\mathrm{peak}}$) = peak of line voltage. Hence, it can be said that $V_{\mathrm{dc}}^{\mathrm{peak}}$ in SOLM is same in magnitude as that of V_{dc} in SVPWM under ideal operating conditions as in (13). However, the dc-bus voltage can be adjusted to enhance efficiency. V/f control of IM requires a supply voltage with a variable magnitude and variable frequency. This can be obtained by either varying the dc-bus voltage and having a fixed modulation index or by having a fixed dc-bus voltage and varying the modulation index. The dc-bus voltage required for SVPWM with fixed modulation index can be obtained using the following equation:

$$V_{\mathrm{dc}} = \sqrt{3} \times \frac{f_r}{f_{sr}} \times V_m = \sqrt{6} \times \frac{f_r}{f_{sr}} \times V_p \tag{17}$$

where f_r is the required supply frequency and f_{sr} is the rated synchronous frequency = 50 Hz.

In the case of SOLM, the dc-bus voltage exhibits a six-pulse profile that fluctuates between a maximum ($V_{\mathrm{dc}}^{\mathrm{max}}$) and a minimum ($V_{\mathrm{dc}}^{\mathrm{min}}$) value as defined by (18) and (19), respectively

$$V_{\mathrm{dc}}^{\mathrm{max}} = \sqrt{3} \times \frac{f_r}{f_{sr}} \times V_m = \sqrt{6} \times \frac{f_r}{f_{sr}} \times V_p \tag{18}$$

TABLE I
THEORETICAL VALUES OF DC-BUS VOLTAGE REQUIRED FOR A 415 V/50 HZ IM AT VARIOUS FREQUENCIES

SOLM with Variable six-pulse DC-bus voltage				SVPWM with Variable DC-bus voltage		SVPWM with fixed DC-bus voltage	
Frequency (Hz)	Modulation Index	Maximum DC-bus voltage (V)	Minimum DC-bus voltage (V)	Modulation Index	Average DC-bus voltage (V)	Modulation Index	Average DC-bus voltage (V)
10	Fixed at max. value	113.2	98	Fixed at max. value	113.2	0.23	566
30	Fixed at max. value	339.6	294.1	Fixed at max. value	339.6	0.69	566
50	Fixed at max. value	566	490.17	Fixed at max. value	566	1.15	566

$$V_{\text{dc}}^{\min} = \frac{\sqrt{3}}{2} \times \frac{f_r}{f_{sr}} \times V_{\text{dc}}^{\max}. \tag{19}$$

For an IM rated at 400-V line voltage with a supply frequency (f_r) of 50 Hz, Table I provides the ideal dc bus voltages necessary to achieve an output voltage that is proportional to the corresponding frequency so as to maintain a constant V/f ratio, at three different frequencies. It can be inferred from Table I that for lower values of supply frequency, the required dc-bus voltage also reduces proportionately for the proposed implementation of SOLM technique with a variable dc-bus. Reducing the dc-bus voltage during low-speed operation of the IM can result in decreased switching losses in the VSI. In this work, we have utilized SOLM and SVPWM for generation of three-phase balanced sinusoidal voltages, considering a balanced load such as three-phase IM. However, SVPWM has multiple applications requiring nonsinusoidal voltage [22], unbalanced voltage [23], and unbalanced loading conditions [24]. The use of SOLM for generation of nonsinusoidal and unbalanced voltages is an area of research, which is yet to be explored.

The converter depicted in Fig. 1 is suitable for achieving fast changes in the dc-bus voltage due to its small capacitance at the dc-bus. The values of the dc-bus voltage provided in Table I are obtained by neglecting the effects of deadtime and device voltage drops while operating within a linear modulation range. As the average pole voltages are the same for SVPWM and SOLM, therefore SOLM can be implemented as an extended version of SVPWM via carrier and modulating signal-based method, which is proposed in Section III.

III. PROPOSED MODULATION SCHEME

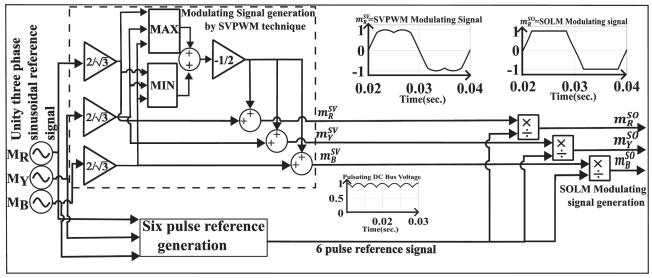
In carrier based PWM technique, if R-phase modulating signal is $m_R(\omega t)$ and dc-bus voltage is $V_{\text{dc}}(\omega t)$ [20], then the averaged pole voltage can be represented as

$$V_{\text{RO}}^{\text{avg.}}\ (\omega t) = m_R\ (\omega t) \times V_{\text{dc}}\ (\omega t)\ /2. \tag{20}$$

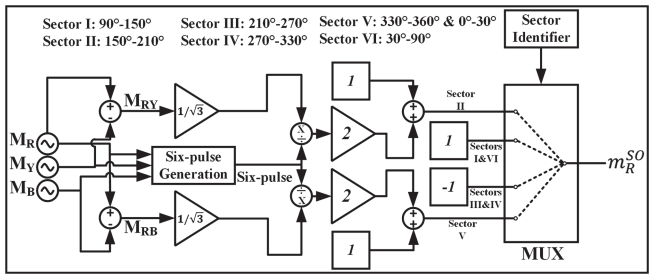
Equation (20) is valid when the time period of the modulating signal and dc-bus waveforms are very large in comparison to the carrier time period T_c in the linear modulation range. It can be extended for other phases of a three-phase VSI. Assuming $m_R^{\text{SV}}(\omega t)$ as R-phase modulating signal for SVPWM and $m_R^{\text{SO}}(\omega t)$ as R-phase modulating signal for SOLM, it can be written as

$$m_R^{\text{SV}}\ (\omega t) \times V_{\text{dc}}^{\text{SV}} = m_R^{\text{SO}}\ \ (\omega t) \times V_{\text{dc}}^{\text{SO}}\ (\omega t)\,. \tag{21}$$

Here, $V_{\text{dc}}^{\text{SV}}$ = Constant dc-bus voltage required for SVPWM and $V_{\text{dc}}^{\text{SO}}(\omega t)$ = Six pulse dc-bus voltage required for SOLM.



(a)



(b)

Fig. 5. Block diagram for the generation of (a) three-phase modulating signal (m_R^{SO}, m_Y^{SO}, and m_B^{SO}) for SOLM as an extended SVPWM technique; (b) R-phase modulating signal (m_R^{SO}) for SOLM using sector identification-based approach.

Hence, the modulating signal for SOLM $m_R^{\text{SO}}(\omega t)$ can be expressed as

$$m_R^{\text{SO}}\ (\omega t) = \frac{m_R^{\text{SV}}\ (\omega t)}{\left(V_{\text{dc}}^{\text{SO}}\ (\omega t)\ /V_{\text{dc}}^{\text{SV}}\right)}\,. \tag{22}$$

From discussion in Section II, $V_{\text{dc}}^{\text{SO}}(\omega t)/V_{\text{dc}}^{\text{SV}} = V_{\text{dc}}^{\text{6pulse}}\ (\omega t)$ in per unit. Therefore, it can be written as in the following equation:

$$m_R^{\text{SO}}\ (\omega t) = \frac{m_R^{\text{SV}}\ (\omega t)}{V_{\text{dc}}^{\text{6pulse}}\ (\omega t)}\,. \tag{23}$$

Equation (23) indicates that modulating signal for SOLM can be implemented directly by dividing SVPWM modulating signal waveform by per unit six pulse reference waveform. It can also be implemented for other phases in a similar manner.

Block diagram for implementation of this proposed method is shown in Fig. 5(a). Fig. 5(a) illustrates the generation of modulating signal of all the three-phases (m_R^{SO}, m_Y^{SO}, and m_B^{SO}) using the extended SVPWM based approach, while Fig. 5(b)

TABLE II
COMPARISON OF MATHEMATICAL OPERATIONS INVOLVED IN SECTOR-BASED AND EXTENDED SVPWM-BASED SOLM IMPLEMENTATIONS

	SOLM using Sector Identification	SOLM as an Extended SVPWM
Additions/Subtractions	12	4
Multiplications	6	3
Divisions	6	3
Six-pulse Generation Algorithm	Required	Required
Sector-identification Algorithm	Required	Not-Required
Max/Min Algorithm	Not-Required	Required
Processing Time (μs)	4.315	2.32

shows the generation of the same for one phase (m_R^{SO}) using sector identification-based approach. There are various ways to implement SOLM using sector identification [4], [5], [6], [7], [8], [9], [10]. However, the implementation shown in Fig. 5(b) follows the conventional approach, utilizing the modulating signal values for each of the six-sectors of a six-pulse, as described in [7]. From Fig. 5(a) and (b), it can be inferred that the sector identification-based approach requires more computational effort compared to the extended SVPWM-based approach as it involves significantly more mathematical operations. Table II outlines the mathematical operations necessary for implementing sector identification and extended SVPWM-based SOLM implementation. The sector identification based SOLM implementation also requires a sector identification algorithm. The sector identifier block provides information about the currently selected sector and determines the output of the 4:1 multiplexer for that given sector. The processing time required by the microcontroller for generation of three-phase SOLM modulating signals using the SVPWM technique was measured to be 2.32 μs, compared to 4.315 μs using the sector-identification approach as given in Table II. This was obtained using the "hardware profiler" feature of MATLAB 2024b [25].

IV. RESULTS AND DISCUSSION

Validity of the proposed modulation technique is verified through simulation and experimental results and these are discussed below.

A. Simulation Results

Simulation is carried out in MATLAB SIMULINK (2021(b)) for SVPWM, existing sector-based SOLM and the proposed SOLM technique for the converter shown in Fig. 1. The block diagram implementation of the control techniques used here are demonstrated in Fig. 6 as discussed later in "Hardware Results".

Fig. 7(a) and (b) shows the waveforms for SVPWM and existing sector-based SOLM techniques. It can be observed that the averaged pole voltage for both techniques is the same, which validates (21). However, dc-bus voltage, modulating signal, and instantaneous pole voltages differ for both the modulation techniques, as observed in Fig. 7. Therefore, the proposed implementation of SOLM technique can be carried out using (23).

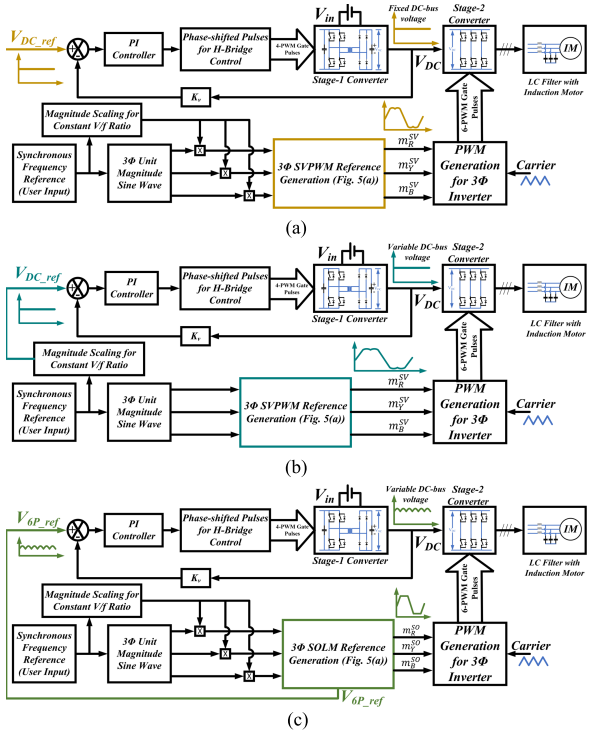
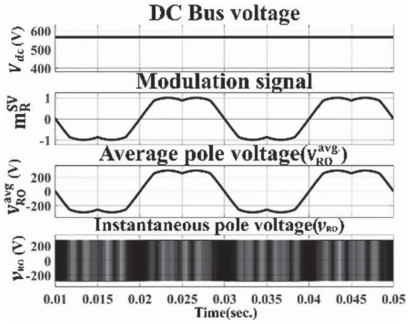


Fig. 6. Block diagram of the converter and its control for: (a) SVPWM with fixed DC-bus voltage; (b) SVPWM with variable DC-bus voltage; and (c) SOLM with variable DC-bus voltage.

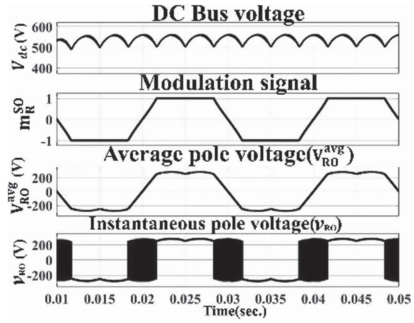
B. Hardware Results

A prototype of 1.25-kVA dc-bus electrolytic capacitor-less VSI, as shown in Fig. 1, has been developed for experimental verification. A nominal value of 48 V is applied at the input from a programmable dc power supply (APLAB 6040). The closed-loop controlled Stage-1 H-bridge converter is operated at a switching frequency of 100 kHz while the carrier frequency of Stage-2 load side three-phase VSI is 10 kHz. The control logic and gate pulse generation have been implemented using TMS320F28379D microcontroller. A bank of *LC* filters with a cut-off frequency of 890 Hz, are connected at the VSI terminals to absorb the switching frequency component. The filter capacitors are connected in star connection. Because of these low-pass *LC* filters, the output voltage and current waveforms have low THD resulting in insignificant current ripple passing through the motor, which leads to low motor torque ripple [24]. The details of the components used to develop the experimental setup are given in Table III. The converter was operated with two different types of loads: 1) a star-connected three-phase balanced resistive load and 2) a 1-hp three-phase IM. The hardware results obtained with the three-phase balanced resistive load have been given in Figs. 8 and 9. The same converter is subsequently employed to run a 1-hp IM drive using constant V/f control at different operating frequencies, in order to test and validate its performance with a variable dc-bus voltage.

The tests conducted with a three-phase resistive load are used to verify the theoretical and simulation results obtained using both SVPWM and SOLM. The results in Fig. 8, with a three-phase resistive load, show the waveforms of the dc-bus voltage (V_{DC}) at the top, the average pole voltage (V_{RO}^{avg}) in the middle and the R-phase modulating signal (m_R) at the bottom. The

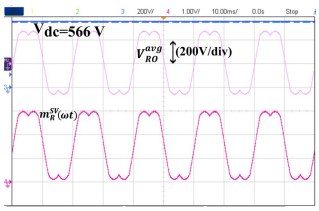


(a)

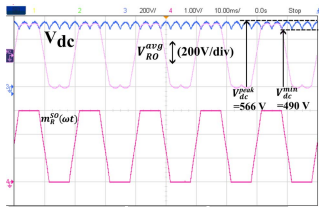


(b)

Fig. 7. Comparison of DC-bus voltage, R phase modulating signal, averaged pole voltage, and the pole voltage for (a) SVPWM and (b) SOLM technique.



(a)



(b)

Fig. 8. DC-bus voltage (V_{dc}), modulating signal (m_R) and averaged pole voltage (V_{RO}^{avg}) for (a) SVPWM and (b) SOLM technique.

R-phase modulating signal (m_R) is obtained from the digital-to-analog converter (DAC) output of the micro-controller, whereas the average of the pole voltage (V_{RO}^{avg}) cannot be directly obtained from the experimental setup. Hence, V_{RO}^{avg} is obtained using (20) by programming the math functions feature of the oscilloscope (Keysight DSO-X 3024T) as explained below.

Since the DAC output of the micro-controller is unipolar, ranging from 0 to 3 V, the following equation is programmed into DSO to obtain V_{RO}^{avg}:

$$V_{RO}^{avg} = (0.5 \times \text{channel\_1}) \times (A \times \text{channel\_2} + B). \quad (24)$$

Here, gain A is equal to 2/3 and offset B is equal to -1.

From Fig. 8, it can be observed that the waveform V_{RO}^{avg} is the same for both the modulation techniques. However, waveforms of the dc-bus voltage (V_{DC}) and the modulating signals are different. This observation validates the theoretical aspect given in (23) and corroborates the simulation results shown in Fig. 7.

Fig. 9 shows the results obtained with a three-phase resistive load at the rated condition with the RMS output phase voltage (v_{RN}) equal to 230 V. Fig. 9(a), (c), and (e) displays the results obtained using SVPWM, while Fig. 9(b), (d), and (f) present the

TABLE III
MAJOR COMPONENTS OF PROTOTYPE

Components	Parameters
H-bridge side MOSFET switches (M_{11}–M_{14})	CSD1953KCS 100 V,133 A, $R_{ds,on}$=3.1 mΩ, TO220 Package
Secondary Schottky diodes (D_{21}–D_{24})	UJ3D1210K2, 1200 V, 10 A, TO247-2
IGBT-based Inverter switches (S_1–S_6)	SEMIX10IG128Ds,1200 V, 25 A IGBT; Six-pack device in SEMITOP package
HF Transformer	Number of Ferrite Toroidal cores=10 (B64290L0048X087), Turns ratio=1:16 Leakage Inductance = 0.9 μH (Referred to Primary)
Filter capacitor	C_F =8 μF, 440 V AC capacitor
DC-bus film capacitor	C=3.3 μF, 1000 V Film capacitor
Filter inductor	L_F=4 mH, Ferromagnetic core
IM	1 hp, 415 V, 1.97 A, 50 Hz, 1425 r/min
Voltage Sensors	Keysight N2791A (25 MHz) and Yokogawa 700924 (100 MHz)
Current Sensors	Keysight N2782B (30 A/50 MHz)

results obtained using the proposed implementation of SOLM as an extension of SVPWM. Fig. 9(a) and (b) shows the waveforms of the dc-bus voltage (V_{DC}), the modulating signal ($m_R(\omega t)$), the inverter line voltage (v_{RY}) and the filtered output load phase voltages (v_{RN}) for SVPWM and SOLM, respectively. From Fig. 9(a) and (b), it can be observed that the line voltage (v_{RY}) is clamped to dc-bus voltage (V_{DC}) for 120° i.e., 1/3rd of the fundamental cycle while using SOLM technique. Fig. 9(c) and (d) show the DC-bus voltages (V_{DC}), the FFT analysis of the pole voltages (v_{RO}), the pole voltages (v_{RO}) and the load phase voltages (v_{RN}) for SVPWM and SOLM, respectively. Frequency spectrum analysis is performed on the pole voltage using the DSO. It is observed from Fig. 9(c) and (d) that at 10 kHz, the maximum value of the switching harmonic component present in the pole voltage waveform is 54.14 V for SOLM and 80 V for SVPWM. From Fig. 9(d), it can be observed that the pole voltage (v_{RO}) is also clamped for 2/3rd of the fundamental cycle while using the SOLM technique. This indicates a reduction in switching loss by 66% compared to the SPWM technique. Fig. 9(e) and (f) shows the FFT analysis of the filtered output phase voltage of one phase for SVPWM and SOLM, respectively. The THD of the load phase voltage (v_{RN}) was found to be 0.62% with SVPWM and 0.71% with SOLM. Thus, the results shown in Figs. 8 and 9 demonstrate that SOLM can be successfully implemented as an extension of the SVPWM technique. In addition, the SOLM technique can enhance the efficiency compared to SVPWM and generate lower switching frequency harmonics in the pole voltage. The behavior of the converter under a step load change is shown in Fig. 10. It shows the waveforms of the dc-bus voltage (V_{DC}), line voltage (v_{RY}), phase voltage (v_{RN}), and the R-phase current (i_R) under the condition of step load change. At the instance of step change there is a step increase in the load current as expected and the

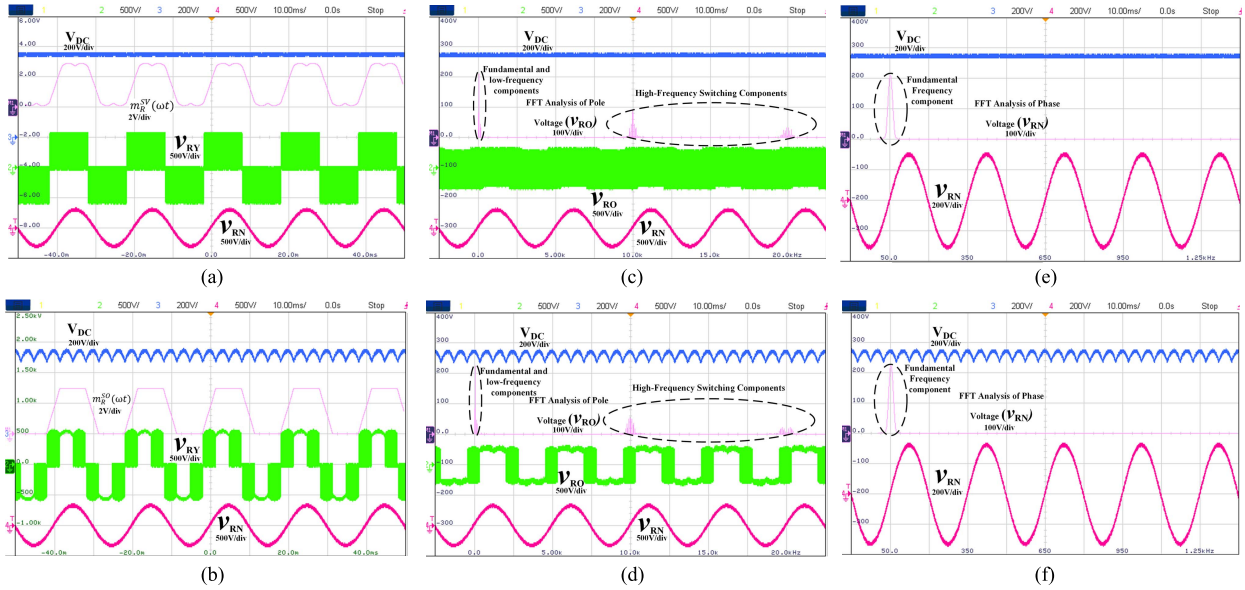


Fig. 9. (a) and (b) DC-bus voltage ($V_{\rm dc}$), modulating signal (m_R), line voltage ($v_{\rm RY}$) and load phase voltage ($v_{\rm RN}$) for SVPWM and the proposed SOLM techniques respectively, Fig. 8(c) and (d) shows the frequency spectrum analysis of pole voltages ($v_{\rm RO}$) for SVPWM and the proposed SOLM techniques respectively, while Fig. 8(e) and (f) shows the frequency spectrum analysis of output phase voltages ($v_{\rm RN}$) obtained with SVPWM (THD = 0.62%) and the proposed SOLM operation (THD = 0.71%) at rated condition (f_r = 50 Hz) with $f_{\rm sw(VSI)}$ = 10 kHz.

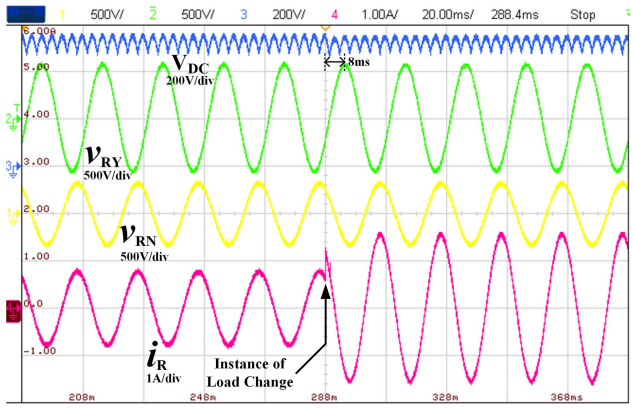


Fig. 10. Waveforms of DC-bus voltage ($V_{\rm DC}$), motor input line voltage ($v_{\rm RY}$), phase voltage ($v_{\rm RN}$), and motor line current (i_R) during step change in resistive load.

dc-bus voltage also exhibits a small drop which is recovered in 8 ms. The initial total power consumption of the load, which was 387 W, increased to 774 W following the step change.

Second set of experiments were carried out by using a 1-hp three-phase IM as a load. The IM was controlled using open-loop V/f control, which requires a VVVF supply. Since the converter used here has a small capacitance (3.3 μF) at the dc-bus, it can achieve rapid changes in the dc-bus voltage waveform. This ability to vary the dc-bus voltage can be used to achieve VVVF operation of an IM drive. This has been achieved using the following three-methods:

1) SVPWM with fixed dc-bus voltage and a variable modulation index,
2) SVPWM with a variable dc-bus voltage and fixed modulation index, and
3) SOLM with a variable six-pulse dc-bus voltage and fixed modulation index.

The block diagram implementation of SVPWM with fixed dc-bus voltage for V/f control of IM is shown in Fig. 6(a). The dc-bus voltage in this case has a constant dc profile whose magnitude is fixed at 566 V using the Stage-1 closed-loop control. The magnitude and frequency of the SVPWM modulating signal is varied to obtain V/f control of IM from a fixed dc-bus. In the second method, the magnitude of the dc-bus voltage is varied as per the required motor supply frequency, given in (17). Now, using the closed-loop control of Stage-1, as shown by the block diagram of Fig. 6(b), the dc-bus voltage is regulated as per the supply frequency. Here, the modulation index is kept constant but the frequency of the modulating signal is varied along with the variable dc-bus voltage for achieving constant V/f ratio. The block diagram implementation of V/f control using SOLM with variable six-pulse dc-bus voltage is shown in Fig. 6(c). The dc-bus in this case has a six-pulse profile with variable magnitude. The six-pulse dc-bus is regulated by Stage-1 closed-loop control, with its magnitude and frequency adjusted according to the required supply frequency, as defined by (18) and (19). The generation of modulating signals for SOLM is explained by the block diagram of Fig. 5(a). The SOLM modulating signals are utilized to generate PWM pulses for controlling the switches of Stage-2 three-phase VSI. The experimental results with IM drive are given in Figs. 11–14, and Table IV.

In the results depicted in Fig. 11, the motor operates in constant V/f mode at various frequencies under SOLM with variable dc-bus voltage. Here, the six pulse reference waveform of $V_{\rm DC}$ is varied dynamically as the motor starts under constant V/f mode. The closed loop control of the dc-bus voltage ensures that $V_{\rm DC}$ follows the reference waveform. The dc-bus voltage required for various frequencies have been obtained using (17), (18), and (19) as given in Table I with 50 Hz as the rated operating frequency. The waveforms of dc-bus voltage ($V_{\rm DC}$), motor line voltage ($v_{\rm RY}$), motor line current (i_R), and the motor speed (N_R) at supply frequencies of 10, 30, and 50 Hz are shown in Fig. 11.

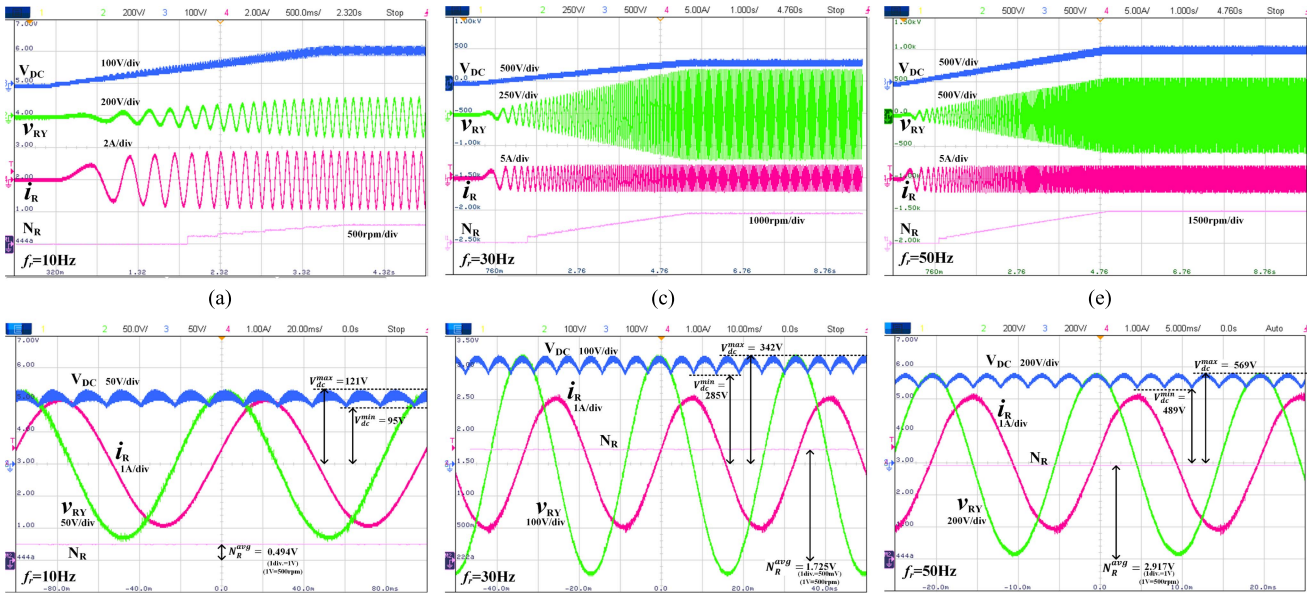


Fig. 11. DC-bus voltage (V_{DC}), motor input line voltage (v_{RY}), motor line current (i_R) and rotor speed (N_R) for: $f_r = 10$, 30, and 50 Hz during: (a), (c), and (e) starting of the motor; (b), (d), and (f) steady-state operation.

TABLE IV
OBSERVATIONS FROM: I) SVPWM WITH FIXED DC-BUS VOLTAGE AND VARIABLE MODULATION INDEX; II) SVPWM WITH VARIABLE DC-BUS VOLTAGE; III) SOLM WITH VARIABLE SIX-PULSE DC-BUS VOLTAGE

Synchronous frequency (Hz)	I_{THD} (%)	V_{THD} (%)	Operating speed (r/min)	Synchronous speed (r/min)	Average DC-bus voltage (V)	DC-bus power (W)	Output power (W)	VSI Efficiency (%)	Line Voltage RMS (V)
SVPWM with Fixed DC-bus voltage and Variable Modulation Index									
10	0.90	0.91	229.845	300	563.65	155.576	132.048	84.876	68.632
20	1.03	0.54	545.35	600	563.48	260.818	239.906	91.982	144.105
30	1.06	0.42	849.25	900	563.85	364.731	341.938	93.751	219.178
40	0.91	0.37	1145.6	1200	563.05	455.872	440.488	96.625	293.567
50	0.90	0.62	1439.95	1500	563.54	555.792	541.285	97.389	371.057
SVPWM with Variable DC-bus voltage									
Synchronous frequency (Hz)	I_{THD} (%)	V_{THD} (%)	Operating speed (r/min)	Synchronous speed (r/min)	Average DC-bus voltage (V)	DC-bus power (W)	Output power (W)	VSI Efficiency (%)	Line Voltage RMS (V)
10	0.89	0.71	263.55	300	112.69	139.263	136.081	97.715	72.896
20	0.61	0.45	563.6	600	225.35	260.724	253.911	97.387	146.478
30	0.72	0.44	858.1	900	332.94	342.18	330.234	96.509	221.153
40	0.84	0.41	1158.25	1200	449.54	487	479.198	98.398	298.004
50	0.85	0.62	1456.55	1500	562.10	561.45	545.388	97.139	371.357
SOLM with Variable Six-pulse DC-bus voltage									
Synchronous frequency (Hz)	I_{THD} (%)	V_{THD} (%)	Operating speed (r/min)	Synchronous speed (r/min)	Max. DC-bus voltage (V)	Min. DC- bus voltage (V)	DC-bus power (W)	Output power (W)	VSI Efficiency (%)	Line Voltage RMS (V)
10	0.84	0.64	247.45	300	121.1	94.6	148.924	146.954	98.677	78.733
20	0.89	0.40	554.15	600	237	192	253.8	250	98.503	158.749
30	1.04	0.49	862.45	900	342	285	349.86	344.212	98.386	238.390
40	1.31	0.52	1150.45	1200	461	388	469.3	465.038	99.091	320.590
50	1.14	0.72	1458.50	1500	569	489	556	547.73	98.513	399.296

The variation in the dc-bus voltage from zero to the value required for a given frequency was successfully achieved, as shown in Fig. 11(a), (c), and (e). Gradually increasing the speed from a standstill condition also helped to ensure that the motor current (i_R) remained within its rated rms value of 1.97 A. The speed of the IM shown in Fig. 11 is obtained from the data provided by an inductive proximity sensor mounted on it. It provides a pulse once every complete rotation of the motor shaft. The frequency of this pulse was calculated in the microcontroller and then scaled to provide the corresponding motor speed. Since the speed sensor data updates only after completion of each shaft rotation, the speed data shown in Fig. 11(a), (c), and (e), during transition, is inherently discrete. Results at steady-state operation for different synchronous frequencies of the motor terminal voltage (v_{RY}) and current (i_R) waveforms are shown in Fig. 11(b), (d), and (f). To run the motor at a speed corresponding to a supply frequency of 10 Hz, the required dc-bus voltage is only 121 V. For supply frequencies of 30 and 50 Hz, the maximum dc-bus voltages are 342 and 569 V, respectively. This demonstrates the successful implementation of variable dc-bus voltage using SOLM. Reducing the dc-bus voltage for speeds below the rated value can improve efficiency compared to a fixed dc-bus voltage technique, as will be demonstrated later in this section.

A thorough comparison has been conducted between the aforementioned three methods of VSI operation for achieving open-loop V/f control of IM drive and its data is shown in Table IV. The comparison between the three methods is based on the efficiency of the three-phase VSI and the THD values of the output voltages and currents for similar values of supply frequency, dc-bus voltage, and output power. Since the VSI output voltages are filtered by a bank of *LC* filters, it is expected that the switching frequency components of current and voltage waveforms will be attenuated. Appropriate dc-bus voltage controller tuning ensures that the output voltage will not have significant low-frequency harmonic components. This is evident from current and voltage THD values shown in Table IV, which are below 1.5% and 1% respectively. The THD data was obtained using the built-in feature of the DSO. The currents and voltages were sensed using high bandwidth active probes with their part numbers given in Table III. The power values given in Table IV were derived from the measured voltage and current data. For all three methods, the VSI was tested with five different output frequencies: 10, 20, 30, 40, and 50 Hz. The efficiency of the Stage-2 three-phase VSI under the three control modes is plotted against the supply frequency, as illustrated in Fig. 12. SOLM with a variable six-pulse dc-bus voltage offers the highest efficiency, amongst the three, in the range of 98.4%–99% followed by SVPWM with a variable dc-bus voltage, which has an efficiency ranging from 97.1% to 98.4% while SVPWM with fixed dc-bus voltage offers the lowest efficiency ranging from 85% to 97.4%. This can be attributed to the fact that at lower values of dc-bus voltage, the switching loss is lower as the voltage across the switches is equal to the dc-bus voltage when the switch is OFF. Although the difference in efficiencies of SOLM and SVPWM with a variable dc-bus voltage is about 0.5%–1% but it may lead to significant energy savings in higher power converters. The efficiency improvements of SOLM over fixed dc-bus voltage SVPWM mode especially at lower speeds make this type of control suitable for variable speed drives such as solar water pumps. Using a variable dc-bus voltage can not only provide a significant improvement in the VSI efficiency

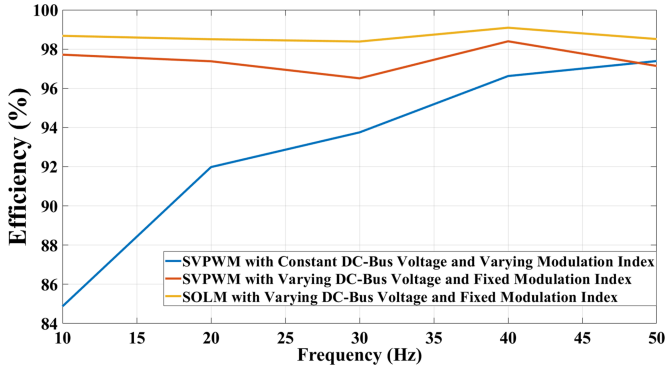


Fig. 12. Efficiency versus VSI output frequency plot for the three-modes of operation compared in Table IV.

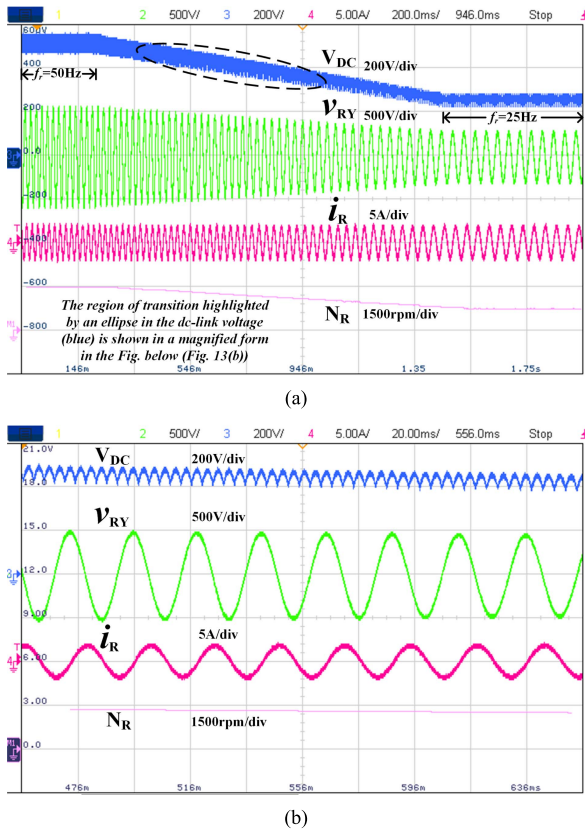


Fig. 13. DC-bus voltage (V_{DC}), motor input line voltage (v_{RY}), motor line current (i_R), and rotor speed (N_R): (a) at the steady-state value of $f_r = 50$ Hz, at transition from $f_r = 50$ to $f_r = 25$ Hz and then at $f_r = 25$ Hz. (b) Magnified version showing transition from $f_r = 50$ Hz to $f_r = 25$ Hz.

but also lead to increased lifespan of the VSI semiconductor switches [14].

Fig. 13 shows the variation of dc-bus voltage (V_{DC}), motor input line voltage (v_{RY}), motor line current (i_R), and rotor speed (N_R) when the supply frequency (f_r) to the motor changes from 50 to 25 Hz. Since this converter does not have bi-directional power flow capability, a sudden drop in motor speed can result in reverse power flow (motor to converter), which can lead to a surge in the dc-bus voltage if the converter internal resistances and the small dc-bus capacitor are unable to absorb this reverse energy. However, in this instance, there was no surge in either

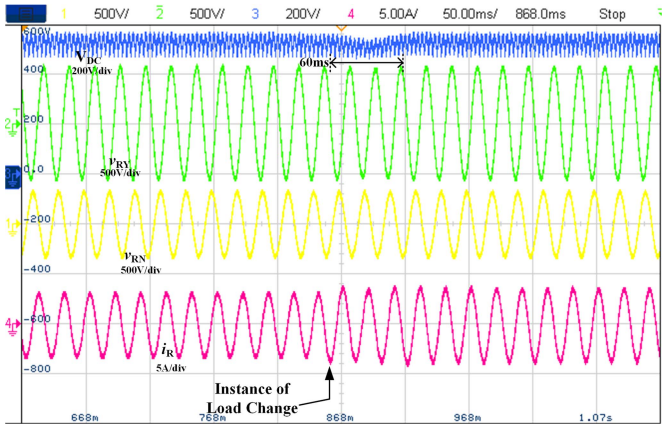


Fig. 14. Waveforms of DC-bus voltage (V_{DC}), motor input line voltage (v_{RY}), phase voltage (v_{RN}), and motor line current (i_R) showing step change in IM load.

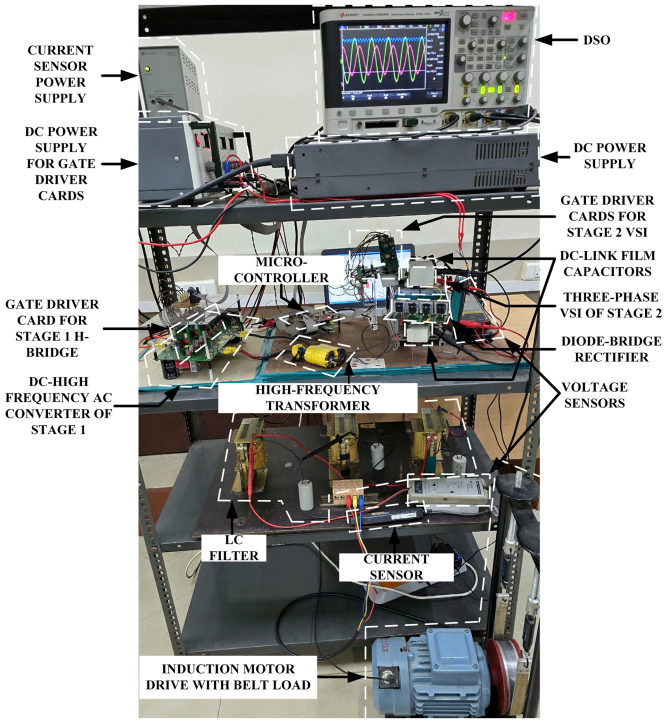


Fig. 15. Experimental setup with IM drive.

the dc-bus voltage (V_{DC}) or the motor current (i_R) during the frequency (f_r) transition from 50 to 25 Hz at a rate of -20 Hz/s. From the results shown in Figs. 11 and 13, it has been demonstrated that under acceleration, different steady-state operating speeds and deceleration of the IM, the six-pulse dc-bus voltage level and its waveform is maintained as per the requirement. Fig. 14 illustrates the converter's behavior in response to a sudden change in the load applied to the IM. This step change in motor load was achieved by abruptly increasing the load connected to a dc generator, which is mechanically coupled to the shaft of the IM. The waveform of the dc-bus voltage (V_{DC}) exhibits a slight dip in its magnitude for approximately 60 ms while the load current (i_R) shows an increase in its magnitude. The power drawn by the motor increases from 242.8 to 858.14 W during this step change. The IM coupled to a dc generator with a resistive load constitutes a higher-order system compared to a system with only resistive loads. This results in an increased transient duration with an IM and dc generator set as compared to a resistive load. Results shown in Figs. 10 and 14 also help establish the fact that this system is able to withstand abrupt changes in load despite having a small dc-bus capacitor. Fig. 15 shows the complete experimental setup used for obtaining the hardware results with appropriate labels.

V. Conclusion

The existing method of SOLM technique uses a sector identification-based approach to generate the modulating signal. SOLM has the advantage of reduced switching loss over the SVPWM technique. SVPWM technique has been in use in a myriad of applications involving both open-loop and closed-loop control of electric motors whereas for applications involving motor control, SOLM has been used in open-loop till now. The proposed implementation of SOLM as an extended SVPWM technique increases the potential of SOLM for use in areas where SVPWM is already in use. This can combine the versatility of SVPWM technique with the efficiency gains of SOLM. Considering these aspects, the contributions and findings of this work have been summarized as follows.

1) The instantaneous value of pole voltage, modulating signal, and dc-bus voltage waveforms are different between SVPWM and SOLM modulation techniques but the averaged pole voltage waveforms individually generated by these techniques are identical. This is proven by mathematical analysis and verified through experiments.
2) Based on the above-mentioned understanding, the implementation of the SOLM technique is proposed as an extension of the conventional SVPWM technique where sector-based selection is not required. It reduces the complexity of implementation.
3) Successful operation of the power converter, from low to the rated speed of IM, has been demonstrated using SOLM with open-loop V/f control of IM drive, unlike the existing methods, which either have a restricted low-speed region or utilize alternate modulation techniques at lower speeds. It is also shown that the dc-bus voltage is not affected by acceleration or deceleration of the motor.
4) A comparison between fixed dc-bus voltage using SVPWM and a variable dc-bus voltage with both SVPWM and SOLM has been provided, clearly highlighting the improvements in the efficiency of VSI using a variable dc-bus.

Based on the above-mentioned findings, the SOLM technique with a variable six-pulse dc-bus voltage can have applications in solar water pumps or light electric vehicles. In this work, SOLM's implementation as an extended SVPWM technique opens the possibility for further use of SOLM where three phase sinusoidal voltage is generated by SVPWM using a VSI. However, SVPWM can also be used for nonsinusoidal voltage generation. Therefore, the possibility to use SOLM for nonsinusoidal voltage generation can be considered as a potential field of research.

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