Gate Driver Power Supply With Low-Capacitance-Coupling and Constant Output Voltage for Medium-Voltage SiC MOSFETs

Zhixing Yan, *Graduate Student Member, IEEE*, Gao Liu, *Graduate Student Member, IEEE*, Shaokang Luan, *Member, IEEE*, Yuan Gao, Rui Wang, *Member, IEEE*, Benjamin Futtrup Kjærsgaard, *Member, IEEE*, Morten Rahr Nielsen, *Graduate Student Member, IEEE*, Bjørn Rannestad, Hongbo Zhao, *Member, IEEE*, and Stig Munk-Nielsen, *Member, IEEE*

***Abstract*—With the development of wide band-gap devices, Silicon Carbide (SiC) semiconductor devices in 10–15 kV voltage class offer potentials in medium-voltage (MV) systems. To ensure the reliable operation of these MV SiC devices, gate driver power supplies must meet specific requirements: MV isolation capability, low coupling capacitance, stable performance across fluctuating voltage potentials, and assembly convenience. This article proposes a customized gate driver power supply solution. The proposed core-series-coupling planar transformer meets the specified requirements and significantly reduces common-mode capacitance by series connection of core, while maintaining ease of manufacturing. In addition, the open-loop voltage regulator circuit model ensures precise output voltage by accounting for winding resistance and magnetizing inductance. This article presents an MV SiC gate driver that achieves a partial discharge inception voltage of 11.5 kV and the transformer exhibits a low coupling capacitance of 0.42 pF. Additionally, this article conducts a 6 kV/30 A double pulse test, demonstrating the robust performance of the gate driver even at switching speeds of 133.9 V/ns during turn-OFF and 111.6 V/ns during turn-ON transients.**

***Index Terms*—Common-mode (CM) capacitance, gate driver power supply (GDPS), medium voltage, silicon carbide (SiC).**

I. Introduction

RECENTLY, the rapid growth of the medium-voltage (MV) architecture in industrial motor drivers, supercharging stations, and data centers has led to a greater demand for MV power electronic converters (PECs) [1], [2], [3]. Thanks to the emergence of wide band-gap power devices, MV Silicon Carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) with blocking voltages ranging from 3.3 to 15 kV have attracted widespread attention, which can enable simplification of converter topology and the associated auxiliary circuits [4], [5], [6].

The MV SiC MOSFETs demonstrate ultra-fast switching speeds, with dv/dt values reaching up to 250 V/ns, resulting in significantly reduced switching losses [7]. In conventional Silicon-based PECs, minimizing parasitic inductance has been a primary concern due to the high di/dt, while relatively fewer attentions has been given to the slow dv/dt [8]. Nevertheless, due to the fast-switching characteristics of SiC power devices, the design focus for SiC-based PECs is increasingly centered on minimizing parasitic capacitive couplings [9]. These couplings can generate high-frequency capacitive displacement currents within the PEC systems, subsequently causing common-mode (CM) noise problems in low-power control signals (e.g., gate driver [10], control circuit [11], voltage/current sensors [12]).

The gate driver plays a critical role in MV SiC-based PECs [13]. Commercially available isolated gate driver power supplies for 650 V to 1.7 kV SiC MOSFETs can achieve a low coupling capacitance of around 3 pF. However, their isolation voltage is typically below 5 kV, limiting their use in MV applications. Therefore, conventional isolated gate driver power supplies and isolated gate drivers are inadequate for controlling the high-side switches due to their insufficient isolation barrier and dv/dt ruggedness [14]. As a result, customized gate drivers specifically designed for MV SiC-based PECs are essential to ensure reliable operation [15]. The diagram of the MV SiC gate driver, as depicted in Fig. 1, includes an isolated converter for powering, an optic fiber for control, and a driving stage. As shown in Fig. 1, there are four typical challenges within the gate driver.

1) *MV insulation capability:* Ensuring insulation between the driver stage and the auxiliary power supply.
2) *Low coupling capacitance:* This helps reduce the CM currents induced by high dv/dt transients.
3) *Constant output voltage:* The implementation of a closed-loop voltage regulator in the gate driver power supply (GDPS) for high-side switches presents challenges due

Received 15 July 2024; revised 24 October 2024 and 9 December 2024; accepted 15 January 2025. Date of publication 5 February 2025; date of current version 20 March 2025. This work was supported in part by MVolt Project, co-funded by AAU Energy of Aalborg University, Innovation Fund Denmark, Siemens Gamesa, Vestas Wind System, and KK Wind Solutions, and in part by TurboDriver Project, funded by Spin-outs Denmark Program. Recommended for publication by Associate Editor Y. Yan. *(Corresponding author: Hongbo Zhao.)*

Zhixing Yan, Gao Liu, Shaokang Luan, Yuan Gao, Benjamin Futtrup Kjærsgaard, Morten Rahr Nielsen, Hongbo Zhao, and Stig Munk-Nielsen are with the AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: zhya@energy.aau.dk; gaol@energy.aau.dk; slu@energy.aau.dk; yuga@energy.aau.dk; bfk@energy.aau.dk; mrni@energy.aau.dk; hzh@energy.aau.dk; smn@energy.aau.dk).

Rui Wang is with the Power Electronics Laboratory (PEL), École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: ru.wang@epfl.ch).

Bjørn Rannestad is with the KK Wind Solutions, 7430 Ikast, Denmark (e-mail: bjran@kkwindsolutions.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3538907.

Digital Object Identifier 10.1109/TPEL.2025.3538907

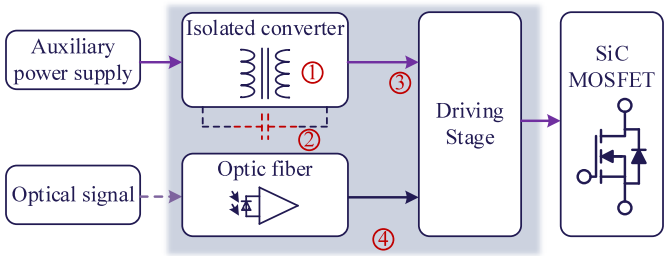


Fig. 1. Diagram of MV SiC gate driver.

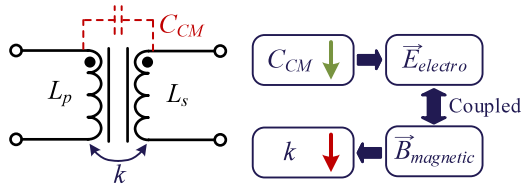


Fig. 2. Electromagnetic field coupling in a transformer.

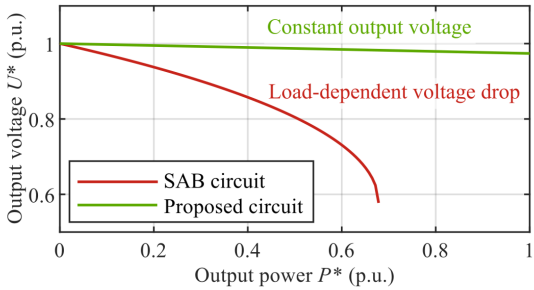


Fig. 3. Output voltages as a function of output power.

to the rapidly fluctuating voltage potentials. However, it is crucial for the GDPS to consistently maintain a constant output voltage across diverse load conditions, remaining unaffected by high dv/dt.

4) *Assembly convenience:* The design and implementation of MV insulation, along with minimizing coupling capacitance, can significantly complicate the manufacturing and assembly of transformers.

To address these challenges, improved conventional approaches [e.g., flyback [16], [17], [18], single active bridge (SAB) [19], [20]] have been put into practice. However, their power capacity remains restricted to a few watts due to the low coupling factor in the isolated transformer. To overcome this limitation, customized approaches are proposed in [21], [22], [23], [24], and [25]. Yet, the complexity of the circuit compensation network and the requirement for specialized mechanical assembly make implementation less straightforward for engineers.

This article proposes a scalable solution based on a novel core-series-coupling planar transformer to reduce CM coupling capacitance, with an open-loop voltage regulator circuit for maintaining the constant output voltage. The performance is verified through a double pulse test (DPT) setup constructed by the 10 kV SiC MOSFET power module.

The rest of this article is organized as follows. Section II formulates the research problem, discussing the challenges and the current state-of-the-art in MV SiC gate driver power supplies. In Section III, the model for the core-series-coupling planar transformer is presented, while Section IV describes the open-loop voltage regulator circuit. Comprehensive experimental verifications are provided in Section V. Finally, Section VI concludes this article.

II. Problem Formulation

With the high dv/dt introduced by SiC-based devices, the switching loss in PECs can be significantly reduced, thereby greatly improving system efficiency [26]. However, it is important to note that the magnitude of CM noise current is directly affected according to $i_{\mathrm{cm}} = C_{\mathrm{cm}}\mathrm{d}v/\mathrm{d}t$ [27]. To mitigate this CM noise, the inclusion of a low-capacitive-coupling GDPS becomes an essential component in SiC-based PEC systems.

Nonetheless, as shown in Fig. 2, when the CM capacitance changes, the electrostatic energy will inevitably be altered. Consequently, the magnetic field distribution is affected due to electromagnetic field coupling [28]. Specifically, when there is a need to reduce CM capacitance and enhance MV isolation capability, the magnetic coupling factor k diminishes [29]. Therefore, while reducing the CM capacitance, it is inevitable that higher leakage inductance will be introduced in the transformer.

The flyback converter is a common topology for GDPS. In [16], a primary-side regulated flyback converter was proposed. By strategically inserting bobbins between the transformer winding and core, the CM capacitance is reduced to only 2.6 pF [17]. However, this reduction in CM capacitance introduces high leakage inductance, leading to complexities in snubber circuit design and limitations in terms of output power handling capability [18]. To streamline circuit design, an open-loop SAB that incorporates linear and low-dropout regulators (LDOs) is developed [19]. This method effectively decouples the voltage regulator from the isolated converter, thereby simplifying the voltage regulation strategy. However, as depicted in Fig. 3, a notable challenge arises due to the load-dependent voltage drop, which is exacerbated by high leakage inductance [20]. Consequently, the converter power level is limited to a few watts.

To tackle the challenges mentioned above, two unconventional approaches are proposed: the current-fed single-turn primary winding approach [21], [22] and wireless power transfer [23], [24], [25]. The single-turn primary winding approach involves transferring power from the primary side through a high-insulation cable carrying a high-frequency current. The energy is then received by a toroidal winding on the secondary side. Wireless power transfer completely separates the primary and secondary sides of the power supply. Both techniques meet the high insulation and low coupling capacitance requirements. However, the challenge lies in the complex circuit compensation network and the need for specialized mechanical assembly, making it less straightforward for engineers to implement.

In order to meet the gate driver requirements for SiC-based PEC systems, the overall architecture of the designed gate driver

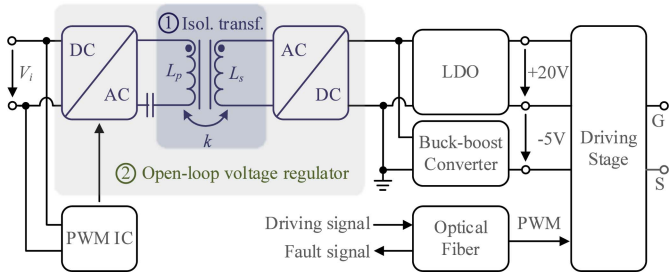


Fig. 4. Overall architecture of the designed gate driver.

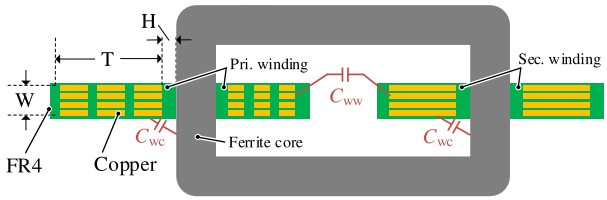


Fig. 5. Cross-section of a single-core planar transformer with parasitic capacitances.

is presented in Fig. 4. The power supply is divided into two parts: a low coupling isolated power supply to minimize interference and provide isolation, and a voltage regulation stage to ensure stable voltage for the driving circuit. Two main contributions of this article, as illustrated in Fig. 4, are outlined as follows.

1) *Designing a core-series-coupling planar transformer:* This transformer ensures MV isolation and reduces CM coupling capacitance. The precise winding-to-core distance can be controlled through PCB layout, eliminating the need of inconvenient wire winding procedures.
2) *Modeling open-loop voltage regulator circuit:* Closed-loop regulation can be challenging at GDPS due to the rapid fluctuations in output voltage potentials. The proposed model enables designers can reasonably adjust circuit parameters, ensuring a constant output voltage.

III. Modeling of the Core-Series-Coupling Planar Transformer

Planar transformers are simpler to manufacture than conventional transformers, resulting in significant cost reductions during assembly [30]. In this section, the detailed implementation of the CM capacitance model for core-series-coupling planar transformers is conducted.

A. Single-Core Planar Transformer

The cross-section of a single-core planar transformer, as shown in Fig. 5, comprises the primary winding, secondary winding, and a ferrite core. In the case of MnZn ferrite cores, the relative permittivity in the nominal frequency range is significantly high, typically ranging from 10^4 to 10^6 (for reference, the relative permittivity of air is 1.0006). This high permittivity means that the core capacitance is much larger compared to the parasitic capacitances between the windings and the core. As a result, MnZn ferrite cores are generally treated as nearly perfect electrical conductors, allowing us to consider the core capacitance as infinite [31]. Consequently, the primary-to-secondary CM capacitance can be expressed as

$$C_{\mathrm{CM.single-core}} = C_{\mathrm{wc}} // C_{\mathrm{wc}} + C_{\mathrm{ww}} \tag{1}$$

where C_{ww} is the winding-to-winding capacitance.

The detailed method for calculating parasitic capacitance in planar transformers is extensively covered in the literature [30]. The capacitance C_{wc} and C_{ww} can be described as follows:

$$C_{\mathrm{wc}} = f(\varepsilon_0, \varepsilon_{r.\mathrm{air}}, \varepsilon_{r.\mathrm{FR4}}, \mathrm{W}, \mathrm{T}, \mathrm{H}, l_{\mathrm{wc}}) \tag{2}$$

$$C_{\mathrm{ww}} = f(\varepsilon_0, \varepsilon_{r.\mathrm{air}}, \varepsilon_{r.\mathrm{FR4}}, \mathrm{W}, \mathrm{T}, \mathrm{H}, l_{\mathrm{ww}}) \tag{3}$$

where ε_0 is the vacuum permittivity, $\varepsilon_{r.\mathrm{air}}$, $\varepsilon_{r.\mathrm{FR4}}$ are the relative permittivity of air and FR4, respectively, W is width of the conductor, H is the distance between two conductors, T is the thickness of the conductor, l_{wc} and l_{ww} are the winding-to-core and winding-to-winding lengths, respectively.

In practice, the significantly high permittivity of the core material can result in a short circuit between the primary-side C_{wc} and the secondary-side C_{wc}. Consequently, a specific core cannot effectively contribute to CM capacitance reduction. The conventional approach to reduce CM capacitance is to increase the distance between the winding and the core. Luan et al. [31] highlight that CM capacitance in a transformer with separated insulated cores is lower than that in a transformer with associated magnetic core. However, the core separation introduces additional challenges [e.g., partial discharge (PD) within airgap and more complex assembly fixture].

B. Core-Series-Coupling Planar Transformer

The schematic diagram of the CM capacitance model for the proposed core-series-coupling planar transformer is shown in Fig. 6. The equivalent capacitor is formed by connecting multiple single-core capacitors in series, which can be represented as follows:

$$C_{\mathrm{CM.series-core}} = \frac{C_{\mathrm{wc}} // (C_{\mathrm{wc}} + 2C_{\mathrm{cc}}) + C_{\mathrm{ww}}}{N_{\mathrm{core}}} \tag{4}$$

where C_{cc} is the core-to-core capacitance.

Therefore, the total MV-class CM voltage is evenly distributed across the series cores due to their identical capacitances. As a result, the voltage stress is not solely concentrated at the small gap between the winding and a single core, as observed in the conventional transformer.

C. Design Guidelines

To provide clear design guidelines for the core-series-coupling planar transformer, the step-by-step process is as follows.

Step 1: Determine Design Requirements: Begin by defining the input/output voltages, power rating, and switching frequency. Use these parameters to calculate the transformer's required Area Product (AP).

Step 2: Select Magnetic Cores: The selection of magnetic cores is influenced by the required AP value from Step 1 and the

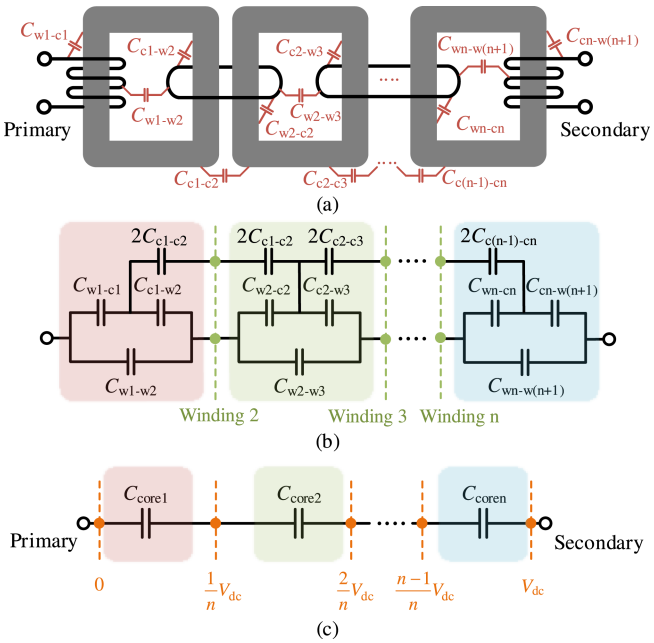


Fig. 6. Schematics of the CM capacitance model for the proposed core-series-coupling planar transformer. (a) Parasitic capacitance network in physical structure. (b) Elementary capacitance network. (c) Simplified series capacitance network.

transformer's size constraints. The isolated capacitance is also important, as it depends on the spacing between the cores and the windings.

Step 3: Optimize PCB Winding and Core Configuration: A balance between the PCB winding trace width and the number of cores is essential. Consider trace width for the rated current, and ensure creepage distances meet insulation standards. Additionally, larger winding-core distances reduce coupling capacitance. As the number of series-coupling cores increases, the coupling capacitance decreases, and the MV-class CM voltage is evenly distributed across the cores.

Step 4: Calculate Capacitance and Simulate: Based on the structure from Step 3, calculate the expected capacitance. For more accurate results, import a simplified model into ANSYS Q3D for preliminary simulations.

Step 5: Develop and Test the Prototype: Design the PCB layout using Altium, then perform a detailed evaluation in ANSYS Q3D. After completing the design, build the prototype and test its performance. If it does not meet the requirements set in Step 1, revisit and adjust the previous steps accordingly.

D. Validations

The detailed specifications of the practical core-series-coupling planar transformer are provided in Table I. Both the primary and secondary windings consist of 12 turns connected in series, while the middle winding comprises 4 turns arranged in parallel.

To validate the above CM capacitance model, mathematical calculations and finite-element method (FEM) simulations are

TABLE I
PARAMETERS OF THE CORE-SERIES-COUPLING PLANAR TRANSFORMER

Parameter	Value	Parameter	Value
$\varepsilon_{r.air}$	1	$\varepsilon_{r.FR4}$	4
Core material	MnZn Ferrite	Core Structure	U25/16/6
Inside trace width	0.5 mm	Inside trace-to-core	1.5 mm
Outside trace width	1 mm	Outside trace-to-core	2 mm
Trace-to-trace	0.24 mm	PCB thickness	1.2 mm
Mid-trace width	3.5 mm	Core-to-core	6 mm
$C_{pri.winding\text{-}core}$	1.63 pF	$C_{core\text{-}core}$	0.61 pF
$C_{mid.winding\text{-}core}$	1.21 pF	$C_{pri.winding\text{-}mid.winding}$	0.36 pF

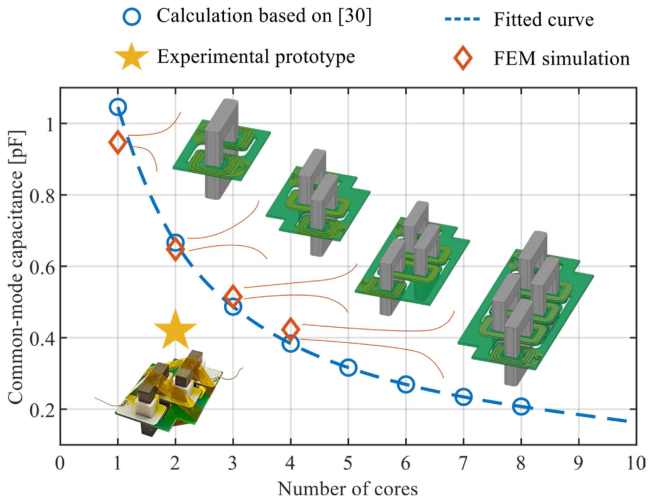


Fig. 7. CM capacitance as a function of the number of cores, including the calculated capacitance, the corresponding fitted curve, FEM-simulated capacitance, and practical prototype.

conducted. Fig. 7 presents the CM capacitance versus the number of cores, including the calculated capacitance, the corresponding fitted curve, FEM-simulated capacitance, and practical prototype. Remarkably, it aligns well with the (4), demonstrating that as the number of cores increases, the CM capacitance decreases. Additionally, a practical dual-core transformer prototype is implemented with a capacitance of 0.42 pF, which closely matches theoretical calculation and FEM simulation.

Fig. 8 illustrates the CM voltage distribution of the core-series-coupling transformer per unit. Fig. 8(a) shows that the MV-class voltage stress concentrates only at the small gap between the winding and core in the conventional single-core structure. In contrast, Fig. 8(b)–(d) reveals that as the number of series cores increases, the total CM voltage is evenly distributed across the scalable series cores due to their identical capacitances.

The number of cores in GDPS is determined by balancing two key factors: reducing CM capacitance and maintaining an acceptable power density. As the number of cores increases, the CM capacitance decreases, which improves the isolation performance. However, this also increases the overall volume of the transformer, thereby reducing the power density.

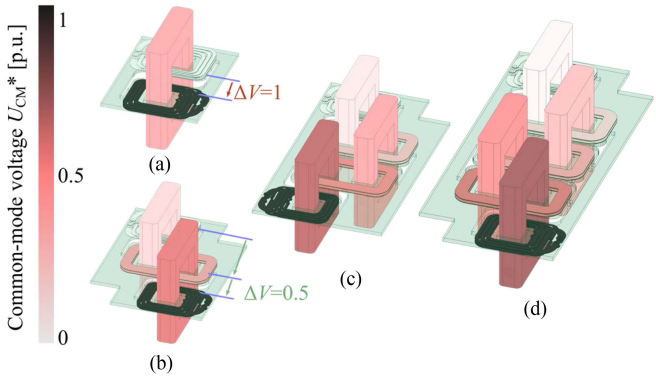


Fig. 8. Voltage distribution at the core-series-coupling transformer. (a) Single core: Voltage difference $\Delta V = 1$. (b) Dual core: $\Delta V = 0.5$. (c) Triple core: $\Delta V = 0.33$. (d) Quadruple core: $\Delta V = 0.25$.

In practical designs, the core-series-coupling technique should be employed alongside other strategies, such as adjusting the space between winding and core, to reduce CM capacitance without significantly increasing the number of cores. This allows for an optimized design that minimizes CM capacitance while preserving power density.

IV. Time-Domain Analysis of the Open-Loop Voltage Regulator Circuit

The scalable core-series-coupling planar transformer structure provides low CM coupling capacitance, easy manufacturing, and evenly distributed voltage. However, reducing the CM capacitance of the transformer typically results in a corresponding decrease in the magnetic coupling factor, leading to relatively large leakage inductance. As shown in Fig. 3, high leakage inductance exacerbates the load-dependent voltage drop in the conventional isolated converter, which poses challenges to power-handling capability [20].

The common circuit models include both frequency-domain and time-domain models. While the frequency-domain model simplifies the system significantly to reduce computational effort, the time-domain model enables quantitative analysis. Therefore, in this section, an accurate time-domain modeling of the open-loop voltage regulator circuit is presented.

A. Series-Resonant Converter

To mitigate the load-dependent voltage drop, the conventional approach involves using a series-resonant converter. This converter compensates for the leakage inductance by inserting a series resonant capacitor, as depicted in Fig. 9. Consequently, the converter can operate at an approximately fixed gain operation point, ensuring that the output voltage remains independent of the load power.

However, in the general model of series-resonant converters, two key parameters related to GDPS are often omitted for the sake of simplification in practical applications.

1) *Transformer winding resistance r_w:* For typical kilowatt-level power converters, the winding resistance is usually just a few milliohms. However, in tens of watt-level GDPS, the winding resistance increases to hundreds of milliohms, which significantly impacts the performance.
2) *Magnetizing inductance L_m:* In typical resonant converters, the magnetizing inductance is often dozens of times greater than that of the leakage inductor. However, in GDPS transformers with low CM coupling capacitance, the values of magnetizing and leakage inductors are in the same order of magnitude.

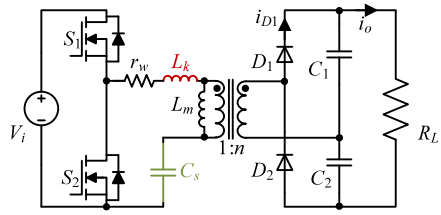


Fig. 9. Schematics of series-resonant converter topology.

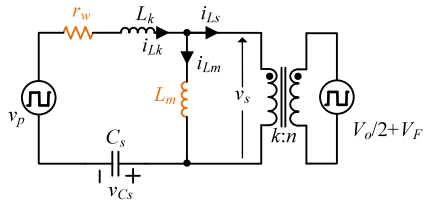


Fig. 10. Equivalent circuit of the series-resonant converter topology.

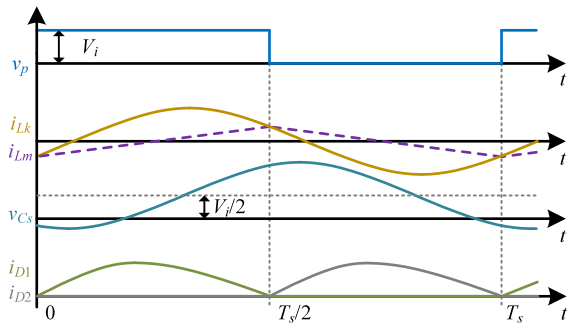


Fig. 11. Steady-state waveforms of the series-resonant converter.

B. Derivation of Circuit Equivalent Model

Taking into account the importance of transformer winding resistance and magnetizing inductance, the time-domain analysis model is constructed. To achieve nearly constant voltage gain, the series-resonant converter operates at the resonant frequency, where the effects of leakage inductance are minimized. The equivalent circuit and the associated steady-state operation waveforms are illustrated in Figs. 10 and 11.

Based on Kirchhoff's laws, the voltage equation during the interval $[0, T_s/2]$ can be expressed as

$$v_{rw} + v_{Lk} + v_{Cs} = v_p - v_s \tag{5}$$

where v_{rw}, v_{Lk}, and v_{Cs} are the voltages across r_w, L_k, and C_s, respectively.

The magnitudes of primary and secondary voltages at the resonant tank, denoted as v_p and v_s are given by

$$|v_p| = V_i, |v_s| = V_s = \frac{k}{n}\left(\frac{V_o}{2} + V_F\right) \tag{6}$$

where V_i, V_o, and V_F represent the input voltage, output voltage, and forward voltage of the output diode, respectively. The coupling coefficient is denoted as k and the turns ratio of the isolation transformer is n.

Considering the voltage-current relations of the inductor and capacitor, the following differential equation can be obtained:

$$L_k C_s {u_{Cs}}'' + C_s r_w {u_{Cs}}' + u_{Cs} = v_p - v_s. \tag{7}$$

Solving this differential equation yields

$$u_{Cs}(t) = (V_i - V_s) + e^{-\alpha t}(E_1 \cos\omega t + E_2 \sin\omega t) \tag{8}$$

$$\begin{aligned} i_{Lk}(t) = i_{Cs}(t) &= C_s \cdot \frac{di_{Cs}(t)}{dt} \\ &= [e^{-\alpha t}(E_2\omega\cos\omega t - E_1\omega\sin\omega t) \\ &\quad -\alpha e^{-\alpha t}(E_1\cos\omega t + E_2\sin\omega t)] \cdot C_s \end{aligned} \tag{9}$$

where E_1 and E_2 are undetermined coefficients. The coefficients α and ω are defined as follows:

$$\alpha = \frac{r_w}{2L_k}, \omega = \sqrt{\frac{1}{L_k C_s} - \frac{{r_w}^2}{4{L_k}^2}} = \frac{2\pi}{T_s}, r_w \le \sqrt{\frac{4L_k}{C_s}}. \tag{10}$$

As depicted in Fig. 11, the magnetizing current i_{Lm} can be obtained

$$i_{Lm}(t) = \begin{cases} i_{Lm}(0) + \frac{V_s}{L_m}t, & t \in [0, \frac{T_s}{2}) \\ i_{Lm}\left(\frac{T_s}{2}\right) - \frac{V_s}{L_m}t, & t \in (\frac{T_s}{2}, T_s] \end{cases} \tag{11}$$

where $i_{Lm}(0) = -V_s \cdot \pi/(2\omega L_m), i_{Lm}(T_s/2) = V_s \cdot \pi/(2\omega L_m)$.

Furthermore, the initial current condition of resonant current, i_{Lk}, can be determined

$$i_{Lk}(0) = i_{Lm}(0), i_{Lk}\left(\frac{T_s}{2}\right) = i_{Lm}\left(\frac{T_s}{2}\right). \tag{12}$$

By substituting $t = 0$ and $t = T_s/2$ into (8)

$$u_{Cs}(0) = V_i - V_s + E_1, u_{Cs}\left(\frac{T_s}{2}\right) = V_i - V_s - e^{-\alpha\frac{\pi}{\omega}} \cdot E_1. \tag{13}$$

The voltage relation, as shown in Fig. 11, is given by

$$u_{Cs}(0) + u_{Cs}\left(\frac{T_s}{2}\right) = V_i. \tag{14}$$

Hence, the output voltage can be expressed based on (6), (13) and (14)

$$V_o = \frac{n}{k}[V_i + E_1(1-\lambda)] - 2V_F \tag{15}$$

where λ is equal to $e^{-\alpha\pi/\omega}$.

The current relationship in the resonant tank is described by

$$i_{Lk} - i_{Lm} = i_{Ls}. \tag{16}$$

TABLE II
EXPERIMENTAL PARAMETERS OF THE SERIES-RESONANT CONVERTER

Parameter	Value	Parameter	Value
Turns ratio n	12:1:12	Couple factor k	0.8777
Leakage inductor L_k	19.4 μH	Magnetizing inductance	65.0 μH
Winding resistance	916 mΩ	Resonant capacitor	100 nF
Input voltage V_i	21 V	Power rating	10 W
Diode forward voltage	0.75 V	Switching frequency f	114 kHz

During the time interval $t \in [0, T_s/2]$

$$i_{Ls} = \frac{n}{k} i_{D1}. \tag{17}$$

Using the amp-second balance theory, the output current can be calculated

$$\begin{aligned} I_o = I_{D1} &= \int_0^{\frac{T_s}{2}} i_{D1}dt \cdot f = \int_0^{\frac{T_s}{2}} \frac{k}{n}(i_{Lk} - i_{Lm})dt \\ &\quad \cdot f = -\frac{kC_sE_1f(1+\lambda)}{n} \end{aligned} \tag{18}$$

where f is the switching frequency.

The output power can be computed as follows:

$$P_o = V_o \cdot I_o. \tag{19}$$

By substituting the output voltage from (15) and output current from (18) into (19)

$$P_o + \frac{(nV_i - 2kV_F)C_sf(1+\lambda)}{n}E_1 + fC_s(1-\lambda^2){E_1}^2 = 0. \tag{20}$$

Next, the undetermined coefficient E_1 can be solved by quadratic formula

$$E_1 = -\frac{nV_i - 2kV_F}{2n(1-\lambda)} + \sqrt{\frac{(nV_i - 2kV_F)^2}{4n^2(1-\lambda)^2} - \frac{P_o}{fC_s(1-\lambda^2)}}. \tag{21}$$

By substituting E_1 from (21) into (15) and rearranging, the voltage gain can be obtained

$$\begin{aligned} \frac{V_o}{V_i} &= \frac{n}{k}\Big(1 - \frac{nV_i - 2kV_F}{2nV_i} \\ &\quad + \sqrt{\frac{(nV_i - 2kV_F)^2}{4n^2{V_i}^2} - \frac{(1-\lambda)P_o}{(1+\lambda)fC_s{V_i}^2}}\Big) - \frac{2V_F}{V_i} \end{aligned} \tag{22}$$

where k and λ are key parameters rated to magnetizing inductance and winding resistances

$$k = \sqrt{\frac{L_m}{L_k + L_m}}, \lambda = e^{-\frac{\pi r_w}{2\omega L_k}}. \tag{23}$$

Therefore, the impact of the output power concerning the voltage drop across different winding resistances can be assessed by using the (22).

By incorporating the experimental parameters from Table II, the output voltage characteristic versus output power at different models is plotted in Fig. 12. Notably, the voltage drop caused by winding resistance and the bias error resulting from the

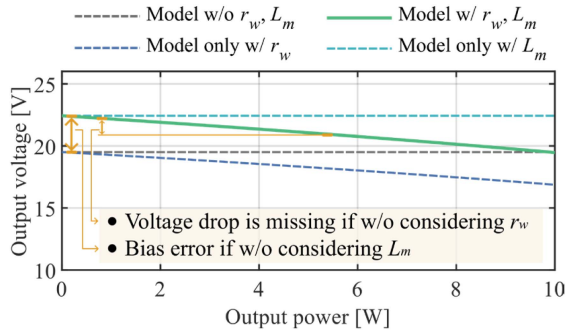


Fig. 12. Output power as a function of the output voltage at different models (w/: with; w/o: without).

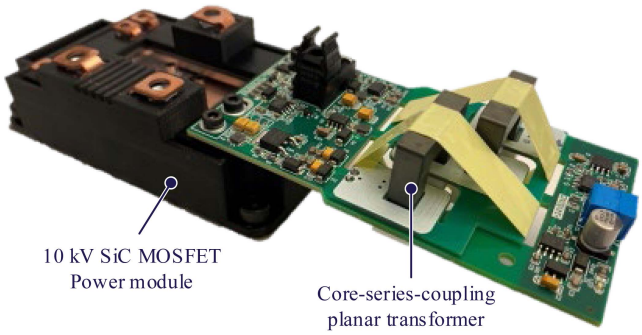


Fig. 13. Experimental prototype with 10 kV SiC MOSFET half-bridge power module.

magnetizing inductance significantly impact the output voltage. These effects cannot be ignored in GDPS modeling. While Yang et al. [20] provide a detailed analysis of a resonant converter model that includes winding resistance for kilowatt-level applications, it neglects the magnetizing inductance, which is insufficient for accurate modeling in GDPS applications. In practical applications, precise evaluation of the voltage drop can be achieved by considering the winding resistance during modeling. Additionally, adjusting the PCB track width and copper thickness allows designers to limit the open-loop output voltage within a reasonable range. This approach overcomes challenges related to high leakage inductance and power limitations without sacrificing power density or increasing parasitic capacitance.

V. Experimental Verification and Comparison

To validate the core-series-coupling planar transformer structure and open-loop voltage regulator circuit model, this article demonstrates an MV SiC gate driver with a dual-core planar transformer for 10 kV SiC MOSFET power module [32], as shown in Fig. 13. PD testing, parasitic capacitance measurement, circuit performance qualification, along with DPT are conducted.

A. PD Testing

For testing the insulation capability of the dual-core transformer, PD measurements were conducted using a standard 50 Hz ac source. Following the IEC60270 standard, the PD detector is employed to measure the PD signals, and the resulting measurements are presented in Fig. 14.

The background noise in the lab is consistently below 1 pC. The threshold for PD detection is set to 1 pC, and the partial-discharge inception voltage (PDIV) is defined as the voltage at

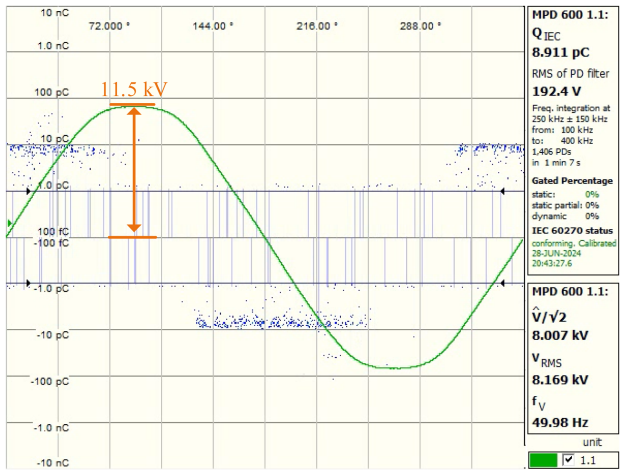


Fig. 14. Experimental PD test result.

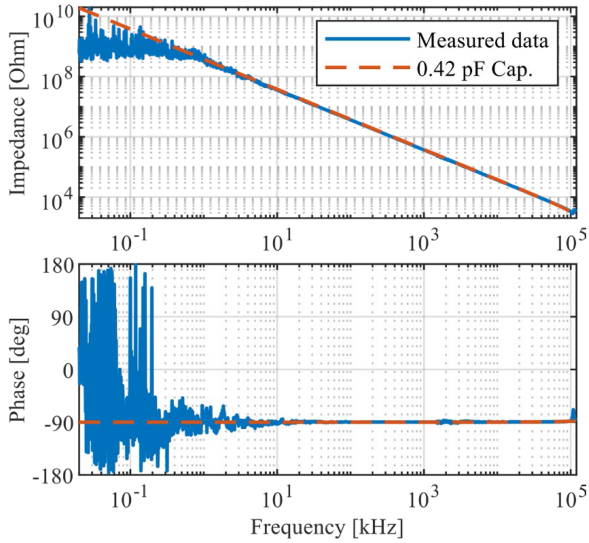


Fig. 15. Measured and fitted impedance of the transformer.

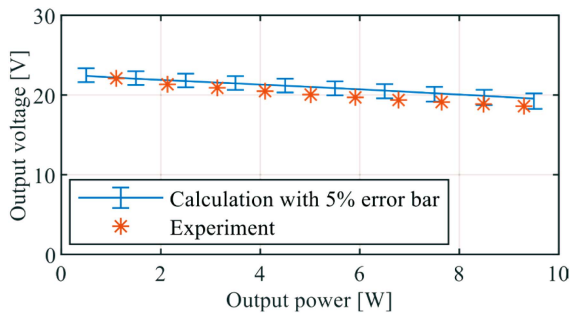


Fig. 16. Comparison of output power as a function of output voltage for calculation and experiment.

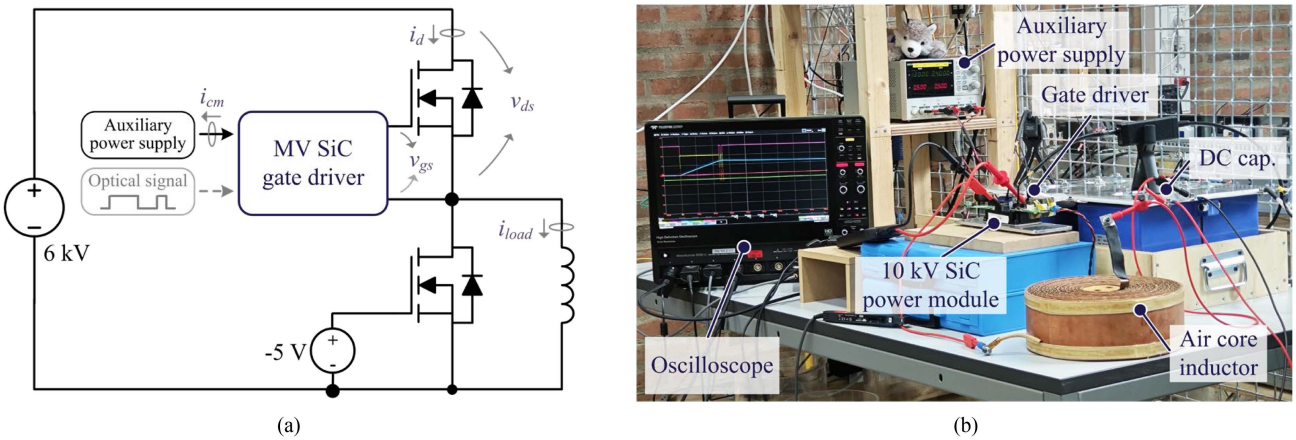


Fig. 17. Double pulse test. (a) Double-pulse-test setup circuit schematic. (b) Experimental setup.

which the discharge exceeds 10 pC. The experimental results reveal the transformer achieves a PDIV of 11.5 kV.

B. Parasitic Capacitance Measurement

The parasitic CM capacitance of the dual-core transformer is measured using the E4990A Impedance Analyzer from Keysight Technologies, along with an adaptor (model 16047). The corresponding bode plot of the measured impedance is depicted in Fig. 15. Based on the measured impedance data, the equivalent fitted impedance closely resembles a capacitor with a value of 0.42 pF. The measured capacitance is lower than the calculated and FEM-simulated results shown in Fig. 7. This discrepancy, approximately 50%, is primarily due to machining tolerances during manufacturing, variations in material properties, and limitations in measurement accuracy. Despite efforts to minimize these sources of error, slight differences in capacitance, particularly at such small values, are inevitable. The relative error is magnified in this case due to the small absolute capacitance values.

The measured total capacitance of the gate driver, which includes the dual-core transformer and the associated 10 kV SiC driver circuit, is 0.9 pF.

C. Circuit Performance Qualification

The open-loop voltage regulator circuit accurately assesses the voltage drop across different output loads. Designers can reasonably adjust the PCB track width and copper thickness to keep the output voltage within the rated range without the need for closed-loop control.

Fig. 16 compares the theoretical and experimental output voltage characteristics as a function of output power. Due to component tolerances, the measured voltage is slightly lower than the theoretical prediction, but it remains well within a 5% error margin. Furthermore, theoretical calculations indicate that even with a 5% variation in component parameters, the system maintains a stable output voltage, demonstrating the robustness of the proposed GDPS.

D. Double Pulse Test

A comprehensive feasibility verification of the demonstrated MV SiC gate driver through a 6 kV/30 A DPT using a 10 kV SiC MOSFET power module is conducted [32]. Fig. 17 provides the schematic of the DPT setup circuit and the experimental configuration.

The gate-source voltage v_{gs}, drain-source voltage v_{ds}, load current i_{load}, drain current i_d, and CM current i_{cm} are measured and presented in Fig. 18. During the turn-OFF transient, the dv/dt switching speed is 133.9 V/ns, while during turn-ON transient, the dv/dt switching speed is 111.6 V/ns. The experimental results demonstrate that the gate driver performs well even under these high switching speed conditions. Based on the equation $i_{\text{cm}} = C_{\text{cm}}\text{d}v/\text{d}t$, the CM capacitance can be calculated by integrating the CM current i_{cm} and dividing by the voltage. The calculated capacitance value is 1.6 pF, which is higher than the measured value of 0.9 pF for the gate driver. This difference is likely due to parasitic capacitances from the connection between the power module and the gate driver, additional cable capacitances, and the limitations in the accuracy of the current probe.

E. Continuous Switching Test

The circuit schematic of the continuous switching test is shown in Fig. 19(a). A 10 mH load inductor is connected between the OUT terminal of the power module and the midpoint of the dc-link capacitors. The modulation schematic, depicted in Fig. 19(b), illustrates that the high-side and low-side MOSFETs are operated alternately with a 50% duty cycle at a switching frequency of 10 kHz. The output voltage v_{out}, load current i_{load}, DC+ current $i_{\text{dc+}}$, DC- current $i_{\text{dc-}}$, and CM current i_{cm} are captured and presented in Fig. 19(c). The continuous switching test further demonstrates the feasibility of the proposed gate driver.

F. Comparison

Table III presents a comparison between the state-of-the-art MV gate driver and the proposed gate driver. Key parameters

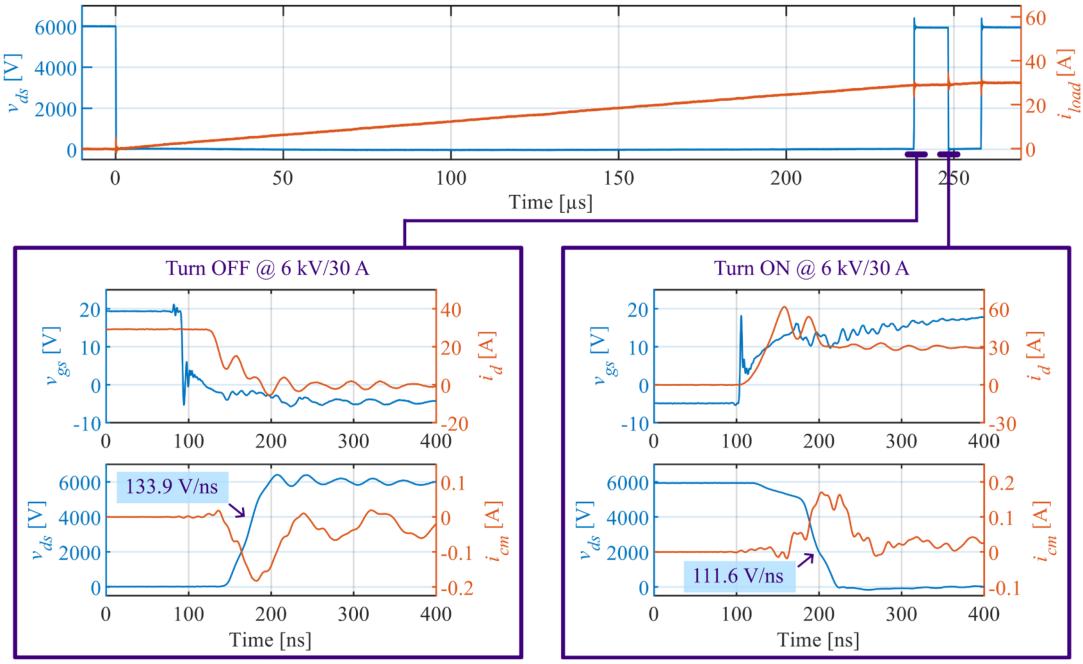


Fig. 18. Experimental DPT waveforms at 6 kV/30 A.

TABLE III
COMPARISON BETWEEN THE STATE-OF-THE-ART MV GATE DRIVER AND THE PROPOSED GATE DRIVER

Circuit topology	Transformer capacitance	Total capacitance	Isolation voltage	Power	Size (mm^3)*	Design complexity
Primary-side regulated flyback [16]	2.6 pF	3.5 pF	8 kV (DC leakage test)	2 W	142×65×30	• Bobbin inserted between winding and core • Leakage inductor compensation control
Single active bridge + LDO [19]	1.6 pF	2.5 pF	20kV (DC leakage test)	N/A	140×50×50	• Voltage drop due to leakage inductor • Customized core
Series-resonant converter [29]	2.6 pF	4.1 pF	20kV (N/A condition)	2 W	60×60×20	• Partial discharge risk in potting • Voltage drop caused by winding resistance
Current-fed single-turn primary winding approach [21], [22]	2.27 pF	3.61 pF	PDIV of 16.4 kV	20 W ×6	Primary: 82×33×10 Secondary: 50×50×28	• Partial discharge risk in potting • Fully potted transformer structure is difficult to assemble
PCB-based wireless power transfer [33]	2.2 pF	4.85 pF	25 kV (AC leakage test)	1.8 W	Primary: 103×69×15 Secondary: 69×69×10	• EMI challenges
Magnetic-shielding-based wireless power transfer [24]	2.78 pF	3.02 pF	PDIV of >30 kV	120 W	80×80×50	• Coil assembly • Magnetic shielding encapsulation process
Power-over-fiber [34]	N/A	N/A	N/A	0.5 W	Secondary: 100×60×20	• Large size of laser transmitter • Low efficiency
Signal-power integrated transmission [35], [36]	N/A	1.9 pF	PDIV of 13.5 kV	2 W	61×30×24	• EMI challenges
This paper	0.42 pF	0.9 pF	PDIV of 11.5 kV	10 W	100×58×50	• Customized core for improving power density

*The size is estimated through photograph in the article.

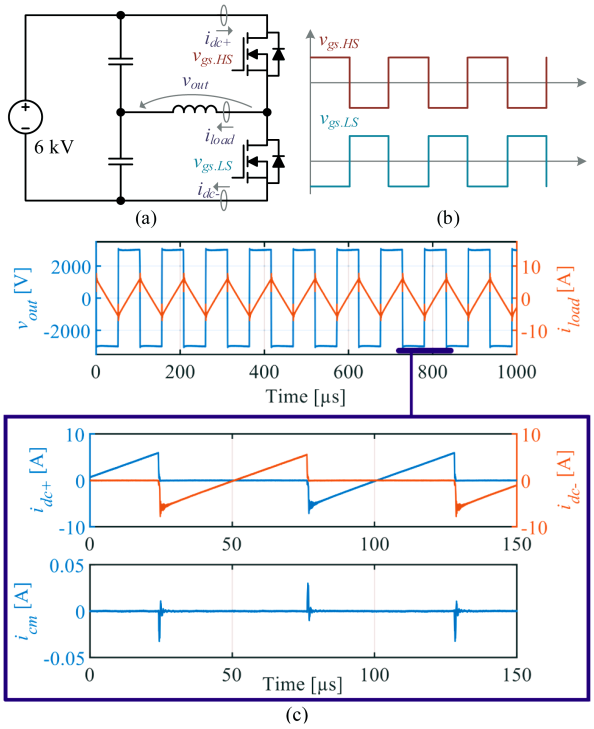


Fig. 19. Continuous switching test. (a) Circuit schematic. (b) Modulation schematic. (c) Experimental waveforms.

such as circuit topology, transformer capacitance, fully assembled driver capacitance, isolation voltage, power level, size, and design complexity are evaluated.

VI. Conclusion

In this article, a GDPS solution for MV SiC-based power electronics converter systems is presented. The key contributions include: 1) The core-series-coupling planar transformer satisfies isolation requirements while reducing coupling capacitance. This design eliminates the need of inconvenient wire winding procedures. 2) The open-loop voltage regulator circuit enables designers can reasonably adjust circuit parameters, ensuring a constant output voltage.

Additionally, this article provides the capacitance model for the scalable core-series-coupling transformer structure and a detailed time-domain model for the open-loop voltage regulator circuit. To validate our approach, an MV SiC gate driver with dual-core planar transformer for 10 kV SiC MOSFET power module is built. The corresponding PD testing, parasitic capacitance measurement, circuit performance qualification are conducted. The 6 kV/30 A DPT shows the demonstrated gate driver continues to perform well until the switching speeds reach 133.9 V/ns during turn-OFF and 111.6 V/ns during turn-ON transients.

References

[1] C. Li et al., "A highly efficient power block with series connection of power SiC MOSFETs-design, characterization and assessment in MV converters," *IET Power Electron.*, vol. 15, no. 7, pp. 605–620, May 2022.

[2] C. G. Dincan, "High power medium voltage DC/DC converter technology for DC wind turbines," Aalborg Universitetsforlag, 2018.

[3] P. Czyz et al., "Analysis of the performance limits of 166 kW/7 kV air- and magnetic-core medium-voltage medium-frequency transformers for 1:1-DCX applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 2989–3012, Jun. 2022.

[4] J. B. Casady et al., "New generation 10 kV SiC power MOSFET and diodes for industrial applications," in *Proc. PCIM Europe*, 2015, pp. 96–103.

[5] S. Mocevic et al., "Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter," *iEnergy*, vol. 1, no. 1, pp. 100–113, Mar. 2022.

[6] X. Li, Y. Chen, H. Chen, R. Paul, X. Song, and H. A. Mantooth, "A 10 kV SiC MOSFET power module with optimized system interface and electric field distribution," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9540–9553, Aug. 2024.

[7] C. DiMarino et al., "Design and experimental validation of a wire-bondless 10-kV SiC MOSFET power module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 381–394, Mar. 2020.

[8] G. Ortiz, "High-power DC-DC converter technologies for smart grid and traction applications," M.S. thesis, ETH Zurich, Zürich, Switzerland, 2014.

[9] B. F. Kjærsgaard et al., "Parasitic capacitive couplings in medium voltage power electronic systems: An overview," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9793–9817, Aug. 2023.

[10] Z. Yan et al., "Construction of a planar transformer with low common-mode capacitance for medium-voltage isolated gate-driver power supply," in *Proc. IEEE 14th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2023, pp. 764–767.

[11] A. Anurag, S. Acharya, and S. Bhattacharya, "Gate drivers for high-frequency application of silicon-carbide MOSFETs: Design considerations for faster growth of LV and MV applications," *IEEE Power Electron. Mag.*, vol. 6, no. 3, pp. 18–31, Sep. 2019.

[12] G. Liu et al., "Investigations on common-mode capacitive couplings in current sensors for medium voltage converter enabled by 10 kV SiC MOSFETs," in *Proc. IEEE 10th Int. Power Electron. Motion Control Conf.*, 2024, pp. 1658–1662.

[13] A. Anurag, S. Acharya, N. Kolli, and S. Bhattacharya, "Gate drivers for medium-voltage SiC devices," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 1, pp. 1–12, Jan. 2021.

[14] Texas Instruments, "IGBT & SiC gate driver fundamentals," 2021. [Online]. Available: https://www.ti.com/lit/pdf/slyy169

[15] C. DiMarino, J. Wang, R. Burgos, and D. Boroyevich, "A high-power-density, high-speed gate driver for a 10 kV SiC MOSFET module," in *Proc. IEEE Electric Ship Technol. Symp.*, 2017, pp. 629–634.

[16] D. N. Dalal et al., "Gate driver with high common mode rejection and self turn-on mitigation for a 10 kV SiC MOSFET enabled MV converter," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.10.

[17] H. Zhao et al., "Modeling and design of a 1.2 pF common-mode capacitance transformer for powering MV SiC MOSFETs gate drivers," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, 2019, pp. 5147–5153.

[18] H. Li, Z. Gao, and F. Wang, "Medium-voltage isolated auxiliary power supply design for high insulation capability, ultra-low coupling capacitance, and small size," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7226–7240, Jun. 2023.

[19] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design considerations and development of an innovative gate driver for medium-voltage power devices with high dv/dt," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5256–5267, Jun. 2019.

[20] N. Yang, J. Zeng, R. Hu, G. Ying, J. Liu, and Z. Yan, "High-frequency characteristics analysis of transformer-based voltage multiplier in lightweight process of unidirectional High step-up converters for offshore wind farms," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6585–6596, May 2023.

[21] J. Hu, J. Wang, R. Burgos, B. Wen, and D. Boroyevich, "High-density current-transformer-based gate-drive power supply with reinforced isolation for 10-kV SiC MOSFET modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2217–2226, Sep. 2020.

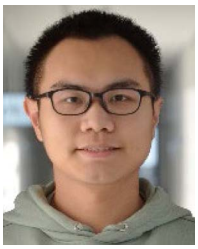
[22] N. Yan, D. Dong, and R. Burgos, "A multichannel high-frequency current link based isolated auxiliary power supply for medium-voltage applications," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 674–686, Jan. 2022.

[23] O. C. Spro, F. Mauseth, and D. Peftitsis, "High-voltage insulation design of coreless, planar PCB transformers for multi-MHz power supplies," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8658–8671, Aug. 2021.

[24] K. Sun, Y. Xu, J. Wang, R. Burgos, and D. Boroyevich, "Insulation design of wireless auxiliary power supply for medium voltage converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4200–4211, Aug. 2021.

[25] X. Du, C. Li, and D. Dujic, "Design and characterization of PCB spiral coils for inductive power transfer in medium-voltage applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6168–6180, May 2022.

[26] Wolfspeed, "Design considerations for Silicon carbide power," 2021. [Online]. Available: https://assets.wolfspeed.com/uploads/2021/04/design-considerations-download.pdf
[27] Z. Yan et al., "Time domain analysis of series-resonant converter in auxiliary power supply for medium-voltage converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 2715–2720.
[28] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for Power Electronics*. Hoboken, NJ, USA: Wiley, 2013.
[29] D. Rothmund, D. Bortis, and J. W. Kolar, "Highly compact isolated gate driver with ultrafast overcurrent protection for 10 kV SiC MOSFETs," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 4, pp. 278–291, Dec. 2018.
[30] W. Tan, "Modeling and design of passive planar components for EMI filters," M.S. thesis, Ecole Centrale de Lille, Villeneuve-d'Ascq, France, 2012.
[31] S. Luan, Z. Yan, and H. Zhao, "Effects of airgaps on parasitic capacitance of magnetic components," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1115–1134, Jan. 2024.
[32] D. N. Dalal et al., "Impact of power module parasitic capacitances on medium-voltage SiC MOSFETs switching transients," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 298–310, Mar. 2020.
[33] V.-T. Nguyen, V. U. Pawaskar, and G. Gohil, "Isolated gate driver for medium-voltage SiC power devices using high-frequency wireless power transfer for a small coupling capacitance," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10992–11001, Nov. 2021.
[34] X. Zhang et al., "A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kV SiC MOSFET," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 946–955, Sep. 2016.
[35] Z. Guo and H. Li, "A fiber-optic-less 50-MHz single transformer isolated gate driver with fault feedback for 10-kV SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 71, no. 9, pp. 10854–10863, Sep. 2024.
[36] Z. Guo and H. Li, "A MHz-pulse-transformer isolated gate driver with signal-power integrated transmission for medium-voltage SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9415–9427, Aug. 2022.



Zhixing Yan (Graduate Student Member, IEEE) is currently working toward the Ph.D. degree in power electronics with Aalborg University, Aalborg, Denmark.

His current research interests include medium-voltage converters and SiC gate driving technique.

Mr. Yan was the recipient of the First Prize Award at the EPE ECCE Europe Innovation Design Challenge in 2023.

Gao Liu (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree in power electronics with AAU Energy, Aalborg University, Denmark.

His research interests include medium-voltage converters enabled by wide band-gap power devices.

Shaokang Luan (Member, IEEE) received the B.Eng. and M.Eng. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2017 and 2020, respectively, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2024.

His research interests include design, modeling, and optimization of high-frequency magnetic components, with emphasis on parasitic capacitance, winding loss, and thermal management.

Yuan Gao received the B.S. and M.S. degrees in electronic engineering from Southwest Jiaotong University, Chengdu, China, in 2017 and 2020, respectively, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2024.

Her research interests focuses on medium voltage SiC power module packaging design.

Rui Wang (Member, IEEE) received the B.Sc. degree in electrical engineering and automation from Hunan University, Changsha, China, in 2017, the M.Sc. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2020, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2023.

He shortly worked with Huawei Technologies Co. Ltd., Dongguan, China, in 2023. He was also a visiting Ph.D. student with KTH Royal Institute of Technology, Stockholm, Sweden, in 2022. Currently, he serves as a postdoctoral researcher with the Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. His research interests include the applications of medium-voltage high-power devices, including IGBT, IGCT, SiC MOSFET, active gate drivers, series-connection technologies, and design of medium-voltage high-power converters.

Benjamin Futtrup Kjærsgaard (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in energy engineering with specialization in power electronics from AAU Energy, Aalborg University, Denmark, in 2019, 2021, and 2024, respectively.

His research interests include high power medium voltage power converter systems and design, wide bandgap semiconductor devices, their switching dynamics and the intra-component impact of parasitic capacitive and inductive couplings.

Morten Rahr Nielsen (Graduate Student Member, IEEE) received the B.Sc. degree in electrical energy technology from Aarhus University, Aarhus, Denmark, in 2020, and the M.Sc. degree in energy engineering, with a specialization in power electronics and drives, from AAU Energy, Aalborg University, Aalborg, Denmark, in 2022.

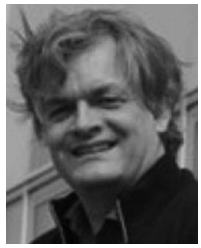
He was a visiting researcher with the Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge, U.K., in 2024. He is currently a Research Assistant with AAU Energy, Aalborg University, Aalborg, Denmark. His research interests include wide bandgap semiconductor devices and control of medium voltage, high-power converters.

Bjørn Rannestad received the M.Sc. and Ph.D. degrees in electrical engineering from AAU Energy, Aalborg University, Denmark, in 1999 and 2019, respectively.

Since 2008, he has been with KK Wind Solutions, Ikast, Denmark, as a senior specialist in front end innovation with high-power converters for wind turbines and renewables. He has 23 years of experience in the power electronic industry. His research interests include the green energy transition, specifically electric energy conversion applications for wind and green hydrogen production.

Hongbo Zhao (Member, IEEE) received the Ph.D. degree in power electronics from AAU Energy, Aalborg University, Denmark, in 2021.

He was a visiting student with the University of Texas at Austin and a visiting scholar with the University of Galway. He is currently an Assistant Professor with Department of Energy, Aalborg University, Aalborg, Denmark. His research interests include high-frequency modeling and analysis of high-power magnetics and filters, as well as medium-voltage wide band-gap power devices.



Stig Munk-Nielsen (Member, IEEE) received the M.Sc. and Ph.D. degrees from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor with AAU Energy, Aalborg University. His research interests include Si, SiC, and GaN components operating in soft and hard switching circuits, design challenges for low and medium-voltage power modules, and converters with intended application in the industry.