Fast and Accurate Three-Dimensional Thermal Model Based on Discrete Green's Function for Power Electronics

Yourun Zhang, *Member, IEEE*, Yuqiao Zhang, Maojiu Luo, Li Li, Wanli Ma, and Bo Zhang, *Senior Member, IEEE*

***Abstract*—A fast and accurate three-dimensional thermal modeling methodology based on discrete Green's function (DGF) is investigated innovatively for power electronics. Due to the demand of high robustness of power electronic systems, power devices require a fast and accurate thermal prediction or monitoring method. DGF is presented as a promising temperature prediction method, especially when facing new challenges in the complex chip packaging of power devices or the multichip layout of power modules. A detailed simulation algorithm is developed, and comparative simulations is conducted, demonstrating that the DGF method reduces computation time by more than 78% compared to the finite element method (FEM), with the same accuracy. In a double chip simulation, the result of DGF method closely matches the FEM's, demonstrating its superior accuracy in dealing with thermal coupling effects compared to traditional thermal network. Finally, an infrared thermography experiment is designed, validating the high accuracy, which indicated by the R-squared value that is over 0.98 between the results of the DGF method and experimental observations.**

***Index Terms*—Discrete green's function, heat conduction, power devices, silicon carbide, thermal model.**

I. Introduction

IN RECENT years, advanced power electronics have witnessed their unique role in various fields such as power transmission, electric vehicles, and renewable energy, which has driven the industry to focus more on the reliability of power electronic components. In some certain applications, such as aircraft, hybrid vehicles, space exploration and gas extraction, power electronic components are likely to operate under harsh conditions with temperatures exceeding 150 °C [1]. Most engineers regard power devices as the weakest component in power electronic systems, and temperature is widely recognized as the primary indicator of system deterioration [2].

As semiconductor technology advances, the dissipation of heat in power semiconductor devices increases. The inability to effectively dissipate heat leads to issues like bond wire failures and thermal runaway [3], [4], thus rendering thermal management a critical concern in electronics manufacturing [5]. Despite the high thermal conductivity of some wide band gap semiconductor like SiC, their lower ON-state resistance and higher breakdown voltage often result in smaller chip areas and shorter drift regions compared to silicon. This reduction in chip size contributes to a decreased thermal capacity and significantly compromises its short-circuit tolerance [6], [7]. Moreover, power devices are frequently employed in multiparallel circuits, where thermal coupling issues arising from chip layout contribute to challenges in predicting device temperature parameters and heat dissipation behaviors [8], [9].

Consequently, for high power density advanced semiconductor devices, a precise temperature monitoring method is imperative. The most commonly used thermal modeling methods currently include thermal network and finite element method (FEM). Compared to thermal networks, FEM, as a three-dimensional (3-D) model, preserves the geometric details of the module structure. This provides FEM with a natural advantage in solving thermal coupling problems, as it can capture the field interactions among multiple heat sources using 3-D partial differential equations. Another advantage of FEM as a 3-D model is its ability to monitor the temperature distribution within a single chip, which is crucial for reliability monitoring in certain applications. In the study by Zhao et al. [10], they developed a coupled field-circuit model and used FEM to calculate the temperature distribution of a SiC MOSFET chip, observing large chip-level temperature difference under surge condition. While FEM simulations yield the most accurate results, the computational time for these simulations is excessive [11]. As a result, FEM is not suitable for real-time thermal monitoring or deployment in other simulation processes.

The thermal network is a compact model that simplifies the heat transfer path from the chip to the package exterior into a network consisting of thermal resistances (Rth) and thermal capacitances (Cth). Due to their simplicity in topology and computational efficiency, these methods are widely employed.

Received 30 September 2024; revised 24 December 2024; accepted 27 January 2025. Date of publication 13 February 2025; date of current version 20 March 2025. This work was supported by the National Natural Science Foundation of China under Grant 62474034. Recommended for publication by Associate Editor K. Ma. *(Corresponding author: Yourun Zhang.)*

Yourun Zhang, Yuqiao Zhang, Maojiu Luo, and Bo Zhang are with the State Key Laboratory of Electronic Thin Films and Integrated Devices, School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu 610054, China (e-mail: yrzhang@uestc.edu.cn).

Li Li and Wanli Ma are with the Gree Electric Appliances, Inc., Zhuhai 519070, China.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3537984.

Digital Object Identifier 10.1109/TPEL.2025.3537984

However, thermal network models face challenges in addressing thermal coupling, prompting the development of 3-D thermal resistance network models. Bahman et al. [12], [13] developed a 3-D Foster thermal resistance network for insulated gate bipolar transistor (IGBT) modules. This model extracts coupled Foster thermal impedances using FEM, enabling accurate and fast temperature estimation under thermal coupling conditions. K. Górecki and P. Górecki [14], [15] proposed a nonlinear Cauer thermal model for IGBT and antiparallel diode systems. Their model constructs multibranch network topologies for heat paths, representing the final temperature response as the sum of internal thermal responses, mutual thermal coupling responses, and dissipation to the external environment.

While such high-dimensional models provide precise characterization of thermal coupling in multichip systems, the extraction of thermal coupling impedance parameters remains a challenge. Heng et al. [16] introduced a 3-D coupled Cauer model for power modules based on heat flux. Wang et al. [17] proposed a method to obtain continuous thermal spectrum through deconvolution based on structural functions. These advancements enhance the physical interpretability of 3-D thermal networks and reduce modeling costs to some extent. Moreover, exploring the ability to represent temperature distribution within chips is another direction for networks. In [16] and [18], multiple temperature points within chips were introduced, achieving coupled multibranch thermal networks for chip-level modeling. Nevertheless, whether modeling multichip thermal coupling or chip-level multipoint coupling, the inevitable increase in branches and *RC* parameters can reduce the flexibility of these models.

Finite difference method (FDM) is another approach, which has high-dimensional capability. Unlike FEM, FDM discretizes the continuous 3-D body into multiple small volume element port networks [19], [20]. Each small volume element contains all thermal components, such as thermal resistance, heat sources, and thermal capacitance. The heat conduction behavior between adjacent volume elements is restricted by energy balance. However, similar to FEM, the drawback of FDM lies in the significant computational time required for 3-D operations [13].

The Green's function method is an analytical approach, and its temperature calculation results are based on the solution of already solved boundary problems, leading to a significant reduction in computation time. Zhan and Sapatnekar [21], using Green's functions, established an ON-chip distributed multiheat source temperature analysis model for multilayer substrate structures. They accelerated the calculation using discrete cosine transform, significantly improving the algorithm's efficiency by several orders of magnitude. Maggioni et al. [22] and Sodan et al. [23], [24] employed a convolution-based Green's function temperature response calculation method. Based on convolution, this method directly establishes a responsive mapping from the power map to the temperature distribution, making it highly suitable for real-time chip temperature monitoring due to its efficiency and convenience.

Even though Green's function methods provide fast and simple solutions, the fundamental challenge lies in the difficulty of obtaining the Green's function for a given system [25]. A promising approach is to combine the advantages of FDM and Green's function methods, meaning to use the numerical calculation method of FDM to obtain Green's functions that are challenging to solve analytically. The result of this idea is the discrete Green's function (DGF). DGF stem from spectral graph theory [26]. It is a matrix obtained by discretizing the Laplace operator in the heat conduction equation and applying the theory of Green's functions. The DGF method has been applied in thermal models in some nonelectronic fields. In the work of Cole et al. [27], [28], they used the DGF method to simulate the thermal effects in additive manufacturing processes, obtaining results that match experimental observations.

Building upon the foundation laid by the aforementioned research, this article proposes a new thermal model based on DGF suitable for power electronics. The following highlights about the proposed DGF method is presented.

1) A pseudo-Laplacian matrix originated from the Laplacian matrix in the DGF method is introduced, enabling DGF to be applied to the multilayer complex packaging structures of power electronic devices and modules. The matrix incorporates all geometric details of the 3-D structure.
2) A fast algorithm for computing the power-to-temperature response based on DGF is developed. This algorithm is validated through FEM simulations, demonstrating the high accuracy and speed of the DGF method, as well as its ability to characterize nonuniform temperature distributions on the chip.
3) By employing real physical parameters for modeling, the DGF method exhibits advantages over thermal network methods in addressing thermal coupling problems. It is entirely independent of FEM for model development and requires minimal parameter extraction during experimental validation.

The rest of this article is organized as follows. Section II specifies the principles of DGF. The construction method of pseudo-Laplacian matrix and the simulation algorithm is also introduced in this section. Section III conducts several simulations on virtual structures. These simulations are supposed to verify the accuracy and speed of DGF method. Comparisons among methods of DGF, FEM, and Thermal Network are also carried out and the thermal coupling effect is addressed. Section IV carries out an infrared thermography experiment for validation purpose. The high consistency between the proposed model and the experiment result foreshadows a promising application for power electronics. Finally, Section V concludes this article.

II. Modeling and Algorithm of DGF

The DGF method follows the idea of Green's Function. In this section, the theory and principles of DGF will be illustrated. Section II-A reviews the DGF theory in heat conduction. Section III-B provides the approaches to construct pseudo-Laplacian matrices, which fundamentally established the DGF based thermal model for power devices. Section III-C illustrated the simulation algorithm.

A. Reviews of DGF

The method of DGF conforms the principles of the original Green's Function method in partial differential equation, which obtains the solution by summing the responses of all effects.

The considered heat conduction equation takes the form of a partial differential equation as follows:

$$\frac{\partial T(r,t)}{\partial t} - D\Delta T\ (r,t) = \frac{q(r,t)}{c \cdot \rho} \tag{1}$$

where D represents the thermal diffusivity, c is the specific heat capacity, and ρ is the mass density. T denotes the temperature distribution in time and space, and q is the heat generation term. In addition to (1) describing heat conduction behavior, boundary conditions (BC) and initial conditions (IC) in the form of (2) and (3) are necessary to obtain the temperature distribution at any given time point in space

$$\text{BC: } k\frac{\partial T}{\partial n_i} + h_i T\ = \mu_i(r_i,t)\ \text{(on Boundry } i\text{)} \tag{2}$$

$$\text{IC: } T(r,t)\ |_{t\,=\,0} = T_0\ (r)\,. \tag{3}$$

For the boundary conditions (2), k represents the thermal conductivity within the domain, and h_i represents the heat transfer coefficient at the boundary.

The Green's function method involves solving the corresponding Green's function problems (4)–(6) to obtain the respective Green's functions. Subsequently, the temperature response is obtained by taking the inner product of the Green's function with specific effect terms

$$\left(\frac{\partial}{\partial t} - D\Delta\right) G(r,t;r',\tau) = \ \delta(r - r', t-\tau) \tag{4}$$

$$\text{BC: } k\frac{\partial G}{\partial n_i} + h_i G\ =\ 0\ \text{(on Boundry } i\text{)} \tag{5}$$

$$\text{IC: } G(r,t;r',\tau)\ |_{t<\tau} =\ 0. \tag{6}$$

Once the Green's function is solved, substituting each of these solutions into (7) allows for the calculation of the corresponding temperature responses [29]

$$\begin{cases} T(r,t)\ = T_i\ (r,t) + T_g(r,t) + T_b(r,t) \\ T_i\ (r,t)\ = \int_V G|_{\tau=0} \cdot T_0(r')\,dr' \\ T_g\ (r,t)\ = \frac{1}{c\,\rho}\ \int_0^t d\tau\ \int_V G \cdot q(r',\tau)\,dr' \\ T_b(r,t)\ = \frac{1}{c\,\rho}\ \sum_i \int_0^t d\tau\ \int_{S_i'} G \cdot \mu_i(r_i',\tau)\,dr' \end{cases} \tag{7}$$

where T_i, T_g, and T_b represent the temperature response of IC, heat generation, and BC, respectively.

However, such Green's functions face the challenge of truncation errors, and their series form undoubtedly adds a significant computational budget. Moreover, analytic Green's functions can hardly be obtained for multilayered thermal conduction systems. In response to such challenges, DGF was proposed.

DGF method discretizes the spatial heat conduction system into undirected graph based on spectral graph theory. The spatial discretization leads to the discretization of the Laplace operator. Let $\boldsymbol{T}$ represent a column vector of temperature defined on all n nodes in the undirected graph, then the discretized Laplace operator can be transformed into a Laplacian matrix L. When L is multiplied by $\boldsymbol{T}$, it yields an n-dimensional column vector, as expressed in

$$L\boldsymbol{T}\ =\ \text{vector}\left\{T_i\sum_{j\neq i} w_{ij} - \sum_{j\neq i} w_{ij}T_j, i\ =\ 1,2,\ldots,n\right\}. \tag{8}$$

In (8), the elements of the column vector are the discretized form of second derivatives at each node. In spectral graph theory, Laplacian matrix L can be represented by adjacency matrix A and degree matrix D. They are defined as in (9) and (10) and the Laplace matrix can be obtained through (11)

$$A\ =\begin{pmatrix} 0 & w_{12} & \ldots & w_{1n} \\ w_{21} & 0 & & \vdots \\ \vdots & & \ddots & w_{n-1\ n} \\ w_{n1} & \ldots & w_{n\ n-1} & 0 \end{pmatrix} \tag{9}$$

$$D\ =\ diag\left\{\sum_{j\neq i} w_{ij}\ , i\ =\ 1,2,\ldots,n\right\} \tag{10}$$

$$L\ =\ D - A. \tag{11}$$

By substituting the Laplace matrix into the heat conduction equation, the focused heat conduction equation transforms into a matrix differential (12). The solution to (12) is given by (13), which is a solution with a matrix exponential, where $\boldsymbol{T}_0$ represents the column vector composed of the initial temperature conditions

$$\frac{\partial \boldsymbol{T}}{\partial t}\ =\ -L\boldsymbol{T} \tag{12}$$

$$\boldsymbol{T}(t)\ = \exp(-Lt)\ \boldsymbol{T}_0. \tag{13}$$

Comparing (13) with the IC response by Green's functions in (7), the expression (14) for DGFs can be obtained [28]. Here, ϕ and Λ represent the eigenvector matrix and the diagonal matrix of eigenvalues of L, respectively, as follows:

$$\text{DGF}(t;\tau)\ =\ \phi\exp(-\Lambda(t-\tau))\,\phi^{-1}. \tag{14}$$

Now, the DGF has an explicit solution. By substituting (14) into the (7) in discretized form, the corresponding temperature response can be obtained.

However, the construction of the DGF mentioned above has not addressed two issues. One is how to determine the weight values w_{ij} in the Laplace matrix (8), and the other is how to determine the DGF under different boundary conditions represented by (2). These two issues will be addressed in the following section.

B. Pseudo-Laplacian Matrix Construction

Although the establishment of DGFs in the previous section may not seem to address the issue of multilayered structures, it can be adapted by making certain modifications to the Laplace matrix. Before discussing that, let's focus on the finite difference form of heat conduction, i.e., energy balance, to determine the weights of the Laplace matrix. Fig. 1 illustrates a simple example of heat conduction in a four-node undirected graph.

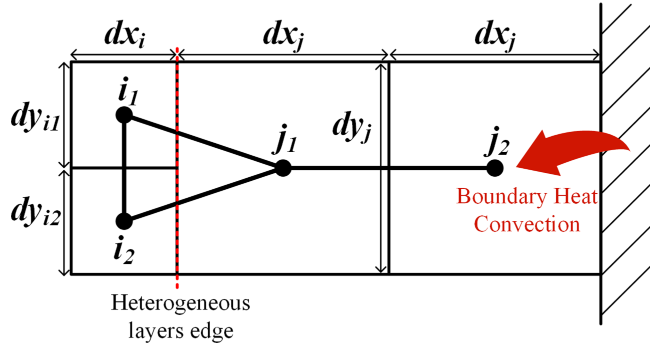


Fig. 1. Heat conduction in a four nodes undirected graph under differential form.

It consists of a heterogeneous multilayer structure composed of two materials denoted by i and j,using h to represent the heat transfer coefficient. Additionally, it includes an external convective heat transfer boundary. The divided volume elements of two materials have different lengths in orthogonal directions, denoted horizontally by dx_i and dx_j, and vertically by dy_i and dy_j. This example almost covers all scenarios of heat exchange between nodes when discretizing spatial points based on the cartesian grid.

The heat conduction behavior conforms to two laws: Fourier's Law and Newton's Law of Cooling, expressed by (15) and (16), respectively, where Q represents heat and A_c represents the contact area. Fourier's Law can describe the heat conduction behavior between different spatial points within the same material, while Newton's Law of Cooling represents the heat transfer behavior between two different materials. Based on these two laws, the energy balance equations for each node in Fig. 1 can be discretized

$$\text{Fourier's law}: \quad Q = -A_c k \nabla T \tag{15}$$

$$\text{Newton's law of cooling}: \quad Q = A_c h \left(T_2 - T_1\right) \tag{16}$$

Energy balance requires that the rate of heat storage at each node is equal to the rate of heat inflow minus the rate of heat outflow. For the energy balance at nodes i_1 and j_1, the following equations are satisfied:

$$\rho_i c_i \frac{\partial T_{i1}}{\partial t} dx_i d\, y_{i1} = k_i \frac{T_{i2} - T_{i1}}{dy_{i1}} dx_i + h\left(T_{j1} - T_{i1}\right) dy_{i1} \tag{17}$$

$$\begin{aligned} &\rho_j c_j \frac{\partial T_{j1}}{\partial t} dx_j dy_j \\ &= k_j \frac{\left(T_{j2} - T_{j1}\right)}{dx_j} dy_j + h\left(T_{i1} - T_{j1}\right) dy_{i1} + h\left(T_{i2} - T_{j1}\right) dy_{i2}. \end{aligned} \tag{18}$$

For the energy balance at j_2, (19) is satisfied. Note that the last term on the right side of (19) represents heat exchange at the boundary, which is the discretized form of the boundary condition for Green's functions (5)

$$\rho_j c_j \frac{\partial T_{j2}}{\partial t} dx_j d\, y_j = k_j \frac{\left(T_{j1} - T_{j2}\right)}{dx_j} dy_j - h_{\text{boundary}} T_{j2} dy_j. \tag{19}$$

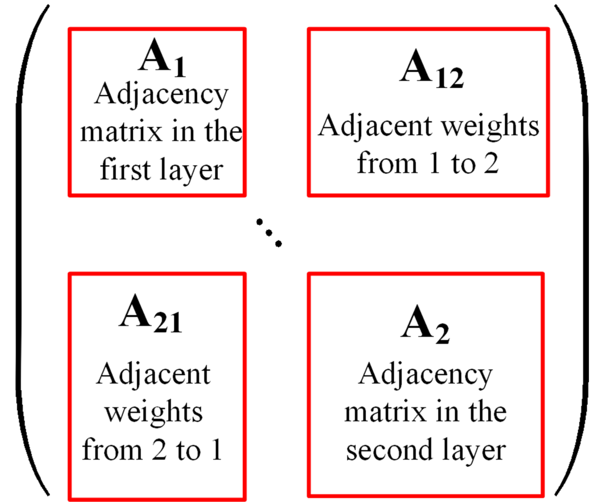


Fig. 2. Matrix block structure of the adjacency matrix of a bilayer structure.

By comparing (17), (18), and (19) with (8) and (12), the following weight values can be obtained:

$$w_{i1i2} = w_{i2i1} = \frac{D_i}{dy_i^2}\, ;\; w_{j1j2} = w_{j2j1} = \frac{D_j}{dx_j^2} \tag{20}$$

$$w_{j1i1} = \frac{dy_{i1}}{dy_j} \cdot \frac{h}{\rho_j c_j dx_j};\; w_{i1j1} = \frac{h}{\rho_i c_i dx_i}. \tag{21}$$

An adjacency matrix in block matrix manner may be helpful to understand how these weight values are arranged, as it is showed in Fig. 2. The Laplacian matrix, established based on the heat conduction equation, is referred to as a pseudo-Laplacian matrix.

Equations (20) and (21) can be written as (22) that relates the weights to the thermal network. Here, $R\mathrm{th}_{ij}$ represents the thermal resistance between nodes i and j, and $C\mathrm{th}_i$ represents the heat capacity at node i

$$w_{ij} = \frac{1}{R\mathrm{th}_{ij} C\mathrm{th}_i}. \tag{22}$$

Equation (19) also includes a boundary convective term. This term does not have the same form of (8), so it does not affect the adjacency matrix A but is directly added to the degree matrix D. Let E_i represents the boundary condition-added weight for a node i located on the boundary. Its expression is given by (23), where dx_i is the width of the discrete volume element at node i in the direction perpendicular to the boundary

$$E_i = \frac{h_{\text{boundary}}}{\rho_i \cdot c_i \cdot dx_i}. \tag{23}$$

Ultimately, the elements L_{ij} of the pseudo-Laplace matrix have the following form:

$$L_{ij} = \begin{cases} -\frac{1}{Rth_{ij} Cth_i}, \ i \neq j, \text{ adjacent} \\ \sum_{k \neq i} \frac{1}{Rth_{ik} Cth_i} + E_i, \ i = j \\ 0, \text{ Otherwise.} \end{cases} \quad (24)$$

C. Applied Algorithm for Simulation

Once the pseudo-Laplacian matrix from (24) is constructed, performing its eigenvalue decomposition to obtain the eigenvector matrix ϕ and the diagonal matrix of eigenvalues Λ, then substituting them into (14) yields the DGF for the thermal conduction system. In the discrete case, the IC response T_i and the heat generation response T_g in (7) becomes

$$\boldsymbol{T_i}(t) = \text{DGF}(t; 0) \ \boldsymbol{T}_0 \quad (25)$$

$$\boldsymbol{T_g}(t) = \int_0^t \text{DGF}(t; \tau) \, \boldsymbol{g}(\tau) \, d\tau \quad (26)$$

where $\boldsymbol{g}$ is a column vector related to internal heat generation, defined as

$$\boldsymbol{g} = \text{vector}\left\{\frac{q_i}{c_i \rho_i}, \ i = 1, 2, \ldots, n\right\}_{n\times 1}. \quad (27)$$

The bolded symbols $\boldsymbol{T}_0$, $\boldsymbol{T_i}$, and $\boldsymbol{T_g}$ represent column vectors of spatial discretized temperature distribution. For systems with non-constant boundary conditions, the boundary response $\boldsymbol{T_b}$ has the same form as (26), considering $\boldsymbol{g}$ to be nonzero only at the boundary.

Using (25) and (26), the temperature responses at any given time under specific power dissipation can be computed by solving the time integral. When the power dissipation value is time-dependent, linear interpolation can be performed between discrete sampled power dissipation points before segmenting the integral. Assuming at t_n and t_{n+1}, two consecutive sampled power dissipation points, within a time interval t_S, are denoted as $\boldsymbol{g_n}$ and $\boldsymbol{g_{n+1}}$. After linear interpolation, the heat generation response $\boldsymbol{T_g}$ within this sampling interval is given by

$$\boldsymbol{T_g} = \int_0^{t_S} \text{DGF}(t_S; \tau) \left(\boldsymbol{g_n} + \frac{\boldsymbol{g_{n+1}} - \boldsymbol{g_n}}{t_S}\tau\right) d\tau. \quad (28)$$

This equation represents the temperature increasement caused by internal heat generation during the period between t_n and t_{n+1}. Likewise, the former temperature distribution undergoes the same diffusion process. The temperature caused by this process at t_{n+1} can be deem as the IC response of temperature at t_n, which is given by

$$\boldsymbol{T_i} = \text{DGF}(t_S; 0) \ \boldsymbol{T_n} \quad (29)$$

where $\boldsymbol{T_n}$ represents the temperature vector at t_n. The integral in (28) can be solved, and the final temperature response is expressed as follows:

$$\begin{cases} \boldsymbol{T_i} = p_0 \, \boldsymbol{T_n} \\ \boldsymbol{T_g} = p_1 \, \boldsymbol{g}_2 - (p_1 + p_2) \, \boldsymbol{g}_1 \end{cases} \quad (30)$$

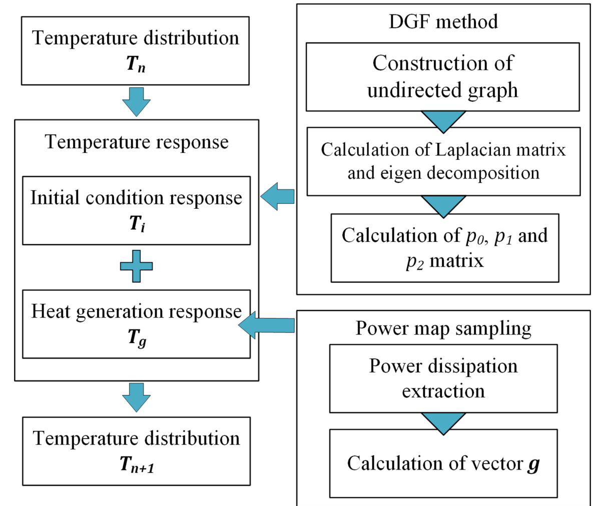


Fig. 3. Steps of temperature simulation algorithm based on DGF method.

where p_0, p_1, and p_2 are all $n \times n$ matrices, defined as follows ($\boldsymbol{I}$ represents the identity matrix):

$$\begin{cases} p_0 = \phi \exp(-\Lambda \, t_S) \, \phi^{-1} \\ p_1 = \phi \, \Lambda^{-1} \, \phi^{-1} + \frac{1}{t_S} \phi \, \Lambda^{-2} \left[\exp(-\Lambda \, t_S) - \boldsymbol{I}\right] \phi^{-1} \\ p_2 = \phi \, \Lambda^{-1} \left[\exp(-\Lambda \, t_S) - \boldsymbol{I}\right] \phi^{-1}. \end{cases} \quad (31)$$

The temperature response $\boldsymbol{T_{n+1}}$ at the next time point is the sum of the IC response and the heat generation response, as represented by $\boldsymbol{T_i}$ and $\boldsymbol{T_g}$ in (30). If the sampling interval t_S is constant, the matrices in (31) remain constant, eliminating the need to repeatedly solve integrals and matrix inversions each time the new temperature response is computed.

The complete temperature distribution simulation algorithm based on DGF is developed, as illustrated in Fig. 3. The process is outlined as follows: first, based on the theory of DGF, a corresponding undirected graph of the system is established, which is then transformed into a pseudo-Laplacian matrix for multilayer structures. Subsequently, the matrix undergoes eigen decomposition to obtain the DGF. For the discrete sampling sequence of power dissipation signals, linear interpolation can be applied between the points before computing the inner product with the DGF. The result of the integral turns out to be the product of n-order matrices p_0, p_1, and p_2 from (31) with the corresponding column vectors $\boldsymbol{T_n}$, $\boldsymbol{g}_1$, or $\boldsymbol{g}_2$. Simulation proceeds sequentially, where the new temperature distribution $\boldsymbol{T_{n+1}}$ is obtained by summing the IC response $\boldsymbol{T_i}$ of the previous temperature distribution $\boldsymbol{T_n}$ with the heat generation response $\boldsymbol{T_g}$ of the power dissipation, computed at each time point using (30).

III. Simulations and Verifications

The accuracy of the DGF method has been validated in some other works [27], [28]. However, the modified DGF method proposed in this article to address multilayered heterogeneous structures (i.e., power device and module structures) still needs validation. In this section, accuracy validation will be carried

TABLE I
VALUES OF PHYSICAL PARAMETERS (@300K)

Material types	Coefficient of Thermal Conductivity $\boldsymbol{k}$ (W/(cm · K))	Specific Heat Capacity $\boldsymbol{c}$ (J/(g · K))	Density $\boldsymbol{\rho}$ (g/cm^3)
4H-SiC	3.7	0.69	3.21
Solder	0.5	0.15	9.0
Copper	4.01	0.386	8.96
AlN	3.21	1.0	3.26

out using virtual structure under multiple operating condition. Section III-A constructed a three-layer structure, which simulates the TO packaging structure of SiC devices. Section III-B compared the simulation results of DGF method and FEM, highlighting the remarkable performance of DGF method. Section III-C provides a double chip structure, which simulates a power module under DBC packaging. Physical parameters used in these sections are given in Table I and are considered to be temperature irrelevant due to the limitation of DGF method.

A. Construction of a SiC Power Device

A virtual 3-D structure with physical parameters in Table I, as depicted in Fig. 4, will be constructed to validate the proposed DGF method. This structure is supposed to simulate the heat dissipation of a SiC power device under TO packaging, excluding composition such as encapsulation, bonding wires, and epoxy resin. The structure is indicated in Fig. 4(a). The structure is discretized into undirected graph, which red, green, blue nodes refers to copper, solder, and SiC chip volume elements, respectively. The nodes within the same material layer of the undirected graph are arranged equidistantly in orthogonal directions. For the undirected graph shown in Fig. 4(a), the SiC chip consists of $10 \times 10 \times 3$ nodes, the solder layer consists of $10 \times 10 \times 2$ nodes, and the copper layer consists of $10 \times 10 \times 4$ nodes. Within the same material layer, all nodes are connected to their nearest neighbors in six orthogonal directions, forming the adjacency matrix. The corresponding weight w_{i1i2} is calculated using (20). In Fig. 4(c), the cross-sectional view of the structure illustrates how edges between heterogeneous layers are set, conforming the principles of the pseudo-Laplacian matrix. For adjacent nodes at the interface between two different material layers, such as the solder layer and the copper layer in Fig. 4(b), the adjacency matrix elements are constructed, as illustrated in Fig. 4(c). In the undirected graph construction shown in Fig. 4(c), i represents the denser nodes of the solder layer, while j represents the less dense nodes of the copper layer. Whether a node i in the upper layer connects to a node j in the lower layer with a weight w_{ij} depends on whether node i lies within the volumetric range of node j 's volume element. The corresponding weight is calculated using (21). The interlayer heat transfer is set to be ideal. In that case, the expression for the heat transfer coefficient h_{ij} is given by

$$h_{ij} = \frac{1}{\frac{d_i}{k_i} + \frac{d_j}{k_j}} . \tag{32}$$

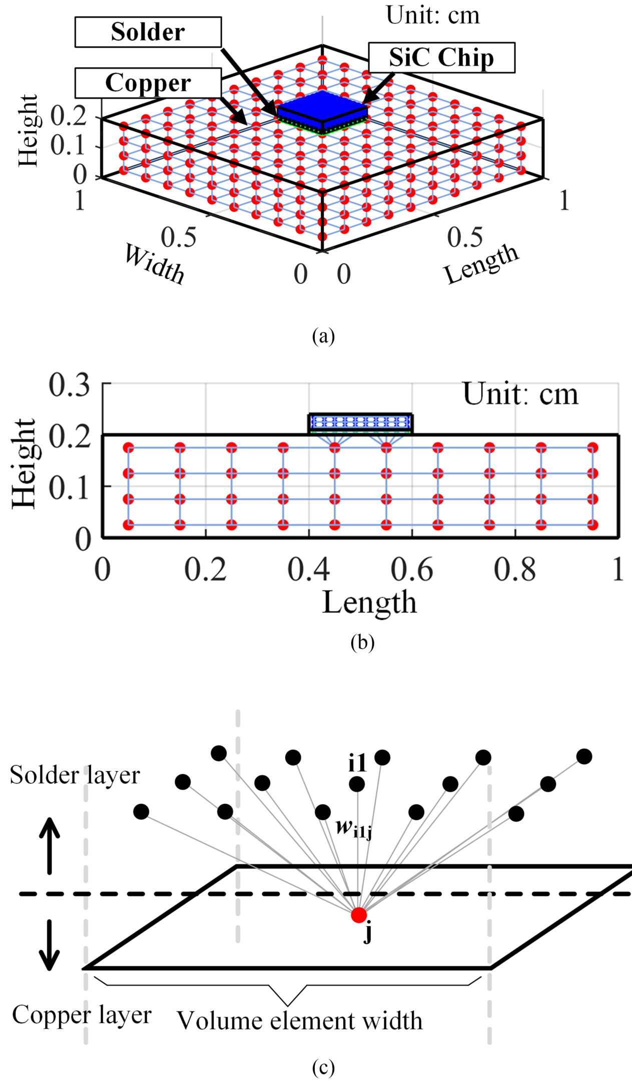


Fig. 4. (a) Undirected graph of a single chip three-layer structure. (b) Cross-sectional view. (c) Schematic view of adjacent nodes connection between solder layer and copper layer.

In (32), i and j denote the two different contacted materials, and d represents the distance from the node at the heterogenous boundary to the boundary. Convective heat exchange between the bottom of the copper substrate and the external environment was characterized by a convective heat transfer coefficient $h_{ex} = 0.05\ W/(\text{cm}^2 \cdot K)$, while any other surfaces are considered to be thermal insulated.

B. Simulations and Comparisons of the Propose Method

Once the construction of the undirected graph was complete, the program would undergo simulation steps of obtaining the pseudo-Laplacian matrix and the corresponding p matrices, according to Fig. 3. The programs are coded using MATLAB. The 4H-SiC layer is designated as the uniform power dissipation layer and three common power dissipation signals will be conducted on it: square wave, high frequency pulse wave,

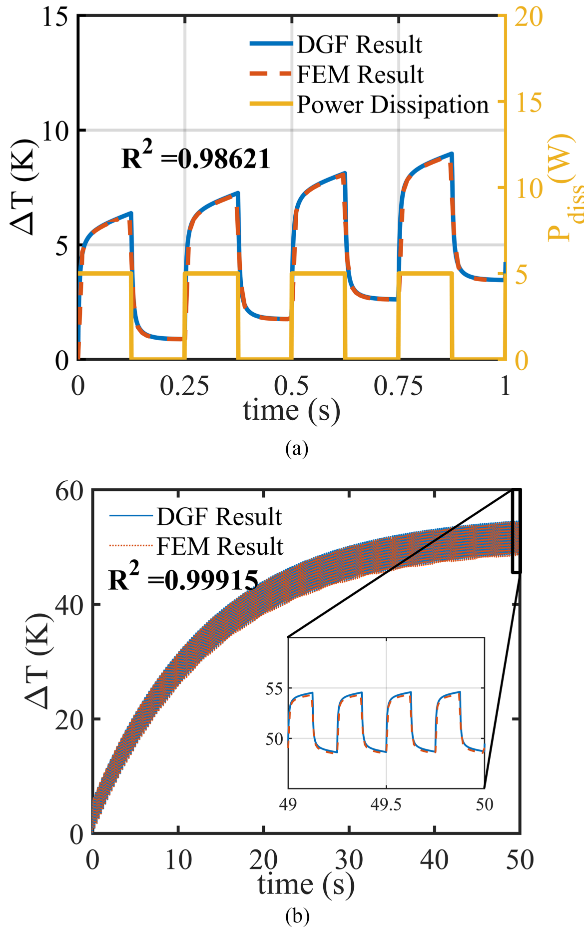


Fig. 5. (a) Response of temperature increasement under square wave power dissipation. (b) Temperature response extended to thermal steady state.

and sinusoidal wave. The accuracy of the DGF method will be verified for all scenarios, with the tested point located at the center of the chip surface on the top. Comparative validation will be achieved through a commercial FEM simulation software – COMSOL Multiphysics, which is widely accepted due to its high accuracy.

In the FEM simulation, the physical structure and the configuration of power dissipation are constructed exactly the same with those in the DGF method. The relative tolerance and the time step of the FEM simulation were adjusted to obtain an acceptable result curve. The computed results from the DGF method would be compared with those from COMSOL by the value of R-squared (Coefficient of determination). R-squared values are calculated

$$R^2 = 1 - \frac{\sum_i (y_i - f_i)^2}{\sum_i (y_i - \bar{y})^2}. \tag{33}$$

Here, y_i and f_i refer to the results of COMSOL and DGF, respectively. $\bar{y}$ refers to the mean value of y_i.

Square wave power dissipation signals, as Fig. 5(a) shows, are common in inverters and dc–dc circuits. For DGF simulation, since the steps of square waves are steep, sampling intervals t_S should be small to achieve a required accuracy. In this

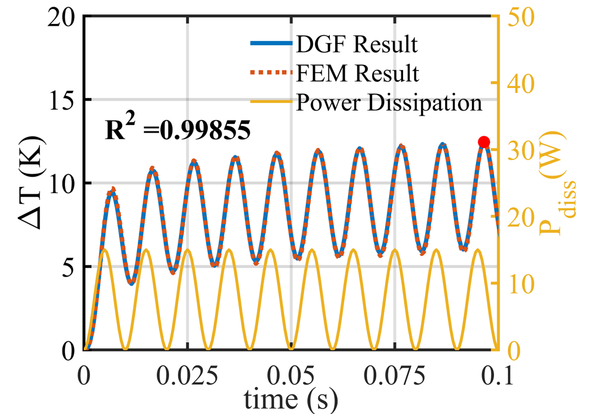


Fig. 6. Response of temperature increasement under sinusoidal wave power dissipation. (The red dot indicates the point where the temperature distribution of Fig. 9 is extracted).

simulation, sampling interval t_S is set to be 1 ms. For FEM simulation, a relative tolerance of 0.01 was configured to obtain a proper solution, and the time step is 10 ms, which means the time steps DGF calculated are ten times of FEM.

Fig. 6 illustrated the comparison of computational time between DGF and FEM at about the same node numbers, which are 735 for DGF and 900 for FEM. Despite the larger quantity of time steps, DGF still shows tremendous reduction on time consumption. In Fig. 6, the blue and red bar represent the computational time of DGF and FEM, respectively, and the blue and red line on the top represent the amount of time steps. In the case of square wave, the computational time of DGF was reduced to less than a quarter compared to FEM. While the R square still maintained at a high value of 0.986, witnessing no degeneracy of accuracy. Fig. 5(b) shows the temperature response extended to thermal steady state. Though the system requires approximately 50 s to reach the steady state, the overall R^2 value remains at a very high value. The deviation of the DGF results from the steady-state temperature response has increased slightly compared to the first second of the simulation, which is approximately 0.2K.

Such profound improvement was also observed in the cases of high frequency pulse wave and sinusoidal wave. Both of these cases are also aiming to simulate the power dissipation of real circuits such as pulse-width modulation (PWM) and rectifiers.

The result of the pulse wave with a high frequency of 1 kHz is shown in Fig. 7. Despite the unchanged peak value and duty cycle of 50% compared with the former square wave, greatly increased frequency yields a rapidly changed temperature response, which leads to a higher demand for accuracy. Since then, FEM simulation needs to be setting in a quite low relative tolerance of 0.0001 to reach the expected accuracy. As for DGF simulation, only the sampling interval needs to be adjusted. The t_S of 0.01 ms was used to cope with the increased frequency, which is also ten time smaller than FEM. However, as Fig. 6 showed, DGF remains a much lower computational time compared to FEM, while still maintain high consistency with R square value of 0.997.

In the sinusoidal wave case, the high efficiency of DGF is revealed more obviously, as Fig. 8 showed. Since the sinusoidal

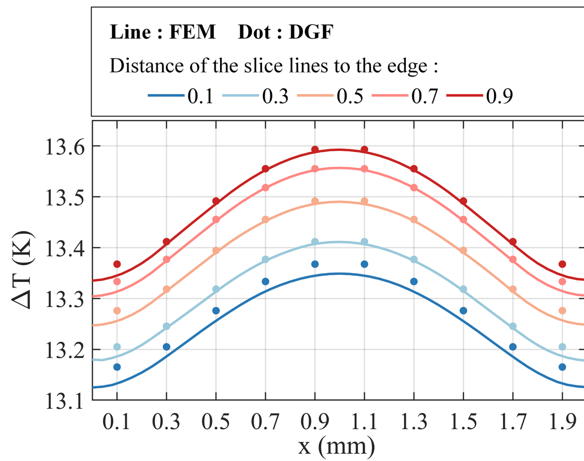


Fig. 7. Surface temperature distribution extracted from the red point of Fig. 8.

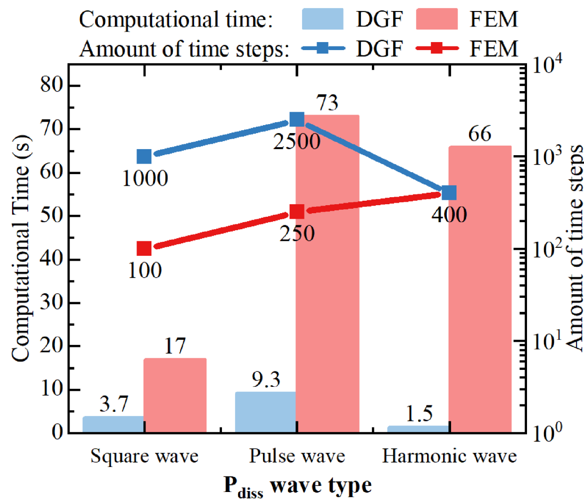


Fig. 8. Comparison of computational time between DGF and FEM. The lines indicate the amounts of time steps in each test scenarios.

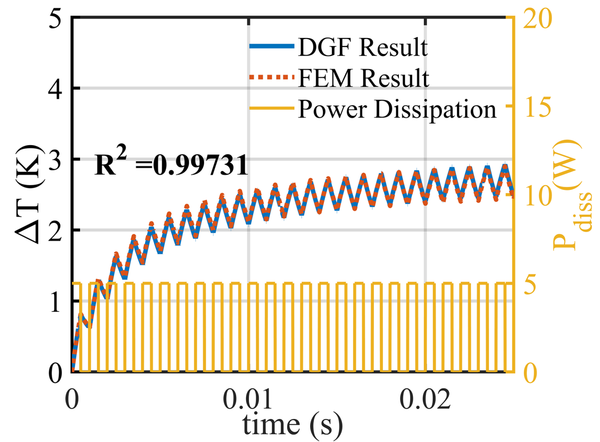


Fig. 9. Response of temperature increasement under high frequency pulse wave power dissipation.

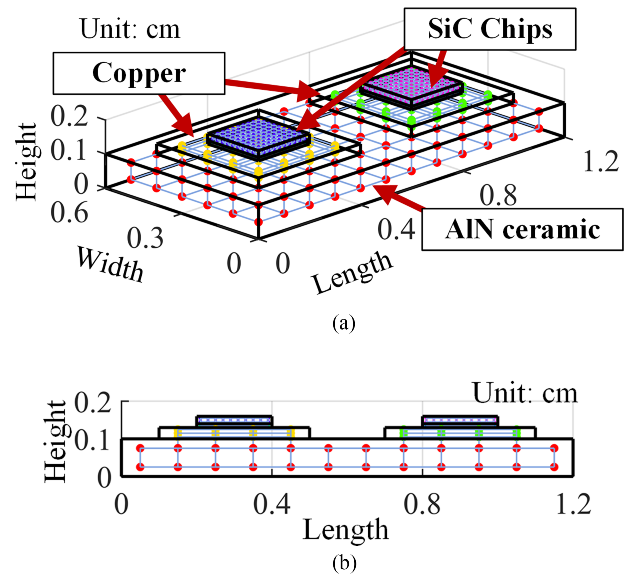


Fig. 10. (a) Undirected graph of the double chip structure. (b) Cross-sectional view.

wave has no "sharp" or "steep" wave change, there is no reason to increase the amount of time steps. On the other hand, FEM still need to maintain a low relative tolerance of 0.0001 due to the oscillating wave forms. Therefore, the computational time of the DGF method is orders of magnitude lower than FEM and still by the way, the R squared value of 0.9985 proved that high accuracy is preserved. Additionally, increasing the number of discrete nodes in the DGF method leads to even higher accuracy, indicating that the results obtained by the DGF method converge to the exact solution of the real physical model.

The extraction of the chip surface temperature distribution under sinusoidal power waveform is presented in Fig. 9. The red dot in Fig. 8 indicates where the extractin g point locates. In this figure, the data extracted along a surface slice line parallel to the chip edges are represented by solid lines (FEM results) and dots (DGF results). As shown, while there is a slight deviation of no more than 0.05K at the chip edges, the DGF results align well with FEM in the central regions, demonstrating the DGF method's capability to accurately capture nonuniform temperature distributions on the chip surface.

C. Simulation of Double Chip Structure With Thermal Coupling

In power modules, like bridge or six-pack, chips may be bonded on one single substrate, which caused thermal coupling effect. Commonly used thermal network can hardly characterize this kind of effect, while DGF method has the capability as this subsection will prove.

The double chip structure was constructed as Fig. 10 showed. This structure is intended to simulate a micro part of a power module under DBC packaging. In Fig. 10, two SiC chips were soldered on two different copper layers as the upper copper of the DBC structure. These copper layers were bonded on the same ceramic layer, which consists of AlN. Interlayer heat transfer was set to be ideal, conforming (32). The bottom of the ceramic layer is exposed to a large convective heat transfer coefficient $h_{ex} = 1.0\ W/(\text{cm}^2 \cdot K)$, since the ceramic layer

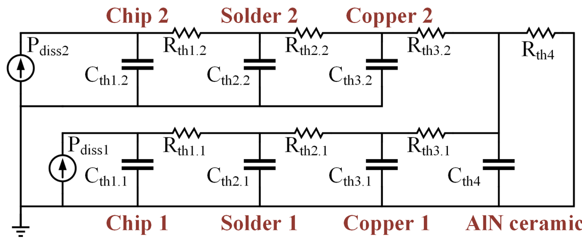


Fig. 11. Cauer thermal network constructed for the double chip structure.

TABLE II
PARAMETERS OF THE CAUER MODEL IN FIG. 11

Number	Thermal Resistance R_{th} (K/W)	Thermal Capacitance C_{th} (mJ/K)
1.1 and 1.2	0.162	1.526
2.1 and 2.2	0.600	0.304
3.1 and 3.2	0.224	9.527
4	0.333	104.2
ext	1.389	None

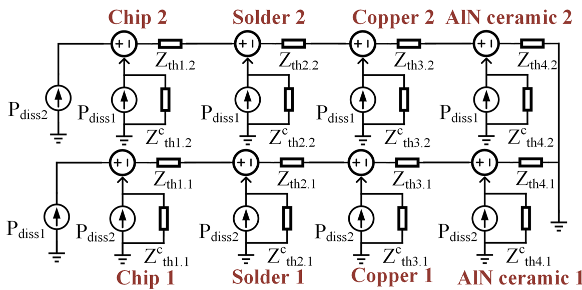


Fig. 12. Foster heat matrix model constructed for the double chip structure.

would practically be bonded on a thick copper substrate with heat sink.

A Cauer thermal network is constructed as Fig. 11 shows. It was supposed to verify its failure of taking thermal coupling effect into account, compared with DGF and FEM results. The parameters of the adopted Cauer thermal network are presented in Table II. These R_{th} and C_{th} parameters are determined using theoretical calculations and global optimizations. The upper and lower bound are defined considering the larger and smaller contact area of each layer with an additional $\pm 20\%$ margin applied, before the global optimization finding the maximum R^2 value to determine the parameters' value. The Cauer model configuration guaranteed its highest accuracy under single chip scenario.

Besides, we adopted Foster heat matrix model as a frequently used compact thermal model dealing with thermal coupling effect. The main reference for this approach is presented by Bahman et al. [12]. The constructed Foster model is presented in Fig. 12. This model introduces power inputs representing thermal coupling into the coupling thermal impedance $Z^c{}_{\mathrm{th}}$, based on the physical layers of the structure. Each thermal impedance Z_{th} and coupling thermal impedance $Z^c{}_{\mathrm{th}}$ is a second-order Foster model. The parameters for Z_{th} and $Z^c{}_{\mathrm{th}}$ were determined

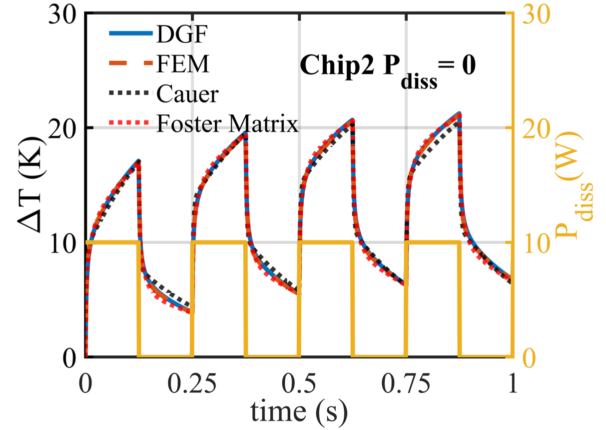


Fig. 13. Temperature response of four methods when chip 1 was turned ON and chip 2 was turned OFF.

TABLE III
R-SQUARED VALUES FOR THE THREE METHODS COMPARED TO FEM

Model Type	Chip 1	Chip 2
DGF	0.9988	0.9994
Foster Matrix Model	0.9952	0.9968
Cauer Model	0.4970	0.6626

via FEM simulations by extracting transient thermal impedance data from specific points in each layer and fitting these results to obtain the resistance and capacitance values.

The curves in Fig. 13 indicates the temperature responses of four different methods, under the single chip being turned ON scenario. Cauer model under this scenario was optimized and managed to obtain the result consistent with FEM. Foster matrix model under this scenario extracted thermal impedance parameters from FEM result. After that, the adopted models of these four methods underwent the double chip scenario, remaining their parameters unchanged. When square wave power was alternately operated on the two chips, as Fig. 14 shows, the temperature response of DGF and Foster matrix model are consistent with that of FEM, but the response of Cauer model deviated distinctly since the second chip was turned ON. From Table III, it can be statistically quantified that the DGF has the highest R squared values among the three methods. Fig. 14(b) shows that the DGF method best simulates the temperature response during the turn OFF period. It clearly illustrated that DGF method perfectly expressed the effect of thermal coupling. Besides, by comparing with the Foster matrix method, which relies on FEM simulations to extract thermal impedance parameters, the DGF method is entirely independent of FEM. All parameters used in the DGF method have clear physical significance, avoiding the complexity of parameter extraction.

Above all, the simulations arranged in this article demonstrated that the DGF method can not only be faster to capture an accurate result than FEM, but also be distinguished in dealing with complex multichip scenarios, which theoretically means

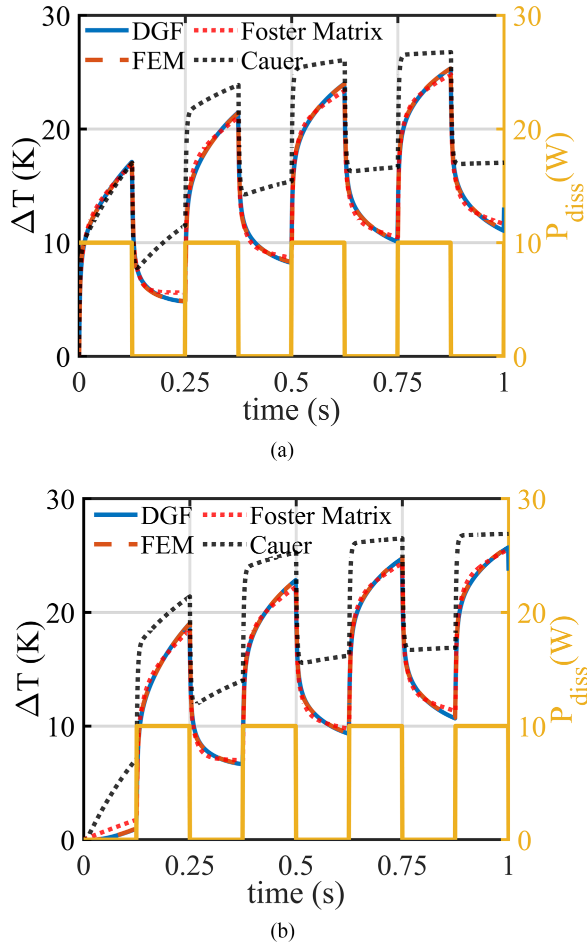


Fig. 14. Temperature response of four methods when both chips are turned ON. (a) Temperature response of chip 1. (b) Temperature response of chip 2.

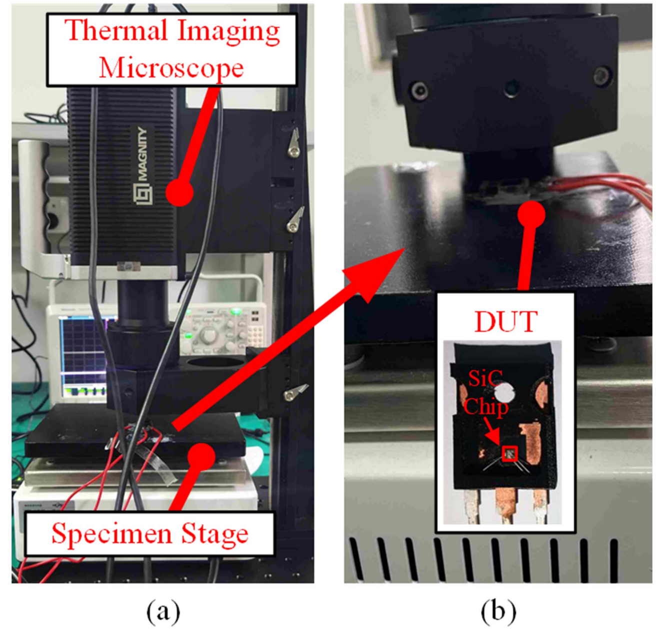
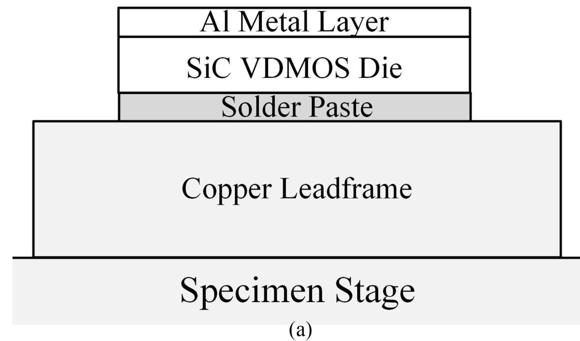


Fig. 15. Equipment setups for the infrared Thermography measurement experiment. (a) Overall view of the setups. (b) Device under test was placed on the specimen stage with thermal grease.



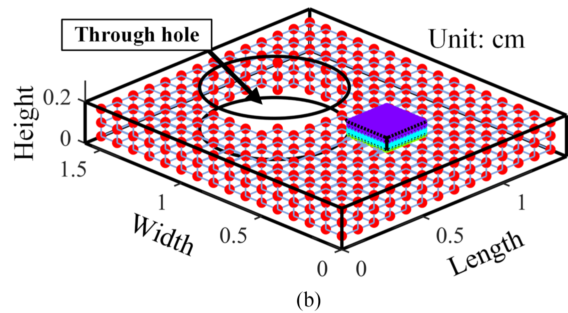


Fig. 16. (a) Vertical structure of the device in the IRT measurement. (b) Corresponding undirected graph set up for experiment validation.

that DGF method is capable of power electronic thermal prediction application.

IV. Experimental Validation

To validate the feasibility and accuracy of the DGF method in practical applications, a transient temperature test experiment was designed for a silicon carbide MOSFET. The experiment employed a commercial 1200 V 160 mΩ SiC VDMOS. An infrared thermography (IRT) microscope MAG-F7 [see Fig. 15(a)] was used to monitor the variation of temperature distribution as the chip self-heated to thermal steady-state under specific power input.

The tested chip is a discrete device under TO-247 packaging. Infrared thermography requires the removal of the external packaging case and internal encapsulation of the tested sample using lasers, exposing the SiC VDMOS die. The sample after laser decapsulation is depicted in Fig. 15(b). The exposed device sample was placed on the specimen stage with thermal grease, as Fig. 15(b) shows, where the specimen stage can control the temperature and maintain a constant temperature during the test. The vertical layered structure of the device during the experiment has been illustrated in Fig. 16(a). The heat flow path extends from the die downward to the constant temperature specimen stage, with the remaining unmarked areas representing air. Since the heat transfer coefficient between solids and air is very low, it can be practically neglected compared to the well-contacted specimen stage. Therefore, in the DGF modeling, all boundaries except the bottom of the copper substrate can be considered as thermal insulated. Reliable temperature measurement in thermal

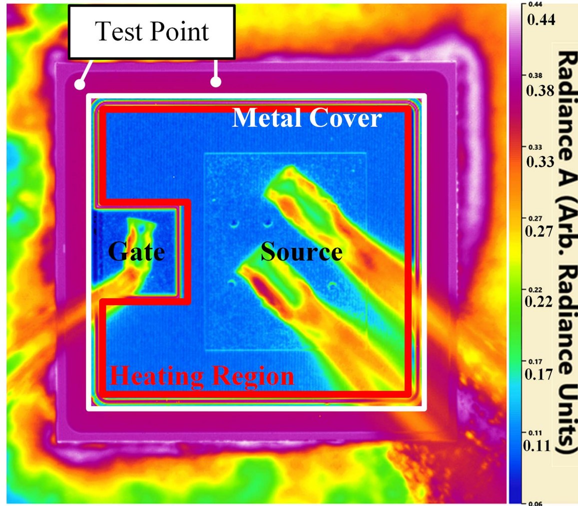


Fig. 17. Surface Radiance of the SiC VDMOS chip at 70 °C.

TABLE IV
VALUES OF PHYSICAL PARAMETERS (@70 °C)

Material types	Coefficient of Thermal Conductivity k (W/(cm · K))	Specific Heat Capacity c (J/(g · K))	Density ρ (g/cm^3)
4H-SiC (n-Type)	3.2	0.75	3.21
Solder (SAC305)	0.58	0.232	7.4
Copper	3.96	0.392	8.96
Aluminum	2.40	0.92	2.7

imaging requires a certain surface emissivity of the sample. At lower temperatures, the surface emissivity of the sample is very low, being less than 0.1 at room temperature. Therefore, in this experiment, the specimen stage is temperature-controlled to maintain the chip's initial state at a constant temperature of 70 °C to meet the required surface emissivity. The surface emissivity of the chip at 70 °C is depicted in Fig. 17. The blue area represents the low-emissivity metal cover layer, while the purple area corresponds to the uncovered high-emissivity SiC semiconductor. Inaccurate temperature measurements may result from excessively low emissivity. Therefore, sampling points need to avoid these blue areas, and are positioned at the termination area as Fig. 17 marked. The region outlined by the red lines indicates the cell region beneath the metal layer. This region is where the chip internally generates heat.

Fig. 16(b) depicts the undirected graph established for the sample structure. The physical parameters utilized in the model with the DGF method are presented in Table IV, while the structural parameters are detailed in Table V. Heat transfer between layers of heterogeneous materials is assumed to be ideal. As most of the epoxy resin encapsulation is removed from the sample during the experiment, and epoxy resin possesses a relatively low thermal conductivity and specific heat capacity, the model considers the negligible impact of epoxy resin.

TABLE V
MODEL PARAMETERS OF THE DEVICE

Parameter		Value	Unit
Copper leadframe	Length	1.4	cm
	Width	1.6	cm
	Thickness	0.2	cm
SiC die	Length	0.24	cm
	Width	0.24	cm
	Thickness	350	μm
Solder thickness		75	μm
Al metal layer thickness		150	μm
Heating Area		0.0346	cm^2

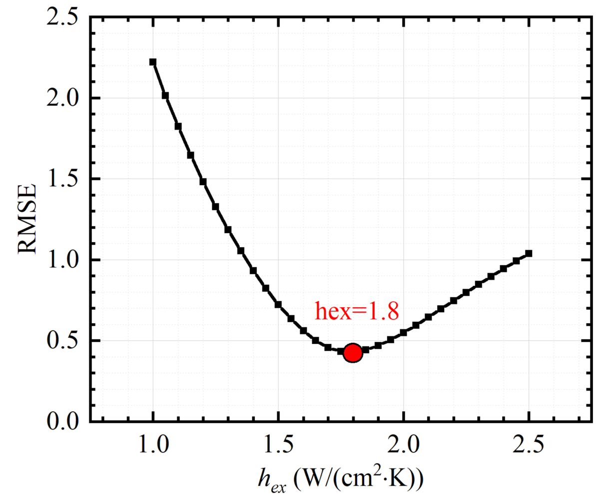


Fig. 18. RMSE between the DGF model and the experimental results under different values of h_{ex}.

The copper leadframe was in contact with the specimen stage through a manually applied layer of thermal grease. However, owing to the unknown thickness of the thermal grease layer, it is not modeled. Besides, since the grease is manually applied, there might be voids and bubbles within the layer, which strongly effected the thermal conductivity. As a result, the heat transfer coefficient h_{ex} cannot be theoretically calculated. Instead, its value was determined by fitting the DGF model to experimental data obtained from infrared thermography measurements under operating conditions of Vgs = 8 V and Vds = 3 V. As shown in Fig. 18, the root-mean-square error (RMSE) between the DGF model and the experimental results was evaluated using (34) for different values of h_{ex}

$$\text{RMSE} = \sqrt{\sum_{i=1}^{n} \frac{(f_i - y_i)^2}{n}}. \tag{34}$$

Here, y_i and f_i refer to the results of experiment and DGF, respectively. The value of h_{ex} corresponding to the minimum RMSE, 1.8 W/(cm^{2}K), was selected for the model.

The IRT experiment employed two dc voltage source. The first one provides a constant drain-source voltage to the VDMOS. The other one was applied to the gate-to-source to control the

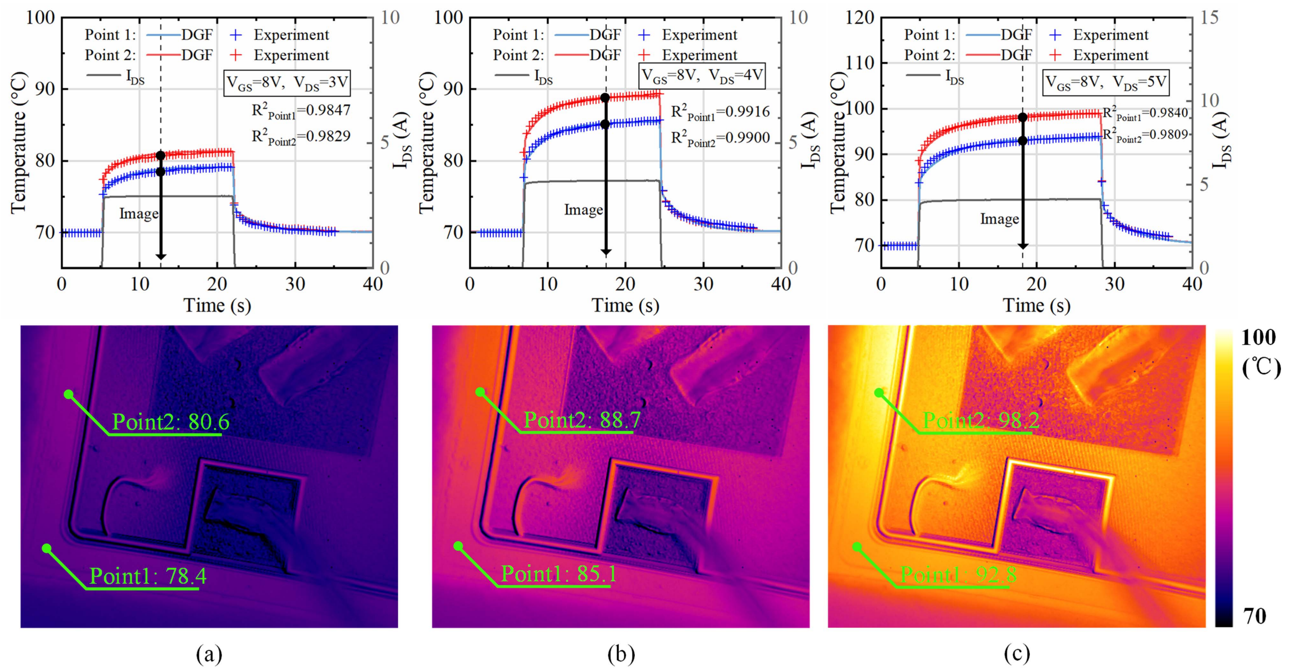


Fig. 19. Comparisons between experimental and DGF-simulated results. The upper graphs represent the temperature response of two points on the SiC chip and I_{DS} are expressed by gray curves. The lower images are the IRT outputs at specific time marked in the upper graphs by the dashed lines. Applied voltages: (a) $V_{DS} = 3\,V$, (b) $V_{DS} = 4\,V$, (c) $V_{DS} = 5\,V$.

switching process. The sample was placed on the stage under the initial temperature of 70 °C. Upon applying a gate-to-source voltage of 8 V, the VDMOS transitioned from the OFF-state to the ON-state, resulting in a rapid increase in drain current to a certain level, as depicted by the I_{DS} curve in Fig. 19 and generated power on the chip. The dissipated power was considered uniformly distributed over the cell area of the VDMOS, as indicated by the red frame in Fig. 17, which is mapped into the model according to the measurement data in simulation. It should be noted that the I_{DS} curve in Fig. 19 was not directly measured from the experiment but obtained by Gaussian filtering of the experimental measurements. The chip, under this power dissipation, started from 70 °C and gradually rose to a steady-state temperature, then transitioned from the ON-state to the OFF-state, cooling down from the higher temperature to 70 °C. The entire process is simulated using the DGF method.

Three different conditions of applied voltages are tested and simulated and Fig. 19 shows the results. In Fig. 19, the upper graph represents the temperature responses under different drain-source voltages which are 3 V, 4 V, and 5 V, respectively. The lower 3 images are the corresponding IRT images, with the specific test point marked on it. Great consistency is revealed between the experimental and simulated results. R-square values are all higher than 0.98. This outcome proved that DGF method is capable to achieve a desirable accuracy in practical temperature monitoring.

V. Conclusion

In this article, a new thermal model based on DGF is presented as a high speed, high accuracy, and flexible 3-D modeling method. This model discretizes the physical structure of a device or module into an undirected graph, calculates the corresponding DGFs by extracting the Laplacian matrix of the graph, and uses a fast matrix algorithm to obtain temperature responses. To address the multilayer packaging structures in power devices and chips, this article introduces the pseudo-Laplacian matrix, improving the DGF method to handle structures with multiple layers of different materials. In addition, a detailed algorithm for implementing the DGF method is provided. The proposed algorithm simplifies the traditional integral-based DGF approach into pure matrix multiplication, significantly enhancing computational efficiency. Validation of the DGF method's accuracy and speed is conducted using a simulated TO-packaged chip structure. Comparisons with FEM simulations demonstrate that the proposed DGF achieves high accuracy while reducing computation time by 78%. The simulation also illustrates the DGF method's capability to represent nonuniform temperature distributions on the chip. Furthermore, the article explores the DGF method's ability to address multichip thermal coupling problems. A simulated module structure containing two chips is analyzed, comparing the results of DGF, Cauer thermal network, and Foster matrix thermal network models. The proposed DGF method shows superior accuracy and highlights the advantage that it does not require parameter extraction, ensuring the physical realism of its modeling parameters. Finally, this article presents an experiment designed to test the time-varying temperature distribution of a SiC VDMOS using infrared thermography, validating the feasibility and accuracy of the DGF method in practical applications. The experiment includes temperature recordings at two different locations under three operating conditions, demonstrating a high level of consistency between

the DGF results and experimental outcomes. In the authors' further research, nonlinear models will be explored to achieve high accuracy across a wide temperature range under extreme chip operating conditions. Additionally, to extend the method to large circuits, studies will focus on reducing the number of nodes and computational budget by investigating nonorthogonal undirected graphs.

References

[1] C. Buttay et al., "State of the art of high temperature power electronics," *Mater. Sci. Eng. B*, vol. 176, no. 4, pp. 283–288, Mar. 2011, doi: 10.1016/j.mseb.2010.10.003.

[2] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[3] H. Wang and F. Blaabjerg, "Power electronics reliability: State of the art and outlook," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6476–6493, Dec. 2021, doi: 10.1109/JESTPE.2020.3037161.

[4] G. Romano et al., "A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 978–987, Sep. 2016, doi: 10.1109/JESTPE.2016.2563220.

[5] C. Qian et al., "Thermal management on IGBT power electronic devices and modules," *IEEE Access*, vol. 6, pp. 12868–12884, 2018, doi: 10.1109/ACCESS.2018.2793300.

[6] R. Green, D. P. Urciuoli, and A. J. Lelis, "Short-circuit robustness testing of SiC MOSFETs," *Mater. Sci. Forum*, vol. 897, pp. 525–528, May 2017, doi: 10.4028/www.scientific.net/MSF.897.525.

[7] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET reliability and implications for qualification testing," in *Proc. IEEE Int. Rel. Phys. Symp.*, Monterey, CA, USA, Apr. 2017, pp. 2A–4.1–2A–4.4, doi: 10.1109/IRPS.2017.7936256.

[8] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power IGBT modules considering heat coupling effects," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, Shanghai, China, Nov. 2014, pp. 1382–1387. doi: 10.1109/PEAC.2014.7038066.

[9] T. Poller, S. D'Arco, M. Hernes, and J. Lutz, "Influence of thermal cross-couplings on power cycling lifetime of IGBT power modules," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, pp. 1–6.

[10] Y. Zhao et al., "Electrical-thermal coupling modeling of SiC MOSFETs based on field-circuit coupling and its application in junction temperature calculation during surges," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 2651–2667, Feb. 2025, doi: 10.1109/TPEL.2024.3493382.

[11] C. Entzminger, W. Qiao, L. Qu, and J. L. Hudgins, "A high-accuracy, low-order thermal model of SiC MOSFET power modules extracted from finite element analysis via model order reduction," in *Proc. IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, USA, Sep. 2019, pp. 4950–4954. doi: 10.1109/ECCE.2019.8912839.

[12] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3-D-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050–1063, Sep. 2016, doi: 10.1109/JESTPE.2016.2531631.

[13] A. S. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018, doi: 10.1109/TPEL.2017.2694548.

[14] K. Górecki and P. Górecki, "Nonlinear compact thermal model of the IGBT dedicated to SPICE," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13420–13428, Dec. 2020, doi: 10.1109/TPEL.2020.2995414.

[15] P. Górecki and K. Górecki, "Measurements and computations of internal temperatures of the IGBT and the diode situated in the common case," *Electronics*, vol. 10, no. 2, Jan. 2021, Art. no. 210, doi: 10.3390/electronics10020210.

[16] K. Heng, X. Yang, X. Wu, and J. Ye, "A 3-D thermal network model for monitoring of IGBT modules," *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 653–661, Feb. 2023, doi: 10.1109/TED.2022.3227004.

[17] H. Wang et al., "A thermal network model for multichip power modules enabling to characterize the thermal coupling effects," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6225–6245, May 2024, doi: 10.1109/TPEL.2024.3355207.

[18] X. Yang, S. Xu, K. Heng, and X. Wu, "Distributed thermal modeling for power devices and modules with equivalent heat flow path extraction," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5863–5876, Dec. 2023, doi: 10.1109/JESTPE.2023.3321210.

[19] J. Reichl, J. M. Ortiz-Rodriguez, A. Hefner, and J. -S. Lai, "3-D thermal component model for electrothermal analysis of multichip power modules with experimental validation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3300–3308, Jun. 2015, doi: 10.1109/TPEL.2014.2338278.

[20] C. H. Van Der Broeck, L. A. Ruppert, A. Hinz, M. Conrad, and R. W. De Doncker, "Spatial electro-thermal modeling and simulation of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 404–415, Jan. 2018, doi: 10.1109/TIA.2017.2757898.

[21] Y. Zhan and S. S. Sapatnekar, "High-efficiency green function-based thermal simulation algorithms," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 26, no. 9, pp. 1661–1675, Sep. 2007, doi: 10.1109/TCAD.2007.895754.

[22] F. L. T. Maggioni, V. Cherman, H. Oprins, E. Beyne, I. De Wolf, and M. Baelmans, "Convolution-based fast thermal model for 3-D-ICs: Transient experimental validation," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 7, no. 2, pp. 221–228, Feb. 2017, doi: 10.1109/TCPMT.2016.2638829.

[23] V. Sodan, S. Stoffels, H. Oprins, M. Baelmans, S. Decoutere, and I. De Wolf, "Distributed electro-thermal model based on fast and scalable algorithm for GaN power devices and circuit simulations," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, Sapporo, Japan, May 2017, pp. 179–182. doi: 10.23919/ISPSD.2017.7988948.

[24] V. Sodan et al., "Fast and distributed thermal model for thermal modeling of GaN power devices," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 8, no. 10, pp. 1747–1755, Oct. 2018, doi: 10.1109/TCPMT.2018.2808680.

[25] Y. Guo, G. Huang, and W. V. Liu, "A new semi-analytical solution addressing varying heat transfer rates for U-shaped vertical borehole heat exchangers in multilayered ground," *Energy*, vol. 274, Jul. 2023, Art. no. 127373, doi: 10.1016/j.energy.2023.127373.

[26] F. Chung and S. -T. Yau, "Discrete green's functions," *J. Combinatorial Theory, Ser. A*, vol. 91, no. 1-2, pp. 191–214, 2000.

[27] K. D. Cole, A. Riensche, and P. K. Rao, "Discrete green's functions and spectral graph theory for computationally efficient thermal modeling," *Int. J. Heat Mass Transfer*, vol. 183, Feb. 2022, Art. no. 122112, doi: 10.1016/j.ijheatmasstransfer.2021.122112.

[28] K. D. Cole, M. R. Yavari, and P. K. Rao, "Computational heat transfer with spectral graph theory: Quantitative verification," *Int. J. Thermal Sci.*, vol. 153, Jul. 2020, Art. no. 106383, doi: 10.1016/j.ijthermalsci.2020.106383.

[29] K. Cole, J. Beck, A. Haji-Sheikh, and B. Litkouhi, *Heat Conduction Using Greens functions*. Boca Raton, FL, USA: CRC Press, 2010, pp. 63–70.