Comprehensive Analysis of Buck Mode Frozen Leg Operation for Three-Phase Dual Active Bridge Converters

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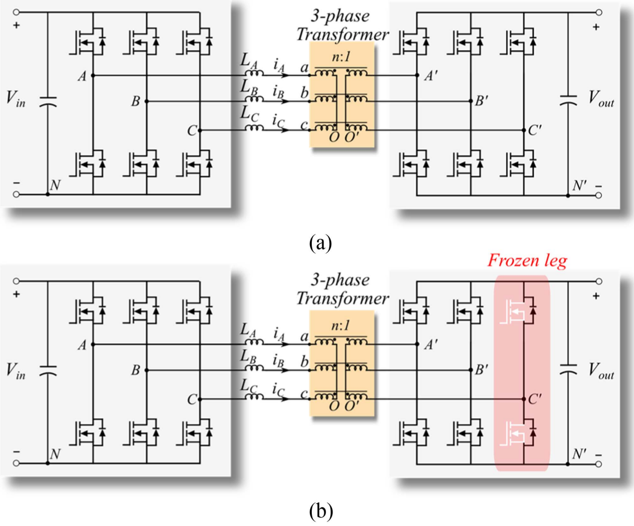
***Abstract*—The three-phase dual-active-bridge converter exhibits an inherent fault-tolerant capability for addressing open-circuit failures (OCFs). The frozen leg method is a notable fault-tolerant technique that mitigates OCFs without additional hardware. Upon OCF detection, this method deactivates the two switches in the faulty leg, enabling the converter to maintain operation at a reduced power level. However, all previous research on the frozen leg method assumes unity voltage gain. Yet, in practical applications, nonunity voltage gain, such as buck operation, is often unavoidable, wherein the voltage, current, and power characteristics significantly deviate from those at unity voltage gain. Thus, this article performs the first investigation of the more complex buck mode of frozen leg operation, and finds the operation must be categorized into three cases. The theoretical analysis derives the voltage, current, and power expressions for these cases, revealing significant deviations from those associated with unity voltage gain. Based on the derived current expressions, a detailed soft-switching analysis for the buck mode is also conducted. Furthermore, the theoretical maximum transferred power in buck mode under the frozen leg operation is proposed, and unique findings for power transfer at zero phase shift are examined. The theoretical analyses are validated through extensive experimental testing.**

***Index Terms*—DC–DC converter, fault tolerance, reliability and diagnostics.**

I. INTRODUCTION

INTRODUCED in the 1990s, the single-phase dual-active-bridge (1p-DAB) converter emerged as an efficient and compact solution for dc–dc power conversion [1], [2]. Concurrently proposed, the three-phase DAB (3p-DAB) converter features an expanded topology with two additional legs, as shown in Fig. 1(a), and can, thus, generate more voltage levels and reduce input and output current ripple. This configuration leads to its advantages of improved power density, lower electromagnetic interference, and smaller filter capacitor size compared with the 1p-DAB [3], [4], [5], [6]. These characteristics make the 3p-DAB converter particularly suitable for high-power-density applications, such as the solid-state transformer in dc distribution grids [7], [8], [9], [10], the power interface in naval vessels, railway auxiliary systems, and electric aircraft [11], [12], [13], [14], the battery-driven interface in energy storage systems [15], [16], the onboard charger and auxiliary power module (APM) in electric vehicles [3], [17], [18], and photovoltaic systems [19].



(a)

(b)

Fig. 1. (a) 3p-DAB converter. (b) Its frozen leg operation.

Despite these advantages, the 3p-DAB converter's inherently higher number of switches increases the risk of switch failures, as well as associated gate driver failures [20]. Nevertheless, this increased number of switches also enhances the fault-tolerant capability of the 3p-DAB, allowing it to maintain power transmission even under certain fault conditions, thereby improving overall system reliability [21], [22].

A survey conducted within the power electronics industry revealed significant insights into the sources of component failures [23]. The findings indicated that 15% of failures are attributed to issues related to gate drivers, which lead to the loss of switch control and open-circuit failures (OCFs) [23]. Additionally, 31% of component failures are linked to semiconductor device failures, which are further categorized into short-circuit failures (SCFs) and OCFs [21]. For 3p-DAB converters, addressing SCFs requires prompt detection mechanisms to identify sudden

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large inrush currents, a need best met through hardware-based protection strategies integrated into the gate driver circuit [21], [24]. In contrast, the impact of OCFs in 3p-DAB converters is less severe than that of SCFs, as the converter can continue to operate at partial power under OCF conditions [22], [24], [25]. The recommended method is to diagnose the faulty switch exhibiting the OCF and then implement a fault-tolerant control strategy, thereby allowing continued power flow until repairs can be undertaken.

Extensive research has been conducted on diagnosing OCFs in 1p-DAB [26], [27], [28], [29], [30], [31] and 3p-DAB converters [21], [24], [32], [33], [34], [35], [36]. For 3p-DAB converters, Khan and Wen [24] presented a comprehensive analysis comparing all pertinent methods, and proposes a novel OCF diagnosis method using a low-cost diagnostic circuit that achieves the fastest diagnosis time reported to date.

Following OCF diagnosis, it is essential to implement fault-tolerant control strategies to mitigate the detrimental impacts of OCFs. Research on fault-tolerant strategies for OCFs in DAB-type converters can be delineated into two primary categories. The first category focuses on enhancing system redundancy through the integration of additional hardware or the reconfiguration of the existing topology. For example, Bhakar and Jayaraman [37] incorporated an additional fault-tolerant capacitor and a rapid fuse in series with the transformer to facilitate fault tolerance in a 1p-DAB converter, and Shi et al. [38] reconfigured the 1p-DAB topology by employing a central-tapped transformer and two symmetrical auxiliary inductors to achieve fault tolerance. Berger et al. [36] incorporated three extra bidirectional switches between the transformer and primary-side converter. By opening the bidirectional switch of the faulty phase, the switches and antiparallel diodes in this phase can be entirely isolated from the original 3p-DAB topology. However, these methods of hardware redundancy and topology reconfiguration increase the complexity and cost of the system [25].

Conversely, the second category emphasizes achieving fault-tolerant control without additional hardware, known as the self-embedded fault-tolerant method [39]. This category typically employs various control techniques to manage switch operations, and is the focus of this article. Various self-embedded fault-tolerant methods for DAB-type converters have been extensively studied, encompassing fault-tolerant strategies for 1p-DAB [29], [40], [41], 2/3-Level DAB [42], and current-fed 3p-DAB converters [33], [43]. However, only a few self-embedded fault-tolerant methods specifically address OCFs in 3p-DAB converters. One notable method is the frozen leg method [20], which disables the two switches in the faulty leg when an OCF has been detected, as shown in Fig. 1(b). For example, if the lower switch in leg *C*' is identified with an OCF, the gate signals of both the upper and lower switches of this leg are set to OFF. In this way, only the two antiparallel diodes in this leg remain freewheeling, allowing the converter to continue operating at reduced power.

Another approach in [32] is proposed to address OCFs in 3p-DAB by disabling more switches. This method suggests simultaneously deactivating all four switches within the faulty phase, on both primary and secondary sides. This results in four antiparallel diodes freewheeling, significantly complicating the analysis of current and voltage waveforms. The maximum power transfer of this method is lower than that of the frozen leg method due to the increased number of deactivated switches. Another self-embedded method for addressing OCFs in 3p-DAB converters is the path-based fault-tolerant method [25]. Under OCF conditions, this approach needs to adjust three variables: 1) the phase shift angle between the primary- and secondary-side bridges, 2) the phase shift angle between phases *A* and *B*, and 3) the phase shift angle between phases *B* and *C*. These adjustments enable the reconfiguration of the current path, thereby reducing current stress and increasing the maximum power transmission capability. While the implementation of this method is sophisticated due to its reliance on three control variables, optimizing these parameters can be quite difficult. Additionally, under certain operating conditions, there may be dc biases in the current that can influence magnetic-flux saturation, add stress to the switching devices, and affect overall efficiency [44].

In comparison, the frozen leg method proposed in [20] offers several advantages, including straightforward control by only needing to regulate the phase shift angle and the complete elimination of dc bias due to the symmetry between the upper and lower switches. However, the existing analysis of the frozen leg method is limited to unity voltage gain ($V_{\text{in}} = nV_{\text{out}}$) [20], but in practical applications, nonunity voltage gain operation is often unavoidable. Various factors lead to the frequent occurrence of buck ($V_{\text{in}} > nV_{\text{out}}$) and boost ($V_{\text{in}} < nV_{\text{out}}$) modes [1], [45], [46]. For instance, in battery-connected systems such as the onboard charger and APM [17], [18] and energy storage systems [15], [16], the 3p-DAB must manage significant variations in battery voltage due to changes in the battery state-of-charge, which leads to operation in buck or boost mode. In renewable energy systems [47], uncertainties in the resource output power can also lead to variations in the dc bus voltage, causing the converter to operate with nonunity voltage gain. Furthermore, in the dc microgrid of railway systems [13], the input voltage of the 3p-DAB varies by up to 700 V, also necessitating buck or boost mode operation. While the unity voltage gain assumption simplifies the frozen-leg analysis, its results do not hold for nonunity gain. Thus, there is a gap in the literature regarding understanding the more complex operation of the 3p-DAB using frozen-leg control during nonunity voltage gain. Buck and boost operations under frozen-leg control are complex and require extensive distinct analyses using different analytical frameworks and mathematical models, and result in different classified cases and current modes. Therefore, this article focuses solely on the buck operation so that the analysis and findings can be presented in sufficient detail and clarity.

For the first time, this article performs a detailed analysis of the 3p-DAB converter with frozen-leg control in buck operation. The key contributions of this article are as follows.

1) The novel derivations of current and voltage expressions for 3p-DAB frozen leg operation in buck mode. Unlike the existing research that assumes unity voltage gain, this study reveals several new findings specific to buck operation. The analysis identifies three distinct cases, with the phase shift angle of the faulty phase taking on three

analytically derived values: ϕ_{FL1}, ϕ_{FL2}, and ϕ_{FL3}. A noteworthy discovery is that for the first case, ϕ_{FL1} is a fixed value determined solely by the dc-port voltages; even if the phase shift angle of the normal phases is zero, ϕ_{FL1} remains a non-zero constant value.

2) The novel investigation into the soft-switching region of the healthy switches, with the new findings showing that while the primary-side healthy switches maintain zero voltage switching (ZVS) across the entire 0° to 90° phase shift angle and 0% to 100% voltage drop, the secondary-side healthy switches do not always achieve ZVS.
3) The novel derivations of the transferred power expressions for the three cases, where the findings show that due to the changed phase shift angle of the faulty phase, the power transfer characteristics of the frozen leg method in buck mode deviate from those observed in normal operation and in frozen leg unity gain mode. Notably, even when the phase shift angle is zero, the transferred power is not zero, attributable to the constant value of ϕ_{FL1}.
4) The novel derivation of the maximum transferred power expression, with analysis of the ratio of normal to frozen leg cases under different voltage drops. It is found that as the voltage drop increases, the maximum transferred power of the frozen leg method approaches that of normal operation.

These contributions have been verified through extensive experimental testing. The rest of this article is organized as follows. Section II describes the mathematical model of the 3p-DAB and analyzes the waveforms of voltages and currents in the buck mode under normal operation. Section III derives new expressions for voltages and currents in the buck mode under frozen leg operation and analyzes the soft-switching regions for all healthy switches. Section IV derives the transferred power equations and maximum power equations for buck mode frozen leg operation. Section V introduces the experimental prototype and validates the theoretical analysis with experiments. Finally, Section VI concludes this article.

II. ANALYSIS OF NORMAL OPERATION BUCK MODE FOR 3P-DAB

A. System Description

Before analyzing the operation of the 3p-DAB converter in buck mode, it is necessary to establish a mathematical model of the system to accurately describe the phase voltages, currents, and inductor voltages. To facilitate the analysis, the three-phase transformer is assumed to be ideal, characterized by infinite magnetic inductance, equal three-phase leakage inductances ($L_A = L_B = L_C = L$), and zero winding resistances [48], as shown in Fig. 1.

Generally, only the leg voltages v_{AN}, v_{BN}, v_{CN}, $v_{A'N'}$, $v_{B'N'}$, and $v_{C'N'}$ can be directly controlled by the primary- and secondary-side dc-port voltages V_{in} and V_{out}, and corresponding switching states. Hence, to describe the phase voltages v_{AO}, v_{BO}, v_{CO}, $v_{A'O'}$, $v_{B'O'}$, and $v_{C'O'}$, the relationship between leg and phase voltages first needs to be determined, as shown in

$$\begin{cases} v_{AO} = v_{AN} - v_{ON} \\ v_{BO} = v_{BN} - v_{ON} \\ v_{CO} = v_{CN} - v_{ON} \end{cases} \tag{1}$$

$$\begin{cases} v_{A'O'} = v_{A'N'} - v_{O'N'} \\ v_{B'O'} = v_{B'N'} - v_{O'N'} \\ v_{C'O'} = v_{C'N'} - v_{O'N'}. \end{cases} \tag{2}$$

The sum of the phase voltages in the ideal transformer should be zero, i.e., $v_{AO} + v_{BO} + v_{CO} = 0$ and $v_{A'O'} + v_{B'O'} + v_{C'O'} = 0$. Therefore, by adding the three equations in (1) and (2), v_{ON} and $v_{O'N'}$ can be calculated as

$$\begin{cases} v_{ON} = \frac{v_{AN}+v_{BN}+v_{CN}}{3} \\ v_{O'N'} = \frac{v_{A'N'}+v_{B'N'}+v_{C'N'}}{3}. \end{cases} \tag{3}$$

Substituting (3) into (1) and (2), the phase voltages in primary- and secondary-side can be described by the leg voltages as

$$\begin{cases} v_{AO} = \frac{2}{3}v_{AN} - \frac{1}{3}v_{BN} - \frac{1}{3}v_{CN} \\ v_{BO} = -\frac{1}{3}v_{AN} + \frac{2}{3}v_{BN} - \frac{1}{3}v_{CN} \\ v_{CO} = -\frac{1}{3}v_{AN} - \frac{1}{3}v_{BN} + \frac{2}{3}v_{CN} \end{cases} \tag{4}$$

$$\begin{cases} v_{A'O'} = \frac{2}{3}v_{A'N'} - \frac{1}{3}v_{B'N'} - \frac{1}{3}v_{C'N'} \\ v_{B'O'} = -\frac{1}{3}v_{A'N'} + \frac{2}{3}v_{B'N'} - \frac{1}{3}v_{C'N'} \\ v_{C'O'} = -\frac{1}{3}v_{A'N'} - \frac{1}{3}v_{B'N'} + \frac{2}{3}v_{C'N'}. \end{cases} \tag{5}$$

Meanwhile, the state equations of the three-phase leakage inductors can be written as (6), where v_{LA}, v_{LB}, and v_{LC} represent the voltages of the three-phase leakage inductors, i_A, i_B, i_C are the phase currents, v_{aO}, v_{bO}, v_{cO} are the secondary-side phase voltages referred to the primary side, as shown in (7), and n is the transformer turns ratio

$$\begin{cases} v_{AO} - v_{aO} = v_{LA} = L\frac{di_A}{dt} \\ v_{BO} - v_{bO} = v_{LB} = L\frac{di_B}{dt} \\ v_{CO} - v_{cO} = v_{LC} = L\frac{di_C}{dt} \end{cases} \tag{6}$$

$$\begin{cases} v_{aO} = nv_{A'O'} \\ v_{bO} = nv_{B'O'} \\ v_{cO} = nv_{C'O'}. \end{cases} \tag{7}$$

Finally, by combining (4)–(7), the mathematical model of the 3p-DAB can thus be obtained as (8), which can analyze the phase voltages, currents, and inductor voltages

$$\begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} v_{AN} - nv_{A'N'} \\ v_{BN} - nv_{B'N'} \\ v_{CN} - nv_{C'N'} \end{bmatrix} = \begin{bmatrix} v_{LA} \\ v_{LB} \\ v_{LC} \end{bmatrix} = \begin{bmatrix} L\frac{di_A}{dt} \\ L\frac{di_B}{dt} \\ L\frac{di_C}{dt} \end{bmatrix}. \tag{8}$$

B. Normal Operation of Buck Mode in 3p-DAB

Despite the numerous modulation schemes proposed for the 3p-DAB converter, the single phase shift (SPS) modulation scheme remains the most commonly used for normal operation in various fault-tolerant strategies [20], [32], [36]. Therefore, this article also considers the SPS modulation scheme as the normal operational scheme. In SPS modulation, the three-phase

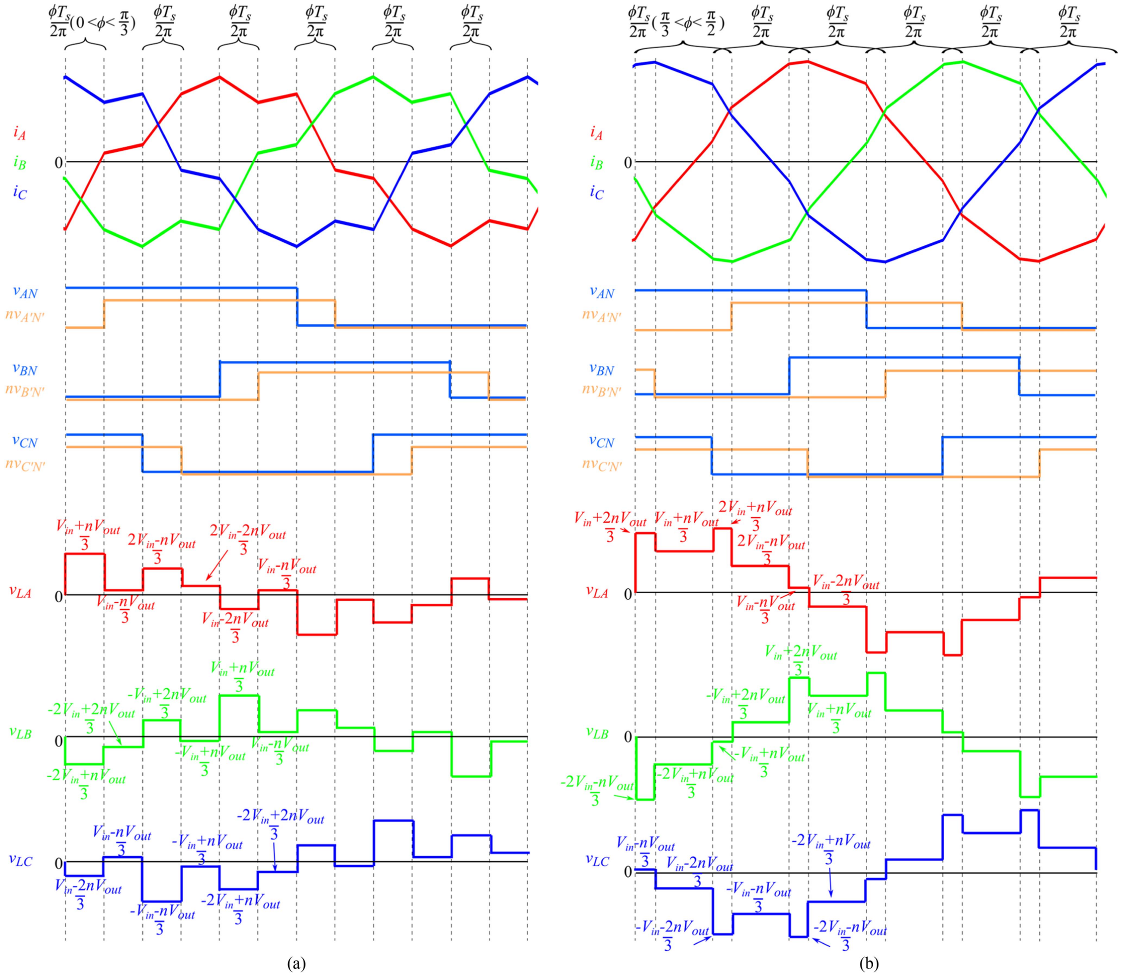


Fig. 2. Buck mode normal operation waveforms of phase currents, phase voltages, and leakage inductor voltages with phase shift angle between (a) 0 to $\pi/3$ (with $\phi = \pi/6$ as the example) and (b) $\pi/3$ to $\pi/2$ (with $\phi = 5\pi/12$ as the example).

legs of each side operate with a phase shift of 120° and a phase shift angle ϕ is introduced between the primary and secondary sides, as shown in Fig. 2. Depending on the value of phase shift angle ϕ, the waveforms within a single switching cycle can be categorized into two cases: $0 \leqslant \phi \leqslant \pi/3$ and $\pi/3 < \phi \leqslant \pi/2$.

From (8), Fig. 2(a) shows voltage and current waveforms of normal operation buck mode for $0 \leqslant \phi \leqslant \pi/3$, and Fig. 2(b) shows the same for $\pi/3 < \phi \leqslant \pi/2$. Since $V_{\text{in}} > nV_{\text{out}}$ in buck mode, v_{XN} has a higher magnitude than $nv_{X'N'}$, as shown in Fig. 2. Also, the discrepancy between V_{in} and nV_{out} prevents the inductor voltages from reaching zero, thereby producing more complex current waveforms than those observed when V_{in} and nV_{out} are equal [20].

In the normal operation of buck mode, the transferred power can be calculated by summing the power through the three-phase transformer [45], as shown in

$$P_{norm} = \begin{cases} \frac{nV_{\text{in}}V_{\text{out}}}{2\pi f_s L}\phi(\frac{2}{3}-\frac{\phi}{2\pi}), 0 \le \phi \le \frac{\pi}{3} \\ \frac{nV_{\text{in}}V_{\text{out}}}{2\pi f_s L}(\phi-\frac{\phi^2}{\pi}-\frac{\pi}{18}), \frac{\pi}{3} < \phi \le \frac{\pi}{2} \end{cases} \qquad (9)$$

where f_s is the switching frequency, which is the reciprocal of the switching period T_s.

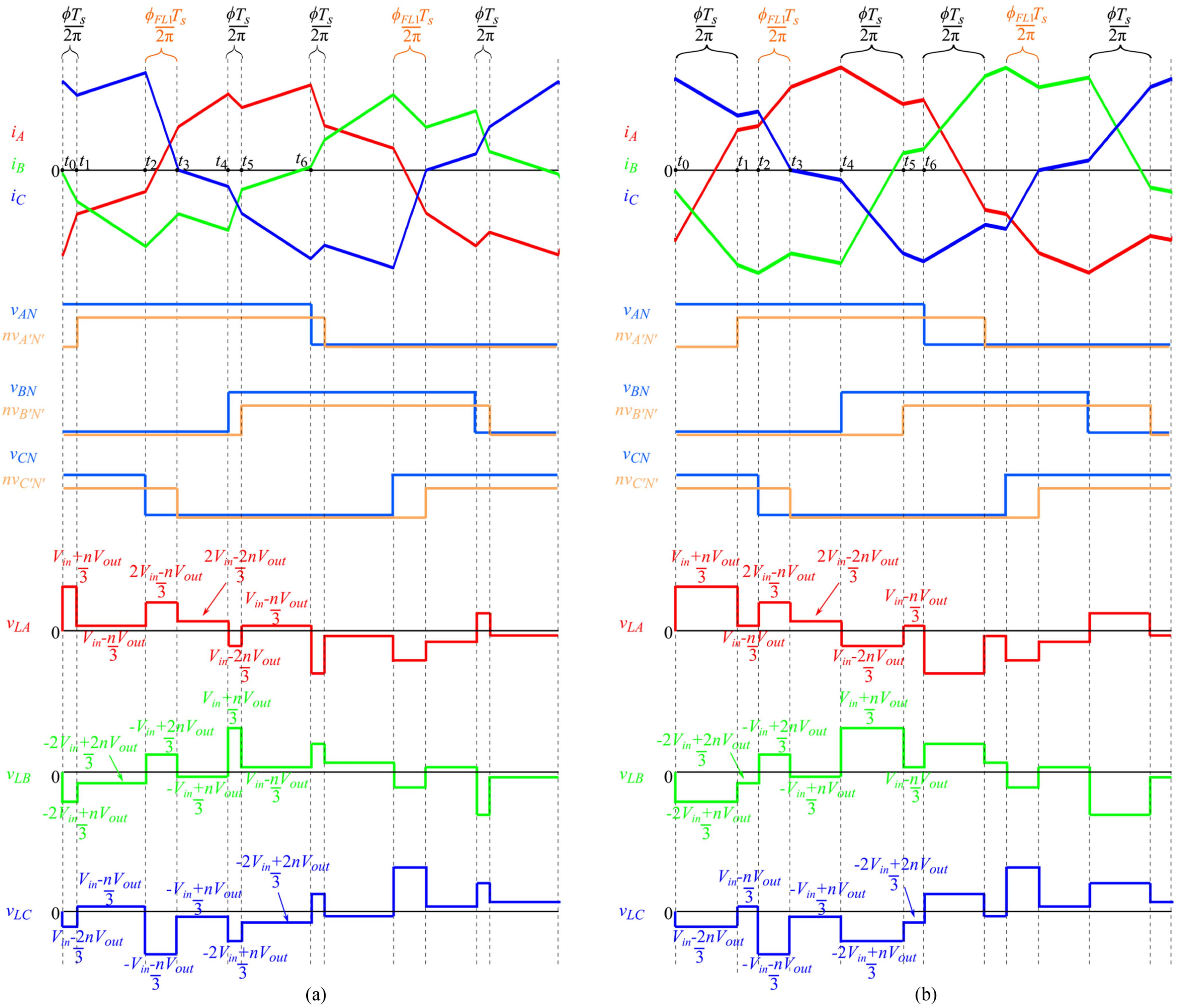
III. ANALYSIS OF FROZEN LEG OPERATION BUCK MODE FOR 3P-DAB

This analysis assumes leg *C'* is the faulty leg, though the findings are applicable to faults in the other legs on the secondary side due to the similarity in operation of the three legs. Consequently, the two switches in leg *C'* will be disabled and only their antiparallel diodes operate as freewheeling.

Unlike the normal operation in buck mode, the frozen leg operation in buck mode must be categorized into three cases: $0 \leqslant \phi \leqslant \pi/3$, $\pi/3 < \phi \leqslant \pi/3 + \phi_{FL1}$, and $\pi/3 + \phi_{FL1} < \phi \leqslant \pi/2$. Here, ϕ_{FL1} is a constant value related to V_{in} and nV_{out} and will be discussed in the subsequent sections.

A. Case I: Phase Shift Angle Between 0 and π/3

The phase voltages V_{AN}, $nV_{A'N'}$, V_{BN}, $nV_{B'N'}$, V_{CN}, and the phase shifts of phases A and B remain consistent with the normal case in Fig. 2(a), as no faults are present in these legs. But for phase C', given that the two switches in leg C' are disabled during the frozen leg operation, only the two antiparallel diodes can conduct. Therefore, when the phase C current undergoes a transition from positive to negative or vice versa, the conducting



(a)

(b)

Fig. 3. Case I waveforms of phase currents, phase voltages, and leakage inductor voltages where (a) $0 < \phi \leqslant \phi_{FL1}$ (with $\phi = \pi/18$ as the example) and (b) $\phi_{FL1} < \phi \leqslant \pi/3$ (with $\phi = \pi/4$ as the example).

devices will be changed to another diode, causing a corresponding alteration in the phase voltage $nV_{C'N'}$, as shown in Fig. 3. This results in a deviation of the actual phase shift angle of phase *C* from the nominal phase shift angle ϕ to a new value defined as ϕ_{FL1}. This variation in the phase shift angle of phase *C* induces an obvious change in the current waveforms of phases *A* and *B* compared to normal operation, as depicted in Fig. 3.

Given the known phase voltages, the corresponding leakage inductor voltages v_L can be calculated using (8), as depicted in Fig. 3. With these leakage inductor voltages, the current expressions can be derived and the newly defined value ϕ_{FL1} can be determined as below.

Based on the half-wave antisymmetric feature of voltage and current waveforms [45], it is sufficient to analyze only half of the switching cycle for each phase, further divided into six segments, as shown in Fig. 3. The current variation for each segment can be calculated by

$$\Delta i_L = \frac{v_L}{L}\Delta t. \tag{10}$$

Two intermediate variables *M* and *N* are defined in (11) in the calculation of current variation

$$M = \frac{T_s V_{\text{in}}}{6\pi L}, N = \frac{T_s nV_{\text{out}}}{6\pi L}. \tag{11}$$

In this article, I_{XI-m} is defined as the current value at t_m for phase *X* in Case I. According to the above analysis, phase *C* current undergoes a transition at t_3, i.e., I_{CI-3} is equal to 0. The value of ϕ_{FL1} can, thus, be determined using (10) for the third segment

$$\phi_{FL1} = \frac{2M - 2N}{M}\frac{\pi}{3} = \frac{2V_{\text{in}} - 2nV_{\text{out}}}{V_{\text{in}}}\frac{\pi}{3}. \tag{12}$$

It can be inferred that ϕ_{FL1} is a constant value solely dependent on V_{in} and nV_{out}, indicating that this value remains constant regardless of changes in the phase shift angle ϕ, as shown in Fig. 3(a) and (b). This consistency has also been verified by the experiments in Section V. Subsequently, using the determined ϕ_{FL1} and current variations for each segment, the current values

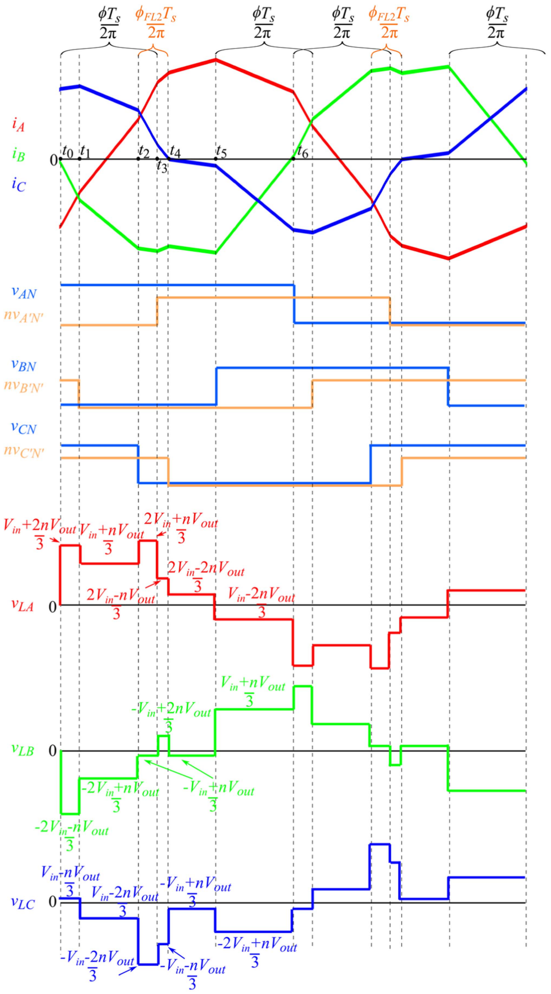


Fig. 4. Case II waveforms of phase currents, phase voltages, and leakage inductor voltages where $\pi/3 < \phi \leqslant \pi/3 + \phi_{FL2}$ (with $\phi = 7\pi/18$ as the example).

of phases A, B, and C can be calculated, as detailed in Table II of Appendix A.

For the frozen leg case with $0 \leqslant \phi \leqslant \pi/3$, notable distinctions in the current waveforms are observed between the buck mode with $V_{\text{in}} > nV_{\text{out}}$ and the unity gain mode with $V_{\text{in}} = nV_{\text{out}}$ [20]. In the unity gain mode, the phase C current exhibits a discontinuous pattern, while in the buck mode, the phase C current is continuous. This discrepancy is conjectured to arise from the voltage differential between the primary and secondary sides, prompting the preferential flow of current from the high voltage level to the low voltage level. Consequently, in buck mode, the current tends to exhibit a continuous pattern through the two antiparallel diodes, as opposed to being discontinuous.

B. Case II: Phase Shift Angle Between π/3 and $\pi/3 + \phi_{FL1}$

When the phase shift angle ϕ enters the range of (π/3, π/2], its waveforms become more complicated compared to the normal case, as shown in Fig. 4. Similar to Case I, the phase shift angle of phases A and B remains unchanged from the normal case. However, due to the freewheeling of the two didoes, the phase shift angle of phase C changes, as shown in Fig. 4. When the phase shift angle ϕ is small, the new phase shift angle of phase C is defined as ϕ_{FL2}, which is a constant value equal to ϕ_{FL1}. When the phase shift angle ϕ exceeds the value of $\pi/3 + \phi_{FL2}$ (i.e., $\pi/3 + \phi_{FL1}$), the new phase shift angle of phase C will go from the defined ϕ_{FL2} to a new value ϕ_{FL3}, as shown in Fig. 5 and discussed in the following section.

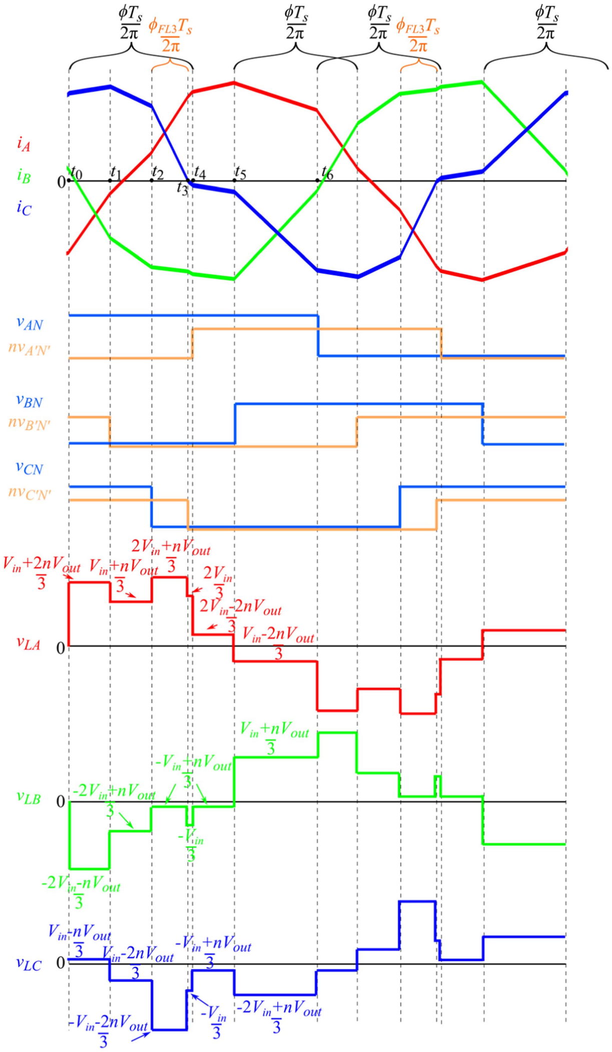


Fig. 5. Case III waveforms of phase currents, phase voltages, and leakage inductor voltages where $\pi/3 + \phi_{FL2} < \phi \leqslant \pi/2$ (with $\phi = 44\pi/45$ as the example).

For this Case II, the first step is also to calculate the leakage inductor voltages, as depicted in Fig. 4. Using these leakage inductor voltages, the current variations of phases A, B, and C for each segment can be calculated, forming the basis for further calculations. It is noted that in this case, phase C current undergoes a transition at t_4, i.e., I_{CII-4} is equal to 0. The value of ϕ_{FL2} can thus be determined using (10) for the fourth segment, as shown in

$$\phi_{FL2} = \frac{2V_{\text{in}} - 2nV_{\text{out}}}{V_{\text{in}}} \frac{\pi}{3} = \phi_{FL1}. \tag{13}$$

The value of ϕ_{FL2} is equal to ϕ_{FL1} and is only related to V_{in} and nV_{out}. This value has also been verified through the experiments in Section V. Subsequently, using the determined ϕ_{FL2}, and the current variations for each segment, the current values of phases *A*, *B*, and *C* can be calculated, as detailed in Table III of Appendix A.

C. Case III: Phase Shift Angle Between π/3 and $\pi/3+\phi_{FL1}$

As discussed in the last section, when the phase shift angle ϕ exceeds the value of $\pi/3+\phi_{FL1}$, the waveforms of phase currents, phase voltages, and leakage inductor voltages undergo further changes, as shown in Fig. 5. The new phase shift angle of phase *C* transitions from ϕ_{FL2} to a new value ϕ_{FL3}.

For this Case III, the initial step is also to calculate the leakage inductor voltages, as depicted in Fig. 5. Compared to the voltages in Fig. 4, there are slight changes around the zero-crossing points of phase currents. Using these leakage inductor voltages, the current variations of phases *A, B,* and *C* for each segment can be calculated.

In this case, I_{CIII-3} is equal to 0, which allows the calculation of the value of ϕ_{FL3}

$$\phi_{FL3}=\frac{nV_{\text{out}}\phi+(2V_{\text{in}}-3nV_{\text{out}})\frac{\pi}{3}}{V_{\text{in}}+nV_{\text{out}}}. \tag{14}$$

It can be observed that ϕ_{FL3} varies with the phase shift angle ϕ, rather than being a constant value. Using the determined ϕ_{FL3}, and the current variations for each segment, the current expression of phases *A*, *B*, and *C* can be calculated, as detailed in Table IV of Appendix A.

D. Soft-Switching Analysis for Three Cases

Soft-switching is usually employed to reduce the switching stress on switch devices. In the 3p-DAB converter, zero voltage switching (ZVS) in the turn-ON process is a widely-used soft-switching technique. The key criterion for ZVS is that the switch voltage must decay to zero before turn-ON, meaning that the turn-ON current should commutate to the antiparallel body diode before the switch takes over the current. This requires the switch to carry a negative current at the turn-ON instant.

This section analyzes the soft-switching behavior of the above three cases, which has not been previously investigated. Due to the asymmetry caused by the faulty phase, the ZVS conditions must be evaluated individually for each phase. Furthermore, as phase *C*' switches ON the secondary side are intentionally open-circuited, ZVS is inapplicable for these two switches.

In Case I, all healthy switches must meet the criteria given in (15) to achieve ZVS, as derived from the current waveform shown in Fig. 3

$$\begin{cases}\text{Primary Phase } A\text{: } I_{AI-0}<0\\ \text{Secondary Phase } A'\text{: } I_{AI-1}>0\\ \text{Primary Phase } B\text{: } I_{BI-4}<0\\ \text{Secondary Phase } B'\text{: } I_{BI-5}>0\\ \text{Primary Phase } C\text{: - } I_{CI-2}<0\end{cases} \tag{15}$$

where I_{XI-j} is the current value when the corresponding switch turns ON in Case I, which has been calculated in Table II of Appendix A. Similarly, the criteria for Cases II and III are provided in (16) and (17), with current values listed in Tables III and IV of Appendix A

$$\begin{cases}\text{Primary Phase } A\text{: } I_{AII-0}<0\\ \text{Secondary Phase } A'\text{: } I_{AII-3}>0\\ \text{Primary Phase } B\text{: } I_{BII-5}<0\\ \text{Secondary Phase } B'\text{: - } I_{BII-1}>0\\ \text{Primary Phase } C\text{: - } I_{CII-2}<0\end{cases} \tag{16}$$

$$\begin{cases}\text{Primary Phase } A\text{: } I_{AIII-0}<0\\ \text{Secondary Phase } A'\text{: } I_{AIII-4}>0\\ \text{Primary Phase } B\text{: } I_{BIII-5}<0\\ \text{Secondary Phase } B'\text{: - } I_{BIII-1}>0\\ \text{Primary Phase } C\text{: - } I_{CIII-2}<0.\end{cases} \tag{17}$$

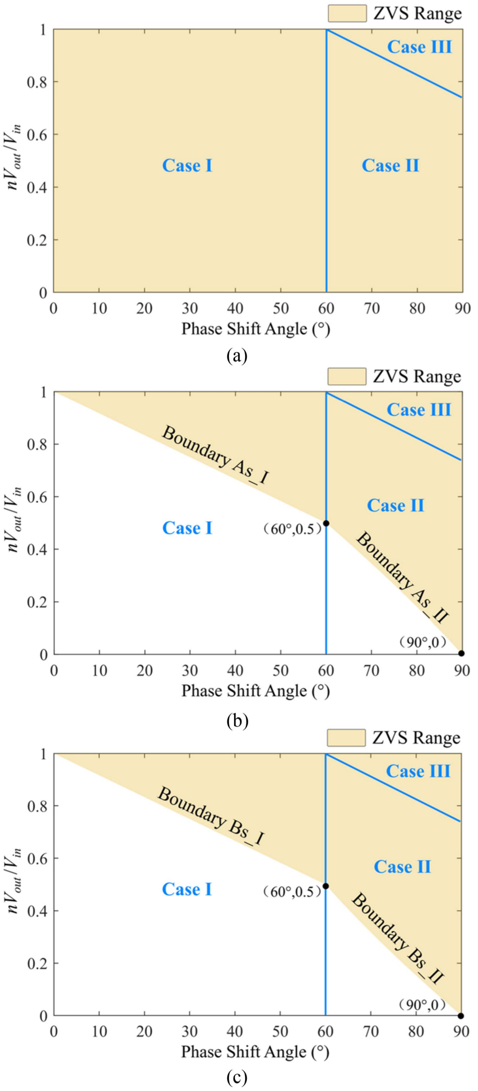


Fig. 6. ZVS regions for (a) switches in primary-side phases *A*, *B*, *C*, (b) switches in secondary-side phase *A*', and (c) switches in secondary-side phase *B*'.

By solving these criteria, the ZVS range can be determined, as shown in Fig. 6(a), (b), and (c). The analysis reveals that for primary-side switches, the ZVS range spans the entire 0° to 90° phase shift angle and 0% to 100% voltage drop, as shown in

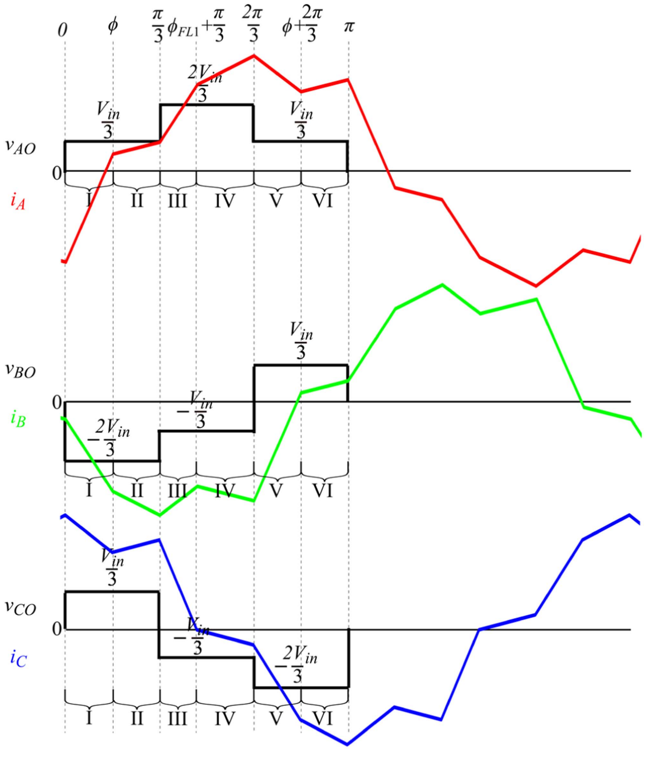


Fig. 7. Case I $(0 < \phi \leqslant \pi/3)$ transferred power calculation using phase voltages and currents.

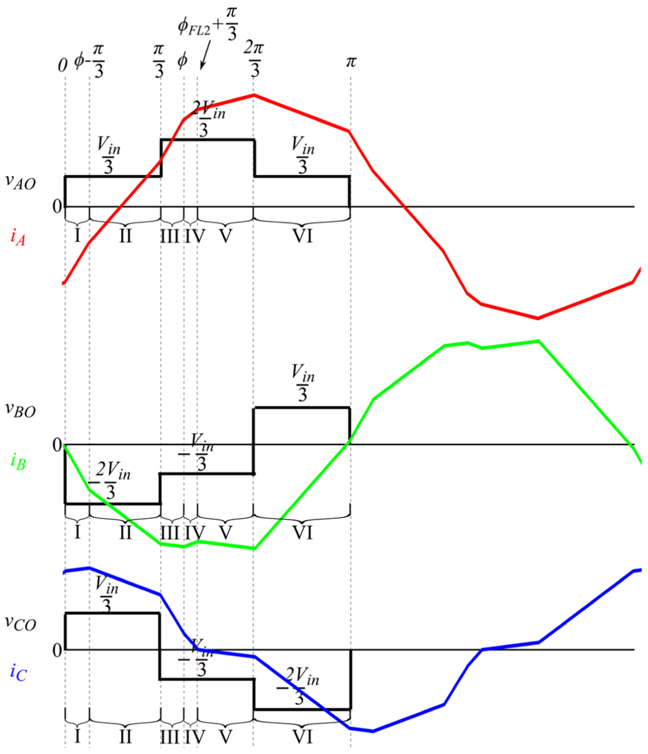


Fig. 8. Case II $(\pi/3 < \phi \leqslant \pi/3 + \phi_{FL2})$ transferred power calculation using phase voltages and currents.

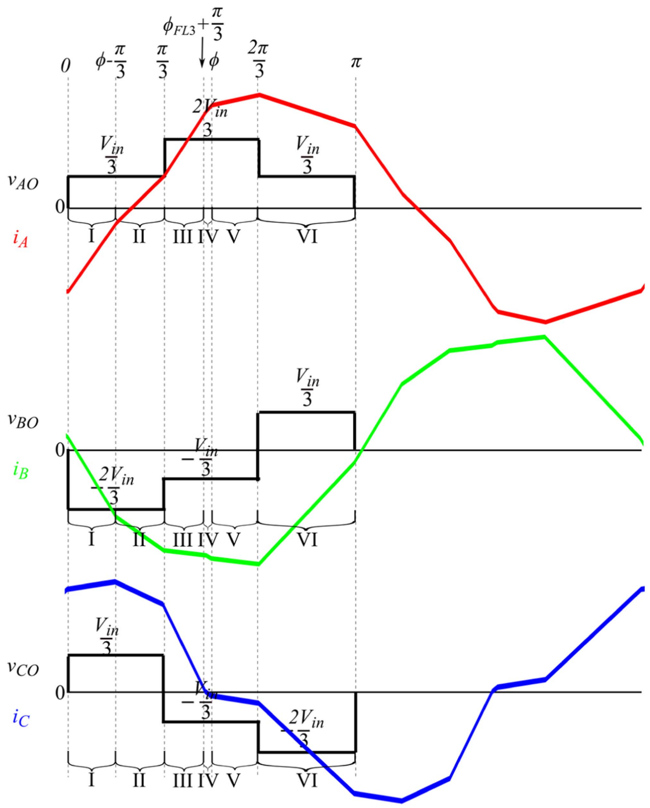


Fig. 9. Case III $(\pi/3 + \phi_{FL2} < \phi \leqslant \pi/2)$ transferred power calculation using phase voltages and currents.

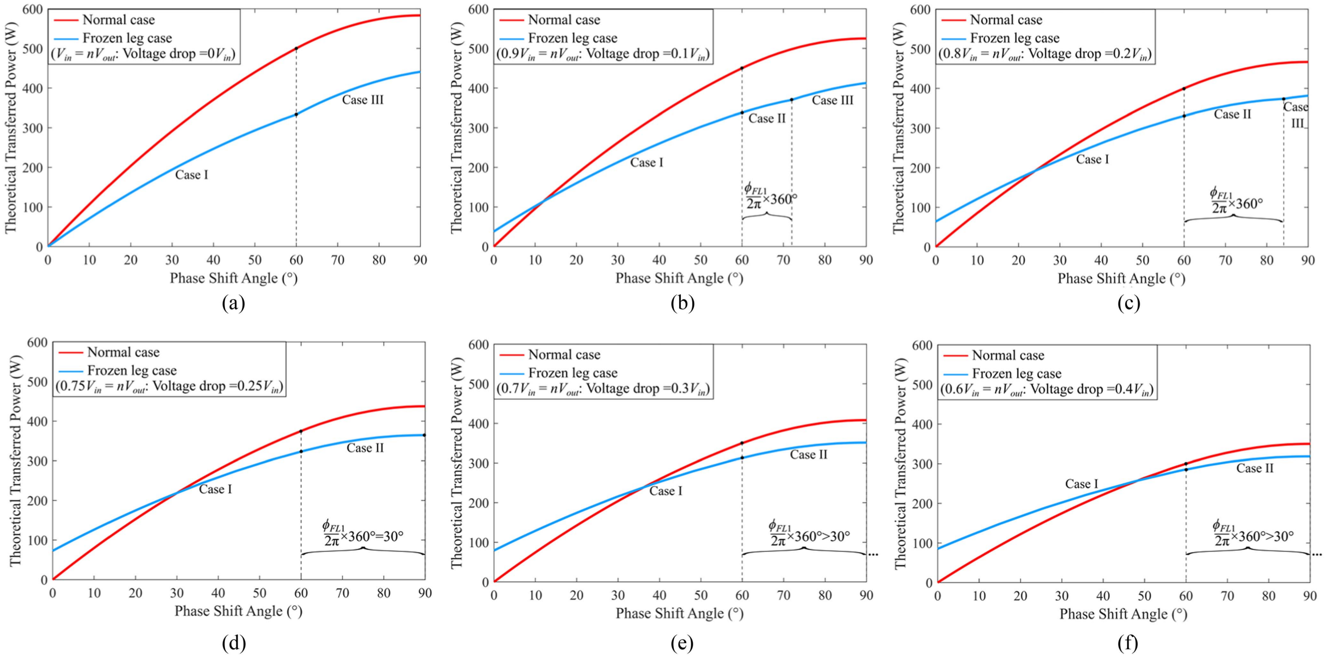
Fig. 6(a). However, the ZVS condition is not always achievable for secondary-side switches and the ZVS range differs slightly between phases *A*' and *B*', as shown in Fig. 6(b) and (c). The boundaries of the ZVS range for secondary-side phases *A*' and *B*' are provided in (18) and (19). While the boundaries appear similar in the figures, they differ slightly in that their mathematical expressions have different curvatures. The derived ZVS range is verified by the experimental results in Section V. Understanding these newly-derived ZVS boundaries will be helpful in the design of thermal management systems, since switch losses will be higher than expected in the non-ZVS ranges

$$\begin{cases} \text{Boundary As\_I} = \\ \dfrac{(-\frac{\phi}{2}-60)+\sqrt{(\frac{\phi}{2}+60)^2-240(\phi-120)}}{120}, \ \phi \in [0,60) \\ \text{Boundary As\_II:} \\ \dfrac{(-\frac{\phi}{2}-60)+\sqrt{(\frac{\phi}{2}+60)^2-240(2\phi-180)}}{120}, \ \phi \in [60,90] \end{cases} \tag{18}$$

$$\begin{cases} \text{Boundary Bs\_I} = \\ \dfrac{(-\frac{\phi}{2}+180)-\sqrt{(\frac{\phi}{2}-180)^2+240(\phi-120)}}{120}, \ \phi \in [0,60) \\ \text{Boundary Bs\_II:} \\ \dfrac{(-\frac{\phi}{2}+180)-\sqrt{(\frac{\phi}{2}-180)^2-240(-2\phi+180)}}{120}, \ \phi \in [60,90]. \end{cases} \tag{19}$$

IV. POWER TRANSFER ANALYSIS OF FROZEN LEG OPERATION BUCK MODE FOR 3P-DAB

To simplify the analysis, it is assumed that the 3p-DAB converter operates without losses [45]. Thus, the output power



(a) (b) (c) (d) (e) (f)

Fig. 10. Power transfer comparison between normal and frozen leg operations under voltage drops of (a) 0 V_{in}, (b) 0.1 V_{in}, (c) 0.2 V_{in}, (d) 0.25 V_{in}, (e) 0.3 V_{in}, and (f) 0.4 V_{in}.

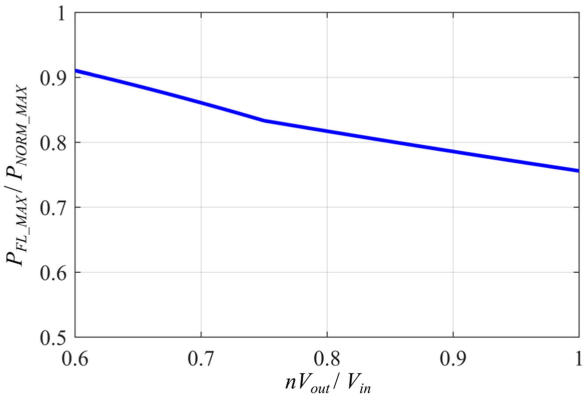
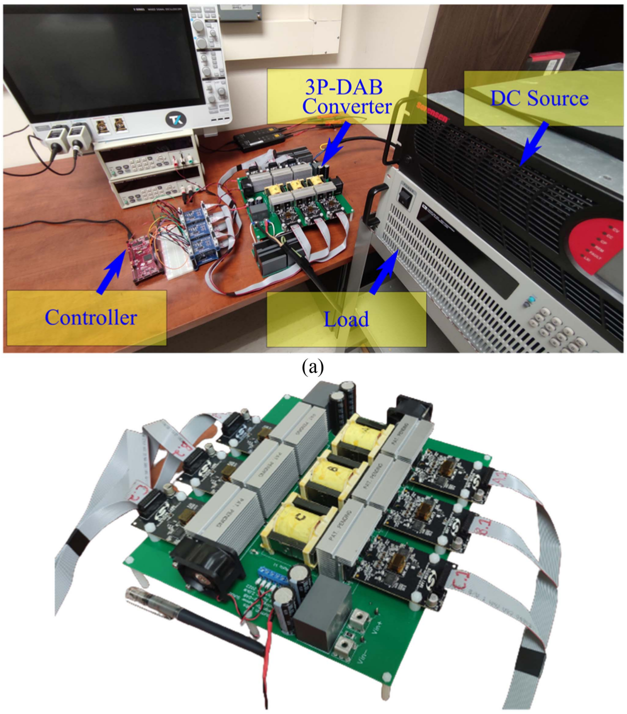


Fig. 11. Maximum transferred power ratio of normal and frozen leg cases with voltage drops ranging from 0 to 0.4 V_{in}.

is equivalent to the power transferred through the three-phase transformer [45], which can be determined using the transformer's phase voltages and currents, as shown in

$$P = P_A + P_B + P_C$$
$$= \frac{1}{\pi}\int v_{AO} i_A d\theta + \frac{1}{\pi}\int v_{BO} i_B d\theta + \frac{1}{\pi}\int v_{CO} i_C d\theta \tag{20}$$

where only half of the switching cycle for each phase is integrated due to the symmetry of the voltage and current waveforms in one switching cycle. Using (20), the transferred power in all three cases can be calculated and analyzed. The derived transferred power expression is valuable for optimizing power control strategies for the frozen leg operation in buck mode.



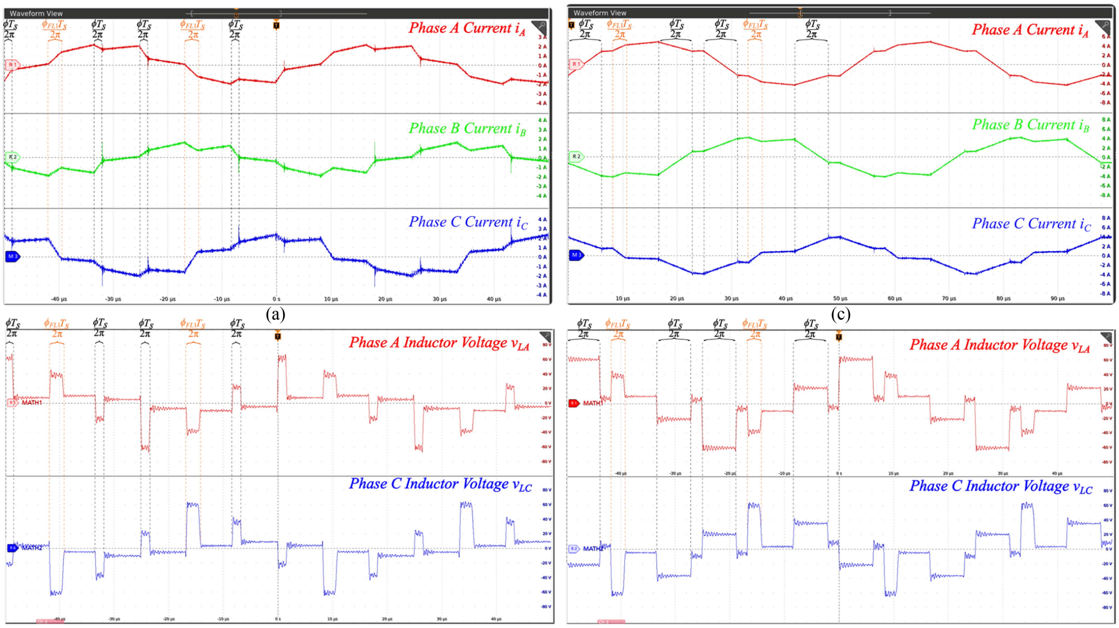
(a)

(b)

Fig. 12. (a) Experimental setup and (b) 3P-DAB converter.

A. *Transferred Power for Case I:* $0 \leqslant \phi \leqslant \pi/3$

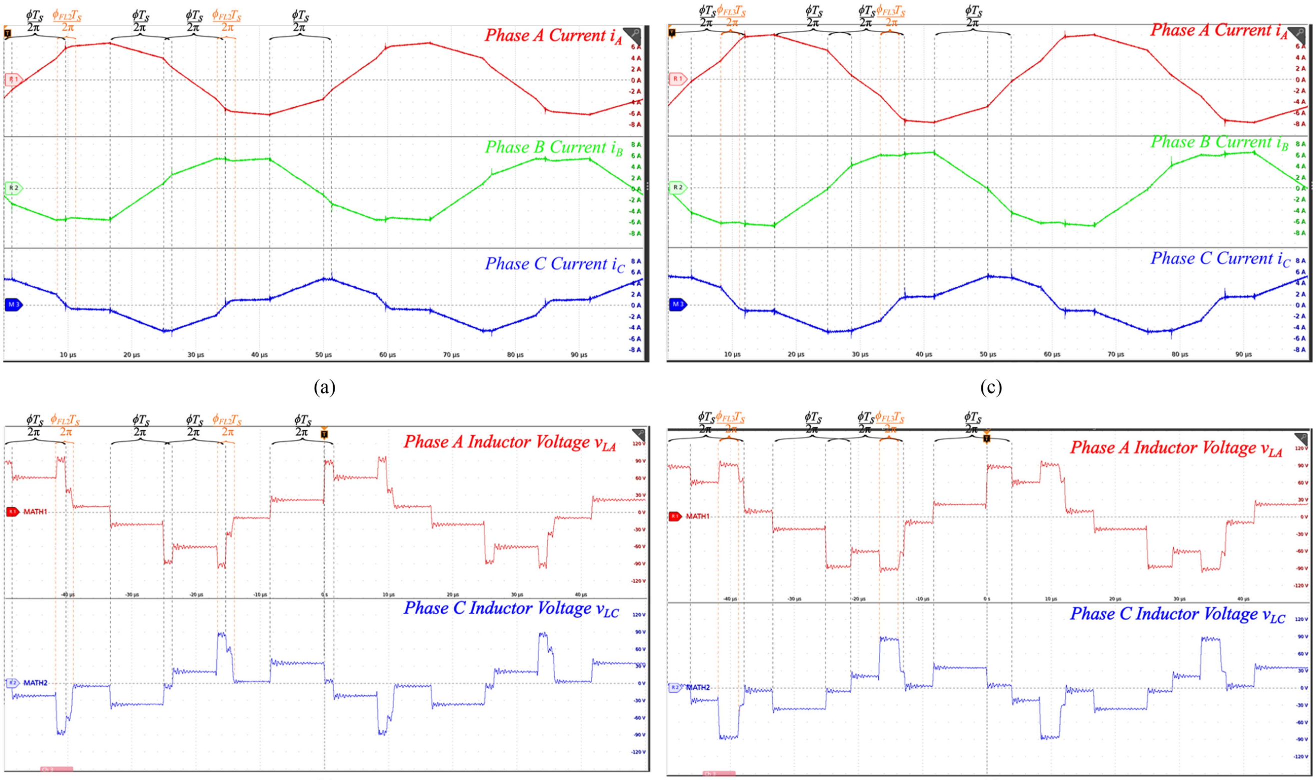
For Case 1, the waveforms of phase voltages and currents can be segmented into 6 intervals according to Fig. 3. In each segment, the primary-side X phase voltage V_{XO} can be calculated through (4), as shown in Fig. 7. The segmental current



(a) (c)

(b) (d)

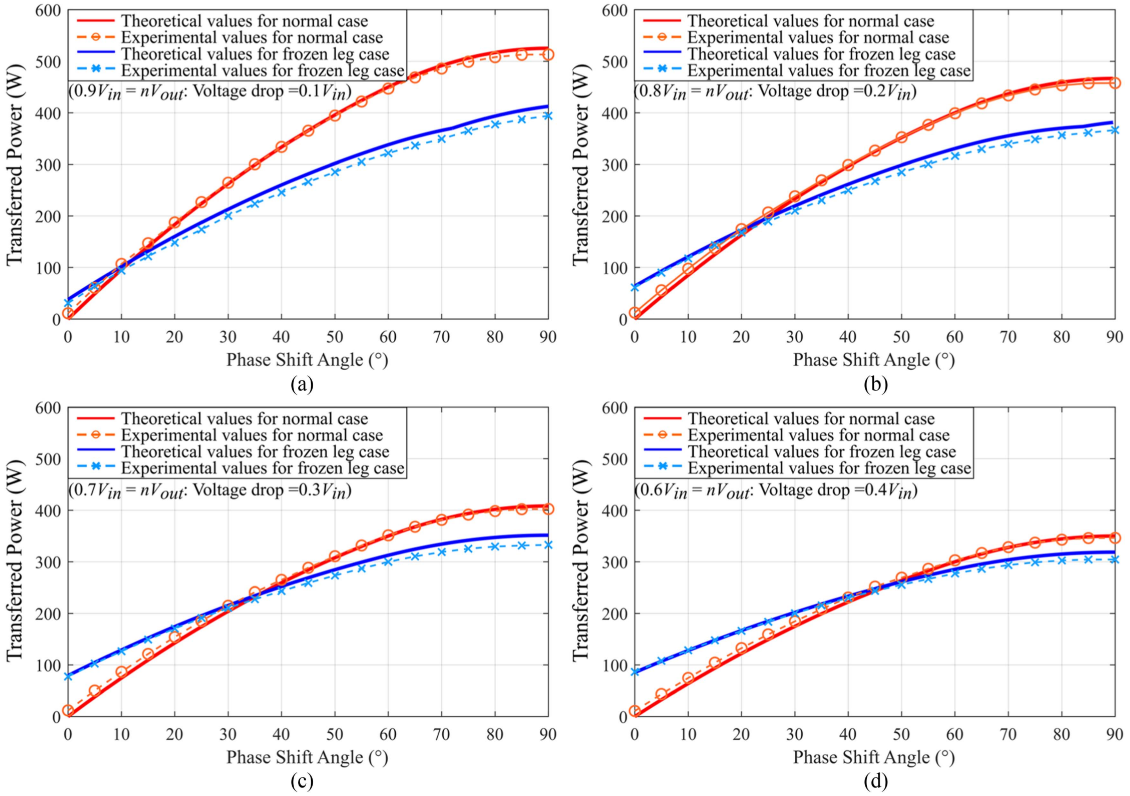
Fig. 13. Experimental results of (a) phase currents, (b) leakage inductor voltages with the phase shift angle of 10° and (c) phase currents, (d) leakage inductor voltages with the phase shift angle of 45°, under voltage drop of 0.2 V_{in}.



(a) (c)

(b) (d)

Fig. 14. Experimental results of (a) phase currents, (b) leakage inductor voltages with the phase shift angle of 70° and (c) phase currents, (d) leakage inductor voltages with the phase shift angle of 88°, under voltage drop of 0.2 V_{in}.



(a) (b)

(c) (d)

Fig. 15. Theoretical and experimental power transfer curves for normal and frozen leg cases with voltage drops of (a) $0.1V_{\text{in}}$, (b) $0.2V_{\text{in}}$, (c) $0.3V_{\text{in}}$, and (d) $0.4V_{\text{in}}$.

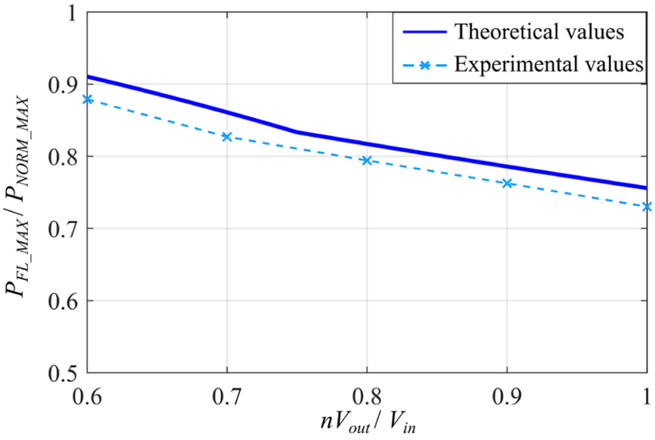
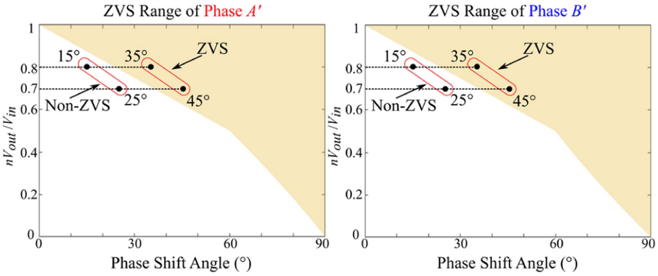


Fig. 16. Experimental results of the maximum transferred power ratio of normal and frozen leg cases with voltage drops ranging from 0 to 0.4 V_{in}.

expressions, previously derived in the last section, are provided in Table II of Appendix A and are also shown in Fig. 7.

According to Fig. 7, the phase X transferred power in Case I can be calculated by summing the average transferred power of the six segments, as shown in

$$\overline{P_{XI}} = \overline{P_{XI-I}} + \overline{P_{XI-II}} + \overline{P_{XI-III}} + \overline{P_{XI-IV}} + \overline{P_{XI-V}} + \overline{P_{XI-VI}} \tag{21}$$



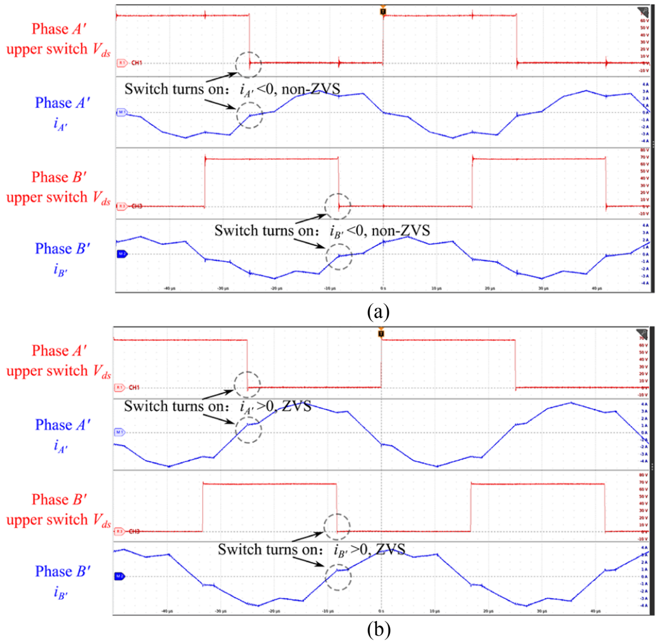
(a) (b)

Fig. 17. Testing point selection for (a) the upper switch of phase *A'*, and (b) the upper switch of phase *B'*.

where each segment's power can be calculated by multiplying the average current, average phase voltage, and the time interval (in radians), then dividing by half of the switching cycle, i.e., π. For example, the first segmental transferred power of phase A in Case I can be calculated as

$$\overline{P_{AI-I}} = \left(\frac{I_{AI-0} + I_{AI-1}}{2} \frac{V_{\text{in}}}{3} \phi \right) / \pi \tag{22}$$

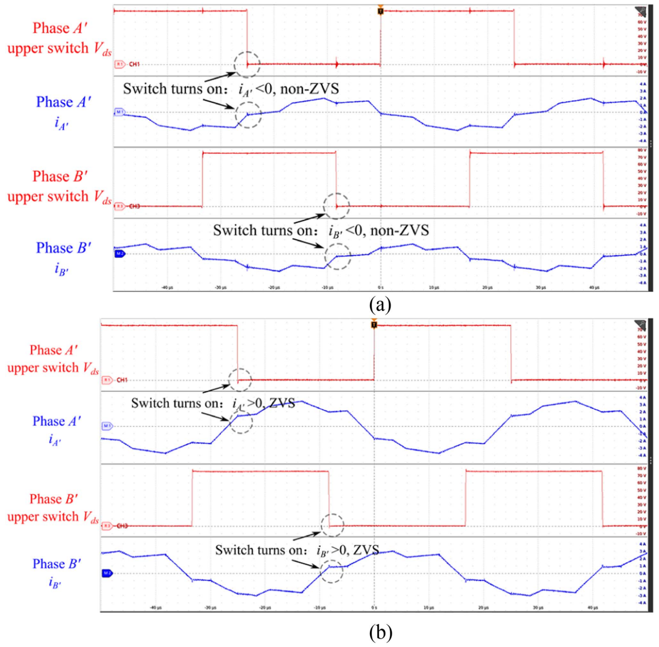
where I_{AI-0} and I_{AI-1} are given in Table II of Appendix A. Following this method, the segmental transferred power for all three phases in Case I can be calculated, as tabulated in Table V of Appendix B. Therefore, the three-phase transferred power



(a)

(b)

Fig. 18. Upper switches V_{ds} and phase currents of phase A' and phase B' at (a) 25° and (b) 45° phase shift angle with $nV_{\text{out}} = 0.7\,V_{\text{in}}$.



(a)

(b)

Fig. 19. Upper switches V_{ds} and phase currents of phase A' and phase B' at (a) 15° and (b) 35° phase shift angle with $nV_{\text{out}} = 0.8\,V_{\text{in}}$.

and their sum for Case I can be calculated as

$$P_{AI} = \frac{V_{\text{in}}}{6\pi}\left(-N\phi^2 + 10N\frac{\pi}{3}\phi + 2N\frac{\pi}{3}\phi_{FL1} - 2N\phi_{FL1}^2\right)$$

$$P_{BI} = \frac{V_{\text{in}}}{6\pi}\left(-4N\phi^2 + 10N\frac{\pi}{3}\phi + 2N\frac{\pi}{3}\phi_{FL1} + N\phi_{FL1}^2\right)$$

$$P_{CI} = \frac{V_{\text{in}}}{6\pi}\left[-N\phi^2 + 4N\frac{\pi}{3}\phi + (-4M+8N)\frac{\pi}{3}\phi_{FL1} - 2N\phi_{FL1}^2 + (8M-8N)\frac{\pi^2}{9}\right] \tag{23}$$

$$\begin{aligned} P_I &= P_{AI} + P_{BI} + P_{CI} \\ &= \frac{V_{\text{in}}}{6\pi}\left[-6N\phi^2 + 24N\frac{\pi}{3}\phi + (-4M+12N)\frac{\pi}{3}\phi_{FL1} - 3N\phi_{FL1}^2 + (8M-8N)\frac{\pi^2}{9}\right]. \end{aligned} \tag{24}$$

B. *Transferred Power for Case II:* $\pi/3 < \phi \leqslant \pi/3 + \phi_{FL1}$

For Case II, the phase voltage and current waveforms are similarly divided into six intervals according to Fig. 4. In each segment, the primary-side phase X voltage, V_{XO}, can also be calculated by (4), as shown in Fig. 8. The segmental current expressions are provided in Table III of Appendix A and are also shown in Fig. 8. Using the method described in the previous subsection, the segmental transferred power for all three phases in Case II can be calculated, as tabulated in Table VI of Appendix B. Consequently, the three-phase transferred power and their sum for Case II can be calculated as

$$P_{AII} = \frac{V_{\text{in}}}{6\pi}\left(-5N\phi^2 + 18N\frac{\pi}{3}\phi + 2N\frac{\pi}{3}\phi_{FL2} - 2N\phi_{FL2}^2 - 4N\frac{\pi^2}{9}\right)$$

$$P_{BII} = \frac{V_{\text{in}}}{6\pi}\left(-5N\phi^2 + 12N\frac{\pi}{3}\phi + 2N\frac{\pi}{3}\phi_{FL2} + N\phi_{FL2}^2 - N\frac{\pi^2}{9}\right)$$

$$P_{CII} = \frac{V_{\text{in}}}{6\pi}\left[-2N\phi^2 + (-4M+10N)\frac{\pi}{3}\phi + (-14M+12N)\frac{\pi}{3}\phi_{FL2} + (2M-2N)\phi_{FL2}^2 + (20M-21N)\frac{\pi^2}{9} + 2M\phi\phi_{FL2}\right] \tag{25}$$

$$\begin{aligned} P_{II} &= P_{AII} + P_{BII} + P_{CII} \\ &= \frac{V_{\text{in}}}{6\pi}\left[-12N\phi^2 + (-4M+40N)\frac{\pi}{3}\phi + (-14M+16N)\frac{\pi}{3}\phi_{FL2} + (2M-3N)\phi_{FL2}^2 + (20M-26N)\frac{\pi^2}{9} + 2M\phi\phi_{FL2}\right]. \end{aligned} \tag{26}$$

C. *Transferred Power for Case III:* $\pi/3 + \phi_{FL1} < \phi \leqslant \pi/2$

For Case III, the waveforms of phase voltages and currents are again divided into six intervals according to Fig. 5. In each segment, the primary-side phase X voltage, V_{XO}, can be calculated through (4), as shown in Fig. 9. The segmental current expressions are provided in Table VII of Appendix A and are also depicted in Fig. 9. Using the method from the previous subsection, the segmental transferred power for all three phases in Case III can be calculated, as tabulated in Table VII of Appendix B. Hence, the three-phase transferred power and their sum for Case III is given by

$$\begin{aligned}P_{AIII} &= \frac{V_{\text{in}}}{6\pi}\Bigg(-5N\phi^2+18N\frac{\pi}{3}\phi+2N\frac{\pi}{3}\phi_{FL3}\\&\quad -2N\phi_{FL3}^2-4N\frac{\pi^2}{9}\Bigg)\\P_{BIII} &= \frac{V_{\text{in}}}{6\pi}\Bigg(-5N\phi^2+12N\frac{\pi}{3}\phi+2N\frac{\pi}{3}\phi_{FL3}\\&\quad +N\phi_{FL3}^2-N\frac{\pi^2}{9}\Bigg)\\P_{CIII} &= \frac{V_{\text{in}}}{6\pi}\Bigg[-2N\phi^2+14N\frac{\pi}{3}\phi+(-12M+6N)\\&\quad\times\frac{\pi}{3}\phi_{FL3}+2\mathrm{M}\phi_{FL3}^2\\&\quad+(16M-25N)\frac{\pi^2}{9}-2N\phi\phi_{FL3}\Bigg]\end{aligned}\tag{27}$$

$$\begin{aligned}P_{III} &= P_{AIII}+P_{BIII}+P_{CIII}\\&= \frac{V_{\text{in}}}{6\pi}\Bigg[-12N\phi^2+44N\frac{\pi}{3}\phi\\&\quad+(-12M+10N)\frac{\pi}{3}\phi_{FL3}+(2M-N)\phi_{FL3}^2\\&\quad+(16M-30N)\frac{\pi^2}{9}-2N\phi\phi_{FL3}\Bigg].\end{aligned}\tag{28}$$

D. Power Transfer Curve Comparison in Buck Mode

To analyze and compare the transferred power of normal and frozen leg operations in buck mode, the power transfer curves for various voltage drops are plotted in Fig. 10, using (9) for normal operation and (24), (26), and (28) for frozen leg operation. In the unity gain mode where the voltage drop is zero, ϕ_{FL1} is equal to zero according to (12) and ϕ_{FL3} is equal to $\phi/2$ according to (14), as shown in Fig. 10(a). With $\phi_{FL1}=0$, the frozen leg operation only comprises two cases: $0\leqslant\phi\leqslant\pi/3$ for Case I and $\pi/3<\phi\leqslant\pi/2$ for Case III, as shown in Fig. 10(a).

As the voltage drop increases from 0 to $0.25\,V_{\text{in}}$, ϕ_{FL1} increases from zero to $\pi/6$, as per (12). Correspondingly, the range of Case II expands from 0 to $\pi/6$, and the range of Case III decreases from $\pi/6$ to 0, as shown in Fig. 10(b)–(d). When the voltage drop exceeds $0.25\,V_{\text{in}}$, ϕ_{FL1} will surpass $\pi/6$. Considering that the phase shift angle ϕ is no more than $\pi/2$, Case II will cover the range of $\pi/3<\phi\leqslant\pi/2$ when the voltage drop exceeds $0.25V_{\text{in}}$, as shown in Fig. 10(e) and (f), thus, Case III is eliminated for these scenarios.

According to Fig. 3, the fixed ϕ_{FL1} in Case I results in a nonzero transferred power even when the phase shift angle ϕ is zero. As the voltage drop increases, the ϕ_{FL1} also increases, leading to higher transferred power at zero phase shift angle, as shown in Fig. 10(b)–(f). These novel findings are corroborated by the experimental results presented in Section V.

TABLE I
3P-DAB CONVERTER PARAMETERS

Description	Parameters
Input DC voltage (V_{in})	100 V
Output DC voltage (V_{out})	60 V-100 V
Rated power (P_{rated})	1.125 kW
Transformer turns ratio (n:1)	1:1
Switching frequency (f_s)	20 kHz
Leakage inductance ($L_{A,B,C}$)	83.33 µH
Switch dead time (t_d)	0.2 µs

Furthermore, considering that fault-tolerant strategies aim to maintain the prefault operational state as closely as possible, the maximum transferred power of such strategy is also a critical focus. According to Fig. 10, when the voltage drop is less than $0.25V_{\text{in}}$, the maximum transferred power happens in Case III with a phase shift angle ϕ of $\pi/2$. When the voltage drop exceeds $0.25V_{\text{in}}$, the maximum transferred power occurs in Case II with the same phase shift angle ϕ of $\pi/2$. The equations describing the maximum transferred power are provided in (29) for voltage drop less than $0.25V_{\text{in}}$ and (30) for voltage drop exceeding $0.25V_{\text{in}}$, and the ratio of maximum transferred powers between frozen leg and normal cases is plotted in Fig. 11

$$\begin{aligned}P_{\text{MAX}} &= \frac{T_s V_{\text{in}}^2}{36L}\left[\frac{nV_{\text{out}}}{V_{\text{in}}}+\frac{16}{9}+\frac{\left(\frac{2}{3}-\frac{nV_{\text{out}}}{2V_{\text{in}}}\right)\left(-4+\frac{7V_{\text{out}}}{3V_{\text{in}}}\right)}{1+\frac{nV_{\text{out}}}{V_{\text{in}}}}\right.\\&\quad\left.+\frac{\left(2-\frac{nV_{\text{out}}}{V_{\text{in}}}\right)\left(\frac{2}{3}-\frac{nV_{\text{out}}}{2V_{\text{in}}}\right)^2}{\left(1+\frac{nV_{\text{out}}}{V_{in}}\right)^2}\right]\ (V_{\text{in}}\geq nV_{\text{out}}\geq 0.75V_{\text{in}})\end{aligned}\tag{29}$$

$$P_{\text{MAX}} = \frac{T_s V_{\text{in}}^2}{36L}\left[\frac{11nV_{\text{out}}}{3V_{\text{in}}}-\frac{4}{3}\left(\frac{nV_{\text{out}}}{V_{\text{in}}}\right)^2\right](nV_{\text{out}}\leq 0.75V_{\text{in}}).\tag{30}$$

Their ratio starts at 75.6% for zero voltage drop and exceeds 90% at $0.4V_{\text{in}}$ voltage drop, indicating that as the voltage drop increases, the maximum transferred power of the frozen leg method approaches that of normal operation. This unique finding is validated by the experimental results in Section V.

V. EXPERIMENTAL RESULTS

An experimental prototype of a 1.125 kW 3p-DAB, as shown in Fig. 12, was tested to validate the theoretical findings. The prototype's parameters are shown in Table I. The employed microcontroller and semiconductor devices are the DSP (TMS320F28379) from TI and the discrete silicon carbide MOSFETS (C3M0045065K) from Wolfspeed. The primary-side dc port (V_{in}) was connected to a Sorenson power supply (SGX 600-25) and the secondary-side dc port (V_{out}) was connected to an ITECH electronic load (IT8906E).

During the experiments, two operational modes were adopted: normal and the frozen leg. In the frozen leg cases, the two switches in phase *C*' are intentionally left open, allowing current to flow only through the two antiparallel diodes.

A. Verification of Phase Currents and Leakage Inductor Voltages

To validate the theoretical analysis of phase currents and leakage inductor voltages in Fig. 3, specific phase shift angles of 10° and 45° within the range [0, π/3] were selected, as shown in Fig. 13. The output voltage is set to 80 V and the theoretical ϕ_{FL1} is calculated to be 24° according to (12). It should be noted that direct measurement of the leakage inductor voltages in the prototype is not feasible because the leakage inductor is integrated into the transformer. Instead, the primary and secondary phase voltages of the transformer were measured, i.e., v_{AO} and $v_{A'O'}$. The difference between the two voltages, representing the inductor voltage v_{LA}, was obtained using the math function of the oscilloscope. Due to the oscilloscope's limitation of four channels, only the leakage inductor voltages of phases *A* and *C* were obtained.

The experimental phase currents and leakage inductor voltages in Fig. 13 are observed to closely match the theoretical waveforms in Fig. 3. Additionally, for both phase shift angles of 10° and 45°, their actual phase shift angles in phase *C* are consistent with the theoretical ϕ_{FL1}.

Subsequently, the experiments with phase shift angles of 70° and 88° are conducted to verify Case II and Case III, as shown in Fig. 14. The output voltage remained at 80 V. Hence, the theoretical ϕ_{FL2}, i.e., ϕ_{FL1}, is also equal to 24° according to (13). The theoretical ϕ_{FL3} for the phase shift angle of 88° is determined to be 25.78° according to (14). The experimental phase currents and leakage inductor voltages in Fig. 14 are also found to closely align with the theoretical waveforms in Figs. 4 and 5, further validating the theoretical analysis. Meanwhile, the experimental values of ϕ_{FL2} and ϕ_{FL3} are in agreement with the theoretical predictions.

B. Verification of Power Transfer Equations and Curves

To validate the derived theoretical power transfer equations in (23)–(28) and the plotted curves in Fig. 10, experiments were conducted with phase shift angles ranging from 0° to 90°, in 5° increments, for both normal and frozen leg cases. The output voltages are set between 60 V and 90 V. The measured power results are plotted in Fig. 15, which shows that the measured power values closely align with the theoretical power curves for both normal and frozen leg cases.

As expected, the measured power is slightly lower than the theoretical predictions due to inherent losses in the prototype that are not accounted for in the theoretical equations [1], [45]. These discrepancies are mainly attributable to dead time, switching losses, and conduction losses. The difference between the experimental and theoretical values increases at higher power levels because switching and conduction losses become more significant. Overall, the experimental results support the theoretical analysis presented in the article.

C. Verification of Maximum Transferred Power

To further validate the accuracy of the maximum transferred power ratio between the normal and frozen leg cases across different voltage drops, experiments are conducted to measure the maximum transferred power with voltage drops ranging from 0 to $0.4V_{\text{in}}$. These experimental measurements are then compared with the theoretical values, as illustrated in Fig. 16. The results indicate that the expected ratio approximately holds true. As anticipated, the measured ratios are slightly lower than the theoretical expectation, again due to the inherent losses of the experimental prototype.

D. Verification of Derived ZVS Regions

The prior ZVS analysis shows that for primary-side switches, the ZVS region extends across the full 0° to 90° phase shift angle and 0% to 100% voltage drop. However, for secondary-side switches, the ZVS condition is not always achievable. To validate the derived ZVS regions for the secondary-side switches in phases *A'* and *B'*, four test points were selected. Among these, two points theoretically fall in the non-ZVS region of phases *A'* and *B'*, and two in the ZVS region, as shown in Fig. 17.

To experimentally verify the ZVS conditions at these four test points, the drain-source voltages (V_{ds}) of the upper switches and the phase currents of *A'* and *B'* were measured. The results for $nV_{\text{out}} = 0.7V_{\text{in}}$ and $nV_{\text{out}} = 0.8V_{\text{in}}$ are shown in Figs. 18 and 19, respectively. For ZVS to occur, the current through the upper switches must be negative at turn-ON, which corresponds to the measured phase current being positive. The experimental results in Figs. 18 and 19 align perfectly with the theoretical analysis in Fig. 17, confirming the accuracy of the derived ZVS regions.

VI. CONCLUSION

For the first time, this article addresses the critical need to extend the frozen leg mode analysis of 3p-DAB operation beyond the unity voltage gain assumption used in all prior related research. By categorizing the analysis into three distinct cases, the paper derives and analyzes their current and voltage expressions, and thus, also calculates the transferred power. It is observed that due to the changed phase shift angle of the faulty phase, the power transfer characteristics of the frozen leg method in buck mode deviate from those observed in normal operation. Importantly, even when the phase shift angle is zero, the transferred power is not zero, which is a critical practical finding. Also, a new ZVS analysis shows that while the primary-side healthy switches maintain ZVS across the entire 0° to 90° phase shift angle and 0% to 100% voltage drop, the secondary-side healthy switches do not always achieve ZVS, which is a useful finding for thermal management design. Finally, it is found that the maximum transferred power in buck mode under frozen leg operation increases towards the normal operation power level as the voltage drop increases, and knowledge of these power transfer curves can aid in control strategy design. Future work will extend this research to the boost mode, which presents greater analytical complexity due to the occurrence of discontinuous current.

APPENDIX A

TABLE II

SOLVED CURRENT VALUES OF PHASE *A*, *B*, *C* FOR $0 \leqslant \phi \leqslant \pi/3$

Phase *A*	Phase *B*	Phase *C*
$I_{AI-0} = -\frac{1}{2}N\phi - (2M-2N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{BI-0} = -\frac{1}{2}N\phi + (M-N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{CI-0} = N\phi - (M-N)\frac{\pi}{3} + (M+N)\phi_{FL1}$
$I_{AI-1} = (M+\frac{1}{2}N)\phi - (2M-2N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{BI-1} = (-2M+\frac{1}{2}N)\phi + (M-N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{CI-1} = (M-N)\phi - (M-N)\frac{\pi}{3} + (M+N)\phi_{FL1}$
$I_{AI-2} = \frac{3}{2}N\phi - (M-N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{BI-2} = -\frac{3}{2}N\phi + (-M+N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL1}$	$I_{CI-2} = (M+N)\phi_{FL1}$
$I_{AI-3} = \frac{3}{2}N\phi - (M-N)\frac{\pi}{3} + (2M-\frac{3}{2}N)\phi_{FL1}$	$I_{BI-3} = -\frac{3}{2}N\phi + (-M+N)\frac{\pi}{3} + (-M+\frac{3}{2}N)\phi_{FL1}$	$I_{CI-3} = 0$
$I_{AI-4} = \frac{3}{2}N\phi + (M-N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL1}$	$I_{BI-4} = -\frac{3}{2}N\phi + (-2M+2N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL1}$	$I_{CI-4} = (-M+N)\frac{\pi}{3} + (M-N)\phi_{FL1}$
$I_{AI-5} = (M-\frac{1}{2}N)\phi + (M-N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL1}$	$I_{BI-5} = (M-\frac{1}{2}N)\phi + (-2M+2N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL1}$	$I_{CI-5} = (-2M+N)\phi + (-M+N)\frac{\pi}{3} + (M-N)\phi_{FL1}$

TABLE III

SOLVED CURRENT VALUES OF PHASE *A*, *B*, *C* FOR $\pi/3 \leqslant \phi \leqslant \pi/3 + \phi_{FL1}$

Phase *A*	Phase *B*	Phase *C*
$I_{AII-0} = -\frac{3}{2}N\phi + (-2M+3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{BII-0} = \frac{3}{2}N\phi + (M-3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{CII-0} = (3M-2N)\frac{\pi}{3} + (-M+N)\phi_{FL2}$
$I_{AII-1} = (M+\frac{1}{2}N)\phi + (-3M+N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{BII-1} = (-2M+\frac{1}{2}N)\phi + (3M-2N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{CII-1} = (M-N)\phi + (2M-N)\frac{\pi}{3} + (-M+N)\phi_{FL2}$
$I_{AII-2} = -\frac{1}{2}N\phi + (-M+3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{BII-2} = -\frac{1}{2}N\phi - M\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{CII-2} = N\phi + (4M-5N)\frac{\pi}{3} + (-M+N)\phi_{FL2}$
$I_{AII-3} = (2M+\frac{1}{2}N)\phi + (-3M+2N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{BII-3} = (-M+\frac{1}{2}N)\phi - N\frac{\pi}{3} - \frac{1}{2}N\phi_{FL2}$	$I_{CII-3} = (-M-N)\phi + (5M-3N)\frac{\pi}{3} - (M-N)\phi_{FL2}$
$I_{AII-4} = \frac{3}{2}N\phi + (-M+N)\frac{\pi}{3} + (2M-\frac{3}{2}N)\phi_{FL2}$	$I_{BII-4} = (-\frac{3}{2}N)\phi - (M-N)\frac{\pi}{3} - (M-\frac{3}{2}N)\phi_{FL2}$	$I_{CII-4} = 0$
$I_{AII-5} = \frac{3}{2}N\phi + (M-N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL2}$	$I_{BII-5} = (-\frac{3}{2}N)\phi + (-2M+2N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL2}$	$I_{CII-5} = (-M+N)\frac{\pi}{3} + (M-N)\phi_{FL2}$

TABLE IV

SOLVED CURRENT VALUES OF PHASE *A*, *B*, *C* FOR $\pi/3 + \phi_{FL1} \leqslant \phi \leqslant \pi/2$

Phase *A*	Phase *B*	Phase *C*
$I_{AIII-0} = -\frac{3}{2}N\phi - (-2M+3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{BIII-0} = \frac{3}{2}N\phi + (M-3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{CIII-0} = N\phi + (3M-3N)\frac{\pi}{3} - M\phi_{FL3}$
$I_{AIII-1} = (M+\frac{1}{2}N)\phi + (-3M+N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{BIII-1} = (-2M+\frac{1}{2}N)\phi + (3M-2N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{CIII-1} = M\phi + (2M-2N)\frac{\pi}{3} - M\phi_{FL3}$
$I_{AIII-2} = (-\frac{1}{2}N)\phi - (M-3N)\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{BIII-2} = -\frac{1}{2}N\phi - M\frac{\pi}{3} - \frac{1}{2}N\phi_{FL3}$	$I_{CIII-2} = 2N\phi + (4M-6N)\frac{\pi}{3} - M\phi_{FL3}$
$I_{AIII-3} = (-\frac{1}{2}N)\phi - (M-3N)\frac{\pi}{3} + (2M+\frac{1}{2}N)\phi_{FL3}$	$I_{BIII-3} = (-\frac{1}{2}N)\phi - M\frac{\pi}{3} + (-M+\frac{1}{2}N)\phi_{FL3}$	$I_{CIII-3} = 0$
$I_{AIII-4} = (2M-\frac{1}{2}N)\phi + (-3M+3N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL3}$	$I_{BIII-4} = (-M-\frac{1}{2}N)\phi + \frac{1}{2}N\phi_{FL3}$	$I_{CIII-4} = (-M)\phi + M\frac{\pi}{3} + M\phi_{FL3}$
$I_{AIII-5} = \frac{3}{2}N\phi + (M-N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL3}$	$I_{BIII-5} = (-\frac{3}{2}N)\phi + (-2M+2N)\frac{\pi}{3} + \frac{1}{2}N\phi_{FL3}$	$I_{CIII-5} = (-N)\phi + (-M+2N)\frac{\pi}{3} + M\phi_{FL3}$

APPENDIX B

TABLE V

THREE-PHASE SEGMENTAL TRANSFERRED POWER FOR $0 \leqslant \phi \leqslant \pi/3$

Phase *A*	
$\overline{P_{AI-I}} = \frac{I_{AI-0}+I_{AI-1}}{2}\frac{V_{in}}{3}\phi/\pi$	$\overline{P_{AI-II}} = \frac{I_{AI-1}+I_{AI-2}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$
$\overline{P_{AI-III}} = \frac{I_{AI-2}+I_{AI-3}}{2}\frac{2V_{in}}{3}\phi_{FL1}/\pi$	$\overline{P_{AI-IV}} = \frac{I_{AI-3}+I_{AI-4}}{2}\frac{2V_{in}}{3}(\frac{\pi}{3}-\phi_{FL1})/\pi$
$\overline{P_{AI-V}} = \frac{I_{AI-4}+I_{AI-5}}{2}\frac{V_{in}}{3}\phi/\pi$	$\overline{P_{AI-VI}} = \frac{I_{AI-5}-I_{AI-0}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$
Phase *B*	
$\overline{P_{BI-I}} = -\frac{I_{BI-0}+I_{BI-1}}{2}\frac{2V_{in}}{3}\phi/\pi$	$\overline{P_{BI-II}} = -\frac{I_{BI-1}+I_{BI-2}}{2}\frac{2V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$
$\overline{P_{BI-III}} = -\frac{I_{BI-2}+I_{BI-3}}{2}\frac{V_{in}}{3}\phi_{FL1}/\pi$	$\overline{P_{BI-IV}} = -\frac{I_{BI-3}+I_{BI-4}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi_{FL1})/\pi$
$\overline{P_{BI-V}} = \frac{I_{BI-4}+I_{BI-5}}{2}\frac{V_{in}}{3}\phi/\pi$	$\overline{P_{BI-VI}} = \frac{I_{BI-5}-I_{BI-0}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$
Phase *C*	
$\overline{P_{CI-I}} = \frac{I_{CI-0}+I_{CI-1}}{2}\frac{V_{in}}{3}\phi/\pi$	$\overline{P_{CI-II}} = \frac{I_{CI-1}+I_{CI-2}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$
$\overline{P_{CI-III}} = -\frac{I_{CI-2}+I_{CI-3}}{2}\frac{V_{in}}{3}\phi_{FL1}/\pi$	$\overline{P_{CI-IV}} = -\frac{I_{CI-3}+I_{CI-4}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi_{FL1})/\pi$
$\overline{P_{CI-V}} = -\frac{I_{CI-4}+I_{CI-5}}{2}\frac{2V_{in}}{3}\phi/\pi$	$\overline{P_{CI-VI}} = -\frac{I_{CI-5}-I_{CI-0}}{2}\frac{2V_{in}}{3}(\frac{\pi}{3}-\phi)/\pi$

TABLE VI
THREE-PHASE SEGMENTAL TRANSFERRED POWER FOR $\pi/3 \leqslant \phi \leqslant \pi/3+\phi_{FL1}$

Phase *A*	
$\overline{P}_{AII-I}=\frac{I_{AII-0}+I_{AII-1}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{AII-II}=\frac{I_{AII-1}+I_{AII-2}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{AII-III}=\frac{I_{AII-2}+I_{AII-3}}{2}\frac{2V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{AII-IV}=\frac{I_{AII-3}+I_{AII-4}}{2}\frac{2V_{in}}{3}(\phi_{FL2}+\frac{\pi}{3}-\phi)/\pi$
$\overline{P}_{AII-V}=\frac{I_{AII-4}+I_{AII-5}}{2}\frac{2V_{in}}{3}(\frac{\pi}{3}-\phi_{FL2})/\pi$	$\overline{P}_{AII-VI}=\frac{I_{AII-5}-I_{AII-0}}{2}\frac{V_{in}}{3}\frac{\pi}{3}/\pi$
Phase *B*	
$\overline{P}_{BII-I}=-\frac{I_{BII-0}+I_{BII-1}}{2}\frac{2V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{BII-II}=-\frac{I_{BII-1}+I_{BII-2}}{2}\frac{2V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{BII-III}=-\frac{I_{BII-2}+I_{BII-3}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{BII-IV}=-\frac{I_{BII-3}+I_{BII-4}}{2}\frac{V_{in}}{3}(\phi_{FL2}+\frac{\pi}{3}-\phi)/\pi$
$\overline{P}_{BII-V}=-\frac{I_{BII-4}+I_{BII-5}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi_{FL2})/\pi$	$\overline{P}_{BII-VI}=\frac{I_{BII-5}-I_{BII-0}}{2}\frac{V_{in}}{3}\frac{\pi}{3}/\pi$
Phase *C*	
$\overline{P}_{CII-I}=\frac{I_{CII-0}+I_{CII-1}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{CII-II}=\frac{I_{CII-1}+I_{CII-2}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{CII-III}=-\frac{I_{CII-2}+I_{CII-3}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{CII-IV}=-\frac{I_{CII-3}+I_{CII-4}}{2}\frac{V_{in}}{3}(\phi_{FL2}+\frac{\pi}{3}-\phi)/\pi$
$\overline{P}_{CII-V}=-\frac{I_{CII-4}+I_{CII-5}}{2}\frac{V_{in}}{3}(\frac{\pi}{3}-\phi_{FL2})/\pi$	$\overline{P}_{CII-VI}=-\frac{I_{CII-5}-I_{CII-0}}{2}\frac{2V_{in}}{3}\frac{\pi}{3}/\pi$

TABLE VII
THREE-PHASE SEGMENTAL TRANSFERRED POWER FOR $\pi/3+\phi_{FL1} \leqslant \phi \leqslant \pi/2$

Phase *A*	
$\overline{P}_{AIII-I}=\frac{I_{AIII-0}+I_{AIII-1}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{AIII-II}=\frac{I_{AIII-1}+I_{AIII-2}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{AIII-III}=\frac{I_{AIII-2}+I_{AIII-3}}{2}\frac{2V_{in}}{3}\phi_{FL3}/\pi$	$\overline{P}_{AIII-IV}=\frac{I_{AIII-3}+I_{AIII-4}}{2}\frac{2V_{in}}{3}(\phi-\phi_{FL3}-\frac{\pi}{3})/\pi$
$\overline{P}_{AIII-V}=\frac{I_{AIII-4}+I_{AIII-5}}{2}\frac{2V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$	$\overline{P}_{AIII-VI}=\frac{I_{AIII-5}-I_{AIII-0}}{2}\frac{V_{in}}{3}\frac{\pi}{3}/\pi$
Phase *B*	
$\overline{P}_{BIII-I}=-\frac{I_{BIII-0}+I_{BIII-1}}{2}\frac{2V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{BIII-II}=-\frac{I_{BIII-1}+I_{BIII-2}}{2}\frac{2V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{BIII-III}=-\frac{I_{BIII-2}+I_{BIII-3}}{2}\frac{V_{in}}{3}\phi_{FL3}/\pi$	$\overline{P}_{BIII-IV}=-\frac{I_{BIII-3}+I_{BIII-4}}{2}\frac{V_{in}}{3}(\phi-\phi_{FL3}-\frac{\pi}{3})/\pi$
$\overline{P}_{BIII-V}=-\frac{I_{BIII-4}+I_{BIII-5}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$	$\overline{P}_{BIII-VI}=\frac{I_{BIII-5}-I_{BIII-0}}{2}\frac{V_{in}}{3}\frac{\pi}{3}/\pi$
Phase *C*	
$\overline{P}_{CIII-I}=\frac{I_{CIII-0}+I_{CIII-1}}{2}\frac{V_{in}}{3}(\phi-\frac{\pi}{3})/\pi$	$\overline{P}_{CIII-II}=\frac{I_{CIII-1}+I_{CIII-2}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$
$\overline{P}_{CIII-III}=-\frac{I_{CIII-2}+I_{CIII-3}}{2}\frac{V_{in}}{3}\phi_{FL3}/\pi$	$\overline{P}_{CIII-IV}=-\frac{I_{CIII-3}+I_{CIII-4}}{2}\frac{V_{in}}{3}(\phi-\phi_{FL3}-\frac{\pi}{3})/\pi$
$\overline{P}_{CIII-V}=-\frac{I_{CIII-4}+I_{CIII-5}}{2}\frac{V_{in}}{3}(\frac{2\pi}{3}-\phi)/\pi$	$\overline{P}_{CIII-VI}=-\frac{I_{CIII-5}-I_{CIII-0}}{2}\frac{2V_{in}}{3}\frac{\pi}{3}/\pi$

REFERENCES

[1] R. W. A. A. de Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991, doi: 10.1109/28.67533.

[2] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020, doi: 10.1109/TPEL.2019.2927930.

[3] H. van Hoek, M. Neubert, and R. W. de Doncker, "Enhanced modulation strategy for a three-phase dual active bridge - boosting efficiency of an electric vehicle converter," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5499–5507, Dec. 2013, doi: 10.1109/TPEL.2013.2251905.

[4] H. Chen, S. Ouyang, J. Liu, and X. Li, "An asymmetrical phase-shift scheme of three-phase dual active bridge with minimum current root-mean-square value control," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14343–14361, Dec. 2022, doi: 10.1109/TPEL.2022.3192781.

[5] J. Sun, L. Qiu, X. Liu, J. Zhang, J. Ma, and Y. Fang, "Optimal simultaneous PWM control for three- phase dual-active-bridge converters to minimize current stress in the whole load range," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5822–5837, Oct. 2021, doi: 10.1109/JESTPE.2020.3047400.

[6] L. M. Cúnico, Z. M. Alves, and A. L. Kirsten, "Efficiency-optimized modulation scheme for three-phase dual-active-bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5955–5965, Jul. 2021, doi: 10.1109/TIE.2020.2992961.

[7] A. Anurag, S. Acharya, S. Bhattacharya, T. R. Weatherford, and A. A. Parker, "A Gen-3 10-kV SiC MOSFET-based medium-voltage three-phase dual active bridge converter enabling a mobile utility support equipment solid state transformer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 1519–1536, Apr. 2022, doi: 10.1109/JESTPE.2021.3069810.

[8] L. Shu et al., "A three-phase triple-voltage dual-active-bridge converter for medium voltage DC transformer to reduce the number of submodules," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11574–11588, Nov. 2020, doi: 10.1109/TPEL.2020.2988280.

[9] J. Hu, Z. Yang, S. Cui, and R. W. De Doncker, "Closed-form asymmetrical duty-cycle control to extend the soft-switching range of three-phase dual-active-bridge converters," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9609–9622, Aug. 2021, doi: 10.1109/TPEL.2021.3055369.

[10] L. M. Cúnico and A. L. Kirsten, "Improved ZVS range for three-phase dual-active-bridge converter with wye-extended-delta transformer," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7984–7993, Aug. 2022, doi: 10.1109/TIE.2021.3102482.

[11] J. Sun, L. Qiu, X. Liu, J. Zhang, J. Ma, and Y. Fang, "Improved model predictive control for three-phase dual-active-bridge converters with a hybrid modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4050–4064, Apr. 2022, doi: 10.1109/TPEL.2021.3126589.

[12] L. Chen, S. Shao, Q. Xiao, L. Tarisciotti, P. W. Wheeler, and T. Dragičević, "Model predictive control for dual-active-bridge converters supplying pulsed power loads in naval DC micro-grids," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1957–1966, Feb. 2020, doi: 10.1109/TPEL.2019.2917450.

[13] N. H. Baars, J. Everts, H. Huisman, J. L. Duarte, and E. A. Lomonova, "A 80-kW isolated DC–DC converter for railway applications," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6639–6647, Dec. 2015, doi: 10.1109/TPEL.2015.2396006.

[14] S. Günter et al., "Load control for the DC electrical power distribution system of the more electric aircraft," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3937–3947, Apr. 2019, doi: 10.1109/TPEL.2018.2856534.

[15] D. Wang, B. Nahid-Mobarakeh, and A. Emadi, "Second harmonic current reduction for a battery-driven grid interface with three-phase dual active bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 9056–9064, Nov. 2019, doi: 10.1109/TIE.2019.2899563.

[16] B. Zhao, Q. Song, W. Liu, and Y. Sun, "A synthetic discrete design methodology of high-frequency isolated bidirectional DC/DC converter for grid-connected battery energy storage system using advanced components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5402–5410, Oct. 2014, doi: 10.1109/TIE.2014.2304915.

[17] S. S. G. Acharige, M. E. Haque, M. T. Arif, N. Hosseinzadeh, K. N. Hasan, and A. M. T. Oo, "Review of electric vehicle charging technologies, standards, architectures, and converter configurations," *IEEE Access*, vol. 11, pp. 41218–41255, 2023, doi: 10.1109/ACCESS.2023.3267164.

[18] C. Wang, P. Zheng, and J. Bauman, "A review of electric vehicle auxiliary power modules: Challenges, topologies, and future trends," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11233–11244, Sep. 2023, doi: 10.1109/TPEL.2023.3288393.

[19] L. M. Cúnico, Z. M. Alves, and A. L. Kirsten, "Efficiency-optimized modulation scheme for three-phase dual-active-bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5955–5965, Jul. 2021, doi: 10.1109/TIE.2020.2992961.

[20] S. Haghbin, F. Blaabjerg, and A. S. Bahman, "Frozen leg operation of a three-phase dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4239–4248, May 2019, doi: 10.1109/TPEL.2018.2865092.

[21] S. K. Rastogi, S. S. Shah, B. N. Singh, and S. Bhattacharya, "Mode analysis, transformer saturation, and fault diagnosis technique for an open-circuit fault in a three-phase DAB converter," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7644–7660, Jun. 2023, doi: 10.1109/TPEL.2023.3241654.

[22] C. Wang and J. Bauman, "Comparative analysis of reliability for single-phase and three-phase dual active bridge converters," in *Proc. IEEE Transp. Electrific. Conf. Expo*, 2024, pp. 1–6.

[23] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011, doi: 10.1109/TIA.2011.2124436.

[24] S. S. Khan and H. Wen, "A fast and low-cost open-circuit fault detection and isolation technique for three-phase dual-active-bridge converters based on finite state machines," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2751–2766, Feb. 2024, doi: 10.1109/TPEL.2023.3337097.

[25] Y. Guan, Y. Xiao, L. Qin, X. Liu, H. Deng, and W. Wu, "A path-based switch open circuit fault-tolerant method for three-phase DAB converter," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1577–1595, Jan. 2024, doi: 10.1109/TPEL.2023.3316265.

[26] A. M. Airabella, G. G. Oggier, L. E. Piris-Botalla, C. A. Falco, and G. O. García, "Semi-conductors analysis in dual active bridge DC-DC converter," *IET Power Electron.*, vol. 9, no. 6, pp. 1103–1110, May 2016, doi: 10.1049/iet-pel.2015.0299.

[27] S. S. Khan and H. Wen, "Universal sensorless open-circuit fault detection and isolation method of dual-active-bridge converters with low-cost diagnostic circuit," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13652–13667, Nov. 2022, doi: 10.1109/TPEL.2022. 3182382.

[28] P. S. Bhakar and K. Jayaraman, "A new fault-tolerant scheme for switch failures in dual active bridge DC-DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7627–7637, Dec. 2022, doi: 10.1109/JESTPE.2022.3177345.

[29] H. Wen, J. Li, H. Shi, Y. Hu, and Y. Yang, "Fault diagnosis and tolerant control of dual-active-bridge converter with triple-phase shift control for bidirectional EV charging systems," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 1, pp. 287–303, Mar. 2021, doi: 10.1109/TTE.2020.3045673.

[30] M. Zheng, H. Wen, H. Shi, Y. Hu, Y. Yang, and Y. Wang, "Open-circuit fault diagnosis of dual active bridge DC-DC converter with extended-phase-shift control," *IEEE Access*, vol. 7, pp. 23752–23765, 2019, doi: 10.1109/ACCESS.2019.2899133.

[31] S. S. Khan, H. Wen, H. Shi, Y. Hu, L. Jiang, and G. Chen, "Multiple open-circuit fault detection and isolation using universal low-cost diagnosis circuits for reconfigurable dual-active-bridge converters," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6504–6521, May 2023, doi: 10.1109/TPEL.2023.3234592.

[32] A. Davoodi, N. Noroozi, and M. R. Zolghadri, "A Fault-tolerant strategy for three-phase dual active bridge converter," in *Proc. 10th Int. Power Electron., Drive Syst., Technol. Conf.*, 2019, pp. 253–258, doi: 10.1109/PEDSTC.2019.8697835.

[33] T.-T. Le, M.-K. Nguyen, T.-D. Duong, C. Wang, and S. Choi, "Open-circuit fault-tolerant control for a three-phase current-fed dual active bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1586–1596, Feb. 2023, doi: 10.1109/TIE.2022.3156036.

[34] S. K. Rastogi, S. S. Shah, B. N. Singh, and S. Bhattacharya, "Vector-based open-circuit fault diagnosis technique for a three-phase DAB converter," *IEEE Trans. Ind. Electron.*, vol. 71, no. 7, pp. 8207–8211, Jul. 2024, doi: 10.1109/TIE.2023.3312430.

[35] A. Davoodi, D. Sadeghpour, M. Kashif, S. A. Albahrani, S. M. Atarodi, and M. Zolghadri, "A novel transistor open-circuit fault localization scheme for three-phase dual active bridge," in *Proc. Australas. Univ. Power Eng. Conf.*, 2018, pp. 1–6, doi: 10.1109/AUPEC.2018.8757901.

[36] M. Berger, I. Kocar, H. Fortin-Blanchette, and C. Lavertu, "Open-phase fault-tolerant operation of the three-phase dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3651–3662, Apr. 2020, doi: 10.1109/TPEL.2019.2933487.

[37] P. S. Bhakar and K. Jayaraman, "A new fault-tolerant scheme for switch failures in dual active bridge DC-DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7627–7637, Dec. 2022, doi: 10.1109/JESTPE.2022.3177345.

[38] H. Shi, H. Wen, G. Chen, Q. Bu, G. Chu, and Y. Zhu, "Multiple-fault-tolerant dual active bridge converter for DC distribution system," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1748–1760, Feb. 2022, doi: 10.1109/TPEL.2021.3106508.

[39] H. Tarzamni, F. P. Esmaeelnia, M. Fotuhi-Firuzabad, F. Tahami, S. Tohidi, and P. Dehghanian, "Comprehensive analytics for reliability evaluation of conventional isolated multiswitch PWM DC-DC converters," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5254–5266, May 2020, doi: 10.1109/TPEL.2019.2944924.

[40] N. Zhao, J. Liu, Y. Shi, J. Yang, J. Zhang, and X. You, "Mode analysis and fault-tolerant method of open-circuit fault for a dual active-bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6916–6926, Aug. 2020, doi: 10.1109/TIE.2019.2937066.

[41] Y. Wang, Y. Guan, M. Molinas, O. B. Fosso, W. Hu, and Y. Zhang, "Open-circuit switching fault analysis and tolerant strategy for dual-active-bridge DC–DC converter considering parasitic parameters," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15020–15034, Dec. 2022, doi: 10.1109/TPEL.2022.3193872.

[42] C. Song, A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "Open-circuit fault diagnosis and tolerant control for 2/3-level DAB converters," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5392–5410, Apr. 2023, doi: 10.1109/TPEL.2022.3233313.

[43] T.-T. Le, T.-T. Pham, M.-K. Nguyen, T.-D. Duong, D.-D. Nguyen, and M.-C. Dinh, "Open-circuit fault-tolerant method for three-phase CF-DAB converter with auto-balancing control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 4, pp. 3482–3493, Aug. 2024, doi: 10.1109/JESTPE.2024.3411038.

[44] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012, doi: 10.1109/TPEL.2011.2108317.

[45] H. van Hoek, "Design and operation considerations of three-phase dual active bridge converters for low-power applications with wide voltage ranges," Ph.D. dissertation, RWTH Aachen Univ., Aachen, Germany, 2017.

[46] G. Schulz and J. Bauman, "Time-domain analysis and optimization of a three-phase dual-active-bridge converter with variable duty-cycle modulation," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15338–15352, Dec. 2023, doi: 10.1109/TPEL.2023.3311314.

[47] M. Hosseinzadeh and F. R. Salmasi, "Robust optimal power management system for a hybrid AC/DC micro-grid," *IEEE Trans. Sustain. Energy*, vol. 6, no. 3, pp. 675–687, Jul. 2015, doi: 10.1109/TSTE.2015.2405935.

[48] Z. Li, Y. Wang, L. Shi, J. Huang, Y. Cui, and W. Lei, "Generalized averaging modeling and control strategy for three-phase dual-active bridge dc-dc converters with three control variables," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1078–1084.

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