Analytical Transient Model of Field-Stop IGBT Accounting for Temperature Dependence

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***Abstract*—The field-stop (FS) insulated gate bipolar transistors (IGBTs) (FS IGBTs) become a mainstay in the IGBT market for medium and high-power applications nowadays. The wide application of FS IGBTs led to a great desire for fast and accurate simulation of the device. In this article, an analytical transient model is proposed for FS IGBT. Based on the improved understanding of the switching behavior of FS IGBT, complete analytical expressions of V_{ce} and I_c at switching transient are derived. The pivotal device characteristics depending on the junction temperature T_{j1} of low-side IGBT and T_{j2} of high-side IGBT are identified and modeled. To extract model parameters, experimental and datasheet-driven parameter extraction methods are proposed. Double-pulse tests are performed on 600 V and 1200 V-rated FS IGBTs under various test conditions. The simulated and experimental results are compared and good agreement is obtained.**

***Index Terms*—Field-stop (FS) insulated gate bipolar transistor (IGBT), IGBT analytical modeling, switching transient, temperature-dependent model.**

I. Introduction

FIELD-STOP insulated gate bipolar transistors (FS IGBTs) are widely used for medium and high-voltage power converters. With a thin and lightly doped field-stop (FS) layer utilized, the FS IGBT can achieve an improved tradeoff between the on-state voltage and switching loss compared to traditional nonpunch-through (NPT) IGBTs and punch through (PT) IGBTs [1]. Due to the merits, the FS IGBTs dominate the medium and high voltage IGBT market nowadays. To design the FS IGBT-based power conversion system, a fast and accurate model is required. In the past, various IGBT models under different levels are presented [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. The models can be roughly categorized into three kinds: behavior models, analytical models, and physics-based models.

The behavior IGBT models only reflect the basic device properties of IGBT [2], [3]. The models can not include the variation of model parameters when different load and junction temperature conditions are applied [2], [3]. As a result, the behavior IGBT models provide rough and fast system-level simulation. The analytical models simplify the IGBT as a physical property-based system [4], [5], [6], [7], which is used to obtain analytical expressions on the switching characteristics of IGBT. The analytical models provide fast simulation. The parameter extraction for the models is also relatively easy. The physics-based IGBT models describe the excess carrier dynamics in the N-base by solving the ambipolar diffusion equation (ADE) [8], [9], [10], [11]. Therefore, the models can include the internal semiconductor physics of IGBT [8], [9], [10], [11]. The physics-based IGBT models have good accuracy. However, the models are often time-consuming and require complex parameter extraction procedures.

Looking into the previous research on the IGBT models [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], the behavior models provide fast simulation. However, the poor accuracy makes them only suitable for basic system-level modeling. The physics-based models are much more accurate since ADE is used to model excess carrier dynamic in the N-base. However, the simulation speed of the models is extremely slow. The requirement of the massive device parameters also hinders its applications.

Compared to other models, the analytical IGBT models can achieve a tradeoff between accuracy and simulation speed. The parameter extraction is also relatively easy. However, the previous proposed analytical IGBT models [4], [5], [6], [7] have a few major drawbacks, which greatly hinder their application. First, since the ADE cannot be solved analytically, previous proposed analytical models often neglect excess carrier dynamics in the N-base of the IGBT. This greatly reduces the accuracy of the models. Second, the turn-ON behavior of IGBT is greatly affected by the reverse recovery of the freewheeling p–i–n diode in the high side. Since the reverse recovery-induced excess charge extraction of the diode is often neglected, the previous analytical models cannot precisely predict the turn-ON behavior of IGBT. Finally, the temperature dependency of the switching behavior is dominated by the temperature-dependent excess carrier dynamics of the IGBT and its freewheeling p–i–n diode. Since the excess carrier dynamics are not considered, the previous proposed analytical models cannot precisely predict the temperature-dependent switching behavior.

To tackle these problems, a transient analytical FS IGBT model is proposed in this study. In Section II, the switching behavior of FS IGBTs is analyzed. The pivotal devices' physics, including excess carrier dynamics of FS IGBT and p–i–n diode, are identified. Based on the improved understanding of the

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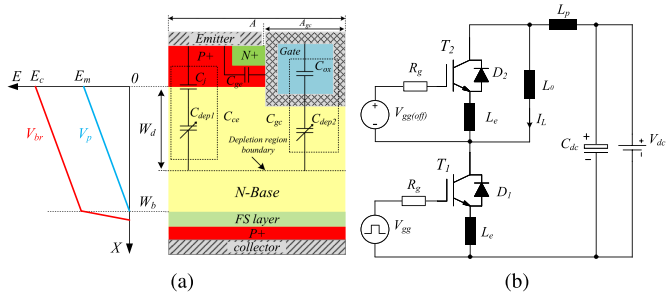


Fig. 1. (a) Structure, stray capacitances, and electric field distribution of FS IGBT when V_p and V_{br} are applied. (b) IGBT-based half-bridge test circuit.

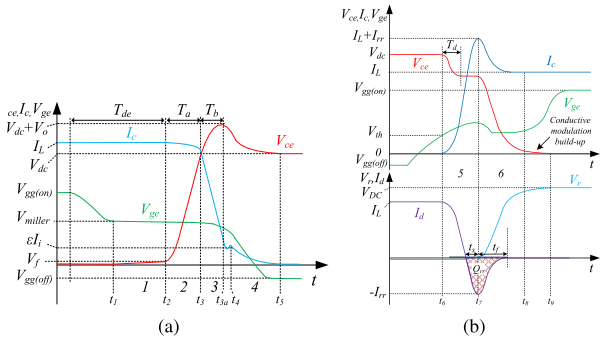


Fig. 2. Switching transient of FS IGBT. (a) Phases 1–4 of turn-OFF transient and (b) phases 5 and 6 of turn-ON transient.

switching characteristics of FS IGBT, a complete analytical model is proposed in Section IV. In Section V, the dominant temperature-dependent physical characteristics and their dependency on the junction temperature T_{j1} for low-side IGBT and T_{j2} for high-side IGBT are identified and included in the proposed model. Section VI proposes the experimental and datasheet-driven parameter extraction methods. In Section VII, the experimental validation is performed. Finally, Section VIII concludes this article.

II. Switching Behavior of FS IGBT

Fig. 1(a) presents the structure and the stray capacitance of the FS IGBT. The electric fields of critical voltages V_p and V_{br} are also presented. V_p is the voltage, which can deplete the N-base. When V_p is applied, a triangular electric field distribution is achieved in the N-base and E_m is the maximum electric field at $X = 0$. When the breakdown voltage V_{br} is applied, a trapezoidal electric field distribution is generated and E_m becomes E_c, which is critical electrical field of silicon. Due to the trapezoidal electric field distribution, the N-base region is much thinner than the NPT IGBTs under the same voltage rating [1]. The FS IGBT thereby can achieve the improved tradeoff between the on-state voltage and switching losses. Fig. 1(a) shows the gate-emitter capacitance C_{ge}, gate-collector capacitance C_{gc}, and collector-emitter capacitance C_{ce} of FS IGBT. C_{ce} consists of series-connected junction capacitance C_j and depletion capacitance C_{dep1}. C_{gc} consists of series-connected gate oxide capacitance C_{ox} and depletion capacitance C_{dep2}. The C_{ox}, C_j, and C_{ge} are constant capacitances. C_{dep1} and C_{dep2} are generated by the depletion region and thereby depends on V_{ce}.

Fig. 1(b) shows IGBT-based half-bridge test circuit. T_1 and D_1 are the low-side active IGBT and its freewheeling p–i–n diode. T_2 and D_2 are the high-side synchronous IGBT and its freewheeling p–i–n diode. L_0 is load inductor, which support load current I_L. R_g is gate resistance. L_e is common emitter stray inductance. L_p is the stray inductance of the power loop. V_{dc} is dc-bus voltage. C_{dc} represent dc-bus capacitor. V_{gg} is gate drive voltage, which drives T_1 to switch. With off-state gate voltage $V_{\text{gg(off)}}$ applied, the diode D_2 is utilized as a freewheeling diode. The gate loop stray inductance is neglected since it only affects the turn-ON/OFF delay time and does not have significant impact on switching behavior [12].

A. Turn-Off Behavior

Fig. 2(a) shows the turn-OFF waveforms of FS IGBT, which is divided into phases 1–4. Fig. 3(a)–(d) shows the equivalent circuits of each phase. The four phases are given as follows.

Phase 1 [$t_1 - t_2$, see Fig. 3(a)]: Phase 1 starts when the V_{ge} reduces to its miller voltage V_{miller} for I_L. In phase 1, V_{ce} increases to generate displacement current on C_{ce} and C_{gc} to compensate the reduction of channel current I_{ch}. As shown in Fig. 3(a), $C_{\text{gc}}dV_{\text{ce}}/dt$ induced displacement current I_{cg} generates voltage V_g, which greatly hider the gate voltage V_{ge} to turn-OFF [13]. With $C_{\text{gc}} \approx C_{\text{ox}}$, the large C_{gc} induce a small dV_{ce}/dt in phase 1. Since the CdV/dt induced displacement current on T_2 is very small, the I_c reduction neglected. Phase 2 [$t_2 - t_3$, see Fig. 3(b)]: Phase 2 initiates when V_{ce} rises above V_f (around tens of volts [14]). In phase 2, the depletion region extends to generate the C_{dep2}, which induces abrupt reduction of C_{gc}, as shown in Fig. 1(a). The $C_{\text{gc}}dV/dt$ induced feedback becomes much weaker, which causes a high dV_{ce}/dt. The depletion region extension extracts the excess charge Q_{ext} in the N-base, which generates current I_{ext}, as shown in Fig. 4(a). A charge extraction capacitance C_{ext} is used to represent the capacitive behavior and $I_{\text{ext}} = C_{\text{ext}}dV_{\text{ce}}/dt$, as shown in Fig. 3(b). C_{ext} is expressed by [15]

$$C_{\text{ext}} = \frac{AP_0\epsilon_{si}}{N_bW_d}\text{sech}^2\left(\frac{W}{2L}\right) \tag{1}$$

where $L = \sqrt{D\tau_L}$ is the diffusion length. D is the ambipolar diffusivity. τ_L is the excess carrier lifetime in the N-base. A is the device's active area. ϵ_{si} is the dielectric coefficient of silicon. N_b is the N-base doping concentration. As shown in Fig. 4(a), P_0 is the excess carrier density at $x = 0$. $W = W_b - W_d$ is the undepleted N-base width. W_b is the N-base width. W_d is the depletion region width given by [16]

$$W_d = \sqrt{\frac{2\epsilon_{si}V_{\text{ce}}}{qN_b}} \tag{2}$$

where q is the electronic charge. In phase 2, the high dV_{ce}/dt induces a large displacement current on T_2, which give rise to the reduction of I_c, as shown in Fig. 2(a).

Phase 3 [$t_3 - t_4$, see Fig. 3(c)]: When V_{ce} reaches V_{dc}, I_L can divert from the T_1 to D_2 and phase 3 starts. In this phase,

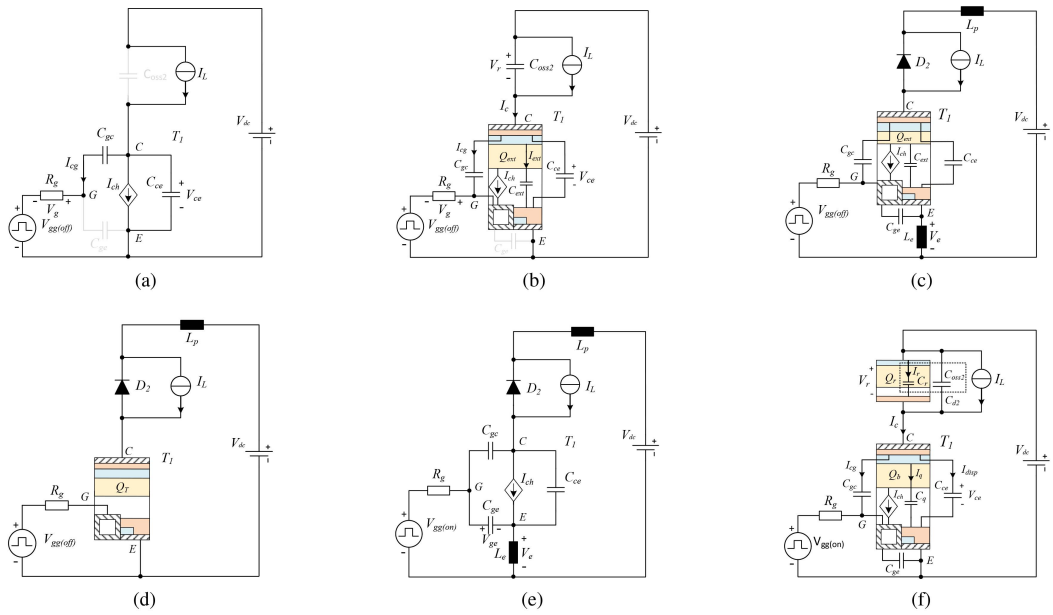


Fig. 3. Equivalent circuit of (a) phase 1, (b) phase 2, (c) phase 3, (d) phase 4, (e) phase 5, and (f) phase 6.

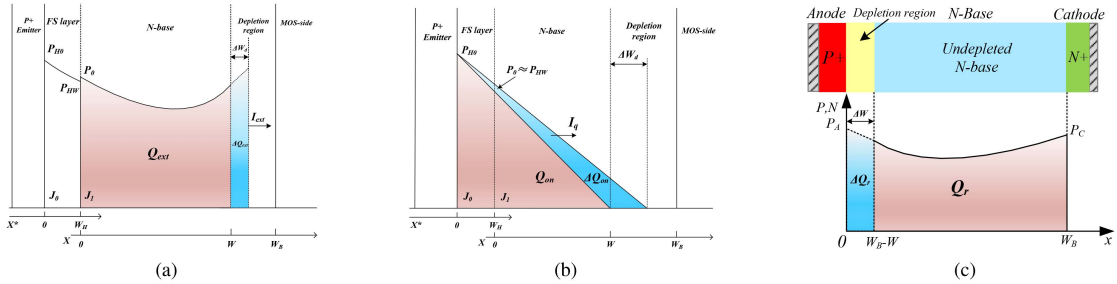


Fig. 4. Charge equivalent capacitance. (a) C_{ext} generated by excess charge extraction at turn-OFF of low-side IGBT. (b) C_q generated by excess charge build up at turn-ON of low-side IGBT. (c) C_r due to excess charge extraction at reverse recovery transient of high-side p–i–n diode.

I_{ch} quickly vanishes, which causes initial reduction of I_c. The dI_c/dt generates a voltage on the inductance $L_p + L_e$, which supports the V_{ce} to overshoot and reaches its peak voltage $V_{\text{dc}} + V_o$ at t_{3a}, as shown in Fig. 2(a). V_o is the overshoot voltage. As shown in Fig. 3(c), the high dI_c/dt generates voltage V_e on the common emitter inductance L_e, which slow down gate voltage turn-OFF and hinders the dI_c/dt to increases.

Phase 4 [$t_4 - t_5$, see Fig. 3(d)]: In the beginning of phase 4, $I_c = \varepsilon I_i$. I_i is the I_c at the initial of phase 3. ε is a constant ratio depends on the properties of IGBT [17]. In this phase, I_c slowly decays due to the recombination of residual excess charge Q_t in the N-base and buffer layer, as shown in Fig. 3(d). A tail current of I_c is thereby generated, as shown in Fig. 2(a). Due to the decay of the tail current, the voltage $dI_c/dt(L_p + L_e)$ on the inductance $L_p + L_e$ reduces. The V_{ce} thereby slowly returns to V_{dc} in this phase.

B. Turn-On Behavior

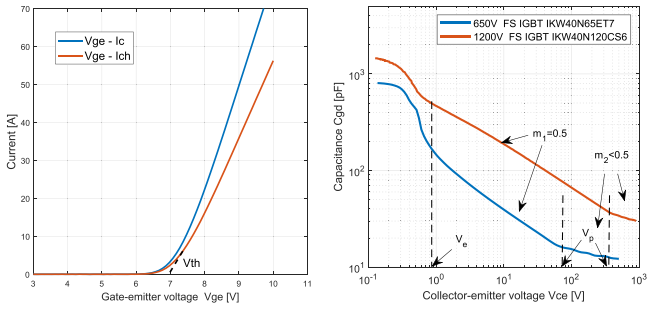
Fig. 2(b) shows the turn-ON waveforms of FS IGBT. The turn-ON transient is divided into two phases, their equivalent circuits are given in Figs. 3(e) and (f).

Phase 5 [$t_6 - t_7$, see Fig. 3(e)]: When V_{ge} reaches V_{th}, phase 5 starts. In phase 5, MOS channel starts to conduct I_{ch}, which supports I_c to increase. With high dI_c/dt, the $L_e dI_c/dt$ induces feedback mechanism presented in phase 3 also occurs. Due to the feedback action, a constant dI_c/dt is achieved, which plateaued V_{ce} when $t > t_6 + T_d$, as shown in Fig. 2(b). Phase 5 ends when I_c reaches its maximum current $I_L + I_{\text{rr}}$ [18], where peak reverse recovery current I_{rr} is

$$I_{\text{rr}} = \sqrt{\frac{2Q_{\text{rr}} dI_c/dt|_{I_c=I_L}}{1+S}} \tag{3}$$

where $dI_c/dt|_{I_c=I_L}$ is the current slope when $I_c = I_L$. As shown in Fig. 2(b), Q_{rr} is the reverse recovery charge. $S = t_f/t_s$ is the softness factor of the body diode.

Phase 6 [$t_7 - t_8$, see Fig. 3(f)]: The phase 6 initiates when I_c reaches $I_L + I_{\text{rr}}$. In this phase, the high-side diode D_2 starts to support reverse voltage and V_{ce} reduces. The depletion region thereby shrinks and excess charge Q_{on} in the N-base and buffer layer starts to build up, as shown in Fig. 4(b). The build-up of Q_{on} generates capacitive current I_q. In Fig. 3(f), a capacitance C_q is used to represent the capacitive behavior with $I_q = C_q dV_{\text{ce}}/dt$.



(a) (b)

Fig. 5. (a) $I_c - V_{ge}$ and $I_{ch} - V_{ge}$ curves of IKW40N120CS6S6 ($V_{ce} = 20\,V$) and (b) $\log(C_{gc})-\log(V_{ce})$ curves of a 650 V and 1200 V FS IGBTs.

C_q can be expressed as [18]

$$C_q = \frac{A\epsilon_{si}P_{H0}}{2W_dN_b} \tag{4}$$

where P_{H0} is the excess carrier density at $x = 0$, as shown in Fig. 4(b). As shown in Fig. 4(c), the depletion region of diode D_2 extends and extract excess charge Q_r in N-base in phase 6, which is similar to the charge extraction in phase 2 to generates the C_{ext}. As shown in 3(f), the Q_r extraction generates a capacitive current I_r and a capacitance C_r ($I_r = C_r dV_r/dt$) is used to represent the capacitive behavior. The total diode capacitance $C_{d2} = C_r + C_{oss2}$, where C_{oss2} is the output capacitance of high-side switch.

After t_8, the depletion region vanishes. However, since conductive modulation is not achieved in N-base, V_{ce} is higher than on-state voltage. From t_8 to t_9, the conductive modulation gradually builds up and V_{ce} slowly reduces to on-state level, as shown in Fig. 2(b). Since the voltage reduction is very small, the conductive modulation process is neglected.

III. Modeling of Pivotal Device Characteristics

A. MOS Channel Transfer Characteristics

Fig. 5(a) shows $I_c - V_{ge}$ curve. The MOS channel current I_{ch} is a part of the collector current I_c and is given by [19]

$$I_{ch} \approx \frac{b}{1+b}I_c \tag{5}$$

where $b = \mu_n/\mu_p$ is the ratio of electron and hole mobilities. With (5) used, $I_{ch} - V_{ge}$ curves is obtained in Fig. 5(a). In Fig. 5(a), a linear relationship between I_{ch} and V_{ge} is approximately obtained and I_{ch} is thereby expressed as

$$I_{ch} = G_m(V_{ge} - V_{th}). \tag{6}$$

As shown in Fig. 5(a), the transconductance G_m is the slope of the $I_{ch} - V_{ge}$ curve. The threshold voltage V_{th} can be obtained by extrapolating the linear part of the $I_{ch} - V_{ge}$ curve to x-axis. Combining (5) and (6), V_{miller} for I_c is

$$V_{miller} = \frac{bI_c}{G_m(1+b)} + V_{th}. \tag{7}$$

TABLE I
Coefficients of Various FS IGBTs

Part number	V_{br}	m_1	m_2	V_p	p
IKW40N65ET7	650V	0.47	0.16	79V	0.20
FGHL75T65MQDTL4	650V	0.58	0.17	62V	0.21
FGZ75XS65C	650V	0.48	0.31	90V	0.14
FGH4L40T120LQD	1200V	0.49	0.17	330V	0.17
IKW40N120CS6S6	1200V	0.45	0.19	375V	0.16
IKW50N120CS7	1200V	0.44	0.17	270V	0.18

B. Capacitances C_{gc} and C_{oss}

Due to the $C_{gc}dV/dt$ induced feedback, C_{gc} is critical for the IGBT switching behavior. Fig. 5(b) shows $\log(C_{gc})-\log(V_{ce})$ curves for 650 V and 1200 V rated FS IGBTs. In Fig. 5(b), the critical voltages V_e and V_p are marked. When $V_{ce} < V_e$, the depletion region is not formed and $C_{gc} \approx C_{ox}$, as shown in Fig. 1(a). When $V_{ce} > V_e$, the depletion region is formed, which generate C_{dep2}. Since $C_{dep2} \ll C_{ox}$, $C_{gc} \approx C_{dep2}$. C_{dep2} can be expressed as [16]

$$C_{dep2} = \epsilon_{si}A_{gc}\left(\frac{2\epsilon_{si}V_{ce}}{qN_b}\right)^{-0.5} \tag{8}$$

where A_{gc} is the gate-collector overlap area, as shown in Fig. 1(a). The slope of $\log(C_{gc})-\log(V_{ce})$ curve is thereby close to -0.5 when $V_{ce} > V_e$, as shown in Fig. 5(b). When $V_{ce} > V_p$, the depletion region reaches through the FS layer, as shown in Fig. 1(a). The relatively highly doped FS layer hinders the extension of the depletion region. The slope of $\log(C_{gc})-\log(V_{ce})$ curve thereby becomes much gentler, as shown in Fig. 5(b). C_{gc} in phases 2, 3, 5, and 6 is expressed by

$$C_{gc} = \begin{cases} \dfrac{C_{gc0}}{V_{ce}{}^{m_1}} & V_e < V_{ce} \le V_p \\ \dfrac{C_{gc1}}{V_{ce}{}^{m_2}} & V_{ce} > V_p \end{cases} \tag{9}$$

where C_{gc0} is the C_{gc} when $V_{ce} = V_e$. $C_{gc1} = C_{gc0}V_p{}^{m_2-m_1}$. The values of coefficients m_1 and m_2 for various devices are shown in Table I. The m_1 is around 0.5 and agrees with (8). The m_2 is around 0.2, which is used as a default value. Fig. 1(a) shows the triangular shape distribution of electric field when V_p is applied. The V_p can be expressed by

$$V_p = \frac{qN_bW_b^2}{2\epsilon_{si}}. \tag{10}$$

As shown in Fig. 1(a), when V_{br} is applied, the maximum electric field becomes E_c. V_{br} can thereby be expressed as

$$V_{br} = E_cW_b - \frac{qN_bW_b^2}{2\epsilon_{si}}. \tag{11}$$

Combining (10) and (11), the expression of V_p is

$$V_p = \frac{\epsilon_{si}}{2qN_b}\left(E_c - \sqrt{E_c^2 - \frac{2qN_bV_{br}}{\epsilon_{si}}}\right)^2. \tag{12}$$

V_p is thereby a function of V_{br}. Table I summaries the V_p of FS IGBTs with various V_{br}. For 650 V IGBTs, V_p is around 80 V. The V_p is around 300 V for 1200 V IGBTs.In phase 2,

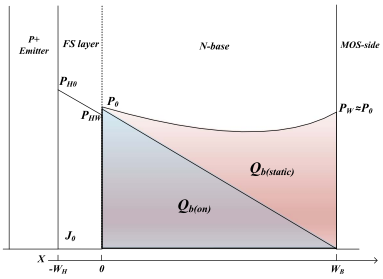


Fig. 6. Definition of excess charges $Q_{B(\text{static})}$ and $Q_{B(\text{on})}$.

the dV_{ce}/dt on the output capacitance C_{oss2} of high-side IGBT induces displacement current, which causes the reduction of I_c. The output capacitance C_{oss} can be approximately expressed as [20]

$$C_{\text{oss}} \approx \frac{C_{\text{oss0}}}{\sqrt{V_{\text{ce}}}} \tag{13}$$

where C_{oss0} is the C_{oss} at $V_{\text{ce}} = V_e$.

C. Capacitances C_{ext}, C_q, and C_{d2} and Charge Q_{rr}.

In this study, the minority carrier dynamics is described by capacitances C_{ext}, C_q, and C_{d2}, which greatly simplified the modeling approach. Assuming $2L \gg W$, (1) can be simplified as

$$C_{\text{ext}} = \frac{AP_0\epsilon_{si}}{N_bW_d}\text{sech}^2\left(\frac{W}{2L}\right) \approx \frac{AP_0\epsilon_{si}}{N_bW_d}. \tag{14}$$

The expression of excess carrier density P_0 is [18], [21]

$$P_0 = \frac{K}{2h_p}\left(\sqrt{1+\frac{4bh_pI_L}{(1+b)qAK^2}}-1\right) \tag{15}$$

where h_p is the emitter recombination coefficient. K is a constant coefficient [18], [21]. Equation (15) can be approximately further simplified as [21]

$$P_0 \approx \left(\frac{bI_L}{qAh_p(1+b)}\right)^p. \tag{16}$$

Using (2), (14), and (16), C_{ext} is obtained

$$C_{\text{ext}} = \frac{C_{e0}}{\sqrt{V_{\text{ce}}}} = \frac{K_e{I_L}^p}{\sqrt{V_{\text{ce}}}} \tag{17}$$

where $C_{e0} = K_eI_L^p$. p and K_e are constant coefficient. Similarly, (4) for C_q can also be expressed as

$$C_q = \frac{C_{q0}}{\sqrt{V_{\text{ce}}}} = \frac{K_q{I_L}^p}{\sqrt{V_{\text{ce}}}} \tag{18}$$

where K_q is a constant coefficient. Table I shows the p extracted for various FS IGBT. p is around 0.2, which is used as the default value.

As shown in Fig. 6, $Q_{b(\text{static})}$ is the excess charge in the N-base at on-state, which is extracted at turn-OFF transient to support C_{ext}. $Q_{b(\text{on})}$, which generates the C_q, is the excess charge at t_9 when the depletion region just vanishes. The relationship between K_q and K_e is obtained as

$$\frac{Q_{b(\text{on})}}{Q_{b(\text{static})}} = \frac{\int_0^{V_{\text{dc}}} C_q dV_{\text{ce}}}{\int_0^{V_{\text{dc}}} C_{\text{ext}} dV_{\text{ce}}} = \frac{K_q}{K_e} \approx 0.5. \tag{19}$$

In FS IGBT, the trench gate is often used, which makes the MOS-side excess carrier density P_W at $X = W_b$ is very close to the carrier density P_0 at $X = 0$ [18], [21], as shown in Fig. 6. $Q_{B(\text{static})} \approx 2Q_{B(\text{on})}$ is thereby assumed in (19).

The charge extraction that generated capacitance C_r for diode is similar to that generates capacitance C_{ext} at turn-OFF [22]. In Fig. 4(c), the excess carrier density P_A and P_C at the boundaries of N-base is very close at on-state [23]. Assuming $P_A \approx P_C$, C_r has the same expression as (1) with P_0 replaced as P_A and V_{ce} replaced as V_r. The C_r can thereby be expressed by

$$C_r = \frac{C_{r0}}{\sqrt{V_r}} \tag{20}$$

where C_{r0} is a constant coefficient. Combing (13) and (20), the capacitance $C_{d2} = C_{\text{oss2}} + C_r$ is obtained as

$$C_{d2} = \frac{C_{d0}}{\sqrt{V_r}}. \tag{21}$$

At reverse recovery transient, V_r increases from 0 V to V_{dc}, which extracts the excess carrier stored in N-base and charges C_{oss2} to generate Q_{rr}, (22) is thereby obtained

$$\int_0^{V_{\text{dc}}} C_{d2}dV_r = Q_{\text{rr}}. \tag{22}$$

With (22) and (21) used, the C_{d0} in (21) is obtained as

$$C_{d0} = \frac{Q_{\text{rr}}}{2\sqrt{V_{\text{dc}}}}. \tag{23}$$

The reverse recovery charge Q_{rr} depends on I_L and has

$$Q_{\text{rr}} \approx K_r(I_L)^a \tag{24}$$

where a and K_r are constant coefficients. Table II shows the extracted a for copackaged p–i–n diodes of various IGBTs. The coefficient a ranges from 0.2 to 0.55 depending on their lifetime control technique.

TABLE II
COEFFICIENT a FOR VARIOUS COPACKAGED SILICON P–I–N DIODES

Part number	Ratings	a
IKW40N65ET7	650 V/40 A	0.34
FGZ75XS65C	650 V/75 A	0.55
FGHL75T65MQDTL4	650 V/75 A	0.39
FGHL50T65MQDTL4	650 V/50 A	0.35
IKW40N120CS6S6	1200 V/40 A	0.20
IKW50N120CS7	1200 V/50 A	0.24
FGH4L40T120LQD	1200 V/40 A	0.22
IKZA40N120CH7	1200 V/40 A	0.39

IV. ANALYTICAL MODEL OF FS IGBT

With the equivalent circuits in Fig. 3 utilized, the analytical models of FS IGBT in phases 1–6 are obtained as follows.

1) *Phase 1:* Fig. 3(a) shows the equivalent circuit in phase 1. Due to $C_{\text{gc}}dV/dt$ induced feedback, V_{ge} is clamped at miller voltage in phases 1 and 2. I_G is thereby expressed as

$$I_g = -C_{\text{gc}}\frac{dV_{\text{ce}}}{dt}. \tag{25}$$

In phase 1, $C_{\text{gc}} = C_{\text{ox}}$. Due to the turn-OFF of V_{ge}, the MOS channel current I_{ch} reduces. I_{ch} can be expressed as

$$I_{\text{ch}} = \frac{bI_L}{1+b} + G_m(V_{\text{ge}} - V_{\text{miller}}) \tag{26}$$

where V_{miller} is the miller voltage at I_L, which is obtained by (7). In (26), the first term is the MOS channel electron current at on-state [15]. The second term is the MOS channel electron current reduction due to the turn-OFF of V_{ge}. In Fig. 3(a), the gate circuit has

$$V_{\text{gg(off)}} = R_g I_g + V_{\text{ge}}. \tag{27}$$

As shown in Fig. 3(a), the load current I_L is expressed as

$$I_L = I_{\text{ch}} + (C_{\text{gc}} + C_{\text{ce}})\frac{dV_{\text{ce}}}{dt}. \tag{28}$$

Combining (25)–(28), (29) can be obtained

$$\frac{dV_{\text{ce}}}{dt} = \frac{\frac{I_L}{1+b} - G_m(V_{\text{gg(off)}} - V_{\text{miller}})}{C_{\text{ox}}(1+G_m R_g) + C_{\text{ce}}}. \tag{29}$$

In (29), C_{ce} can be neglected since $C_{\text{ox}}(1+G_m R_g) \gg C_{\text{ce}}$. In phase 1, $I_c = I_L$ due to the low dV_{ce}/dt.

2) *Phase 2:* In Fig. 3(b), I_L is expressed as

$$\begin{aligned} I_L &= I_{\text{ch}} + (C_{\text{gc}}+C_{\text{ce}}+C_{\text{ext}})\frac{dV_{\text{ce}}}{dt} - C_{\text{oss2}}\frac{dV_r}{dt} \\ &= I_{\text{ch}} + (C_{\text{gc}} + C_{\text{ce}} + C_{\text{ext}} + C_{\text{oss2}})\frac{dV_{\text{ce}}}{dt}. \end{aligned} \tag{30}$$

Since the reduction of V_r is mainly caused by the increase of V_{ce}, $dV_r/dt \approx dV_{\text{ce}}/dt$ is assumed in (30). Combining (25)–(27) and (30), (31) is obtained

$$\frac{dV_{\text{ce}}}{dt} = \frac{\frac{I_L}{1+b} - G_m(V_{\text{gg(off)}} - V_{\text{miller}})}{C_{\text{gc}}(1+G_m R_g)+C_{\text{ce}}+C_{\text{ext}}+C_{\text{oss2}}}. \tag{31}$$

The C_{ce} and C_{oss2} are much smaller than $C_{\text{gc}}(1+G_m R_g)$ and C_{ext} and can be neglected. In phase 2, I_c reduces due to the displacement current on the C_{oss2}, then

$$\frac{dI_c}{dt} = -\frac{C_{\text{oss(avg)}}}{T_a}\frac{dV_{\text{ce}}}{dt}\bigg|_{t_3} \tag{32}$$

where T_a is the duration of phase 2, as shown in Fig. 2(a). $dV_{\text{ce}}/dt|_{t_3}$ is the dV_{ce}/dt at t_3. $C_{\text{oss(avg)}}$ is charge equivalent capacitances of C_{oss}, which is obtained using (13)

$$C_{\text{oss(avg)}} = \frac{\int_0^{V_{\text{dc}}} C_{\text{oss}}}{V_{\text{dc}}} = \frac{2C_{\text{oss0}}}{\sqrt{V_{\text{dc}}}}. \tag{33}$$

3) *Phase 3:* As shown in Fig. 3(c), the gate current is

$$I_g = C_{\text{ge}}\frac{dV_{\text{ge}}}{dt} + C_{\text{gc}}\frac{d(V_{\text{ge}} - V_{\text{ce}})}{dt}. \tag{34}$$

In this phase, I_c abruptly deduces mainly due to the turn-OFF of MOS channel current. I_c can be expressed as

$$I_c = I_3 + G_m(V_{\text{ge}} - V_{\text{miller3}}) \tag{35}$$

where $I_3 = I_c(t = t_3)$. V_{miller3} is the Miller voltage at I_3. As shown in Fig. 3(c), the gate loop has

$$V_{\text{gg(off)}} = R_g I_g + V_{\text{ge}} + L_e\frac{dI_c}{dt}. \tag{36}$$

In the power loop, (37) is obtained

$$V_{\text{dc}} = V_{\text{ce}} + (L_e + L_p)\frac{dI_c}{dt}. \tag{37}$$

Combining (34)–(37), (38) is obtained

$$\alpha\frac{d^2 I_c}{dt^2} + \beta\frac{dI_c}{dt} + I_c = G_m(V_{\text{gg(off)}} - V_{\text{miller1}}) + I_3 \tag{38}$$

where $\alpha = (L_e + L_p)R_g C_{\text{gc}} G_m$ and $\beta = R_g(C_{\text{gc}} + C_{\text{ge}}) + L_e G_m$. The initial condition of phase 3 is

$$I_c(t = t_3) = I_3 \tag{39}$$

$$\frac{dI_c}{dt}\bigg|_{t=t_3} = S_3 \tag{40}$$

where S_3 is the current slope at t_3, which is obtained by (32). The solution of (38) is

$$\begin{aligned} I_c = {} & \frac{S_3 + G_m\tau_2(V_{\text{gg(off)}} - V_{\text{miller1}})}{\tau_1 - \tau_2}e^{\tau_1(t-t_3)} \\ & + \frac{S_3 + G_m\tau_1(V_{\text{gg(off)}} - V_{\text{miller1}})}{\tau_2 - \tau_1}e^{\tau_2(t-t_3)} \\ & + I_3 + G_m(V_{\text{gg(off)}} - V_{\text{miller1}}) \end{aligned} \tag{41}$$

where the coefficients $\tau_1 = (-\beta + \sqrt{\beta^2 - 4\alpha})/2\alpha$, and $\tau_2 = (-\beta - \sqrt{\beta^2 - 4\alpha})/2\alpha$. The dI_c/dt is obtained by

$$\begin{aligned} \frac{dI_c}{dt} = {} & \frac{(S_3 + G_m\tau_2(V_{\text{gg(off)}} - V_{\text{miller1}}))\tau_1}{\tau_1 - \tau_2}e^{\tau_1(t-t_3)} \\ & + \frac{(S_3 + G_m\tau_1(V_{\text{gg(off)}} - V_{\text{miller1}}))\tau_2}{\tau_2 - \tau_1}e^{\tau_2(t-t_3)}. \end{aligned} \tag{42}$$

In this phase, V_{ce} can still be obtained by (31). As shown in Fig. 2(a), V_{ce} increases in this phase until it researches $V_o + V_{\text{dc}}$ at $t_{3a} = t_3 + T_b$. V_o is obtained by

$$V_o = (L_e + L_p)\frac{dI_c}{dt}\bigg|_{t=t_3+T_b}. \tag{43}$$

At $t_3 + T_b$, maximum dI_c/dt is achieved. T_b thereby has

$$\frac{d^2 I_c}{dt^2}\bigg|_{t=T_b} = 0 \tag{44}$$

With (42) and (44) used, T_b is obtained as

$$T_b = \frac{\ln\left(\frac{(S_3 + G_m\tau_1(V_{\text{gg(off)}} - V_{\text{miller1}}))\tau_2^2}{(S_3 + G_m\tau_2(V_{\text{gg(off)}} - V_{\text{miller1}}))\tau_1^2}\right)}{\tau_1 - \tau_2}. \tag{45}$$

4) *Phase 4:* As shown in Fig. 7, in phase 4, electron current I_{n1} and I_{n2} turns OFF, I_c is supported by the hole diffusion

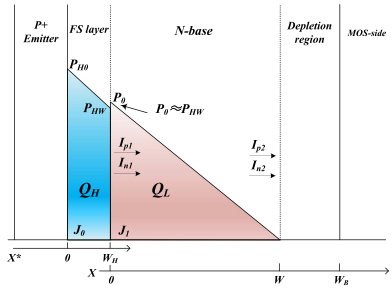


Fig. 7. Excess carrier dynamics in phase 4 at turn-OFF transient.

current I_{p1}[24]. Since N-base and FS layer are under high-level injection conditions [8], [15], (46) is obtained [24]

$$I_c = I_{p1} = 2qAD_P\frac{P_0}{W} = 2qAD_P\frac{P_{H0}-P_{\text{HW}}}{W_H}. \tag{46}$$

As shown in Fig. 7, P_{HW}, P_{H0}, and P_0 are the carrier density at $x^*=0$, $x^*=W_H$, and $x=0$. W_H is the FS layer width. In Fig. 7, the charge Q_L in the N-base and charge Q_H in FS layer can be expressed as

$$Q_L = \frac{qAP_0W}{2} \tag{47}$$

$$Q_H = \frac{qA(P_{H0}+P_{HW})W_H}{2}. \tag{48}$$

With $P_{HW}\approx P_0$ assumed [18], [25], combining (47) and (48), the total charge Q_T is obtained as

$$Q_T = Q_H + Q_L = AqP_0\left(\frac{W}{2}+W_H+\frac{W_H^2}{2W}\right). \tag{49}$$

Substitute (49) and (47) into (46), I_c is expressed as

$$I_c = \frac{4D_PQ_T}{(W+W_H)^2} = \frac{4D_PQ_L}{W^2}. \tag{50}$$

In phase 4, Q_T decays mainly due to the excess carrier recombination. Neglecting the carrier injection into the P+ emitter, (51) is obtained [24]

$$\frac{dQ_T}{dt} = -\frac{Q_L}{\tau_L}-\frac{Q_H}{\tau_H} = -\frac{Q_L}{\tau_L}-\frac{(Q_T-Q_L)}{\tau_H} \tag{51}$$

where τ_H carrier lifetime in FS layer. Combining (47), (49), (50), and (51), the current decay rate can be expressed

$$\frac{dI_c}{dt} = \frac{dI_c}{dQ_T}\frac{dQ_T}{ddt} = -\frac{I_c}{\tau_{\text{eff}}} \tag{52}$$

where the effective carrier lifetime τ_{eff} is expressed as

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{(W+W_H)^2}\left(\frac{W^2}{\tau_L}+\frac{(2W+W_H)W_H}{\tau_H}\right). \tag{53}$$

With initial condition $I_c(t_4)=\varepsilon I_i$, the solution of (52) is

$$I_c = \varepsilon I_i\text{exp}\left(-\frac{t-t_4}{\tau_{\text{eff}}}\right). \tag{54}$$

As shown in Fig. 2(a), after t_{3a}, V_{ce} slowly decay from its peak value to V_{dc}. With initial condition is $V_{\text{ce}}(t_{3a})=V_{\text{dc}}+V_o$, V_{ce} can be obtained using (37) and (54)

$$V_{\text{ce}} = V_{\text{dc}}+V_o\text{exp}\left(-\frac{t-t_{3a}}{\tau_{\text{eff}}}\right). \tag{55}$$

V_o is obtained by (42) and (43). In Fig. 2(a), a short gap may appear between t_{3a} and t_4 due to the excess carrier redistribution. In this model, the gap is neglected and $t_{3a}\approx t_4$.

5) *Phase 5:* In phase 5, I_c is mainly supported by MOS current due to the forward conduction of high-side diode, then

$$I_c = I_{\text{ch}} = G_m(V_{\text{ge}}-V_{\text{th}}). \tag{56}$$

The turn-ON behavior in phase 5 is close to that of turn-OFF in phase 3 and (34), (36) and (36) are valid with $V_{\text{gg(off)}}$ modified as $V_{\text{gg(on)}}$. Combining (34), (36), (37), and (56), the same methods utilized in phase 3 is applied with following initial conditions:

$$I_c(t=t_6) = 0 \tag{57}$$

$$\left.\frac{dI_c}{dt}\right|_{t=t_6} = 0. \tag{58}$$

The solution of I_c is obtained as

$$I_c = (V_{\text{GG}}-V_{\text{th}})\left(\frac{G_m\tau_2}{\tau_1-\tau_2}e^{\tau_1(t-t_6)}+\frac{G_m\tau_1}{\tau_2-\tau_1}e^{\tau_2(t-t_6)}\right) + G_m(V_{\text{GG}}-V_{\text{th}}). \tag{59}$$

The dI_c/dt can be obtained using (59)

$$\frac{dI_c}{dt} = \frac{G_m\tau_1\tau_2(V_{\text{GG}}-V_{\text{th}})}{\tau_1-\tau_2}(e^{\tau_1(t-t_6)}-e^{\tau_2(t-t_6)}). \tag{60}$$

As shown in Fig. 2(b), in phase 4, the V_{ce} reduces in the beginning and plateaued at t_6+T_d. With $d^2I_c/dt^2|_{t=T_d}=0$, T_d can thereby be obtained as

$$T_d = \frac{ln\tau_1-ln\tau_2}{\tau_2-\tau_1}. \tag{61}$$

In this phase, dV_{ce}/dt is expressed as

$$\frac{dV_{\text{ce}}}{dt} = \frac{(L_p+L_S)\left.\frac{dI_c}{dt}\right|_{t=t_6+T_d}}{T_d} \tag{62}$$

where $dI_c/dt|_{t=t_6+T_d}$ is obtained using (60) and (61).

6) *Phase 6:* As shown in Fig. 3(f), I_L is expressed as

$$I_L = I_{\text{ch}}+(C_{\text{gc}}+C_{\text{ce}}+C_q)\frac{dV_{\text{ce}}}{dt}-C_{d2}\frac{dV_r}{dt} = I_{\text{ch}}+(C_{\text{gc}}+C_{\text{ce}}+C_q+C_{d2})\frac{dV_{\text{ce}}}{dt}. \tag{63}$$

In this phase, (25) and (27) are valid with $V_{\text{gg(off)}}$ modified as $V_{\text{gg(on)}}$ in (27). Combining (25), (27) and (6) and (63), the V_{ce} can be obtained as

$$\frac{dV_{\text{ce}}}{dt} = \frac{I_L-G_m(V_{\text{gg(on)}}-V_{\text{th}})}{C_q+C_{\text{ce}}+C_{d2}+C_{\text{gc}}(1+G_mR_g)}. \tag{64}$$

C_{ce} is much smaller than other terms in the denominator and can be neglected. In phase 6, I_c is expressed as [26]

$$I_c = I_L+I_{\text{rr}}\text{exp}\left(-\frac{t-t_7}{T_R}\right) \tag{65}$$

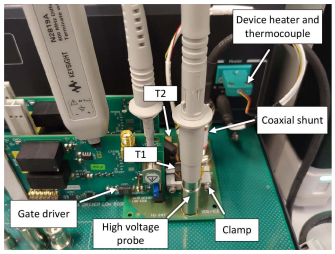


Fig. 8. Double-pulse test fixture.

where T_R is the reverse recovery time constant. The peak reverse recovery current $I_{\rm rr}$ can be obtained by (3).

V. Temperature-Dependent Modeling of FS IGBT

With the double-pulse test fixture presented in Fig. 8 utilized, the impacts of junction temperature T_{j1} of high-side T_1 and junction temperature T_{j2} of low-side T_2 on switching behavior of FS IGBT are investigated. The device under test is attached to a device heater with a thermocouple integrated. The heater can heat T_{j1} and T_{j2} to preset temperatures.

Fig. 9 shows the T_{j1} and T_{j2} dependencies of switching behavior for FS IGBT. As shown in Fig. 9(a), the T_{j1} has a negligible impact on the dI_c/dt during turn-ON at phase 5 and turn-OFF at phase 4. This is because the $V_{\rm th}$ and transconductance of IGBT has negative temperature coefficient. With higher T_{j1}, the reduced $V_{\rm th}$ generates stronger gate driving force, whereas as the reduction of transconductance makes the gate driving force weaker. The two impacts counteract, which generates the negligible T_{j1} dependency of dI_c/dt. The temperature dependency of $V_{\rm th}$ and transconductance can thereby be neglected to simplify the model.

The turn-ON $V_{\rm ce}$ only shows relatively significant temperature dependency when $V_{\rm ce}$ drops to tens of volts. In this phase, the excess carrier builds up in the entire N-Base, which induces temperature dependency [18]. However, since the high-level injection is not achieved until the end of the turn-ON transient, the temperature dependency is weak and can be neglected [18].

As shown in Fig. 9(b), the turn-OFF $dV_{\rm ce}/dt$ greatly reduces with the increase of T_{j1}. The reduction of $dV_{\rm ce}/dt$ is mainly due to the increased $C_{\rm ext}$, which is expressed by (17). In (17), the K_e can be obtained using (2), (14), and (16)

$$K_e = A\left(\frac{q\epsilon_{si}}{2N_b}\right)^{0.5}\left(\frac{b}{qAh_p(1+b)}\right)^{p}. \tag{66}$$

In (66), h_p is temperature-dependent parameters [20]

$$h_p(T_{j1}) = h_{p0}\left(\frac{300}{T_{j1}}\right)^{c}. \tag{67}$$

h_{p0} is h_p at room temperature (27 °C). The typical value of coefficient c is 2.5 [20]. With (17), (66), and (67) used, the temperature-dependent $C_{\rm ext}$ is

$$C_{\rm ext}(T_{j1}) = K_{e0}\frac{I_L^p}{\sqrt{Vce}}\left(\frac{T_{j1}}{300}\right)^{\delta} \tag{68}$$

where K_{e0} and δ are constant coefficients. With $p = 0.2, \delta = 1.2$ is obtained as the default value.

In Fig. 9(b), the tail current of turn-OFF I_c becomes larger with the increase of T_{j1}, which is due to the increased ε, lifetime τ_H and τ_L. The temperature-dependent model of ε is

$$\varepsilon(T_{j1}) = \varepsilon_0\left(\frac{T_{j1}}{300}\right)^{\eta} \tag{69}$$

where ε_0 is the ratio ε at room temperature. η is constant coefficient. The temperature-dependent τ_H and τ_L are [27]

$$\tau_{H(L)}(T_{j1}) = \tau_{H0(L0)}\left(\frac{T_{j1}}{300}\right)^{\zeta_{H(L)}}. \tag{70}$$

τ_{H0} and τ_{L0} are lifetime at room temperature. Coefficients ζ_H and ζ_L range from 0.57 to 1.77 depending on the injection level of excess carrier [28]. The typical value of ζ_H and ζ_L is 1.5 [27], which is used as the default value in this model.

As shown in Fig. 9(c), with the increase of T_{j2}, the reverse recovery charge Qrr and softness factor S increases, which induces the temperature dependency of the snap-back current. The increased $Q_{\rm rr}$ also induces a larger C_{d2}, which causes reduction of turn-ON $dV_{\rm ce}/dt$. The temperature-dependent $Q_{\rm rr}$ is given by (71) [33]

$$Q_{\rm rr}(T_{j2}) = Q_{\rm rr0}\left(\frac{T_{j2}}{300}\right)^{\alpha} \tag{71}$$

where $Q_{\rm rr0}$ is Qrr at room temperature. α is the coefficient. Assuming $\alpha \approx \zeta_H$ [33], $\alpha = 1.2$ is used as default value. The temperature-dependent C_{d2} is obtained using (23) and (71)

$$C_{d2} = \frac{Q_{\rm rr0}}{2\sqrt{V_{\rm dc}}}\left(\frac{T_{j2}}{300}\right)^{\alpha}. \tag{72}$$

The temperature-dependent softness factor S is [18]

$$S(T_{j2}) = S_0\left(\frac{T_{j2}}{300}\right)^{\beta} \tag{73}$$

where β is the temperature-dependent coefficient. S_0 is the softness factor at room temperature.

The turn-OFF behavior of IGBT is determined by low-side IGBT T_1[15]. The T_{j2} of T_2 thereby has no impact on turn-OFF behavior of T_1, as shown in Fig. 9(d).

VI. Application of the FS IGBT Model

A. Parameter Extraction

In this section, the experimental and datasheet-driven parameter extraction methods. The experimental approach can provide accurate parameter extraction but various tests are required. Utilizing the limited information provided in datasheet, the parameters can also be roughly estimated using the datasheet-driven methods. Table III summarizes the experimental and datasheet-driven parameter extraction methods.

1) Experimental Approach: The $V_{\rm th}$ and G_m are extracted from $I_c - V_{\rm ge}$ curves, as shown in Fig. 5(a). The capacitance $C_{\rm ge}$ has $C_{\rm ge} \approx C_{\rm iss}$ when $V_{\rm ce} \gg V_e$. The capacitance $C_{\rm gc0}$, $C_{\rm oss0}$, and V_p are extracted from $V_{\rm ce} - C_{\rm rss}$ and $V_{\rm ce} - C_{\rm oss}$ waveforms. $C_{\rm ox}$ is extracted $dV_{\rm ce}/dt$ at phase 1 using (29). V_f and ε_0 are extracted

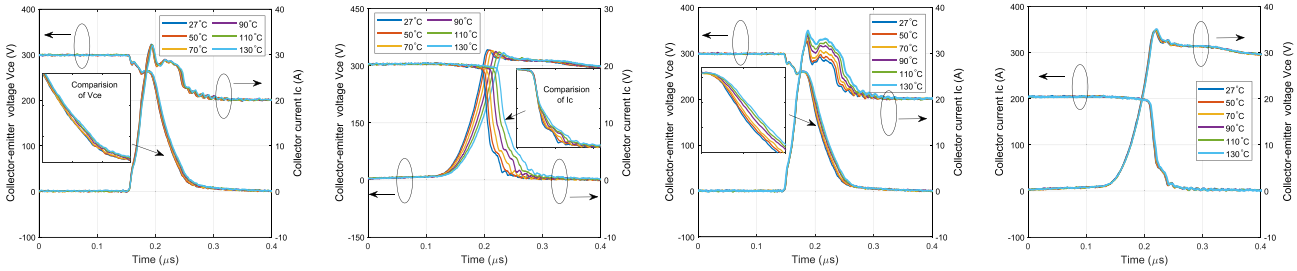


Fig. 9. T_{j1} and T_{j2} dependent switching waveforms of IKW40N65ET7 using various T_{j1} or T_{j2} ranging from 27 °C to 130 °C. (a) Turn-ON and (b) turn-OFF waveforms using various T_{j1} while $T_{j2} = 27°C$. (c) Turn-ON and (d) turn-OFF waveforms using various T_{j2} while $T_{j1} = 27°C$.

TABLE III
PARAMETER EXTRACTION

Parameters	Experimental based parameter extraction	Datasheet-based parameter estimation
V_{th} and G_m	Extract from $I_c - V_{ge}$ curves.	
C_{ge}, $C_{\text{gc}0}$ and $C_{\text{oss}0}$	Extract from $V_{ce} - C_{iss}$, $V_{ce} - C_{rss}$ and $V_{ce} - C_{oss}$ waveforms.	
V_f	From turn-OFF V_{ce} waveforms.	$V_f \approx 10V$ [14].
C_{ox}	From the dV_{ce}/dt at phase 1 using (29).	From the $V_{ce} - C_{\text{iss}}$ waveforms [29].
V_p	Extract from $V_{ce} - C_{rss}$ waveforms.	Use the (12).
T_R, S_0, $Q_{\text{rr}0}$, a, α and β	T_R, S_0 and $Q_{\text{rr}0}$: From reverse recovery waveforms. a: Fit (24) using extracted Q_{rr0}. α and β: fit (71) and (73) using extracted Q_{rr} and S.	Q_{rr0}: From datasheet. S_0 and T_R: Use (74) and (75) based on the extracted Q_{rr0}. a, α and β: Same as the experimental approach.
ε_0 and η	ε_0: From turn-OFF current. η: Fit (69) using the extracted ε.	$\varepsilon_0 = 0.25$ and $\eta = 2$
W_b and N_b	Extract from breakdown voltage V_{br} [29].	
N_H and W_H	Extract from tail current [29].	N_H: $10^{15} - 10^{16} cm^{-3}$. W_H: $4 - 10\mu m$ [1], [30].
τ_{H0}, τ_{L0}, ζ_H and ζ_L	τ_{H0} and τ_{L0}: Extract from tail current [29]. ζ_H and ζ_L: Fit (70) using extracted τ_H, τ_L.	$\tau_{H0} = 1\mu s$, $\tau_{L0} = 0.1\mu s$, $\zeta_H = \zeta_L = 1.5$
K_{e0}, K_q and δ	K_{e0}: Use (17) and (31). K_q: Use (18) and (64). δ: Fit extracted K_e using (68).	K_{e0}: Extract from $t_{d(off)}$ using (76) - (79). $K_q \approx 0.5K_{e0}$ and $\delta = 1.2$.
L_e	Using methods proposed in [29], [31].	Typical value of L_e is presented in [32].
L_p	From turn-OFF dI_c/dt and overshoot voltage [29].	Extracted from PCB design file.

from the turn-OFF V_{ce} waveform, as shown in Fig. 2(a). T_R, $Q_{\text{rr}0}$, and S_0 are obtained from reverse recovery waveforms [4], [13], [26]. τ_{H0} and τ_{L0} are extracted using the decay rate of tail current [29], [34]. The temperature coefficients $\eta, \zeta_H, \zeta_L, \alpha$, and β are obtained using (69), (70), (71), and (73) to fit the related parameters obtained at various temperature. a can be extracted by fitting (24) using the Q_{rr} extracted at various load current. The K_e is extracted by turn-OFF dV_{ce}/dt using (17) and (31). The K_q is extracted by turn-ON dV_{ce}/dt using (18) and (64). The stray inductance L_e and L_p are extracted using methods in [29] and [31]. The W_b, N_b, W_H, and N_H are extracted using the method in [29].

2) Datasheet-Driven Method: With datasheet used, the parameters $V_{\text{th}}, G_m, C_{\text{ge}}, C_{\text{gc}0}, C_{\text{oss}0}, Q_{\text{rr}0}, \alpha$, and a can be directly obtained using experimental approach since the related data are provided in the datasheet. The datasheet-driven parameter extraction approach for the other parameters are discussed as follows.

The V_p is calculated by (12) using E_c, V_{br} and N_b. $E_c = 2.5 \times 10^5 V \cdot \text{cm}^{-1}$ and $N_b = 1 \times 10^{14} \text{cm}^{-1}$ can be used as default value. The V_{br} is the rated breakdown voltage plus 100 V of typical voltage margin [29]. $V_f \approx 10\,V$[14]. C_{ox} can be roughly estimated by $V_{\text{ce}} - C_{\text{rss}}$ waveforms [29]. The softness factor S is extracted by

$$S = \frac{t_{\text{rr}0}^2}{2Q_{\text{rr}}} \frac{dI_F}{dt} - 1 \tag{74}$$

where t_{rr} reverse recovery time. dI_F/dt is the forward current slop to obtain the Q_{rr}. The S_0 and β can thereby be extracted by using the temperature-dependent Q_{rr} provided in the datasheet. With (65) utilized, T_R is obtained as

$$T_R = -\frac{t_f}{\log(0.1)} \tag{75}$$

where $t_f \approx t_{\text{rr}} S/(1+S)$. K_e is extracted by turn-OFF delay time $T_{d(\text{off})}$. As shown in Fig. 2(a), $T_{d(\text{off})} = T_{\text{de}} + T_a$, T_{de} is turn-OFF delay time and T_a is voltage rise time. With the increase of I_L, T_a reduces while T_{de} is constant. When I_L is very large, $T_{de} \gg T_a$ and T_{de} equals to minimum $T_{d(\text{off})}$ ($T_{d(\text{off})(\text{min})}$) in $I_L - T_{d(\text{off})}$ curve in datasheet. T_a at I_L is

$$T_a(I_L) \approx T_{d(\text{off})}(I_L) - T_{d(\text{off})(\text{min})} \tag{76}$$

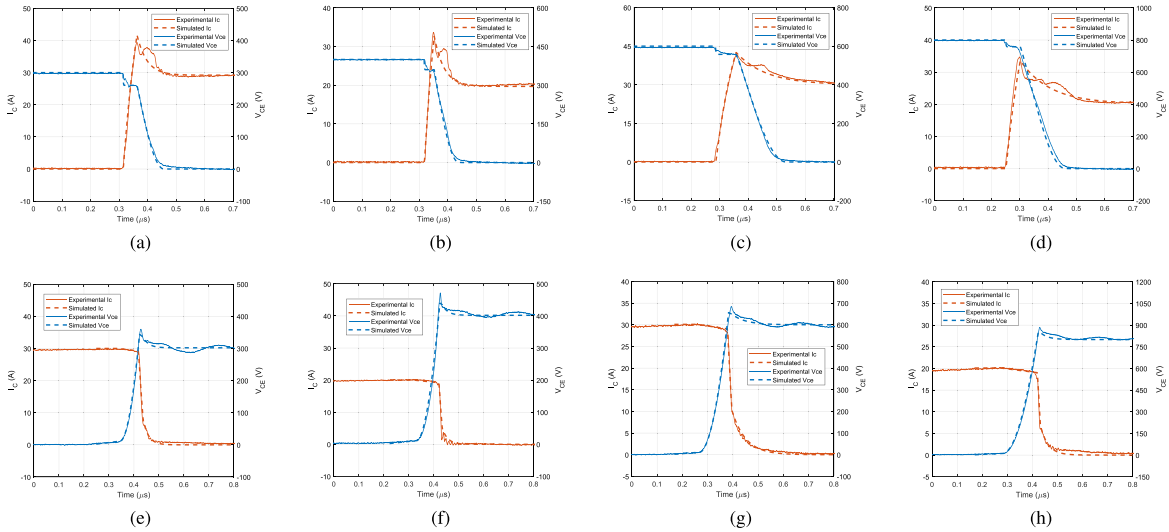


Fig. 10. Experimental and simulated waveforms at room temperature. (a) 300 V/30 A turn-ON of IKW40N65ET7. (b) 400 V/20 A turn-ON of IKW40N65ET7. (c) 600 V/30 A turn-ON of IKW40N120CS6S. (d) 800 V/20 A turn-ON of IKW40N120CS6S6. (e) 300 V/30 A turn-OFF of IKW40N65ET7. (f) 400 V/20 A turn-OFF of IKW40N65ET7. (g) 600 V/30 A turn-OFF of IKW40N120CS6S6. (h) 800 V/20 A turn-OFF of IKW40N120CS6S6.

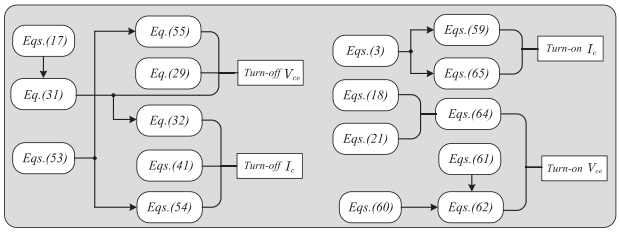


Fig. 11. Flowchart for calculate the V_{ce} and I_C at turn-ON and turn-OFF.

where $T_{d(\text{off})}(I_L)$ is $T_{d(\text{off})}$ at I_L. With (31) utilized, T_a is

$$T_a = \frac{V_{\text{dc}}(C_{\text{gc(avg)}}(1+G_m R_g)+C_{\text{ext(avg)}})}{I_L - G_m(V_{\text{gg(off)}} - V_{\text{th}})} \tag{77}$$

where charge equivalent capacitance $C_{\text{ext(avg)}}$ for C_{ext} is

$$C_{\text{ext(avg)}} = \frac{\int_0^{V_{\text{dc}}} C_{\text{ext}}}{V_{\text{dc}}} = \frac{2K_e I_L^p}{\sqrt{V_{\text{dc}}}}. \tag{78}$$

The charge equivalent capacitance $C_{\text{gc(avg)}}$ for C_{gc} is

$$C_{\text{gc(avg)}} = \frac{\int_0^{V_{\text{dc}}} C_{\text{gc}}}{V_{\text{dc}}} \approx \frac{2C_{\text{gc0}}}{\sqrt{V_{\text{dc}}}}. \tag{79}$$

With (76)–(79) utilized, K_{e0} is roughly estimated. $K_q \approx 0.5K_{e0}$. L_p can be extracted using a PCB design file. The typical values of L_e are provided in [32].

Since the related experimental data are not provided in the datasheet, the following parameters can not be extracted based on the datasheet. The empirical values are thereby used. ε_0 is around 0.1–0.5 [4], [5], [8], [35]. $\delta \approx 1.2$, $\varepsilon_0 = 0.25$, and $\eta = 2$. $\tau_{H0} = 1\mu s$ and $\tau_{L0} = 0.1\mu s$ are typical values of lifetime according [8], [29], [35]. ζ_H and ζ_L are 1.5 [27].

When the parameters are extracted, the parameter optimization method proposed in [29] can be used to fine-tune the extracted parameters to obtain an optimized parameter set. However, the inclusion of parameter optimization can make the parameter extraction complex and time-consuming.

B. Model Implementation

With the parameters utilized, the proposed model can be implemented following the routine of calculation presented in Fig. 11. First, use (53) and (14) to obtain τ_{eff} and C_{ext}. Then, use (29), (31), and (55) to calculate turn-OFF V_{ce}, use (32), (41), and (54) to calculate turn-OFF I_c. Second, use (3) to calculate I_{rr}, then the turn-ON I_c is obtained by (59) and (65). In the end, use (18) and (21) to obtain C_q and C_{d2}. Use (61) to obtain T_d. The turn-ON V_{ce} is obtained by (60), (62), and (64). The temperature-dependent parameters can be calculatedly using (68)–(73).

VII. Experimental Validation

Figs. 8 and 1(b) show the test fixture and its equivalent circuit. In the test, $R_g = 10\,\Omega$, V_{gg} switches at 15 V/0 while $V_{\text{gg(off)}} = 0\,V$. The V_{ce} and I_c are measured by a high voltage probe 10076C and a current shunt SSDN-414-01, respectively. The experimental validation is performed on a 1200 V/40 A FS IGBT IKW40N120CS6S6 and a 650V/40A FS IGBT IKW40N65ET7. Their parameters are extracted using the experimental approach provided in Section VI.

A. Comparison on Switching Waveforms

1) Turn-On Waveforms at Room Temperature: Fig. 10(a)–(d) compares the experimental and simulated turn-ON waveforms of IKW40N65ET7 and IKW40N120CS6S6 at room temperature (27 °C). The simulated turn-ON current waveforms agree with experimental data except for the phase when I_c snaps back to its peak current to load current. In the test waveforms, the snaps-back current oscillates due to redistribution of residual excess charge in the N-base of diode D_2, which causes oscillation [18].

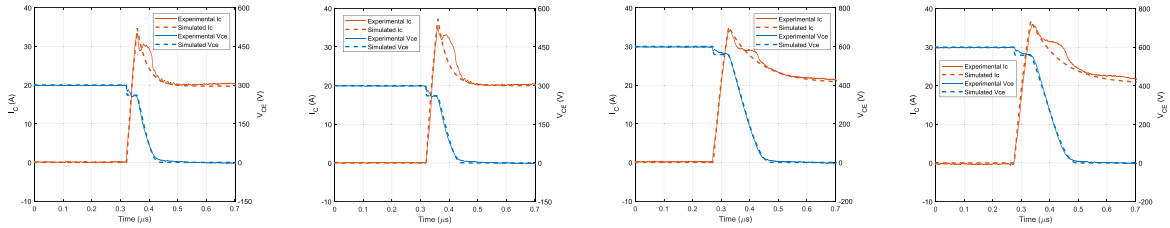


Fig. 12. Experimental and simulated turn-ON waveforms of IKW40N65ET7 (300 V/20 A) and IKW40N120CS6S6 (600 V/20 A) of (a) IKW40N65ET7 at $T_{j2} = 70\,^{\circ}\text{C}$, (b) IKW40N65ET7 at $T_{j2} = 130\,^{\circ}\text{C}$, (c) IKW40N120CS6S6 at $T_{j2} = 70\,^{\circ}\text{C}$ and (d) IKW40N120CS6S6 at $T_{j2} = 130\,^{\circ}\text{C}$, while $T_{j1} = 27\,^{\circ}\text{C}$.

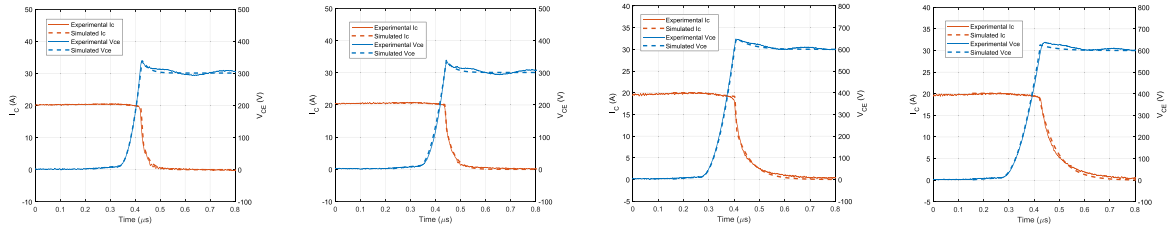


Fig. 13. Experimental and simulated turn-OFF waveforms of IKW40N65ET7 (300 V/20 A) and IKW40N120CS6S6 (600 V/20 A) of (a) IKW40N65ET7 at $T_{j1} = 70\,^{\circ}\text{C}$. (b) IKW40N65ET7 at $T_{j1} = 130\,^{\circ}\text{C}$. (c) IKW40N120CS6S6 at $T_{j1} = 70\,^{\circ}\text{C}$ and (d) IKW40N120CS6S6 at $T_{j1} = 130\,^{\circ}\text{C}$, while $T_{j2} = 27\,^{\circ}\text{C}$.

Since the excess charge redistribution is not included in the proposed model, the oscillation is not captured.

In Fig. 10(a)–(d), simulated and experimental turn-ON V_{ce} waveforms matches except for the phase when V_{ce} drops to below around 10 V. In this phase, conductive modulation builds up, which causes the slow reduction of experimental V_{ce}. Since the conductive modulation process is not included, the simulated V_{ce} quickly drops to zero.

2) Turn-Off Waveforms at Room Temperature: Fig. 10(e)–(h) compares the experimental and simulated turn-OFF waveforms of IKW40N65ET7 and IKW40N120CS6S6 at room temperature. The simulated waveforms agree with experimental data.

3) Turn-On Waveforms Using Various T_{j2}: Fig. 12 shows the experimental and simulated turn-ON waveforms of IKW40N65ET7 and IKW40N120CS6S6 using various T_{j2}. Thanks to the temperature-dependent model of reverse recovery charge Qrr and softness factor S, the T_{j2} dependency of I_c is captured by the proposed model. Due to the temperature-dependent model of C_{d2}, the T_{j2} dependency of V_{ce} is also captured by the simulated turn-ON waveforms.

4) Turn-Off Waveforms Using Various T_{j1}: Fig. 13 shows 300 V/20 A experimental and simulated turn-OFF waveforms of IKW40N65ET7 and 600 V/20 A turn-OFF waveforms of IKW40N120CS6S6 using various T_{j1}. With temperature-dependent model of capacitance C_{ext} included, the T_{j1} dependency turn-OFF V_{ce} is captured. Due to the temperature-dependent models of τ_H, τ_L, and ε, the T_{j1} dependent turn-OFF I_c is accurately predicted.

B. Comparison on Switching Losses

The turn-ON loss E_{on} and turn-OFF loss E_{off} are calculated by the time integration on the products of V_{ce} and I_c. The error E of simulated switching losses is calculated by

$$\text{E} = \frac{|\text{Simulated } E_{\text{Loss}} - \text{Experimental } E_{\text{Loss}}|}{\text{Experimental } E_{\text{Loss}}}. \tag{80}$$

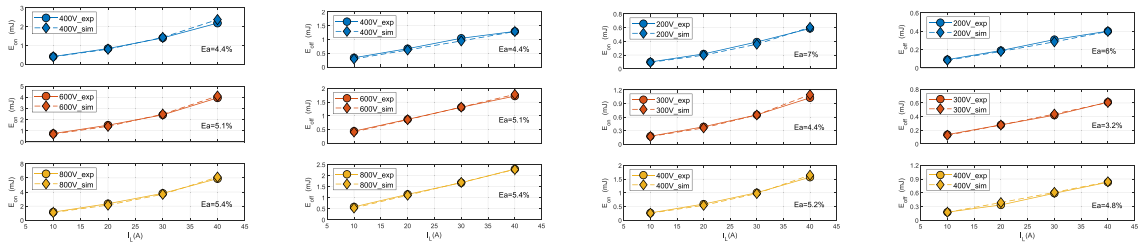
Fig. 14(a)–(d) compares the simulated and simulated and experimental E_{on} and E_{off} at room temperature for IKW40N120CS6 and IKW40N65ET7 using various V_{dc} and I_L. Under each V_{dc} condition, the average error $Ea = \overline{E}$ is calculated. For IKW40N120CS6, the $\overline{E}$ is within 5.4% for simulated E_{on} and E_{off}. For IKW40N65ET7, $\overline{E}$ is within 7% and 6% for simulated E_{on} and E_{off}.

Fig. 15 compares the simulated E_{on} and E_{off} for IKW40N65ET7 and IKW40N120CS6 with various T_{j2} and T_{j1} utilized. For IKW40N65ET7, the average error of the temperature-dependent E_{on} and E_{off} are 2.3% and 2%. For IKW40N120CS6S6, the average error of the temperature-dependent E_{on} and E_{off} are 1.3% and 3.3%.

C. Comparison on Proposed and Established Spice Models

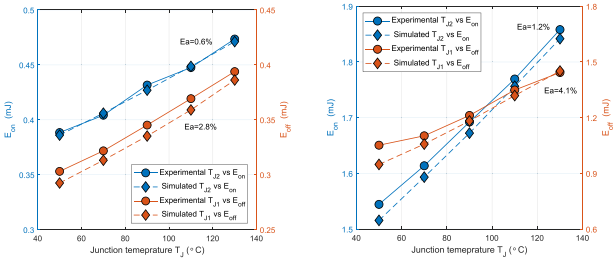
The proposed model is compared with the established Spice model provided by the manufacturer. With LTspice spice utilized, the simulation is performed using the same circuit parameters as that used in the test. Fig. 16 compares the turn-ON and turn-OFF waveforms obtained by proposed and Spice models for IKW40N120CS6S6 at 600 V/20 A. At the turn-OFF transient, the Spice model can make reasonable predictions on dI_c/dt of initial current falling phase, but the tail current and turn-OFF V_{ce} have big errors. At turn-ON transient, the Spice simulated current rising phase of I_c matches with the test data. But the overshoot of I_c and turn-ON V_{ce} is not accurate.

The errors of the Spice model on dV_{ce}/dt are mainly due to the lack of consideration of excess carrier dynamics in the N-base.



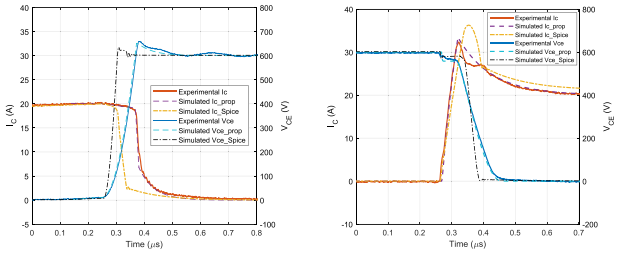
(a) (b) (c) (d)

Fig. 14. Experimental and calculated switching losses of IKW40N120CS6 ($V_{\rm dc}$ is 400–800 V, I_L is 10-30A) and IKW40N65ET7 ($V_{\rm dc}$ is 200–400 V, I_L is 10-40 A) at room temperature. (a) $E_{\rm on}$ of IKW40N120CS6. (b) $E_{\rm off}$ of IKW40N120CS6. (c) $E_{\rm on}$ of IKW40N65ET7. (d) $E_{\rm off}$ of IKW40N65ET7.



(a) (b)

Fig. 15. Experimental and calculated T_{j1} dependent $E_{\rm off}$ and T_{j2} dependent $E_{\rm on}$. (a) IKW40N65ET7 and (b) IKW40N120CS6S6.



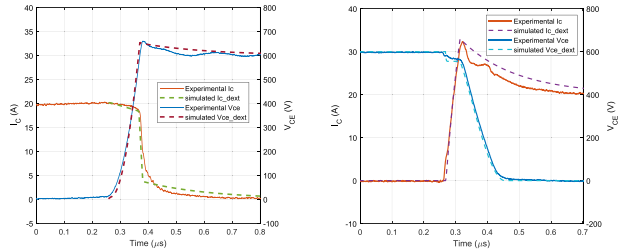
(a) (b)

Fig. 16. Comparison of waveforms obtained by proposed and Spice models for IKW40N120CS6S6 with $R_g = 10\,\Omega$ at 600 V/20A at room temperature. (a) Turn-OFF waveforms. (b) Turn-ON waveforms.

The lack of consideration on residual charge recombination of IGBT at turn-OFF and excess charge extraction of p–i–n diode at turn-ON also contribute to the errors.

D. Experimental and Datasheet-Driven Parameter Estimation

Fig. 17 shows the simulated switching waveforms using datasheet-based parameter extraction methods. In datasheet-based approach, some important parameters, like the excess carrier lifetime τ_H, τ_L, and ratio ε, cannot be extracted and typical values are used. This induced significant errors in tail current. Moreover, the simplifications in the approach also introduce some errors in the extracted parameters. Due to errors of extracted G_m and $Q_{\rm rr}$, the turn-OFF and turn-ON current show minor discrepancies compared to the experimental data. Despite the discrepancies, datasheet-driven parameter extraction is still a decent option since it still more accurate than the Spice simulation, as shown in Fig. 16.



(a) (b)

Fig. 17. Experimental and simulated 600 V/20 A switching waveforms for IKW40N120CS6S6 at room temperature using datasheet-driven parameter estimation. (a) Turn-OFF waveforms. (b) Turn-ON waveforms.

VIII. Conclusion

This article present a novel transient model for FS IGBTs. To describe the excess carrier dynamics, the models of charge equivalent capacitances $C_{\rm ext}$, C_q are proposed to describe the excess carrier extraction and build up processes at switching transient of FS IGBT. The capacitance C_d is used to represent the excess carrier extraction at reverse recovery transient of p–i–n diode. With the capacitances utilized, complete expressions of $V_{\rm ce}$ and I_c are derived, which includes the pivotal device physics, like excess carrier dynamics, nonlinear stray capacitances induced by FS layer, $L_e dI_c/dt$ and $C_{\rm gc} dV/dt$ induced feedback. To model the temperature dependency of FS IGBT, the key parameters depends on temperature T_{j1} for low-side IGBT and temperature T_{j2} for high-side p–i–n diode are identified. The analytical models of temperature-dependent parameters are included.

In the end, the comparison of experimental and simulated waveforms validates the proposed model can accurately predict the switching behaviors and its temperature dependency. Compared with established Spice models, the proposed model can make much more accurate predictions on switching behavior.

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