An Improved Synchronous Rectification *LLC* Resonant Converter for Hold-Up Time Operation

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***Abstract*—An innovative improved synchronous rectification *LLC* (ISR *LLC*) resonant converter is proposed for applications that demand extended hold-up time, such as data center power supplies. The design greatly simplifies the hold up operation circuit by integrating only one switch into the conventional synchronous rectification *LLC* converter. Utilizing a fixed-frequency phase shift control strategy, the converter achieves an enhanced voltage gain, which in turn, substantially prolongs the hold-up time. Compared with the traditional pulse frequency modulation *LLC* resonant converter, a larger magnetizing inductance can be employed, effectively diminishing the system's conduction losses and elevating conversion efficiency. The topology, operation principle, voltage gain characteristics, and design considerations of the converter will be elaborately introduced. The prototype converter with 200–400 V input and 48 V/500 W output is presented to validate its effectiveness.**

***Index Terms*—Fixed frequency control, hold-up time, improved synchronous rectification, *LLC* resonant converter.**

I. Introduction

THE LLC converter has been widely applied in recent years due to excellent performance. In data center applications, when the ac input voltage drops, the dc-bus voltage will continue to decrease, and voltage output needs to remain stable for tens of milliseconds until uninterruptible power supplies are connected, allowing servers to continue operating normally [1], [2], [3]. This requirement is known as the hold-up time requirement. As illustrated in Fig. 1, to maintain the output voltage unchanged after the input voltage drops during the hold-up time, it is necessary to increase the gain of the *LLC* converter. Due to the gain characteristics of the traditional *LLC* resonant converter's frequency modulation control, it is difficult to achieve a wide input range within a narrow switching frequency range. Therefore, improvements on the traditional *LLC* converter are needed to meet the requirements of hold-up time.

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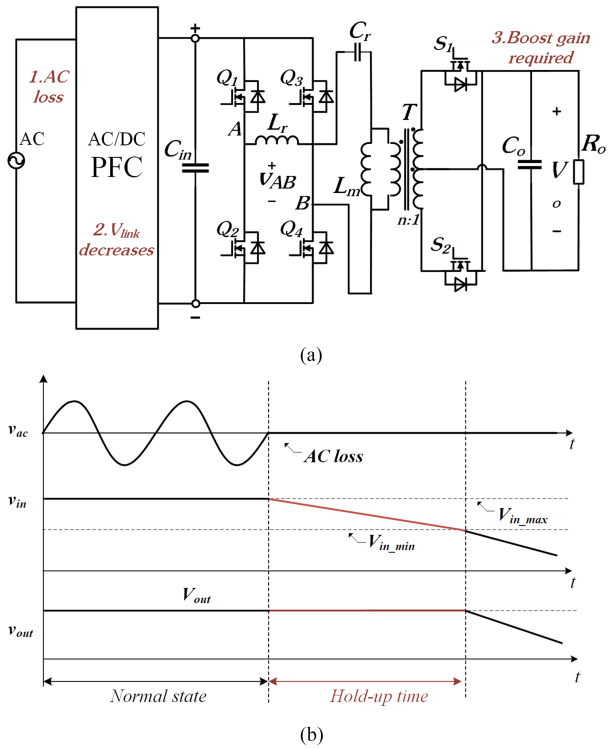


Fig. 1. (a) AC-DC power supply with *LLC* converter and hold-up time requirement. (b) Hold-up time operation for DC–DC converter after AC loss.

The reported improvement schemes can be divided into four categories: power factor corrector (PFC) output control, resonant tank, secondary side networks, and primary side networks.

The first approach involves improving PFC control strategies. The dc gain is adjusted by regulating the output voltage of the PFC [4], [5], [6]. Although this method does not require additional circuitry, the PFC circuit has limited capability to regulate the output voltage, which consequently restricts its ability to achieve higher output gain.

The second approach is to upgrade the resonant tank. This includes making the resonant inductance and capacitance variable by adding transformers or switches to the resonant tank [7], [8], [9], [10]. Adjusting the resonant inductance, capacitance, or the equivalent magnetizing inductance can effectively enhance the gain. However, these approaches inherently require the addition of control devices for variable inductors and capacitors, leading to increased costs and energy losses.

The third approach is to optimize the primary side network. These methods structurally add switches to the primary side or include a boost stage. By controlling the duty cycle and phase shift of the switches, the adjustability of voltage gain is enhanced [11], [12], [13], [14]. Such methods often require an excessive number of switching devices, making the control relatively complex. In some cases, asymmetric control is necessary, which can result in the generation of bias current.

The fourth approach is to refine the secondary side rectifier. These methods mainly involve adding windings to the transformer on the secondary side, the structure of the chopper rectifier, and secondary short-circuiting. By controlling the switch duty cycle or phase shift angle, a higher voltage gain is achieved. Some of these methods face challenges in transformer optimization and complex parameter design during mode switching [15], [16], [17], [18], [19], [20], [21]. The short-circuit of synchronous rectifier (SR) switch is considered as a competitive scheme to increase the gain. However, this kind of scheme can only be applied to the full bridge structure and voltage doubling rectification scheme, and cannot be applied to center-tapped rectifiers because this will cause a huge current while the output capacitor discharges.

Overall, each of these schemes has its advantages and disadvantages. However, improvements are needed to reduce the number of additional circuit components and transformer complexity, eliminate bias magnetism, and reduce control and parameter design difficulty.

This article proposes a novel improved synchronous rectification *LLC* (ISR *LLC*) topology for hold-up time operation with the following advantages.

1) *Simplified Topology:* Compared with other hold up operation schemes that add more than two switches or transformers, only one mode switch is added to the synchronous rectification (SR) LLC topology. The topology is greatly simplified and can be applied to the center-tapped rectifier.
2) *Enhanced Voltage Gain:* By employing fixed-frequency phase shift modulation, which significantly increases the system voltage gain, thereby it effectively prolongs the hold-up time and reduces input capacitance.
3) *Optimized Efficiency:* A larger magnetizing inductor can be designed to minimize conduction losses and enhance overall efficiency.
4) *Symmetrical Control:* The implementation of symmetrical control mitigates bias current, thereby optimizing the magnetic core's utilization rate.

The rest of this article is organized as follows. In Section II, the topology, operating principle, modulation is discussed. In Section III, voltage gain analysis is discussed. In Section IV, simulation verification is discussed. Experimental results are discussed in Section V. Section VI presents the comparison with prior works. Finally, Section VII concludes this article.

II. Topology and Modulation

As shown in Fig. 2, the primary side of the proposed ISR *LLC* converter is composed of a full bridge inverter, resonant cavity

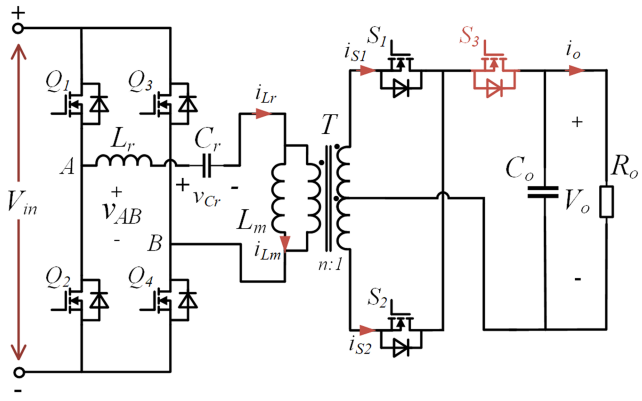


Fig. 2. Proposed ISR *LLC* resonant DC–DC converter.

L_r, C_r, L_m. Full-wave SR and mode switch S_3 are utilized by the second side. This novel ISR *LLC* resonant converter distinguishes itself from conventional *LLC* converters by the unique switch S_3.

The S_3 switch is ON in the normal state. In the hold-up state, S_3 is turned OFF, and the body diode of S_3 can prevent the reverse flow of current from the output capacitor when both S_1 and S_2 are conductive simultaneously.

Under normal operating conditions, the mode switch S_3 remains ON, allowing the converter to operate as a conventional SR *LLC* converter. When the input ac source loses, the mode switch S_3 is turned OFF. If S_1 and S_2 are turned ON at the same time, the secondary side is short-circuited to charge L_r. Conversely, when S_1 and S_2 are deactivated, L_r discharges its stored energy, functioning similarly to a boost converter.

A. Operation in the Normal State

In the normal state, where the input voltage is within the range of 400 V $\pm$ 10%, the system operates with pulse frequency modulation (PFM) for voltage regulation. During this state, S_3 remains ON, while S_1 and S_2 function as synchronous rectification switches. The key waveforms are illustrated in Fig. 3. As the system operates near the resonant frequency, fundamental component analysis can be employed. The voltage conversion ratio $M = nV_O/V_{\text{in}}$ can be calculated as

$$M = \frac{1}{\sqrt{[(1-1/(f_s^*)^2)Qf_s^*]^2 + [(1-1/(f_s^*)^2)\frac{1}{m}+1]^2}} \quad (1)$$

where n is the primary-to-secondary turns ratio of the transformer, f_r is the resonant frequency of resonant inductor L_r and resonant capacitor C_r, f_s is the operatation frequency, Q is quality factor, m is inductor ratio of magnitizing inductor L_m and resonant inductor L_r, and Z_r represent the resonant resistance of L_r, C_r. The parameter can be calculated as $f_s^* = f_s/f_r$, $Q = \frac{\pi^2 Z_r}{8n^2 R_o}$, $m = \frac{L_m}{L_r}$, $Z_r = \sqrt{L_r/C_r}$.

B. Operation During the Hold-Up Time

Figs. 4–6 depict the critical waveforms, current paths, and equivalent resonant circuits of the proposed converter during the hold-up time. Different from traditional frequency control,

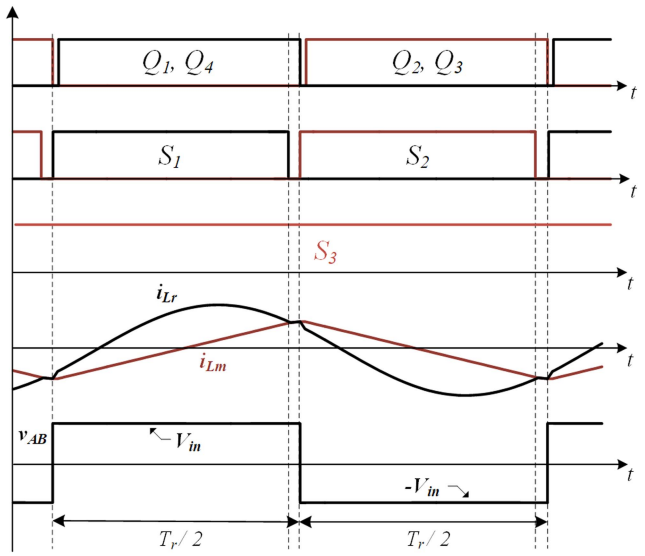


Fig. 3. Key waveforms of normal state.

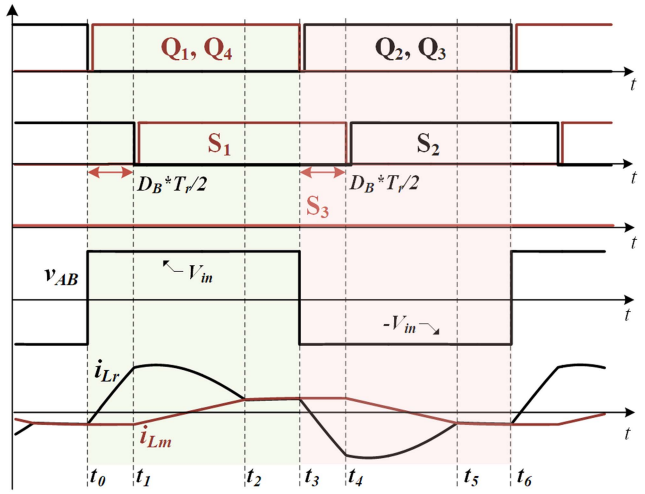


Fig. 4. Key waveforms of hold-up operation.

the ISR *LLC* converter controls the voltage gain with the shift angle D_B between S_2 and Q_1, Q_4. The modulation of $Q_1 - Q_4$ is fixed at the resonant frequency, and S_3 is OFF. The converter operates at the resonant frequency $f_s = f_r$. The shift angle of S_2 is $D_B \cdot T_r/2$ within one resonant cycle. The control method of S_1 is similar to that of S_2.

The modulation of the proposed ISR *LLC* resonant converter can be divided into two half-cycles: $t_0 - t_3$ and $t_3 - t_6$. Since two half-cycles are symmetric, only the interval from t_0 to t_3 is introduced.

Resonant frequency f_r and resonant impedance Z_r and Z_m of the resonant tank are defined as follows: $\omega_r = 1/\sqrt{L_r \cdot C_r}$, $f_r = \omega_r/2\pi$, $Z_r = \sqrt{L_r/C_r}$, $\omega_m = 1/\sqrt{(L_r + L_m) \cdot C_r}$, $f_m = \omega_m/2\pi$, $Z_m = \sqrt{(L_r + L_m)/C_r}$.

Stage 1 $[t_0 - t_1]$: Before t_0, S_2, Q_1, Q_4 are OFF, while S_1 is ON. Resonant cavity is composed of $L_r + L_m$ and C_r. At time t_0, Q_1, Q_4 are ON, resulting in the voltage v_{AB} changing to V_{in}. Due to S_1 being turned ON and diode of S_2 being forced on, the

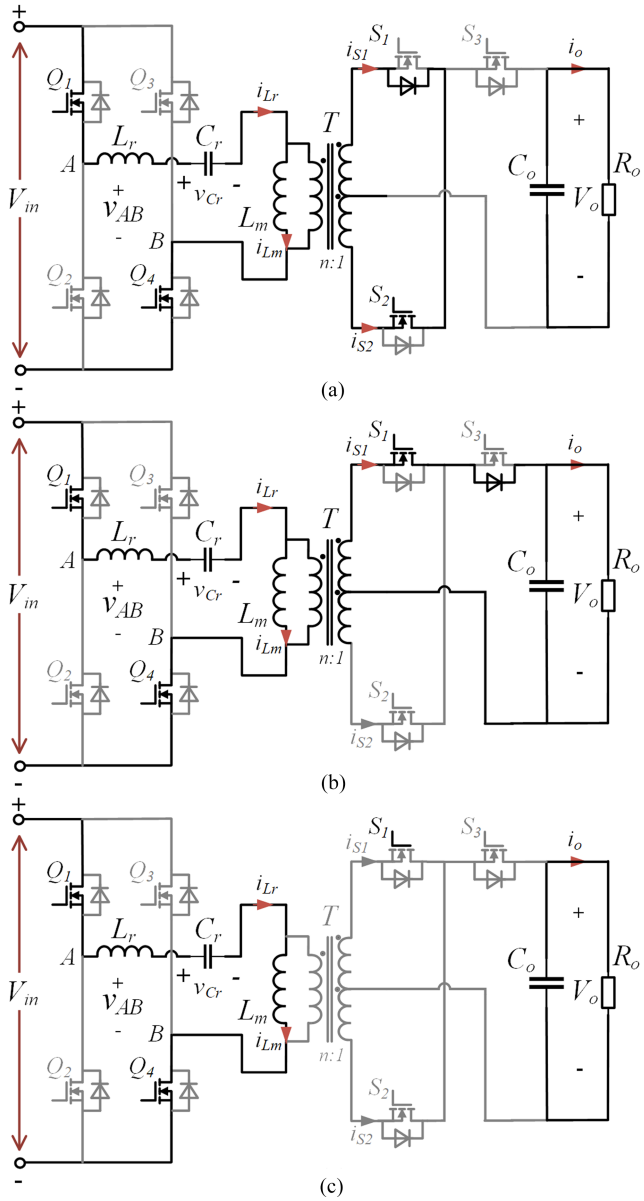


Fig. 5. Current paths of the proposed converter during the hold-up period are as follows: (a) $t_0 - t_1$, (b) $t_1 - t_2$, and (c) $t_2 - t_3$.

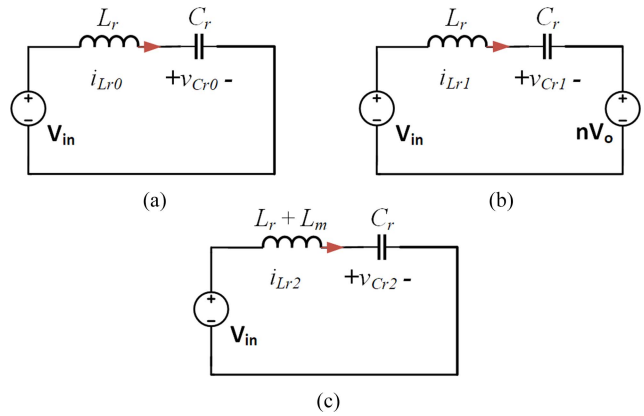


Fig. 6. Equivalent resonant circuits of the proposed converter during the hold-up period are as follows: (a) $t_0 - t_1$, (b) $t_1 - t_2$, and (c) $t_2 - t_3$.

transformer's secondary winding is short-circuited, which leads to the magnetizing inductance L_M voltage being zero. The L_r and C_r begin to resonate. The capacitor voltage and V_{in} charge the L_r, causing the current i_{Lr} to increase, while the current i_{Lm} remains unchanged. In this stage, the circuit's state equation can be expressed as follows:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + V_{\text{in}} \\ i_{Lm}(t) = i_{Lm}(t_0) \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{2}$$

Stage 2 $[t_1 - t_2]$: At time t_1, the resonant cavity input voltage V_{AB} is maintained at V_{in}. Switch S_2 is ON and switch S_1 is OFF. Due to the voltage across the magnetizing inductance L_m being clamped by the positive output voltage nV_o, the magnetizing inductor current i_{Lm} increases linearly. The L_r and C_r resonate under the new voltage $V_{in} - v_{C_r} - nV_o$, with the current i_{Lr} decreasing after reaching its peak. The difference between i_{Lr} and i_{Lm} is the current that flows into the secondary side. This stage ends when $i_{Lr} = i_{Lm}$. In this stage, the circuit's state equation can be expressed as follows:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + V_{in} - nV_o \\ L_m \frac{di_{Lm}(t)}{dt} = nV_o \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{3}$$

Stage 3 $[t_2 - t_3]$: At time t_2, $i_{Lr} = i_{Lm}$. Although S_2 is ON, the voltage across the magnetizing inductance L_m is not clamped by the positive output voltage. The resonant capacitor C_r is resonating with both L_r and L_m. In this stage, the circuit's state equation can be expressed as follows:

$$\begin{cases} (L_m + L_r) \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + V_{\text{in}} \\ i_{Lm}(t) = i_{Lr}(t) \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{4}$$

III. Characteristics and Design Considerations

A. DC Voltage Gain Analysis

The traditional method for calculating voltage gain is the fundamental harmonic approximation [22]. It can be utilized by the proposed ISR *LLC* resonant converter while the converter operates in the normal state because the working waveform of i_{Lr} is fundamentally close to a sine wave.

However, when the converter operates in the hold-up state, the time-domain analysis method [23] should be selected to achieve more precise gain characteristics.

By solving the differential equations for Stage 1 to Stage 3, (5)–(7) can be obtained (5) and (6) shown at the bottom of this page

$$i_{Lm}(t) = \begin{cases} i_{Lr}(t_0), & t_0 \le t < t_1 \\ i_{Lr}(t_1) + (nV_o/L_m)t, & t_1 \le t < t_2 \\ i_{Lr}(t), & t_2 \le t < t_3. \end{cases} \tag{7}$$

Due to the waveforms of $v_{Cr}(t)$ and $i_{Lr}(t)$ are half-wave symmetric signals, the following relationships as shown in (8) can be established. At time t_2, both L_r and L_m are involved in resonance. These relationships can be expressed as

$$\begin{cases} i_{Lr}(t_0) = -i_{Lr}(t_3) \\ v_{Cr}(t_0) = -v_{Cr}(t_3) \\ i_{Lr}(t_2) = i_{Lm}(t_2). \end{cases} \tag{8}$$

In addition, the average value of the difference between i_{Lr} and i_{Lm} over half a cycle is the output average current. Consequently, the average output current can be calculated as

$$\frac{1}{T_r/2} \int_{t_1}^{T_r/2} (i_{L_r}(t) - i_{L_m}(t))\, dt = I_o/n = \frac{V_o}{nR_o} = \frac{8nV_oQ}{Z_r\pi^2} \tag{9}$$

$$Q = \frac{\pi^2 Z_r}{8n^2 R_o}. \tag{10}$$

When D_B and V_i take different values, by numerically solving the above (5)–(9), the values of four parameters $(i_{Lr}(t_0), v_{Cr}(t_0), t_2, V_o)$ can be obtained. Therefore, the gain ratio $M = nV_o/V_i$ of the dc converter versus boost duty cycle D_B inputs can be derived under different the quality factor Q and the inductor ratio $m = i_{Lm}/i_{Lr}$, which is illustrated in Fig. 7.

As illustrated in Fig. 7(a), the converter's gain M increases with an increase in D_B. At $D_B = 0$, the system operates at $f_s = f_r$, with a system gain of $M = 1$. When $D_B = 0.5$, the system gain reaches its maximum value of 2.75. With the system's $Q = 0.4$, as the value of m varies from 5 to 10, the change of M for the same D_B is minimal, with the maximum deviation in M being approximately 0.04. It means that the inductor ratio m exerts little impact on the gain characteristics. This behavior is markedly different from that of the conventional *LLC* converter with PFM control, where m is a significant factor in the voltage gain M. To reduce the magnetizing current i_{Lm} and loop currents i_{Lr}, a larger value of m can be adopted without affecting the soft-switching of MOSFETs.

As depicted in Fig. 7(b), the converter's gain curves vary under different load conditions. At a system load of 10 %, corresponding to $Q = 0.04$, the maximum system gain can reach 5.6. However, at full system load with $Q = 0.4$, the maximum system gain is limited to 2.75. Therefore, to achieve the corresponding

$$i_{Lr}(t) = \begin{cases} i_{Lr}(t_0)\cos(\omega_r(t-t_0)) - (v_{Cr}(t_0) - V_{in})\frac{1}{Z_r}\sin(\omega_r(t-t_0)), & t_0 \le t < t_1 \\ i_{Lr}(t_1)\cos(\omega_r(t-t_1)) - (v_{Cr}(t_1) - (V_{in} - nV_o))\frac{1}{Z_r}\sin(\omega_r(t-t_1)), & t_1 \le t < t_2 \\ i_{Lr}(t_2)\cos(\omega_m(t-t_2)) - (v_{Cr}(t_2) - V_{in})\frac{1}{Z_m}\sin(\omega_m(t-t_2)), & t_2 \le t < t_3 \end{cases} \tag{5}$$

$$v_{Cr}(t) = \begin{cases} i_{Lr}(t_0)Z_r\sin(\omega_r(t-t_0)) + (v_{Cr}(t_0) - V_{in})\cos(\omega_r(t-t_0)) + V_{\text{in}}, & t_0 \le t < t_1 \\ i_{Lr}(t_1)Z_r\sin(\omega_r(t-t_1)) + (v_{Cr}(t_1) - (V_{in} - nV_o))\cos(\omega_r(t-t_1)) + (V_{\text{in}} - nV_o), & t_1 \le t < t_2 \\ i_{Lr}(t_2)Z_m\sin(\omega_m(t-t_2)) + (v_{Cr}(t_2) - V_{in})\cos(\omega_m(t-t_2)) + V_{\text{in}}, & t_2 \le t < t_3. \end{cases} \tag{6}$$

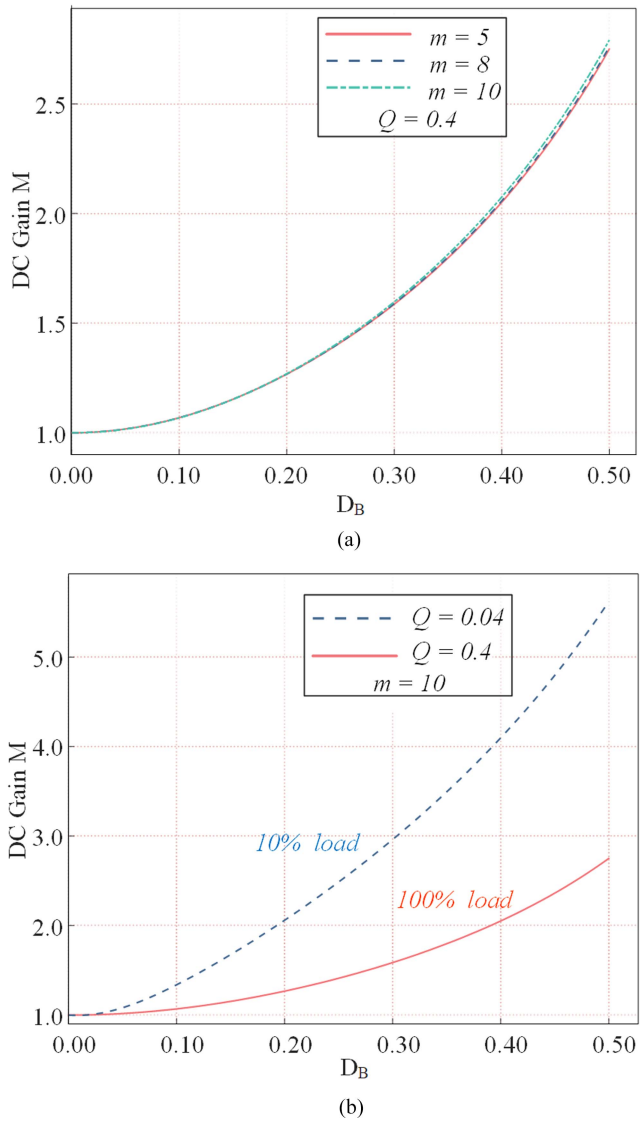


Fig. 7. Gain curves versus D_B for the ISR *LLC* converter: (a) $m = 5$; (b) $Q = 0.4$.

gain at full load, it is necessary to design the maximum gain value using the full-load Q value.

B. Transition Between Two Modes

As shown in Fig. 8, in the normal stage, the output voltage of the PFC is around 400 V ± 10%. Therefore, the system operates in normal mode when the voltage is within 10% below the rated input voltage and the output voltage is controlled using PFM with switch S_3 normally ON, and switches S_1 and S_2 operating in synchronous rectification mode.

When the converter's input voltage falls below 90% of the rated input voltage, the converter enters the hold-up mode. As the input voltage decreases, the conduction pulse width D_B of switches S_1 and S_2 increases, leading to a corresponding rise in the variable output gain. A proportional and integral (PI) controller is introduced to stabilize the output voltage at the rated level. When the voltage drops to the designed lower limit,

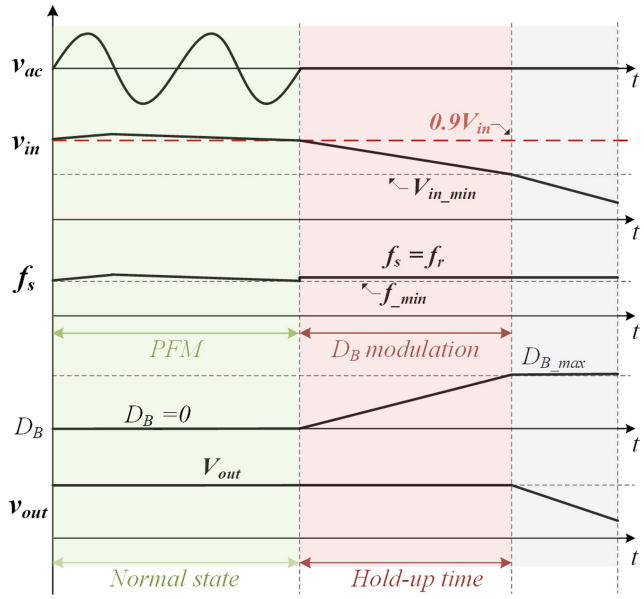


Fig. 8. Principles and sequence of transition between two stages.

D_B reaches its maximum value and remains constant, resulting in a decrease in the output voltage. The principles and sequence of transition between the two stages are illustrated in Fig. 8.

C. Design Consideration

To achieve soft switching for each switch, it is essential to ensure that the body diode conducts just before the switch is turned ON. Before the conduction control signal is ON, the voltage on both sides of the switch must be reduced to zero or below. Assuming the dead time of the two switches is t_d, and the junction capacitance of the switch is C_{OSS}. To ensure that the voltage across the junction capacitance drops to zero within the dead time, the following condition must be satisfied

$$\frac{I_{Lm}}{2C_{OSS}} \cdot t_d \geq V_{\text{in}} \tag{11}$$

where

$$I_{Lm} = \frac{nV_o}{4L_m f_r}. \tag{12}$$

From this, we can derive that:

$$L_m \leq \frac{t_d}{8C_{OSS} f_r}. \tag{13}$$

From the analysis of the dc gain part, it can be concluded that the system gain M is mainly determined by the Q value of the resonant cavity and the duty cycle D_B of the boost stage. With the same duty cycle D_B, the larger the Q value, the smaller the corresponding system gain. Therefore, to ensure a stable output voltage even at the minimum input voltage, the output gain limits the maximum value of the Q value. However, a smaller Q value also increases the peak of i_{Lr}, which subsequently raises the cost of the MOSFET. Therefore, choosing a larger Q value within the gain conditions is beneficial for reducing system costs.

The design process for the experimental parameters is as follows.

1) *System rated parameters:* Define the input voltage range, output voltage, and rated power of the system.
2) *Transformer turns ratio:* Determine the transformer's turns ratio based on the rated input voltage and output voltage, where $n = V_{\text{in\_max}}/V_{\text{out}}$.
3) *Voltage gain range:* Establish the system voltage gain range. The maximum gain is $M_{\max} = V_{\text{in\_max}}/V_{\text{out}}$, and the minimum gain is $M_{\min} = V_{\text{in\_min}}/V_{\text{out}}$.
4) *Resonant tank parameters.* Following the classical *LLC* design process, selecting $Q = 0.4 - 0.6$ allows for the calculation of L_r and C_r. Using the traditional design method, the m value is generally set to approximately 5. Accordingly, L_m is calculated as $L_m = m \cdot L_r$. For the proposed ISR-LLC, a larger m value can be used ($m = 10$). In addition, soft switching must be ensured by considering the dead time t_d and the MOSFET C_{OSS} parameter. The calculation formula is as (13).
5) *Trial calculations and simulations:* Perform trial calculations and simulations to verify whether the parameters satisfy the gain range M required in step 3. If the requirements are not met, adjust the values of Q, m, and L_m iteratively until the requirements are fulfilled.
6) *Switch parameters:* On the primary side, the theoretical maximum voltage of the switching device is equal to the maximum input voltage. To ensure safety, a margin of 1.5 times the maximum voltage is recommended. The current rating should be based on the maximum value of i_{L_r} obtained in the simulation (see Section III), with an additional safety margin of 2 times. On the secondary side, the SR experiences a maximum voltage of twice the output voltage, with a recommended safety margin of 1.5 times. Using the values of i_{L_r} and i_{L_m} calculated in Section III, the maximum current of the SR, i_{SR}, can be determined. Adding a safety margin of 2 times allows for the calculation of the SR current rating.

IV. Simulation Verifications

To validate the proposed control strategy, an ISR *LLC* converter has been designed within the PLECS simulation environment. The hardware parameters were designed according to the guidelines detailed in Section III. This setup can accommodate a wide input voltage range from 200 to 400 V, while maintaining a stable output voltage of 48 V and facilitating a maximum output power of 500 W. Additional parameters are systematically cataloged in Table I.

Fig. 9 illustrates the dynamic behavior of the proposed control strategy. Specifically, it depicts a scenario where the output power is maintained at full load while the input voltage decreases from 400 V to 0 V. The voltage regulation method employs simple PI control based on the D_B (Boost Duty Cycle).

There is a continuous and monotonic positive correlation between the converter's output voltage gain and the D_B (Boost Duty Cycle) value, as shown in Fig. 7. To maintain the output voltage at 48 V, the duty cycle D_B gradually increases as the input voltage decreases. When the input voltage drops to 200 V, the duty cycle is adjusted to $D_B = 0.4$. The period from the drop

TABLE I
Circuit Parameters of the Simulation

Parameters	Value
Input voltage V_i	200 ∼ 400 V
Output voltage V_o	48 V
Rated power P_w	500 W
Transformer turns ratio n	40 : 5 : 5
Switching frequency f_s	100 kHz
Resonant capacitance C_r	33 nF
Resonant inductance L_r	76 μH
Magnetizing inductance L_m	760 μH
Output capacitance C_o	900 μF
Primary switches $Q_1 - Q_4$	IPW60R070C6 (650 V, 70 mΩ)
SR switches $S_1 - S_3$	IRFP4568PBF (150 V, 5.9 mΩ)

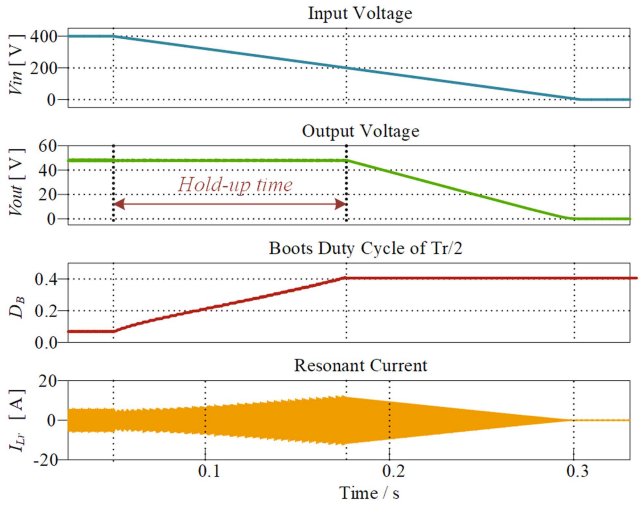


Fig. 9. Dynamic waveform of proposed ISR LLC converter.

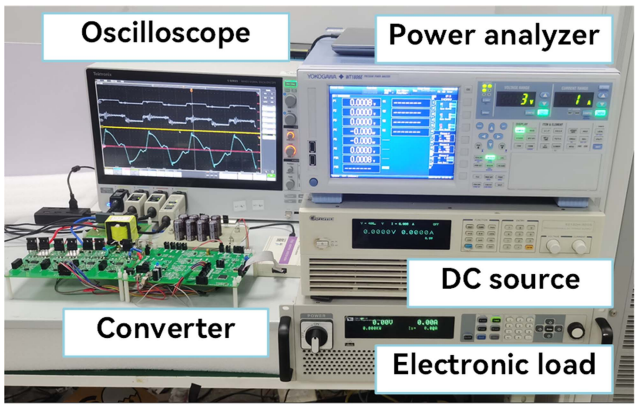
of the input voltage drop to 200 V is referred to as the hold-up time, as shown in the simulation figure. When the voltage falls below 200 V, D_B remains constant, and the output voltage also decreases with the input voltage.

Within the specified input voltage range, the output voltage consistently maintains the rated value, confirming the effectiveness of the theoretical design.

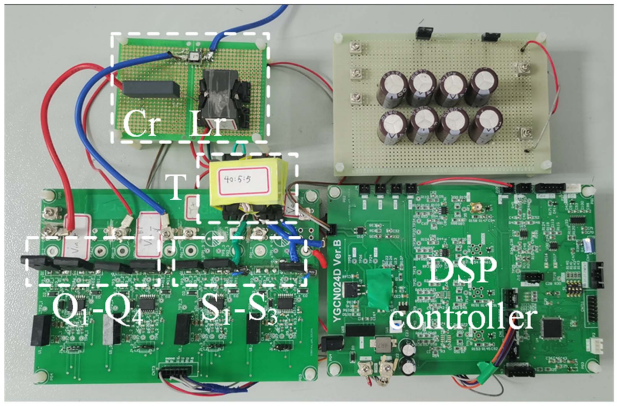
V. Experimental Results

To verify the functionality and performance of the proposed converter, an experimental prototype was built as shown in Fig. 10. Table II presents the design parameters for both the conventional *LLC* converter and the ISR *LLC*. For ease of comparison, the identical parameters of the two systems are displayed in a combined column, while differing parameters are shown in two separate columns. The experimental system parameters differ only in L_m and the operating frequency f_s. The conventional *LLC* a variable-frequency control approach, with frequencies ranging from 56 to 100 kHz.

Traditional *LLC* converters require a smaller value of L_m to achieve a higher output gain. However, the influence of L_m on



(a)



(b)

Fig. 10. (a) Prototype converter and (b) experimental platform.

TABLE II
CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameters	Convertional *LLC*	Proposed ISR-*LLC*
Input voltage V_i	200–400 V	
Output voltage V_o	48 V	
Rated power P_w	500 W	
Transformer turns ratio n	40 : 5 : 5	
Switching frequency f_s	56 ∼ 100 kHz	100 kHz
Resonant capacitance C_r	33 nF	
Resonant inductance L_r	76 μH	
Magnetizing inductance L_m	380 μH	760 μH
Output capacitance C_o	900 μF	
Primary switches $Q_1 - Q_4$	IPW60R070C6(650 V, 70 mΩ)	
SR switches $S_1 - S_3$	IRFP4568PBF (150 V, 5.9 mΩ)	

the gain of the *LLC* converter proposed in this article is minimal, allowing for the selection of a larger L_m. Consequently, compared to traditional *LLC* converters, the average current $i_{Lm-\text{avg}}$ of the L_m in the proposed converter is relatively smaller during normal operation.

Fig. 11(a) displays the key waveforms of the proposed converter when operating at normal state with an input voltage of 400 V and providing an output of 48 V at 10 A. As previously discussed, the converter operates around its resonant frequency, S_1, and S_2 work as the SR MOSFET. ZVS is realized by utilizing

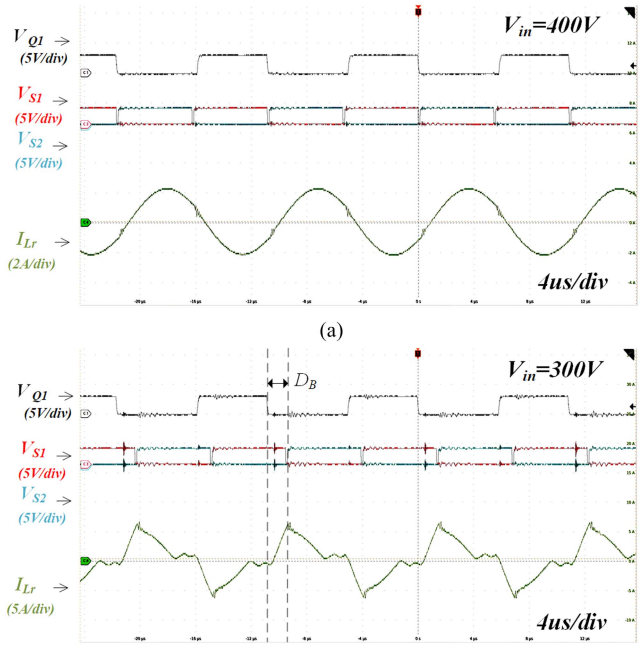


Fig. 11. Key waveforms with full load condition at (a) 400-V input and (b) 300-V input.

the energy stored in magnetizing inductor, with a low current to minimize the circulating current.

Fig. 11(b) depicts the key waveforms of the proposed converter during the hold-up state, under input voltage of 300 V and output of 48 V at 10 A. The gate switch signals for the SRs S_1 and S_2 are delayed by D_B (Boost Duty Cycle), causing a temporary short circuit across the resonant tank. During this interval, the resonant current increases, and the waveform is distorted due to the pulsewidth modulation (PWM) control.

Soft switching can be achieved on both the primary and secondary sides of the converter in Fig. 12. The waveforms were tested under normal operating conditions with input voltage of 400 V and full load. The results demonstrate that ZVS was successfully achieved for both the primary and secondary switches.

As shown in Fig. 13, the ISR-*LLC* demonstrates dynamic transitions between 10% and 100% load under the fixed-frequency phase-shift control mode. It can be observed that the converter maintains the output voltage stable at the target value across various load conditions, validating the effectiveness of the fixed-frequency phase-shift control method.

Fig. 14 shows the key waveforms of the proposed converter throughout the entire hold-up period with feedback control. As V_{in} varies from 400 to 200 V, the hold-up operation can be realized stably at 48 V when the converter gradually increases the boost duty cycle D_B from 0 to 0.5, as illustrated in Fig. 14.

Fig. 15 presents the efficiency performance of the prototype converter. Across all load conditions, the proposed converter exhibits superior efficiency compared to traditional LLC converters. Compared with conventional SR *LLC* converter, a larger L_m can be selected by the proposed ISR *LLC*, which can depress the average magnetizing current $i_{Lm-\text{avg}}$ and conduction

TABLE III
COMPARISON RESULTS WITH 6 HOLD-UP SCHEMES

Requirements / Technologies	Additional components	Secondary rectifier topologies	Circulating current	Bias current of transformer	Input voltage range
PFC output control [4], [6]	None.	Any	High	No	Medium (320-420V)
Variable resonant tank [8], [24]	Variable capacitor and inductor and their control circuit.	Any	High	No	Wide (200-400V)
Primary side boost stage [13], [25]	Primary side boost circuit.	Any	Medium	Yes	Wide (36-72V)
Second side SR PWM control [17], [26], [27]	1 or 2 MOSFETs replace diode with half SR.	H bridge or voltage doubler rectifier	Low	No	Wide (200-400V)
Second side partial power processing [10], [28], [29]	One more transformer and rectifier.	Any	Low	No	Medium (300-400V)
Proposed	1 MOSFET.	Full wave rectifier	Low	No	Wide (200-400V)

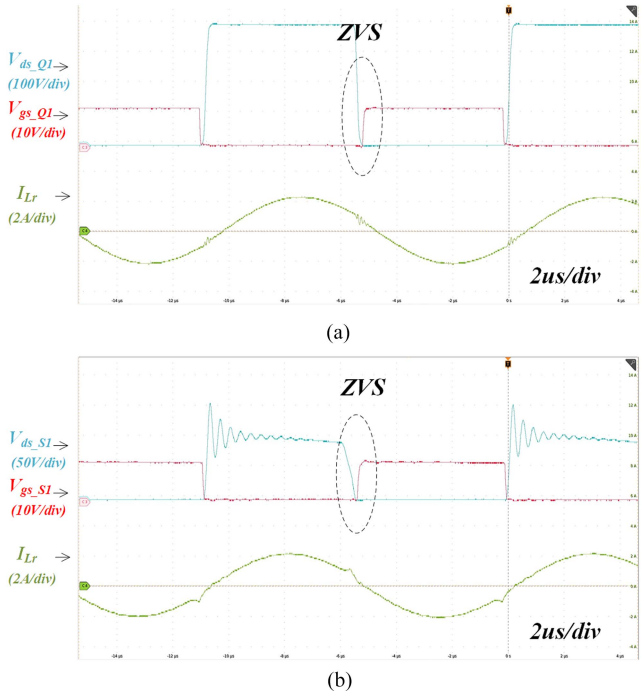


Fig. 12. ZVS waveforms at normal operation: (a) primary-side switch and (b) secondary-side switch.

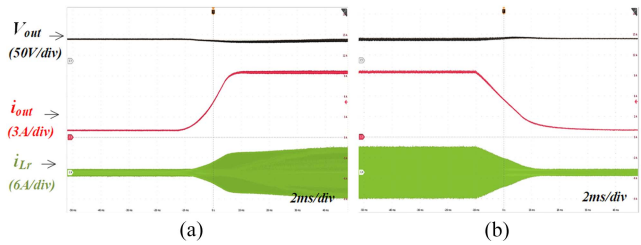


Fig. 13. Dynamic performance of the ISR *LLC* in response to step changes in the load. (a) Step increase of load from 10% load to full load. (b) Step decrease of load from full load to 10% load.

losses, therefore, higher efficiency can be achieved. This high efficiency, particularly at light and medium loads, is crucial for data center applications, where power systems are typically designed with sufficient power and traffic margins. Thus, the

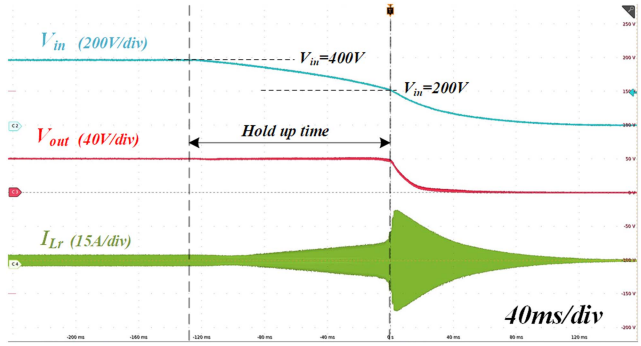


Fig. 14. Waveforms during the hold-up time at full load.

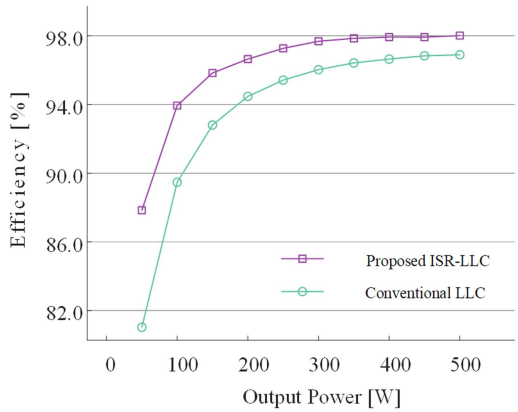


Fig. 15. Efficiency of ISR *LLC* converter and conversational converter.

efficiency characteristics of the proposed converter align well with the operational requirements of data centers.

VI. COMPARISON WITH PRIOR WORKS

Following the review of prior research detailed in Section I, Table III represents the characteristics of the proposed converter compared to previous works to evaluate potential solutions for hold-up time compensation.

1) *Less additional components:* This converter provides a wide input voltage gain with only one additional MOSFET. Compared to other solutions, it does not require complex

circuits, such as partial power processing circuits or boost stage circuits. This approach simplifies the circuit design and reduces the cost.

2) *Smaller circulating current:* By employing a larger magnetizing inductance (L_m), the proposed converter can get a smaller circulating current in the resonant circuit, thereby reducing conduction losses. This is in contrast to some methods that increase the gain by reducing the value of L_m, especially those that modify the resonant tank.
3) *No bias current in transformer:* The converter utilizes a symmetrical resonant control method, which eliminates bias current in the transformer, thereby enhancing the utilization rate of transformer. In comparison, some methods that employ asymmetrical control methods can generate bias current in the transformer.
4) *Wider input voltage range:* As the above analysis and experiments described, this converter can achieve a wide input voltage range of 200 to 400 V. A broader voltage input range makes the converter get a longer output hold-up time under the same output power and bus capacitance conditions.

VII. Conclusion

In this article, a novel ISR *LLC* converter designed for extended hold-up time operation is introduced. This novel topology integrates only a single switch to the traditional SR *LLC* converter, where the auxiliary hold-up circuit is greatly simplified. Utilizing this topology alongside a fixed-frequency phase shift control method, the voltage gain is substantially increased, and the hold-up time is markedly extended. Moreover, compared to traditional *LLC* converters, a larger magnetizing inductance can be selected, thereby effectively diminishing the system's conduction losses. The system adopts a symmetrical control method to reduce the impact of bias magnetization. This article provides an in-depth analysis of the converter's topology, operational principles, gain analysis, and design considerations.

Although this study presents a novel ISR *LLC* topology and control method, the output gain range remains limited. In the future, increasing the gain could allow for further reduction in the bus capacitor value. In addition, the research approach could be extended to explore gain enhancement in similar topologies.

Experiment results demonstrate the converter's high efficiency in standard mode and an improved dc gain during hold-up time. Consequently, the proposed ISR *LLC* converter emerges as a strong contender for power supply solutions in data center applications.

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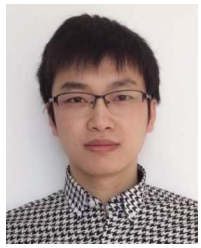

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