# An Efficient Dual-Output Bipolar Buck-Boost AC-AC Converter With Flexible Operation Range

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***Abstract*—Three-phase flexible ac-link (FACL) converter configuration enables the production of three-phase ac voltages with decoupled magnitude and phase using single-phase ac–ac converters. However, traditional FACL converter require six discrete ac–ac converters. Building upon the recently introduced FACL configuration that utilizes only three dual-output converters, this article proposes a new and efficient single-input, dual-output bipolar ac–ac converter for applications in the new FACL topology. It can provide independent control of buck and boost voltage transfer ratios, and both outputs are completely independent of each other, capable of producing the same or opposite phase outputs with independent control of their magnitudes. Moreover, all devices experience significantly smaller (and identical) voltage stresses and current stresses. The proposed converter avoids the use of bidirectional ac switches, thus simplifying the commutation process of traditional ac–ac converters. The input and output currents are continuous, avoiding harmonic pollution in the input supply and saving additional filters. Furthermore, the proposed converter has reversible operation and can provide bidirectional power flow. An in-depth analysis of the proposed converter is provided based on the proposed switch modulation strategies for various operation scenarios. Detailed comparisons with existing counterpart converters prove its better circuit performance with smaller component stresses and ripples and improved input/output power quality. Finally, experimental results prove the feasibility of the proposed converter.**

***Index Terms*—AC–AC power conversion, bipolar operation, dual-output, flexible ac link (FACL) converter, voltage compensation.**

## I. Introduction

THE integration of intermittent renewable energy sources, coupled with diverse grid disturbances, dynamic states, and varying loads, has significantly increased uncertainties in grid operations. ac–ac power converters can improve grid voltage flexibility and control [1], [2]. Traditional ac–ac power conversion is typically achieved through back-to-back connected indirect ac–dc–ac converters with a dc-link [3], [4]. However, using dc-link capacitors adds weight, cost, and failure rates while reducing system lifespan [4], [5].

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Recently, there has been increased interest in direct pulsewidth modulation ac–ac converters [6], [7] due to their single-stage power conversion, elimination of dc-link electrolytic capacitors, simple operation, and smaller footprint. Traditional ac–ac converters [8] are adapted from dc–dc converters by replacing unidirectional voltage-blocking devices with bidirectional ac switches. However, these converters are unipolar, providing either same-phase or antiphase output voltages, which limits their applications primarily to full load rating direct ac voltage regulation [9]. While simple to implement, they require a three-winding transformer with opposite polarity taps to generate a bipolar output [10].

Bipolar output ac–ac converters [7], [10] are primarily being developed to provide both negative and positive series voltage, addressing grid voltage sags and swells in dynamic voltage restorer applications [2], [7], [10]. The basic bipolar ac–ac converter [11] is derived from a Z-source network, utilizing a unique combination of inductors and capacitors for inverting and noninverting operations. However, it lacks noninverting buck operation, and the presence of numerous passive components increases its footprint. The unified bipolar ac–ac converter [12] reduces the number of passive components but still lacks noninverting boost operation and features discontinuous input/output currents.

Various classes of bipolar ac–ac converters have been developed to address commutation problems associated with standard bidirectional ac device-based converters [11], [12]. These include continuous input/output current converters [13], switching-cell-based converters [2], [7], [14], [15], and nondifferential ac chopper-based converters [16], [17], [18]. However, a fundamental limitation of these ac–ac converters is their inability to produce a finite output voltage when the input voltage crosses zero, restricting the synthesized output voltage phase to be either in-phase or antiphase with the input voltage. The dual-virtual quadrature source control method [19] can adjust the output voltage phase within a limited range but requires an auxiliary transformer to filter out the third harmonic component. Additionally, there is a trade-off between the achievable phase shift and the amplitude of the output voltage.

In a three-phase ac system, a novel method for synthesizing a single-phase output voltage with adjustable amplitude and phase has been developed using two ac–ac converters fed from two phase lines [20], [21], [22], [23], [24]. Conventional flexible ac-link (FACL) converters [20], [21], [22] utilize unipolar ac choppers, restricting output phase-shift control to a single quadrant. A recent proposal [23] replaces unipolar converters

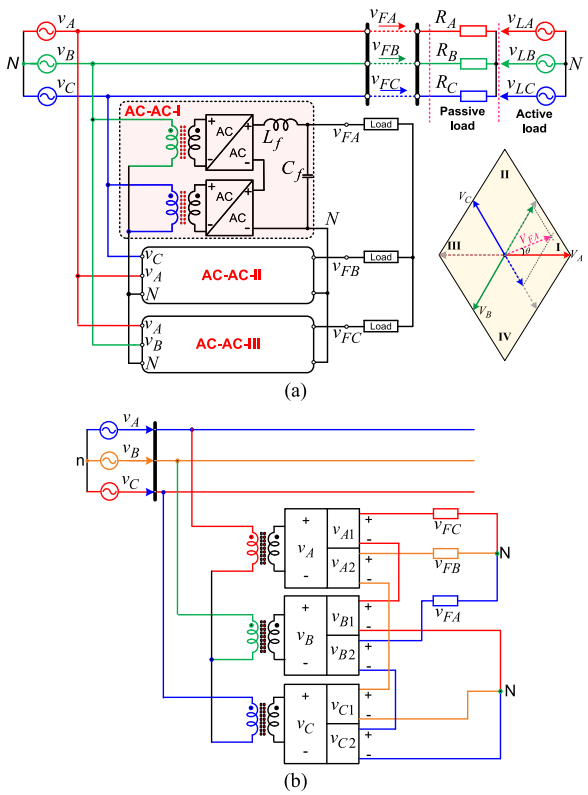



Fig. 1. Three-phase FACL topologies. (a) Developed in [23] implemented with single output converters of [16] and its voltage synthesis process. (b) Developed in [24].

with bipolar ac–ac converters [16], enabling operation across all four quadrants. This three-phase FACL converter configuration, depicted in Fig. 1(a), features two bipolar ac–ac converters, each supplied from separate phase lines, with their outputs connected in series to generate a single-phase output with controllable amplitude (only step-down) and phase (fully adjustable). For example, the phase-A output voltage $v_{FA}$ can be synthesized by integrating the outputs of two converters fed from phase-B and phase-C supply lines ($v_A$ and $v_B$). The generated phase voltages ($v_{FA}, v_{FB}$, and $v_{FC}$) can independently feed loads and manage full-load power processing or be injected in series with input line voltages ($v_A, v_B$ and $v_C$), providing controllable voltage across the load bus line to mitigate voltage sags and swells, including phase jumps, for passive loads. Additionally, the phase-shifted voltage across the load bus can regulate power flow when an active load is connected. However, this FACL configuration has several limitations: it requires six ac–ac converters to provide three-phase output voltages, increasing component count, implementation cost, and complexity; it uses buck-type ac choppers [16], limiting the achievable voltage amplitude; and it draws discontinuous current from ac mains, increasing input current total harmonic distortion (THD) and necessitating sizeable *LC* filters.

Introducing a significant step-forward in FACL converter development, the research in [24] proposed an improved three-phase FACL converter [24], consisting of four-leg dual-output converters, as illustrated in Fig. 1(b). This configuration necessitates only three converters, thereby reducing the FACL design and implementation complexity with reduced component count and cost. However, the dual-output converter in [24] imposes certain constraints on the buck and boost duty ratios and voltage gains. Specifically, the boost module operates with half the duty cycle range of a traditional boost converter, with a minimum voltage gain of 2, while the buck module is limited to a duty ratio of [0, 0.5] and a voltage gain below 0.5. These constraints increase the voltage stress on switches, the current and voltage ripples in passive components, and require the large and costly components.

Inspired from the work in [24], this research proposes a new dual-output bipolar buck-boost ac–ac converter and its modulation strategies for application in FACL converter. The proposed converter has the following salient characteristics and improvements over the previous work in [24].

1) Buck and boost stages are fully decoupled and independent. Boost voltage gain can be adjusted from 1 to beyond, and buck voltage gain can be varied from 0 to 1, independent of each other. This solves the duty ratio and gain constraints of the previous work, improving the operation range of the converter.
2) The proposed operations are very efficient with much smaller component voltage and current stresses.
3) Both outputs can be modulated independently of each other in terms of both their amplitude and voltage polarity.
4) It draws continuous current from ac mains and provides continuous output currents. Moreover, its inductor demand is significantly reduced.
5) Only three proposed converters are required to implement three-phase FACL.
6) Proposed converter does not have commutation issues of traditional ac–ac converters with bidirectional ac switches.

The rest of this article is organized as follows. Section II introduces proposed topology and its operation. Section III analyzes voltage/current stress and ripple in the proposed converter. Section IV compares it with conventional FACL converters, while Section V presents simulation and experimental results. Finally, Section VI concludes the article.

## II. Proposed AC–AC Converter and Its Operation

Fig. 2 illustrates the proposed dual-output bipolar buck-boost ac–ac converter, for application in improved three-phase FACL converter, as illustrated in Fig. 1(b). It comprises a boost input module, which includes an input *LC* filter $L_{\text{in}}C_{\text{in}}$ along with switches $S_1 - S_4$. This module provides a step-up and rectified voltage across capacitor $C_i$ with a voltage gain of 1 and beyond. Two output buck modules are fed from capacitor $C_i$: Buck module-1 consists of switches $S_5 - S_8$ and output *LC* filter $L_{o1}C_{o1}$ and generates output voltage of $v_{o1}$; Buck module-2 comprises of switches $S_9 - S_{12}$ and output *LC* filter $L_{o2}C_{o2}$ and produces voltage of $v_{o2}$. The gains of the buck modules1 and 2 can be adjusted within a complete range of [0, 1] independent of each other and that of input boost module.

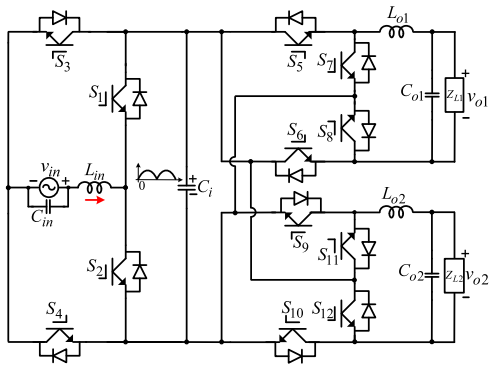


Fig. 2. Proposed dual-output bipolar buck-boost AC–AC converter.

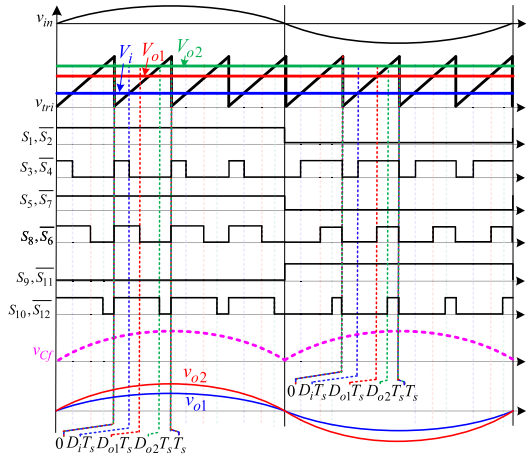


Fig. 3. Switch control signals for noninverting outputs with different amplitudes.

In order to meet the requirements of FACL converter, the proposed topology is required to generate two output voltages with independent magnitudes and provide four polarity combinations: both outputs are noninverting, both outputs are inverting, output-1 is noninverting while output-2 is inverting, and output-1 is inverting while output-2 is noninverting.

### A. Both Noninverting Outputs With Different Amplitudes

Fig. 3 shows the proposed switch modulation strategy to produce two noninverting buck-boost outputs with different amplitudes. Input side switches $S_1$ and $S_2$ are line-frequency modulated, and switches $S_2$ and $S_3$ are modulated at switching frequency by comparing reference signal $V_i$ with triangular carrier signal $v_{\text{tri}}$. For positive input half-cycle $v_{\text{in}} > 0$, switch $S_1$ is completely ON and $S_2$ is completely OFF. On-time of switch $S_3$ represents the interval $D_iT_s$, and on-time of its complementary switch $S_4$ makes up interval $(1 - D_i)T_s$. Switches $S_5, S_7$ (of module-1) and $S_9, S_{11}$ (of module-2) are line-frequency modulated. Switches $S_6, S_8$ (of module-1) and $S_{10}, S_{12}$ (of module-2) are high-frequency modulated by comparing reference signals $V_{o1}$ and $V_{o2}$ with $v_{\text{tri}}$. For $v_{\text{in}} > 0$, switches $S_5, S_{11}$ are completely ON and $S_7, S_9$ are OFF. On-time of switches $S_8$ and $S_{12}$ represent the time intervals $D_{o1}T_s$ and $D_{o2}T_s$, respectively. Switches $S_6$ and $S_{11}$ are switched complementary to switches $S_8$ and $S_{12}$, respectively. Notably, references $V_i$, $V_{o1}$, and $V_{o2}$ can be independently adjusted from 0 to 1, offering greater operational flexibility in the proposed converter compared to [24]. For $v_{\text{in}} > 0$, four equivalent circuits exist as shown in Fig. 4. Circuit operation for $v_{\text{in}} > 0$ is explained later.

*1) Interval-1[0∼ $D_iT_s$]:* Switches $S_1$, $S_3$, $S_5$, $S_8$, $S_{10}$ and $S_{11}$ are ON [see Fig. 4(a)]. The other switches are OFF. The input inductor $L_{\text{in}}$ stores energy from the input source through switches $S_1$ and $S_3$. Capacitor $C_i$ provides energy to inductor $L_{o1}$ and load-1 through switches $S_5$ and $S_8$. It also supplies energy to output inductor $L_{o2}$ and load-2 through switches $S_{10}$ and $S_{11}$. Positive capacitor $C_i$ voltages appear across both output $LC$ filters. Applying KVL, we get the following circuit voltage relations:

$$\{v_{Lin} - v_{\text{in}} = 0; v_{Lo1} - v_{Ci} = -v_{o1}; v_{Lo2} - v_{Ci} = -v_{o2}\ . \tag{1}$$

*2) Interval-2 [$D_iT_s \sim D_{o1}T_s$]:* All switching states remain same except input side switch $S_3$ is turned-OFF and $S_4$ is turned-ON [see Fig. 4(b)]. Input source $v_{\text{in}}$ and inductor $L_{\text{in}}$ together provide energy to charge capacitor $C_i$ through switches $S_1$ and $S_4$. Capacitor $C_i$ keeps providing energy to inductors $L_{o1}, L_{o2}$ and both loads as in previous interval. Applying KVL, we get the following circuit voltage relations:

$$\{v_{Lin} - v_{\text{in}} = -v_{Ci}; v_{Lo1} - v_{Ci} = -v_{o1}\ ; v_{Lo2} - v_{Ci} = -v_{o2}\ . \tag{2}$$

*3) Interval-3 [$D_{o1}T_s \sim D_{o2}T_s$]:* Switching signals and states of input boosting stage and buck module-2 remain same as in interval-2. For buck module-1, switch $S_8$ is turned-OFF and $S_6$ is turned-ON [see Fig. 1(c)[. Load-1 is disconnected from the main circuit and it is feed by energy from inductor $L_{o1}$. Inductor $L_{o1}$ current freewheels through switches $S_5$ and $S_6$. Applying KVL, we get

$$\{v_{Lin} - v_{\text{in}} = -v_{Ci};\ v_{Lo1} = -v_{o1}\ ; v_{Lo2} - v_{Ci} = -v_{o2}\ . \tag{3}$$

*4) Interval-4 [ $D_{o2}T_s \sim T_s$]:* The buck module-2 undergoes switching transition. Switch $S_{10}$ is turned-OFF and $S_6$ is turned-ON. Now load-2 is also disconnected from input circuit and inductor $L_{o2}$ supports the load. Inductor $L_{o2}$ current freewheels through switches $S_{11}$ and $S_{12}$. Switching states and operations of input boosting stage and load-1 remain the same as in previous interval. Applying KVL, we get

$$\{v_{Lin} - v_{\text{in}} = -v_{Ci};\ v_{Lo1} = -v_{o1}\ ;\ v_{Lo2} = -v_{o2}\ . \tag{4}$$

By making average inductors voltages zero for a switching-cycle, capacitor $C_i$ voltage and output voltages $v_{o1}$ and $v_{o2}$ can be determined as

$$\{v_{Ci} = \tfrac{1}{1-D_i}\ v_{\text{in}};\ v_{o1} = D_{o1}\ v_{Ci};\ v_{o2} = D_{o2}\ v_{Ci}\ . \tag{5}$$

In (5), assume $G_{\text{i}} = \frac{v_{Ci}}{v_{\text{in}}}$ , $G_{o1} = \frac{v_{o1}}{v_{Ci}}$ and $G_{o2} = \frac{v_{o2}}{v_{Ci}}$ . Then input to output voltage transfer ratios $G_{oi1} = \frac{v_{o1}}{v_{\text{in}}}$ and $G_{oi2} = \frac{v_{o2}}{v_{\text{in}}}$ of both outputs are given by

$$\left\{G_{oi1} = \tfrac{v_{o1}}{v_{\text{in}}} = \tfrac{D_{o1}}{1-D_i}\ ;\ G_{oi2} = \tfrac{v_{o2}}{v_{\text{in}}} = \tfrac{D_{o2}}{1-D_i}\ . \right. \tag{6}$$

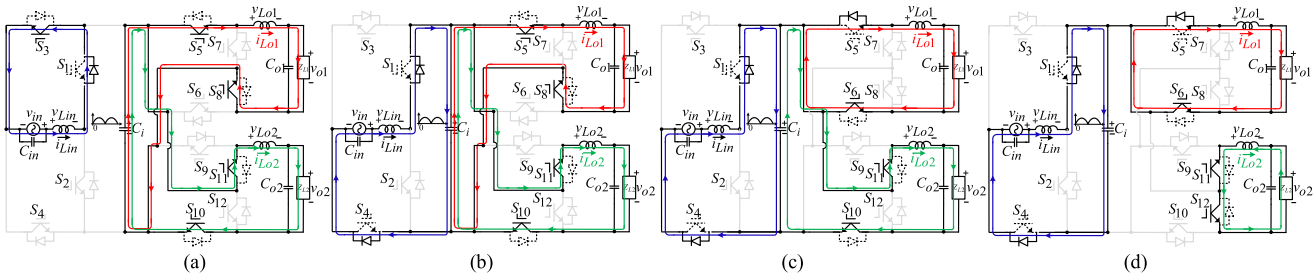



Fig. 4. Equivalent circuits for both noninverting buck-boost outputs with different amplitudes. (a) Interval-1. (b) Interval-2. (c) Interval-3. (d) Interval-4.

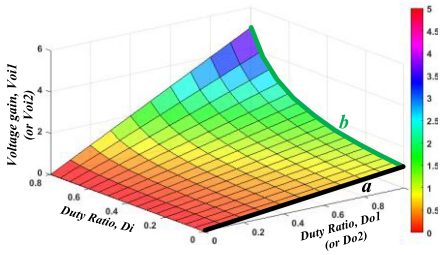



Fig. 5. Three-dimensional voltage gain plots versus two duty ratios.

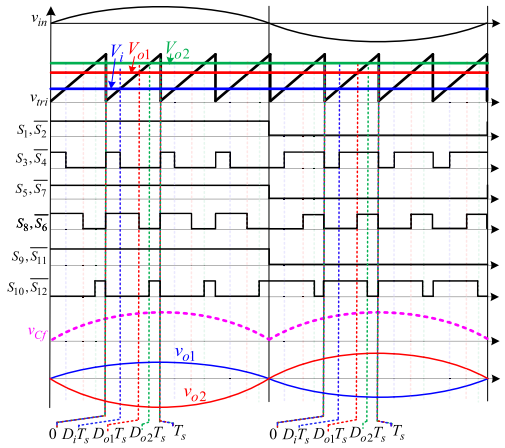



Fig. 6. Switch control signals for one noninverting output and one inverting output with different amplitudes.

All three duty ratios $D_i$, $D_{o1}$ and $D_{o2}$ can be adjusted in the full range [0,1] and completely independent of each other. Fig. 5 shows a three-dimensional plot of gain $G_{\text{oi1}}$ (or $G_{\text{oi2}}$) with variations in duty ratios $D_i$ and $D_{o1}$ (or $D_{o2}$). As observed, they are numerous combinations of $D_i$ and $D_{o1}$ (or $D_{o2}$) which provide the same gain $G_{oi1}$ (or $G_{oi2}$). The bold lines "*a*" and "*b*" on the curve are special cases when $D_i = 0$ and $D_{o1} = 1$ (or $D_{o2} = 1$), respectively. For operation along curve '*a*', switches $S_3$ and $S_4$ are power-frequency modulated, $G_{\text{i}} = 1$ and $G_{oi1} = G_{o1}$ . Thus, this is an efficient buck operation scenario where only the duty ratios $D_{o1}$ and $D_{o2}$ are modulated (and hence only buck modules are activated). Similarly, the operation along curve '*b*' is efficient boost operation scenario in which switches $S_6$, $S_8$, $S_{10}$, and $S_{12}$ are power-frequency modulated with $G_{o1} = G_{o2} = 1$, and only the boost duty ratio $D_i$ is modulated.

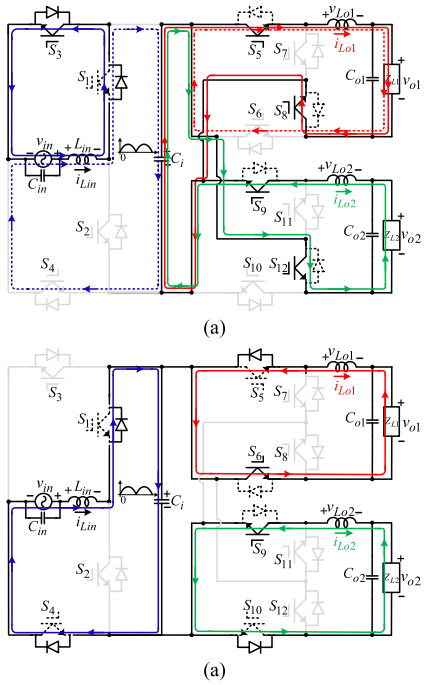
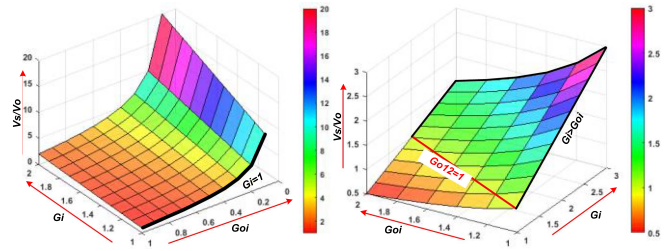



Fig. 7. Equivalent circuits for noninverting output-1 and inverting output-2. (a) Interval-a. (b) Interval-b.

### *B. One Noninverting Output and One Inverting Output With Different Amplitudes*

Fig. 6 illustrates the proposed switch modulation to generate noninverting output-1 and inverting output-2. The reference signals $V_i$, $V_{o1}$ and switch control signals ($S_1 - S_8$) of the input boost stage and buck module-1 remain the same. The only difference lies in modulation signals of switches $S_9 - S_{12}$ of module-2. Switches $S_9$ and $S_{11}$ operate complementary at the power frequency again, but switch $S_9$ is now fully turned-ON for $v_{\text{in}} > 0$. Switches $S_{10}$ and $S_{12}$ operate at switching frequency by comparing $V_{o2}$ with $v_{\text{tri}}$. However, the on-time of switch $S_{12}$ now constitutes the time interval $D_{o2}T_s$, while that of switch $S_{10}$ constitutes the time interval $(1 - D_{o2})T_s$. There are four operation intervals again, but the operation of the boosting stage and output-1 remains the same as in the previous operation. Therefore, only two intervals are explained corresponding to the operation of output module-2.

*1) Interval-a [0∼ $D_{o2}T_s$]:* During this interval, switches $S_9$ and $S_{12}$ are turned on (Fig. 7(a)). Capacitor $C_i$ provides energy




(a) (b)

Fig. 8. Switch voltage stresses as function of voltage gains $G_i$ and $G_{oi}$. (a) Buck operation. (b) Boost operation.

to output inductor $L_{o2}$ and load-2. The polarity of capacitor $C_i$ voltage as applied across the output *LC* filter of load-2 is reversed. This inverts the load-2 voltage $v_{o2}$ in comparison with the input voltage$v_{\text{in}}$. This interval combines intervals-1 $[0 \sim D_i T_s]$, interval-2 $[D_i T_s \sim D_{o1} T_s]$, and interval-3 $[D_{o1} T_s \sim D_{o2} T_s]$ of the previous operation, and current loops of the input boosting stage and output module-1 are illustrated by solid and dotted lines. The voltage across inductor $L_{o2}$ is given by as a function of capacitor $C_i$ voltage and load-2 voltage $v_{o2}$

$$\{v_{Lo2} = -v_{o2} + v_{Ci} \ . \tag{7}$$

*2) Interval-b [$D_{o2}T_s \sim T_s$]:* The output module-2 undergoes switching transition (Fig. 7(b)). Switch $S_{12}$ is turned-OFF, and $S_{10}$ is turned-ON. Now, the output module-2 is disconnected from the input, and inductor $L_{o2}$ supports the load-2. Inductor $L_{o2}$ current freewheels through switches $S_9$ and $S_{10}$. Switching states and operations of the input boosting stage and output module-1 remain the same as in the previous interval. The voltage across inductor $L_{o2}$ is given by

$$\{v_{Lo2} = -v_{o2} \ . \tag{8}$$

Input to output voltage gains $G_{oi1}, G_{oi2}$ for both outputs are given by

$$\left\{G_{oi1} = \frac{v_{o2}}{v_{\text{in}}} = \frac{D_{o1}}{1-D_i};\ G_{oi2} = \frac{v_{o2}}{v_{\text{in}}} = -\frac{D_{o2}}{1-D_i} \ . \right. \tag{9}$$

Negative sign "-" in expression of $G_{\text{oi2}}$ represents the reversal of its output voltage polarity.

## III. Component Stresses and Design Discussion

### A. Switch Voltage and Current Stresses

The blocking voltages of switches $v_s$ are same as capacitor $C_i$ voltage $v_{Ci}$. They are given by

$$\left\{v_{\text{s}} = \frac{v_o}{G_{o12}} = v_o \frac{G_{oi12}}{G_i} \ . \right. \tag{10}$$

From (10), normalized switch voltage stresses $(v_{\text{s}}/v_o)$ are plotted against variations in boosting gain $G_i$ and overall (input to output) gain $G_{oi12}$ for buck and boost operations in Fig. 8(a) and (b), respectively. From the graphs, for the same gain $G_{oi12}$, there are different voltage stresses for different values of $G_i$ (and $G_{o12}$). However, for buck operation, the minimum $v_s/v_o$ occurs along the points in graphs where $G_i$ is 1 (i.e., $G_{oi12} = G_{o12}$ ), as highlighted by the black line in Fig. 8(a). This voltage stress $v_{\text{s}}$ will be maximum for minimum $G_{oi12}$, i.e., when the input voltage $v_{\text{in}}$ is highest. Similarly, for boost operation, the minimum voltage stress $v_{\text{s}}/v_o$ is equal to 1 (when $v_{\text{s}} = v_o$ ) for boost operation when $G_{oi12} = G_i$ (or buck module gain $G_{oi12} = 1$) as shown by the red line in Fig. 8(b).

The current stresses $i_s$ of switching devices are given by

$$\begin{cases} i_{s1-s4} = i_{\text{in}} = i_{o1}\, G_{oi1} + i_{o2} G_{o2} \\ i_{s5-s8} = i_{o1}\ ; i_{s9-s12} \end{cases} . \tag{11}$$

As observed, current stresses of switches $S_5 - S_8$ and $S_9 - S_{12}$ are same as the load-1 and load-2 currents, respectively, which only depends on load power. Switches $S_1 - S_4$ experience maximum current stresses for maximum gain (or minimum input voltage) during boost operation.

### B. Passive Components

The current ripples $\Delta i_{Lin}$ of inductors $L_{\text{in}}$, $L_{o1}$ and $L_{o2}$ can be find as

$$\begin{cases} \Delta\, i_{Lin} = \frac{v_{o1,2}}{f_s L_{\text{in}}} \frac{G_i - 1}{{G_i}^2} \\ \Delta\, i_{Lo1,2} = \frac{v_{o1,2}}{f_s L_o} \ (1 - G_{o1,2}) \end{cases} . \tag{12}$$

Inductor $L_{\text{in}}$, $L_{o1}$ and $L_{o2}$ values can be decided to contain their current ripples to $\alpha\%$ of their peak current stresses$I_L$, $\Delta\, i_L = \alpha\% I_L$.

The voltage ripple of capacitor $C_i$ is given by

$$\left\{\Delta\, v_{Ci} = \frac{i_o}{f_s C_i} \frac{G_i - 1}{G_i} \ . \right. \tag{13}$$

The maximum capacitor voltage stress $V_{Ci}$ can be determined by (21). Capacitor value $C_i$ can be decided to limit its voltage ripple to $\beta\%$ of its voltage stress $V_{Ci}$, $\Delta\, v_{Ci} = \beta\% V_{Ci}$.

## IV. Comparison With Existing Converters for FACL Converter Applications

Table I gives a comparison of the salient features of the proposed dual-output bipolar ac–ac converter and existing unipolar [22] and bipolar ac–ac converters [15], [23], [24] for FACL converter applications. The unipolar converter in [22] limits the phase control range to a single quadrant and requires a safe-commutation strategy due to the use of bidirectional ac switching devices. The bipolar converter in [15] adopts a dual-buck structure to eliminate the commutation issue; however, it requires too many semiconductor devices (16) for a single converter and suffers from lower magnetic utilization. Moreover, its noninverting and inverting outputs are asymmetric, complicating circuit design, control, and optimization. The converter in [23] provides a symmetric bipolar output, but has a limited voltage transfer ratio due to its only step-down operation, and it produces discontinuous input current. All these topologies [15], [22], [23] provide a single output, necessitating the use of six discrete converters for FACL converter implementation. On the other hand, the converter in [24] reduces the number of discrete converters to three and maintains continuous input current. Nevertheless, its restricted duty ratio range and limitations on buck and boost voltage gains result in significantly higher component

TABLE I
COMPARISONS WITH EXISTING CONVERTER TOPOLOGIES FOR FACL APPLICATIONS

| Parameters | Single output unipolar [22] | Single output bipolar [15] | Single output bipolar [23] | Dual-output bipolar [24] | Proposed converter |
|---|---|---|---|---|---|
| Operations | Noninverting buck | Noninverting buck<br>Inverting buck-boost | Bipolar buck | Bipolar buck-boost | Bipolar buck<br>Bipolar boost<br>Bipolar buck-boost |
| Voltage gain $G(\frac{v_o}{v_{in}})$ | $D$ | $D, -\frac{D}{1-D}$ | $\pm D$ | $\pm\frac{0.5-D_{o1,2}}{0.5-D_i}$ | $\pm D_{o12}, \pm\frac{1}{1-D_i}\pm\frac{D_{o1,2}}{1-D_i}$ |
| Input to output voltage transfer range | Restricted | Restricted | Restricted | Restricted | Flexible |
| Number of discrete converters needed for three-phase FACL | 6 | 6 | 6 | 3 | 3 |
| No. of switches for implementation three-phase FACL | $24(S_1-S_{24})$ | $48(S_1-S_{48})$ | $48(S_1-S_{48})$ | $24(S_1-S_{24})$ | $36\,(S_1-S_{36})$ |
| No. of inductors | 12 | 12 | 6 | 9 | 9 |
| No. of capacitors | 6 | 12 | 12 | 6 | 6 |
| Switch voltage stresses | $v_{in}$ (Buck) | $v_{in}$+$v_o$ | $v_{in}$ (Buck) | $>2v_{in}$ (Buck),<br>$>2v_o$ (Boost) | $v_{in}$ (Buck),<br>$v_o$ (Boost) |
| Available duty ratio range | Flexible,<br>$0\le D\le 1$ | Flexible,<br>$0\le D\le 1$ | Flexible,<br>$0\le D\le 1$ | Restricted,<br>$0\le D_i\le 0.5$<br>$0\le D_{o1,2}\le 0.5$ | Flexible,<br>$0\le D_i\le 1$<br>$0\le D_{o12}\le 1$ |
| Continuity of input current | Discontinuous | Discontinuous | Discontinuous | Continuous (High ripple) | Continuous<br>(Very low ripple) |
| Input filter inductor requirement | Very high | Very high | Very high | High | low |
| Compensation magnitude and phase in series voltage injection applications | Very Narrow | Very Narrow | Narrow | Narrow | Wide |
| Three-phase symmetrical sag compensation | Below 50% | Below 50% | Below 50% | Below 50% | Below and above 50% |
| The phase-shift compensation range for series voltage application | $\frac{2\pi}{3}\,[-\frac{\pi}{3},\frac{\pi}{3}]$ | $\frac{2\pi}{3}\,[-\frac{\pi}{3},\frac{\pi}{3}]$ | $\frac{2\pi}{3}\,[-\frac{\pi}{3},\frac{\pi}{3}]$ | $\frac{2\pi}{3}\,[-\frac{\pi}{3},\frac{\pi}{3}]$ | $2\pi\,[-\pi,\pi]$ |

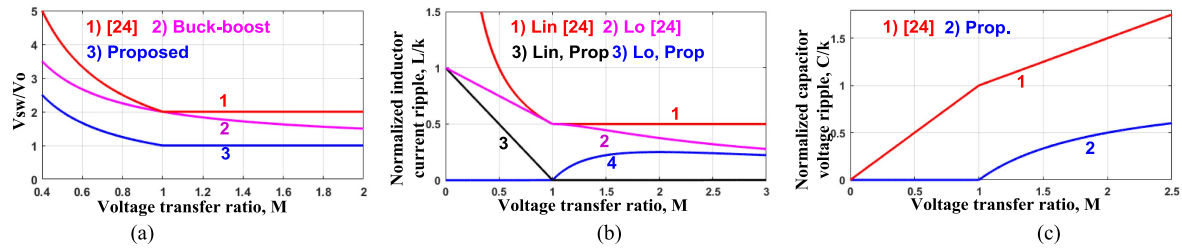



Fig. 9. Theoretical comparison plots. (a) Switch voltages. (b) Inductor current ripples. (c) Capacitor voltage ripples.

voltage stresses and ripples, increasing component demand and cost while compromising input/output power quality.

The proposed converter stands out as the only reported solution employing three discrete modules for FACL topology implementation while achieving complete decoupling between the input boost and output buck modules. This enables flexible and efficient operation with reduced component stresses, lower ripples, and enhanced power quality. A detailed comparison of the proposed converter with [24] is provided below.

### A. Switching Devices Stress Comparisons

The switch voltage stresses $v_s$ of the proposed and the latest developed dual-output bipolar ac–ac converter [24] are given by

$$\begin{cases} v_s = v_o\,\frac{(G_{oi}+1)}{G_{oi}} \text{ Basic buck} - \text{boost} \\ v_s = \frac{2}{G_{oi}}\,v_o \text{ (Buck)},\ 2v_o \text{ (Boost) [24]} \\ v_s = \frac{v_o}{G_{oi}} \text{ (Buck)},\ v_o \text{ (Boost) Proposed} \end{cases} . \quad (14)$$

The switch voltage stresses $v_s$ of the proposed, four-leg converter [24], and basic (inverting) buck-boost ac–ac converters are plotted in Fig. 9(a). It is observed that the switches of the proposed converter have the least voltage stresses. The switch voltage stresses of the four-leg converter are even higher than those of a basic (inverting) buck-boost converter. The switch current stresses of the proposed and converter in [24] are same, and therefore, proposed converter require switching devices with smaller voltage and power ratings.

### B. Passive Component Comparisons

The inductor current ripples $\Delta i_L$ of the counterpart four-leg converter [24] are given by

$$\begin{cases} \Delta\, i_{Lin} = \frac{v_{o1,2}}{f_s L_{in}}\,\frac{1}{G_{oi12}};\ \Delta\, i_{Lo} = \frac{v_{o1,2}}{f_s L_{o1,2}}\,(1-0.5G_{oi12}) \text{ Buck} \\ \Delta\, i_{Lin} = \frac{0.5v_{o1,2}}{f_s L_{in}};\ \Delta\, i_{Lo} = \frac{v_{o1,2}}{f_s L_{o1,2}}\,\frac{G_{oi12}-0.5}{G_{oi12}^2} \text{ Boost} \end{cases} . \quad (15)$$

The normalized inductor current ripples $\Delta i_L/k$ ($k=\frac{v_{o1,2}}{f_s L_{in}}$) of the proposed converter [from (12)] and four-leg converter

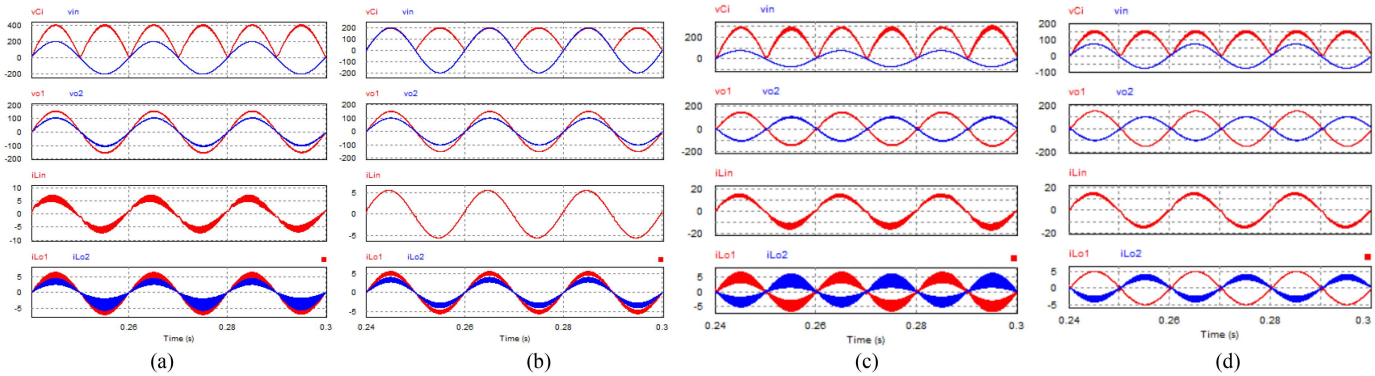



Fig. 10. (a) and (b) Simulation waveforms for step-down operation with two noninverting outputs: (a) Converter in [24]. (b) Proposed converter. (c) and (d) Simulation waveforms for boost operation with noninverting output-1 and inverting output-2. (c) Converter in [24]. (d) Proposed converter.

[24] are plotted in Fig. 9(b). It is observed that the input and output inductor current ripples of the proposed converter are much lower than those of the four-leg converter for both buck and boost operations. Moreover, the input and output inductor current ripples of the proposed converter are negligible for buck and boost operations, respectively, due to the absence of high-frequency switching; while the same inductors of the four-leg converter have much higher ripples. Therefore, the proposed converter can reduce its inductance requirement. Additionally, the volume of the inductors is directly proportional to their stored energy $W_L$ ( $= \frac{1}{2}\ LI_L^2$), where $L$ is the inductance, and $I_L$ is the peak inductor current. The peak currents are the same for both converters. However, the proposed converter uses much smaller inductance values [see Fig. 9(b)], leading to a significant reduction in inductor requirement and volume.

The capacitor $C_i$ voltage ripples $\Delta v_{Ci}$ of the proposed and counterpart converter are provided as follows:

$$\left\{\Delta\, v_{Ci} = \frac{i_o}{f_s C_i}\ \frac{G_{oi12}{}^{+1}}{2}\ [24]\ . \right. \tag{16}$$

The capacitor $C_i$ voltage ripples $\Delta v_{Ci}/k$ ($k = \frac{i_o}{f_s C_i}$ ) of the proposed converter [from (13)] and counterpart converter [24] are plotted in Fig. 9(c). It is observed that the proposed converter has much lower capacitor voltage ripple, and therefore, much lower capacitor $C_i$ requirement. Moreover, it would have much lower stored energy due to the smaller capacitor value and its voltage stress, thus reducing the capacitor requirement, volume, and cost.

### C. Simulation Results and Comparisons

Fig. 10(a) and (b) depict the simulated waveforms of the input voltage $v_{\text{in}}$, output voltages $v_{o1}, v_{o2}$, capacitor $C_i$ voltage $v_{Ci}$, input inductor current $i_{L\text{in}}$ and output inductor currents $i_{Lo1}, i_{Lo2}$ of the conventional converter [24] and proposed converter, respectively. Two noninverting decoupled outputs of $v_{o1} = 150\ V_{\text{peak}}$ and $v_{o2} = 100\ V_{\text{peak}}$ are produced for buck operation when input line voltage $v_{\text{in}}$ is 200 $V_{\text{peak}}$. Notably, the capacitor voltage $v_{Ci}$ of topology in [24] is raised to a much higher value of 400 $V_{\text{peak}}$, which represents the minimum achievable voltage across capacitor $C_i$. Consequently, the switching devices in [24] would also experience the same voltage stress of 400 $V_{\text{peak}}$, significantly increasing their voltage rating. In the proposed converter, the capacitor $C_i$ voltage is only 200 $V_{\text{peak}}$, which is half of the voltage stress than [24]. Therefore, the switches in the proposed converter also experience only half of the voltage stresses compared to those in [24]. Moreover, the input and output inductor current ripples ($\Delta i_{L\text{in}}, \Delta i_{Lo1}$, and $\Delta i_{Lo2}$) of the proposed converter are much smaller.

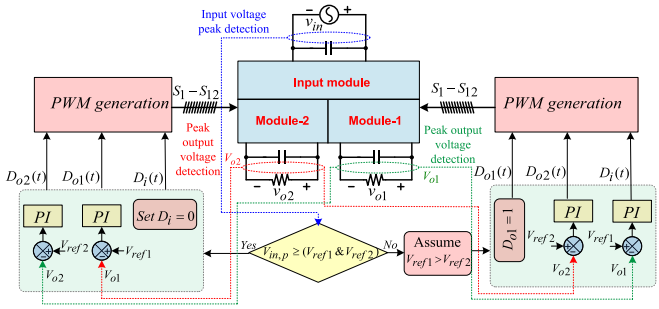



Fig. 11. Block diagram of the close loop control of the proposed dual-output converter.

Fig. 10(c) and (d) illustrates the same simulated waveforms of $v_{\text{in}}, v_{o1}, v_{o2}, v_{Ci}, i_{L\text{in}}, i_{Lo1}$, and $i_{Lo2}$ for the converter in [24] and the proposed converter, respectively, to generate noninverting output-1 and inverting output-2. Output-1 and output-2 have peak values of $v_{o1} = 150\ V_{\text{peak}}$ and $v_{o1} = 100\ V_{\text{peak}}$, respectively, achieved by boosting an input voltage $v_{\text{in}}$ of 75 $V_{\text{peak}}$. Notably, the capacitor $C_i$ voltage of the proposed converter is only 150 $V_{\text{peak}}$ compared to 300 $V_{\text{peak}}$ for [24]. Once again, the capacitor $C_i$ and switch voltage stresses are reduced for the proposed converter. Furthermore, the input inductor and output inductor current ripples of the proposed converter are also significantly lower compared to those in [24].

The numerical values of capacitor $C_i$ voltage, inductor current ripples, and THDs of input and outputs for simulation results of Fig. 11(a), (b), (c), and (d) are compared in Table II, for both buck and boost operations. All numerical values show the superiority of the proposed converter in terms of its lower component voltage stresses, current ripples, less THD and improved power quality of its input and outputs.

TABLE II
COMPARISON OF VOLTAGE STRESSES, CURRENT RIPPLES AND THDS OF TWO CONVERTERS

| Buck operation [see Fig. 10(a) and (b)] | | | | | | | |
|---|---|---|---|---|---|---|---|
| Parameter | $v_{Ci}$ | $\Delta i_{Lin}$ | $\Delta i_{Lo1}$ | $\Delta i_{Lo1}$ | $THDi_{in}$ | $THDv_{o1}$ | $THDv_{o2}$ |
| Zhu et al. [24] | 400 V | 2.44 A | 2.23 A | 1.75 A | 12.5 % | 1.65 % | 2.47 % |
| Proposed | 200 V | 0 A | 0.93 A | 1.25 A | 1.1 % | 0.57 % | 1.01 % |
| Boost operation [see Fig. 10(c) and (d)] | | | | | | | |
| Zhu et al. [24] | 300 V | 2.63 A | 3.61 A | 3.2 A | 9.29 % | 2.8 % | 3.56 % |
| Proposed | 150 V | 1.83 A | 0 A | 1.65 A | 4.45 % | 2.15 % | 2.49 % |

TABLE III
COMPONENT SPECIFICATIONS AND EXPERIMENTAL CONDITIONS

| | | |
|---|---|---|
| Input supply voltage ( $v_{in}$ ) | Buck | 200 $V_{peak}$ |
| | Boost | 75 $V_{peak}$ |
| Output ac voltages ( $v_{o1}, v_{o2}$ ) | | 100 $V_{peak}$ or 150 $V_{peak}$ |
| Switch operating frequency ( $f_s$ ) | | 25 kHz |
| Switching devices ($S_1 - S_{12}$) | | 47N60CFD |
| Inductors ($L_{in}, L_{o1}, L_{o2}$) | | 500 µH, 600 µH, 600 µH |
| Capacitors ( $C_i, C_{o1}, C_{o2}$ ) | | (2.2 µF , 2.2 µF, 2.2 µF) |

### D. Close-Loop Control of the Proposed Converter

The control block diagram is shown in Fig. 11. The input voltage $v_{\text{in}}$ and output voltages ($v_{o1}$ and $v_{o2}$) are sensed, and their peak values ($V_{\text{in}}, V_{o1}$, and $V_{o2}$) are detected using a peak voltage detector [25], through the following relation:

$$\sqrt{V_{\text{in}/o}^2 \text{Sin}^2(\omega t) + V_{\text{in}/o}^2 \text{Cos}^2(\omega t)} = V_{\text{in}/o}. \quad (17)$$

The converter operates in two modes depending on the value of the input voltage compared to the output voltages.

*Mode-1 [$V_{\text{in}} > (V_{o1}$ and $V_{o2})$]:* When the peak input voltage $V_{\text{in}}$ is higher than both peak output voltages $V_{o1}$and $V_{o2}$, the buck mode is activated. In this mode, the duty ratio ($D_i$) of the input stage is set to 0, and the input switches are modulated at line frequency, providing $v_{Ci} = v_{\text{in}}$ . The peak detected values of the output voltages ($V_{o1}$and $V_{o2}$) are compared with their respective reference values ($V_{\text{ref1}}$and $V_{\text{ref2}}$), and the error signals are fed to two PI controllers, generating the dynamic control duty ratios ($D_{o1}(t)$ and $D_{o2}(t)$).

*Mode-2 [$V_{\text{in}} < (V_{o1}$ or/and $V_{o2})$]:* In this case, the peak input voltage $V_{\text{in}}$ is lower than at least one of the output voltages ($V_{o1}$or $V_{o2}$) or both. The duty ratio of the one of the output modules is set to 1. For instance, when $V_{o1} > V_{o2}$, the duty ratio $D_{o1}$ is set to 1, and $v_{Ci} = v_{o1}$ . The peak output voltage $V_{o1}$ is then compared with $V_{\text{ref1}}$, and the error signal is fed to a PI controller to adjust the duty ratio $D_i$ (instead of $D_{o1}$) and regulate $V_{o1}$ to the desired value. Additionally, the duty ratio $D_{o1}$ for output module-2 is generated by comparing $V_{o2}$ with $V_{\text{ref2}}$ and feeding the error signal to the PI controller. This way, the voltage $v_{Ci}$ is only raised to the maximum required output voltage ($V_{o1}$ in this case), keeping the voltage stresses on the switching devices to a minimum.

## V. EXPERIMENTAL RESULTS

To validate the theoretical analysis, we constructed a hardware prototype with specifications outlined in Table III. Figs. 12 and 13 exhibit the experimental outcomes for buck operation, aiming to produce $v_{o1} = 150\ V_{\text{peak}}$ and $v_{o2} = 100\ V_{\text{peak}}$ from a high input voltage $v_{\text{in}}$ of 200 $V_{\text{peak}}$. In this operation, both outputs are noninverting. The boost duty ratio $D_i$ is set to 0, and buck module duty ratios $D_{o1}, D_{o2}$ are fixed at 0.75 and 0.5, respectively. Fig. 12(a) illustrates the waveforms of input voltage $v_{\text{in}}$, capacitor $C_i$ voltage, output-1 voltage $v_{o1}$, and output-2 voltage $v_{o2}$ when both outs are noninverting. Fig. 12(b) shows the same waveforms when output-1 is noninverting but output-2 is inverting. As observed, the voltage across capacitor $C_i$ is clamped to $v_{\text{in}}$ with a peak value of 200 $V_{\text{peak}}$. Fig. 13 displays the waveforms of input (inductor) current, output-1 inductor current and voltage stresses of switches $S_7$ and $S_{11}$.

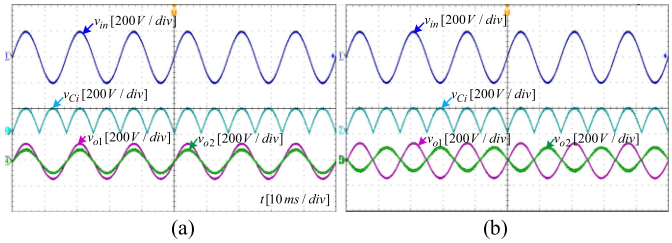



Fig. 12. Experimental results for buck operation with two different output voltage magnitudes. (a) Both outputs are noninverting. (b) Output-1 is noninverting and output-2 is inverting.

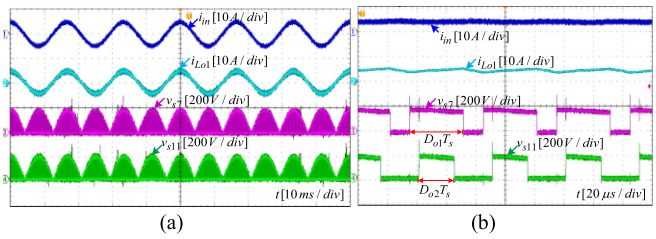



Fig. 13. (a) Experimental results of input and output-1 inductor currents and switch voltage stresses. (b) Zoom-in waveforms of Fig. 12(a).

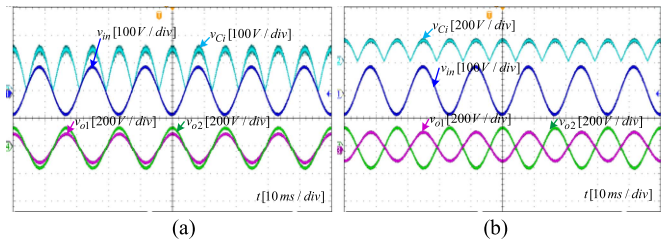



Fig. 14. Experimental results for boost operation with two different output voltage magnitudes. (a) Both outputs are inverting. (b) Output-1 is noninverting and output-2 is inverting.

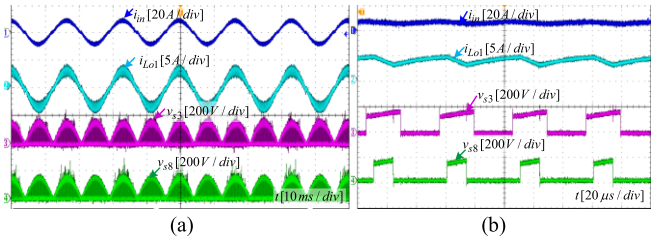



Fig. 15. (a) Experimental results of input and output-1 inductor currents and switch voltage stresses. (b) Zoom-in waveforms of Fig. 14(a).

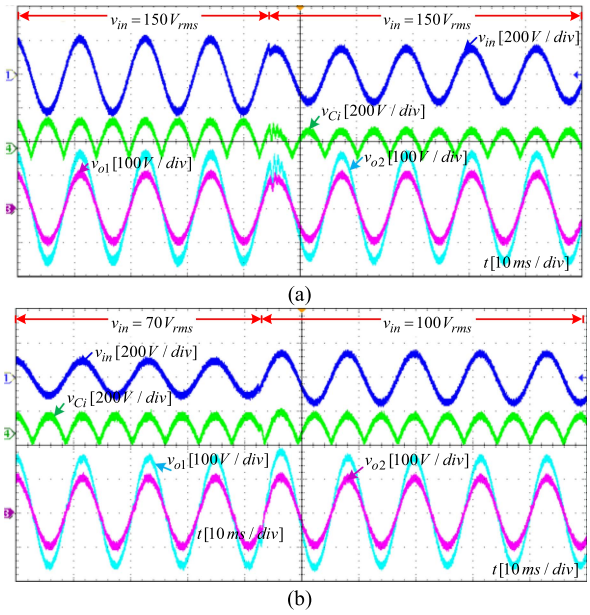



Fig. 16. (a) Experimental results of input and output-1 inductor currents and switch voltage stresses. (b) Zoom-in waveforms of Fig. 14(a).

Figs. 14 and 15 depict the experimental outcomes for boost operation to generate $v_{o1} = 100\, v_{\text{peak}}$ and $v_{o2} = 150\, v_{\text{peak}}$ from a low input voltage $v_{\text{in}}$ of 75 $v_{\text{peak}}$. The boost duty ratio $D_i$ is set to 0.5 to elevate $v_{Ci}$ to 150 $V_{\text{peak}}$, while the buck module duty ratios $D_{o1}$ and $D_{o2}$are set at 0.67 and 1, respectively. In Fig. 14(a), the measured waveforms include the input voltage $v_{\text{in}}$, output-1 voltage $v_{o1}$, output-2 voltage $v_{o2}$, and capacitor $C_i$ voltage when both outputs are inverting. Fig. 14(b) illustrates the same waveforms when output-1 become noninverting and output-2 is inverting. Fig. 15 displays the waveforms of input (inductor) current $i_{L\text{in}}$, output-1 inductor current $i_{Lo}$ and voltage stresses of switches $S_3$ and $S_8$.

To demonstrate the effectiveness of the developed control (see Fig. 10), transient experimental results of the input voltage $v_{\text{in}}$, capacitor $C_i$ voltage $v_{Ci}$, and output voltages ($v_{o1}$, $v_{o2}$) are shown in Fig. 16. Fig. 16(a) presents the waveforms of $v_{\text{in}}$, $v_{Ci}$, $v_{o1}$, and $v_{o2}$ when $v_{\text{in}}$ drops from 150 $V_{\text{rms}}$ to 110 $V_{\text{rms}}$. Whereas, output voltages $v_{o1}$ and $v_{o2}$ are regulated at 70 $V_{\text{rms}}$ and 110 $V_{\text{rms}}$, respectively. In this case, the input boost stage duty ratio $D_b$ is set to 0, and the rectified input voltage appear across $C_i$, $v_{Ci} = |v_{\text{in}}|$. Meanwhile, $v_{o1}$ and $v_{o2}$ are maintained at their desired values of 70 $V_{\text{rms}}$ and 110 $V_{\text{rms}}$, respectively, by dynamically adjusting the duty ratios $D_{o1}(t)$ and $D_{o2}(t)$. Fig. 16(b) illustrates the waveforms of $v_{in}$, $v_{Ci}$, $v_{o1}$, and $v_{o2}$ when $v_{o1} = 110\ V_{rms}$ and $v_{o2} = 70\ V_{\text{rms}}$, as the input voltage $v_{\text{in}}$ is stepped up from 70 $V_{\text{rms}}$ to 100 $V_{\text{rms}}$. In this scenario, duty ratio $D_{o1}$ is set at 1, and $v_{o1}$ is realized by simply unfolding of the capacitor $C_i$ voltage, $v_{Ci} = |\, v_{o1}|$. The boost duty ratio $D_b(t)$ is dynamically controlled to regulate $v_{o1} = v_{Ci} = 110\ V_{\text{rms}}$, while buck duty ratio $D_{o2}(t)$ is also dynamically adjusted to maintain $v_{o2}$ at 70 $V_{\text{rms}}$.

Fig. 17 shows the measured THDs of the input current (THD$i_{\text{in}}$) and output voltage (THD$v_o$) for a wide input voltage range, $V_{\text{in}} = 75 \sim 200\ V_{\text{peak}}$, with a fixed output voltage of

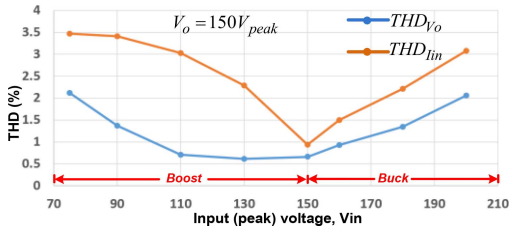



Fig. 17. Measured total harmonic distortion (THD) of the proposed converter.

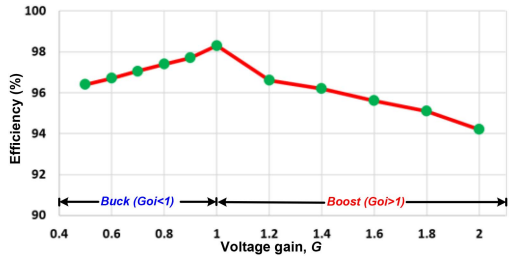



Fig. 18. Variations of power conversion efficiency versus voltage gain.

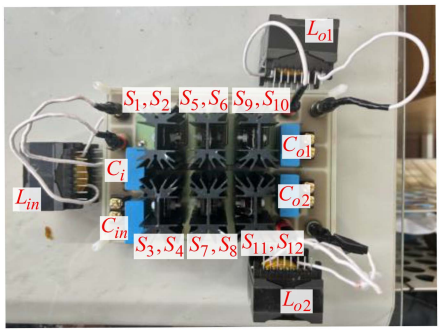



Fig. 19. Photo of the hardware prototype.

$V_o = 150\ V_{\text{peak}}$. The THD is minimized at $V_{\text{in}} = 150\ V_{\text{peak}}$ (when $V_{\text{in}} = V_o$), as there is no high-frequency switching, resulting in negligible current ripple. THD increases as $V_{\text{in}}$ deviates from $V_o$ in both buck and boost operation. Overall, the output voltage THD remains below 2.5%, and the input current THD is limited to within 3.5%.

Fig. 18 shows the measured power conversion efficiency of the proposed converter for both buck and boost operations with different voltage gains (and input voltages) when $v_o = 100\ V_{\text{peak}}$. As observed, efficiency is maximum at unity gain ($v_{\text{in}} = v_o = 100\ V_{\text{peak}}$) due to the absence of high-frequency switching and related loss. Efficiency decreases as voltage gain deviates from unity (with increase in different between input and output voltages). Fig. 19 shows the hardware prototype of the proposed converter. The experimental results confirm the advantages of the proposed converter.

## VI. Conclusion

This article presents a single-input and dual-output bipolar buck-boost ac–ac converter along with its modulation strategies. The two outputs of the proposed converter are fully decoupled, allowing for independent adjustment of magnitudes and polarities relative to each other and the input voltage. Key advantages

of the proposed converter include the use of unidirectional switching devices, eliminating commutation issues, as well as continuous input and output currents, bidirectional operation, and support for nonunity power factor loads. Comprehensive comparisons with recently developed solutions demonstrate that the proposed converter offers more flexible operation across wider ranges, with lower component voltage stresses, reduced current and voltage ripples, and improved input and output power quality. Theoretical claims are supported by detailed simulation and experimental results. The proposed converter is well-suited for implementing flexible ac-link converters with decoupled control of three-phase amplitudes and phases in distributed networks, without relying on conventional back-to-back ac–dc–ac converters with enormous and less reliable dc-link capacitors.

## REFERENCES


[1] C. A. dos Santos, L. C. dos Santos Mazza, F. L. Tofoli, D. de Souza Oliveira Junior, P. P. Praça, and F. L. M. Antunes, "Four-port, single-stage, multidirectional AC–AC converter for solid-state transformer applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4596–4606, May 2022.

[2] S. Kim, H. Kim, and H. Cha, "Dynamic voltage restorer using switching cell structured multilevel AC–AC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8406–8418, Nov. 2017.

[3] A. E. L. da Costa, C. B. Jacobina, N. Rocha, E. R. C. da Silva, and A. V. d. M. Lacerda Filho, "A single-phase AC–DC–AC unidirectional three-leg converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3876–3886, May 2021.

[4] F. Liu, X. Ruan, X. Huang, Y. Qiu, and Y. Jiang, "Control scheme for reducing second harmonic current in AC–DC–AC converter system," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2593–2605, Mar. 2022.

[5] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative evaluation of three-phase AC–AC matrix converter and voltage DC-link back-to-back converter systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4487–4510, Dec. 2012.

[6] M. Schramm Dall'Asta, I. Barbi, and T. B. Lazzarin, "AC–AC hybrid boost switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13115–13125, Dec. 2020.

[7] H. F. Ahmed, M. S. E. Moursi, B. Zahawi, K. A. Hosani, and A. A. Khan, "Switching-cell buck–boost AC–AC converter with common-ground and noninverting/inverting operations," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13944–13957, Dec. 2021.

[8] F. Z. Peng, L. Chen, and F. Zhang, "Simple topologies of PWM AC-AC converters," *IEEE Power Electron. Lett.*, vol. 1, no. 1, pp. 10–13, Mar. 2003.

[9] J.-C. Wu, H.-L. Jou, K.-D. Wu, and S.-J. Jan, "Three-arm AC automatic voltage regulator," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 567–575, Feb. 2011.

[10] J. Kaniewski, Z. Fedyczak, and G. Benysek, "AC voltage sag/swell compensator based on three-phase hybrid transformer with buck-boost matrix-reactance chopper," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3835–3846, Aug. 2014.

[11] F. Xu Peng, Q. Zhao Ming, and P. Fang Zheng, "Single-phase Z-source PWM AC-AC converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 121–124, Dec. 2005.

[12] P. Li and Y. Hu, "Unified non-inverting and inverting PWM AC-AC converter with versatile modes of operation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1137–1147, Feb. 2017.

[13] H. F. Ahmed, M. S. E. Mousri, H. Cha, K. H. A. Hosaini, and B. Zahawi, "A reliable single-phase bipolar buck-boost direct PWM AC-AC converter with continuous input/output currents," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10253–10265, Dec. 2020.

[14] A. A. Khan, H. Cha, and H. F. Ahmed, "High efficiency single-phase AC-AC converters without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5655–5665, Aug. 2016.

[15] U. A. Khan, A. A. Khan, H. Cha, H. Kim, J. Kim, and J. Baek, "Dual buck AC–AC converter with inverting and non-inverting operations," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9432–9443, Nov. 2018.

[16] C. Liu et al., "Novel bipolar-type direct AC-AC converter topology based on non-differential AC choppers," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9585–9599, Oct. 2019.

[17] Y. Wang et al., "An improved bipolar-type AC-AC converter topology based on non-differential dual-buck PWM AC choppers," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9585–9599, Oct. 2019.

[18] H. F. Ahmed, C. H. Chung, A. A. Khan, Z. Aleem, F. Akbar, and O. Alzaabi, "Non-differential AC choppers based identical bipolar buck– boost AC-AC converter without commutation issue," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4988–4999, Apr. 2023.

[19] D. M. Divan and J. Sastry, "Voltage synthesis using dual virtual quadrature sources—A new concept in AC power conversion," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3004–3013, Nov. 2008.

[20] S. Subramanian and M. K. Mishra, "Interphase AC–AC topology for voltage sag supporter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 514–518, Feb. 2010.

[21] S. Jothibasu and M. K. Mishra, "A control scheme for storageless DVR based on characterization of voltage sags," *IEEE Trans. Power Del.*, vol. 29, no. 5, pp. 2261–2269, Oct. 2014.

[22] S. Jothibasu and M. K. Mishra, "An improved direct AC–AC converter for voltage sag mitigation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 21–29, Jan. 2015.

[23] B. Zhu et al., "Line-frequency-isolation flexible AC-link converter based on direct AC-AC choppers," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4195–4210, Apr. 2022.

[24] J. Zhu, Q. Wang, T. Zhang, and T. Wei, "Topology and corresponding modulation strategy of AC–AC converters with multiple decoupled outputs," *IEEE Trans. Ind. Electron.*, vol. 71, no. 10, pp. 12213–12222, Oct. 2024, doi: 10.1109/TIE.2024.3352161.

[25] B. H. Kwon, G. Y. Jeong, S. H. Han, and D. H. Lee, "Novel line conditioner with voltage up/down capability," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 1110–1119, Oct. 2002.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