A Single-Switch ZVS High Step-Up DC–DC Converter With Stacked Voltage Multiplier Cell

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***Abstract*—This article proposes a new single-switch high step-up dc–dc converter with soft-switching characteristics in renewable energy systems. The converter consists of a Sepic-based network integrating a build-in transformer and a voltage multiplier cell (VMC) stacked on the output. It achieves ZVS turn-ON for the switch in a certain load range by designing proper components' parameters without adding any additional devices. In addition, the converter has a simple structure with a small number of components, which contributes to the power density and efficiency. Because of the three-winding build-in transformer and stacked VMC, the voltage gain is increased, the voltage stress on the output capacitors is reduced, and the converter is more flexible. Furthermore, all diodes achieve ZCS turn-OFF, which improves the efficiency. A resonant operation reduces the turn-OFF current, which in turn reduces the turn-OFF loss of the switch. The steady-state operation principle, soft-switching conditions, and comparisons have been analyzed in detail. Then, the properties of the converter are verified by designing a 500 W prototype in the laboratory. The peak efficiency reaches 95.44% at 300 W and the efficiency at a rated power is 94.16%. The typical experimental waveforms of the proposed converter agree well with the theoretical analysis.**

***Index Terms*—Build-in transformer, low voltage stress, single-switch, soft-switching, step-up DC–DC converter.**

I. Introduction

THE global transition towards renewable energy sources, such as photovoltaic (PV) systems and fuel cells, has necessitated the development of efficient power conversion technologies. High step-up dc–dc converters are pivotal in this context, as they boost the low voltage output from renewable energy sources to higher dc voltage levels suitable for grid integration and other high voltage applications. Achieving high reliability, high efficiency, high voltage gain, and low electromagnetic interference are critical requirements for these converters, prompting continuous research into innovative topologies [1], [2].

The conventional dc–dc boost converter is unable to support high-voltage gain PV applications because it can only achieve high voltage gain with an extreme duty cycle that causes high voltage stress on the power device and increases the power losses [3], [4]. Researchers have combined various voltage multiplier techniques, such as switched capacitors, switched inductors, and cascading techniques, with conventional boost converters to increase the voltage gain [5]. Due to the high number of components used in the voltage multiplier cell (VMC) [6], [7], it requires more than one VMCs in higher voltage gain applications. As a result, the cost as well as the size of the converter will increase, limiting its application in ultrahigh voltage gain applications. To address this problem, the coupled inductor (CI)/build-in transformer (BIT) voltage multiplier technique has been proposed. The voltage gain can be flexibly adjusted by regulating the turns ratio of the CI/BIT without adding any other components [8], [9], [10], [11], [12]. Simultaneous use of coupled inductors and transformers can further increase the voltage gain and design freedom of the converter [13], [14], however, the increase in magnetic components will bring about an increase in the size of the converter. In conclusion, magnetic coupling technology can realize high voltage gain with simple structure and small size.

Soft-switching technique is highly effective in improving the converter efficiency as well as the electromagnetic environment. In recent years, many high step-up dc–dc converters with soft-switching characteristics have been presented. Most of these converters utilize the leakage inductance of magnetic elements or use auxiliary resonant circuits to achieve soft switching condition [15], [16], [17], [18], [19]. Poorali and Adib [20] and Ding et al. [21] proposed some soft-switching high voltage gain dc–dc converters based on Quasi-Z-Source network. Although these converters can provide a high voltage gain and soft-switching conditions, the current stresses of the switches are usually high. Moreover, these converters require two switches to realize soft-switching by setting the dead time, thus, there is some attenuation to the voltage gain and complexity of control and drive circuit.

Single-switch high step-up dc–dc converters of the VMCs cascade type and VMCs stack type have received increasing attention in recent years due to their high efficiency [22]. Most of these VMCs integrate coupled inductors to increase the voltage gain of the converter. Some researchers have combined a modified Sepic converter with coupled inductor VMCs to obtain Sepic-integrated coupled inductor boost converters [23], [24], [25], [26], [27], [28], [29]. These converters can achieve ZCS turn-ON transition for the switch because of the leakage inductance. In addition, the resonant cavity circuit formed by

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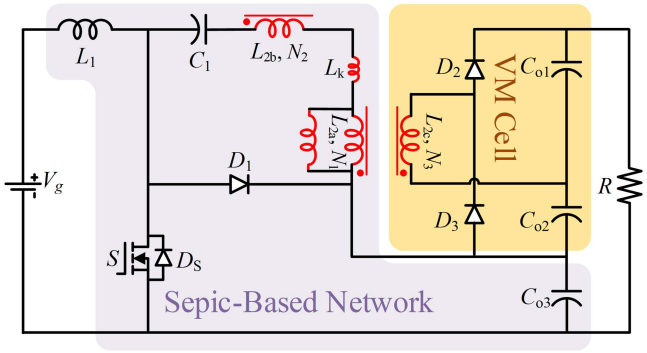


Fig. 1. Proposed output stacked single-switch high step-up DC–DC converter.

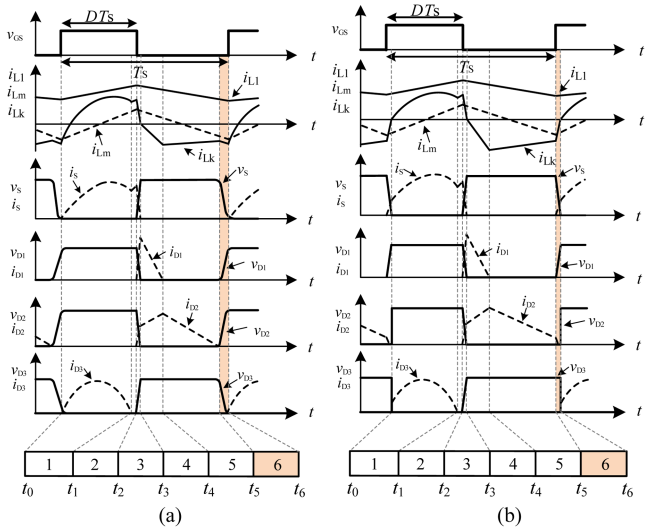


Fig. 2. Typical waveforms of converter operation. (a) Waveforms in ZVS-ON condition. (b) Waveforms in ZCS-ON condition.

the leakage inductance, a resonant capacitor, and a clamping capacitor provides a quasi-resonant (QR) operation. However, for MOSFETS, the ZCS turn-ON is far less advantageous than ZVS turn-ON. In [30], [31], [32], and [33], the step-up dc–dc converters integrated with three-winding coupled inductor are presented. These converters possess a more flexible adjustment of voltage gain and voltage stresses. However, the power switch in these converters suffers high switching losses.

This article proposes a novel single-switch high step-up dc–dc converter based on a Sepic network integrating a three-winding build-in transformer. It inherits the properties of input current continuity, passive clamping, and voltage boost of Sepic network. A three-winding build-in transformer and stacked VMC used to increase the voltage gain makes the converter design more flexible and the low number of components, which make the converter simple, stable, and reliable. A resonant tank created by the leakage inductance and capacitors helps to decrease the switching loss and improve the EMC environment [34], [35]. Moreover, the converter uses the build-in transformer and parasitic capacitors to achieve ZVS-ON of the switch, and makes full use of the parasitic parameters of the converter without adding extra components. Also, the structure of convertor leads to ZCS turn OFF for all diodes, which reduces the power losses of the converter.

The rest of this article is organized as follows. Section II analyses the operation principle, the steady-state characteristics, and the soft-switching principle of the converter. Parameter design and efficiency estimation are given in Section III. Section IV compares the performance of the proposed converter with the previous published converters. The experimental setup and results are given in Section V. Finally, Section VI concludes this article.

II. Structure and Converter Analysis

A. Proposed Converter

The proposed single-switch high step-up dc–dc converter is shown in Fig. 1, which consists of a Sepic-based network and a VMC stacked on the output. The structure is simple with small number of components. The Sepic-based network inherently has continuous input current and switch-clamping properties. The three-winding build-in transformer integrated into the converter not only has a function of voltage enhancement and makes the converter design more flexible but also provides a condition of soft switching for the switch and diodes. In addition, there is no dc component in magnetizing current of the build-in transformer, which makes the ferrite core less susceptible to saturation. The output-side stacked construction also reduces the voltage stress on the output capacitors and diodes.

Assuming that the proposed converter operates in continuous conduction mode (CCM) of the input inductor current. Switch S is N-MOSFET considering its body diode D_s and parasitic capacitances C_s. The inductor and the capacitors are linear, time invariant, and frequency independent. All voltages on capacitors are considered to be constant in a switching period.

The proposed converter operates either in zero voltage turn-ON (ZVS-ON) transition or in zero current turn-ON (ZCS-ON) condition for the switch S, which depends on the converter parameters and load. Fig. 2(a) shows the typical waveforms of the components with the switch in ZVS-ON transition and Fig. 2(b) shows the typical waveforms in ZCS-ON. There are six operating modes in a switching period, modeling the build-in transformer by a leakage inductance L_k, a magnetizing inductance L_m, and an ideal three-winding transformer with turns ratio $n_1 = N_2/N_1$ and $n_2 = N_3/N_1$, as shown in Fig. 3.

B. Operating Modes in ZVS-ON Condition

1) Mode 1[t_0-t_1]: At t_0, the power switch S begins to conduct with ZVS. During this subinterval, diodes D_1 and D_2 are OFF due to the reverse voltages applied on them, and diode D_3 is forward biased so that the voltages across the windings of build-in transformer are clamped. The inductor L_1 is charged by the voltage source V_g while capacitor C_{o3} transfers energy to capacitors C_1 and C_{o2} by means of the three-winding build-in transformer. The load R takes energy from capacitors C_{o1} and C_{o3}. In order to reduce the current amplitude when the switch is turned OFF, a resonant tank formed by the primary and secondary

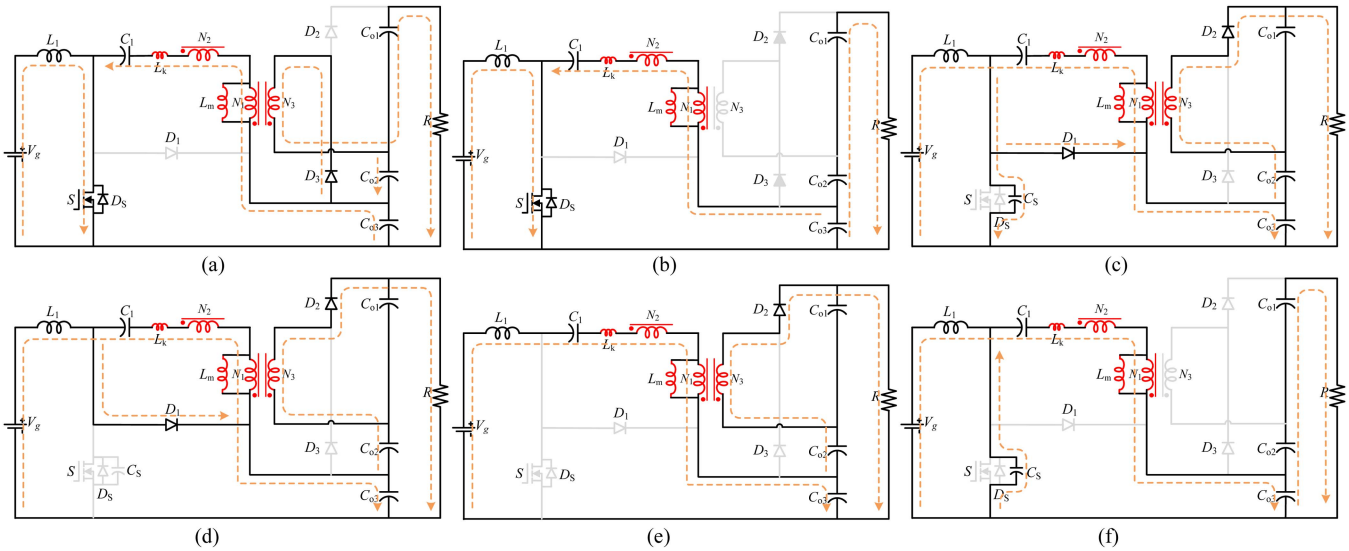


Fig. 3. Operating modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

sides of the three-winding build-in transformer, C_1, and C_{o3} is adopted.

As shown in Fig. 3(a), due to quasi-resonant characteristic, the currents of the switch S along with D_3 varies sinusoidally. This reduces the switch turn-OFF power dissipation. Moreover, the quasi-resonant operation provides a natural drop of the current through D_3 to zero at the end of this mode, which suppresses the reverse recovery loss of the diode. The resonant frequency f_R can be obtained as

$$f_R = \frac{1}{2\pi\sqrt{L_k C_{eq}}}, C_{eq} = \frac{C_1 C_{o3}}{C_1 + C_{o3}}. \tag{1}$$

The switching frequency f_s of the converter is close to the resonant frequency to ensure the quasi-resonant operation and the best state of operation for reducing the peak and turn-OFF currents of switch is that the duration of switch in ON-state equals to half cycle resonating time ($DT_s = T_R/2$). In this mode, the following voltage equations can be listed:

$$v_{L1}(t) = V_g \tag{2}$$

$$v_{C1}(t) + L_k \frac{di_{Lk}(t)}{dt} + (1-n_1) L_m \frac{di_{Lm}(t)}{dt} - v_{Co3}(t) = 0 \tag{3}$$

$$L_m \frac{di_{Lm}(t)}{dt} = \frac{1}{n_2} v_{Co2}(t). \tag{4}$$

And the current through D_3 can be derived as

$$i_{D3}(t) = \frac{(1-n_1) i_{Lk}(t) - i_{Lm}(t)}{n_2}. \tag{5}$$

2) Mode 2[t_1-t_2]: As shown in Fig. 3(b), at t_1, i_{D3} drops to zero naturally and D_3 reverse biased. During this subinterval, the voltages applied on the windings of the build-in transformer are not being clamped. The rising slope of leakage current is in line with the magnetizing inductance current, which is increasing linearly in both cases. Inductor L_1 and capacitor C_1 continuously charged by V_g and C_{o3}, respectively. Capacitors C_{o1}, C_{o2}, and C_{o3} together provide energy to the load. This mode ends when switch S is turned OFF. The current relationship in this mode can be obtained as

$$i_{Lk}(t) = \frac{i_{Lm}(t)}{1-n_1} \tag{6}$$

$$i_S(t_2) = i_{L1}(t_2) + i_{Lk}(t_2) = I_{L1(\max)} + \frac{I_{Lm(\max)}}{1-n_1} \tag{7}$$

where $I_{L1(\max)}$ and $I_{Lm(\max)}$ is the maximum value of i_{L1} and i_{Lm}.

3) Mode 3[t_2-t_3]: As shown in Fig. 3(c), this transient mode starts when switch S receives the turn OFF signal. Since the capacitor C_s decreases the variation rate of v_s, the switch S turns OFF under ZVS condition. Meanwhile, the diodes D_1 and D_2 start to conduct due to the voltage across them becoming forward. The voltages on the windings of build-in transformer are clamped by voltage of C_{o1}. This mode ends with the current i_s decreasing to zero. Equations can be obtained at the end of this mode as follows:

$$L_m \frac{di_{Lm}(t)}{dt} = -\frac{1}{n_2} v_{Co1}(t) \tag{8}$$

$$i_{D1}(t_3) \approx i_S(t_2) \tag{9}$$

$$i_{D2}(t_3) = \frac{-(1-n_1) i_{Lk}(t_3) + i_{Lm}(t_3)}{n_2} \approx \frac{I_{Lm(\max)}}{n_2}. \tag{10}$$

4) Mode 4[t_3-t_4]: As illustrated in Fig. 3(d), during this mode, diodes D_1 and D_2 are forward biased, and D_3 is still OFF. Inductor L_1 and capacitor C_1 transfer energy to capacitor C_{o1}, C_{o3}, and load through diodes D_1, D_2, and build-in transformer. At the same time, capacitor C_{o2} also releases energy to the load. The current i_{L1} decreases positively and i_{Lk} increases negatively, leading to the decrease of i_{D1} and the increase of i_{D2}. When i_{D1} drops to zero, this mode ends and diode D_1 turns OFF under ZCS condition. At t_4, the current i_{D2} reaches its maximum value and

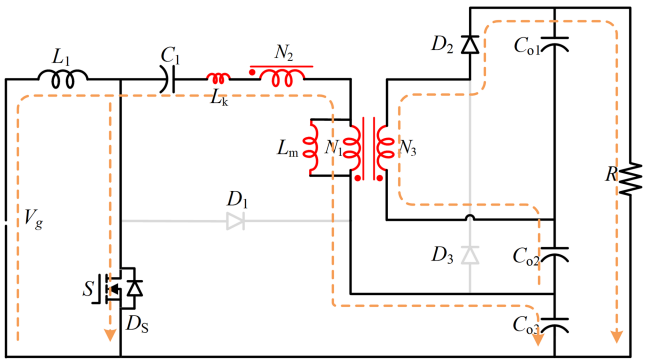


Fig. 4. Operating Mode 6 in ZCS condition.

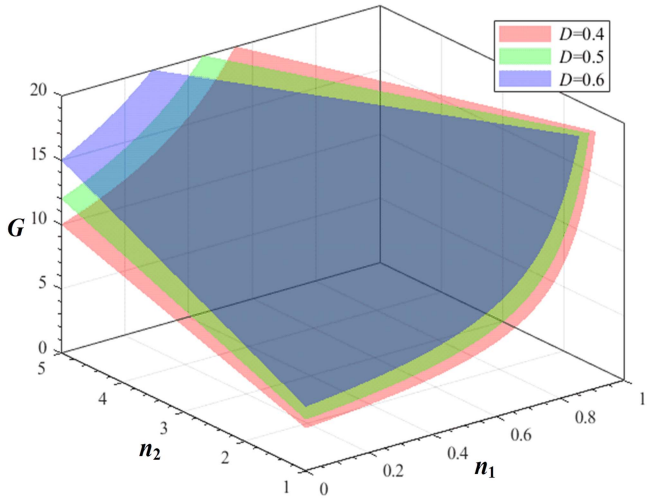


Fig. 5. Voltage gain versus turns ratio n_1 and n_2 for different duty cycles.

it can be estimated by

$$i_{D2}(t_4) = -\frac{(1-n_1)i_{Lk}(t_4) - i_{Lm}(t_4)}{n_2} = \frac{(1-n_1)i_{L1}(t_4) + i_{Lm}(t_4)}{n_2}. \quad (11)$$

And the voltage of L_1 during this mode can be expressed as

$$v_{L1}(t) = V_g - v_{Co3}(t). \quad (12)$$

5) Mode 5[t_4-t_5]: In this subinterval, diodes D_1 and D_3 are OFF, and D_2 are ON. The voltages on the windings of build-in transformer are still clamped. The energy exchange process is the same as in the previous mode. The current i_{L1} together with i_{Lk} decrease linearly because L_1 and L_k are in series during this time interval, as shown in Fig. 3(e). Thus, the current i_{D2} also decreases linearly until it reaches zero, which allows D_2 to achieve ZCS-OFF, and this mode ends.

6) Mode 6[t_5-t_6]: During this subinterval, all diodes are reverse biased, as shown in Fig. 3(f). The voltages of the windings of build-in transformer are no longer clamped. Hence, the primary and secondary sides of the three-winding build-in transformer begin to resonate with C_s. When the voltage of switch drops to zero, the switch S is turned ON, thus achieving ZVS-ON. Capacitors C_{o1} and C_{o2} discharge to the load while C_{o3} charge from i_{Lk}. The equation of v_s can be obtained as

$$v_S(t) = (V_S - V_g)\cos\omega_r(t-t_5) + V_g \quad (13)$$

where $\omega_r = \frac{1}{\sqrt{C_S L_{eq}}}$, $L_{eq} = \frac{(1-n_1)^2 L_1 L_m}{L_1 + (1-n_1)^2 L_m}$.

C. Operating Modes in ZCS-ON Condition

When the converter operates in ZCS-ON transition, only mode 6 is different, the rest are the same as the modes when the converter operates in ZVS condition.

Mode 6[t_5-t_6]*:* At t_5, the switch S receives turn-ON signal and starts to conduct in ZCS-ON condition because of the leakage inductance L_k. Meanwhile, the diode D_2 remains on and continues the current i_{D2}. The diodes D_1 and D_3 are OFF during this subinterval, as shown in Fig. 4. The value of i_{D2} at t_5 can be approximated as

$$i_{D2}(t_5) = \frac{(1-n_1)i_{L1}(t_5) + i_{Lm}(t_5)}{n_2} = \frac{(1-n_1)I_{L1(\min)} + I_{Lm(\min)}}{n_2} \quad (14)$$

where $I_{L1(\min)}$ and $I_{Lm(\min)}$ is the minimum value of i_{L1} and i_{Lm}.

At t_6, the diode D_2 achieves ZCS turn OFF and D_3 begins to conduct. The current of diode D_3 and switch S at t_6 can be approximated as

$$i_{D3}(t_6) \approx \frac{-i_{Lm}(t_6)}{n_2} \approx -\frac{I_{Lm(\min)}}{n_2} \quad (15)$$

$$i_S(t_6) \approx I_{L1(\min)}. \quad (16)$$

D. Steady State Analysis

Due to the short duration of modes 3 and 6 in a switching period, only the modes 1, 2, 4, and 5 are considered in the steady state analysis. By applying the volt-second balance law on the L_1 and L_m, the voltages of capacitors C_1, C_{o1}, C_{o2}, and C_{o3} can be derived as

$$\begin{cases} V_{C1} = \frac{D}{1-D}V_g, V_{Co1} = \frac{n_2 D}{(1-n_1)(1-D)}V_g \\ V_{Co2} = \frac{n_2}{1-n_1}V_g, V_{Co3} = \frac{1}{1-D}V_g. \end{cases} \quad (17)$$

From Fig. 3, the ideal voltage gain G of the proposed converter in CCM can be expressed as

$$G = \frac{V_o}{V_g} = \frac{V_{Co1} + V_{Co2} + V_{Co3}}{V_g} = \frac{1 - n_1 + n_2}{(1-n_1)(1-D)}. \quad (18)$$

Thus, the ideal voltage stresses across switch S and diodes are

$$V_S = V_{D1} = \frac{1-n_1}{1-n_1+n_2}V_o, V_{D2} = V_{D3} = \frac{n_2}{1-n_1+n_2}V_o. \quad (19)$$

Fig. 5 depicts the ideal voltage gain versus turns ratios n_1 and n_2 at different duty cycle. It is clear that the converter

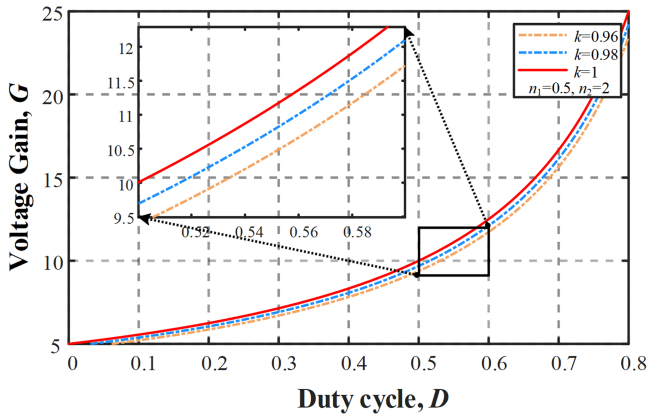


Fig. 6. Voltage gain versus duty cycle at various coupling coefficients with $n_1 = 0.5, n_2 = 2$.

achieves high voltage gain with low turns ratio for a duty cycle 0.5<D<0.6, helping to reduce the leakage inductance of the build-in transformer.

Actually, the build-in transformer has leakage inductance which has effect on the voltage gain of the proposed converter. The voltage gain considering L_k is calculated as

$$G_k = \frac{\frac{1}{k} - n_1 + n_2}{\left(\frac{1}{k} - n_1\right)(1 - D)} \tag{20}$$

where k is coupling coefficient of the build-in transformer, which is expressed as

$$k = \frac{L_m}{L_k + L_m}. \tag{21}$$

Fig. 6 shows the voltage gain versus duty cycle with different values of k. As it can be seen from Fig. 6, the effect of leakage inductance on the voltage gain is more significant as the duty cycle increases. Thus, it is necessary to reduce the leakage inductance as much as possible when designing the build-in transformer.

The average current I_g of inductor L_1 in ideal condition can be obtained by employing the law of energy conservation

$$I_g = GI_o = \frac{1 - n_1 + n_2}{(1 - n_1)(1 - D)} I_o. \tag{22}$$

Consequently, the maximum and the minimum value of i_{L1} can be calculated as

$$\begin{cases} I_{L1(\max)} = I_g + \frac{V_g D}{2L_1 f_s} = GI_o + \frac{DRI_o}{2GL_1 f_s} \\ I_{L1(\min)} = I_g - \frac{V_g D}{2L_1 f_s} = GI_o - \frac{DRI_o}{2GL_1 f_s} \end{cases} \tag{23}$$

where f_s is the switching frequency, I_o is the output current, and R is the load.

By applying the amp-second principle on the capacitors, the average currents of the diodes are derived as

$$I_{D1} = \frac{1}{1 - D} I_o, I_{D2} = \frac{1}{1 - D} I_o, I_{D3} = \frac{1}{D} I_o. \tag{24}$$

And the average value of i_{Lm} is zero, thus, the maximum and the minimum value of i_{Lm} can be calculated as

$$\begin{cases} I_{Lm(\max)} = \frac{V_g D}{2(1-n_1)L_m f_s} = \frac{DRI_o}{2(1-n_1)GL_m f_s} \\ I_{Lm(\min)} = -\frac{V_g D}{2(1-n_1)L_m f_s} = \frac{-DRI_o}{2(1-n_1)GL_m f_s}. \end{cases} \tag{25}$$

Combining (7), (9), (23), and (25), the turn-OFF current of switch S and the maximum current through diode D_1 can be estimated as

$$I_{S\_OFF} = I_{D1(\max)} = GI_o + \frac{DRI_o}{2GL_{eq} f_s}. \tag{26}$$

So, the duration of modes 3 and 4 is

$$t_4 - t_2 = \frac{2}{\left(G + \frac{DR}{2GL_{eq} f_s}\right) f_s}. \tag{27}$$

The maximum currents of diodes D_2 and D_3 at $DT_s = T_R/2$ are estimated as

$$I_{D2(\max)} = \frac{(1 - n_1)}{n_2} \left(\frac{D(1 - D - 2D_{24})R}{2(1 - D)GL_{eq} f_s} + G \right) I_o \tag{28}$$

where $D_{24} = (t_4 - t_2) f_s$

$$I_{D3(\max)} = \frac{\pi I_o}{2D}. \tag{29}$$

And the maximum current of switch S is estimated as

$$I_{S(\max)} = GI_o + \frac{n_2 \pi I_o}{2(1 - n_1)D}. \tag{30}$$

Combining (25), (28), and (29), the duration of modes 5 is calculated approximately to be

$$t_5 - t_4 = \left(\frac{2I_o}{I_{D2(\max)}} - D_{24} \right) T_s. \tag{31}$$

E. Boundary Conditions for ZVS

Whether the converter operates in ZVS-ON transition depends mainly on the condition of mode 6. When operating in the mode 6 shown in Fig. 3(f), the switch of the converter can achieve ZVS-ON. In this mode, the switch S is in OFF state and the current through tertiary winding N_3 is zero. We define this operating mode as the tertiary winding zero current mode (TW-ZCM) and its opposite as Tertiary winding continuous current mode (TW-CCM). TW-ZCM is the first necessary condition for the switch to realize ZVS-ON, at which time the parasitic capacitor C_s resonates with the primary and secondary windings of the build-in transformer. The second necessary condition is that the voltage v_s on the switch is able to drop to zero during the resonant cycle. And the last condition is that the switch S is turned ON when the v_s is zero. The conditions for the switch to fulfill ZVS-ON can be summarized as follows: 1) The current of the third winding of the build-in transformer is zero, and there is no clamping function of the output voltage. The parasitic capacitor of the switch can resonate with windings of the build-in transformer, 2) the duration of mode 6 ensures that the switch voltage v_s resonates to zero, 3) switch voltage v_s remain zero before the switch is turned-ON. Detailed descriptions of the above three conditions are given as follows.

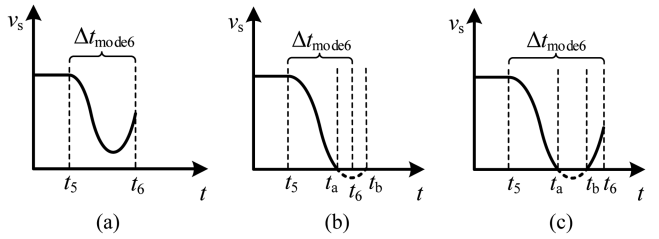


Fig. 7. Waveforms of v_s in mode 6 with different operation states. (a) $D < 0.5$. (b) $D \geq 0.5$, and $t_a - t_5 \leq \Delta t_{mode6} \leq t_b - t_5$. (c) $D \geq 0.5$, and $\Delta t_{mode6} > t_b - t_5$.

The voltage of switch during this interval is

$$v_S(t) = \frac{DV_g}{1-D}\cos\omega_r(t-t_5) + V_g. \tag{32}$$

Consequently, the necessary condition for the switch to be able to realize ZVS is that the minimum value of v_s in this mode can reach zero. It is necessary for the duty cycle D to satisfy the constraint as follows:

$$D \geq 0.5. \tag{33}$$

Fig. 7 depicts the waveforms of v_s for different operation states. In Fig. 7, t_a and t_b are the moments that make v_s equal to zero. $\Delta t_{mode6} = t_6$-t_5.is the duration of mode 6. When $D < 0.5$, the minimum value of v_s is greater than zero, which does not meet the condition of ZVS-ON. When $D \geq 0.5$, and $\Delta t_{mode6} > t_b - t_5$, the converter operates in ZCS condition. Only when $D \geq 0.5$, and $t_a - t_5 \leq \Delta t_{mode6} \leq t_b - t_5$, the converter achieves ZVS-ON transition of switch. Thus, the constraint can be derived as

$$\begin{cases} \frac{1-n_1}{n_2}\left(\frac{D(1-D-2D_{24})R}{2(1-D)GL_{eq}f_s}+G\right) > \frac{2}{1-D-\frac{f_s}{\omega_r}\arccos\frac{D-1}{D}} \\ \frac{1-n_1}{n_2}\left(\frac{D(1-D-2D_{24})R}{2(1-D)GL_{eq}f_s}+G\right) < \frac{2}{1-D-\frac{2\pi f_s}{\omega_r}+\frac{f_s}{\omega_r}\arccos\frac{D-1}{D}} \\ \frac{\pi}{2} < \arccos\frac{D-1}{D} \leq \pi. \end{cases} \tag{34}$$

According to (34), the dependence of the ZVS boundary on parameters can be depicted in Fig. 8. It is clear that the ZVS-ON of the switch can be achieved by designing the values of L_1, L_m, D, and f_s properly.

III. Parameters Design and Efficiency Analysis

A. Design Guidelines

The following quantities need to be specified before designing the parameters of the components.

1) Input voltage V_g.
2) Output voltage V_o.
3) Rated power P_o.
4) Switching frequency f_s.
5) Parasitic capacitance of the switch C_s.

The value of input inductor L_1 mainly takes into account the requirement of input current ripple. During the switch ON mode,

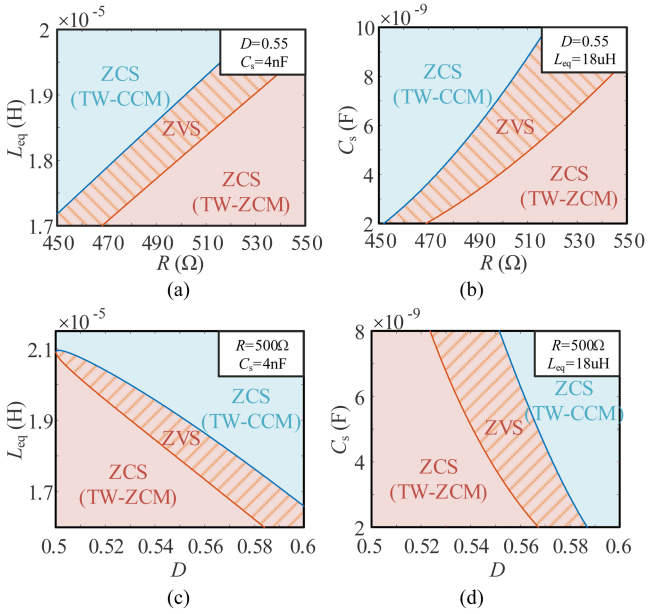


Fig. 8. Dependence of the ZVS boundary on parameters ($n_1 = 0.5$, $n_2 = 2$, $f_s = 50$ kHz). (a) L_{eq} versus R. (b) C_s versus R. (c) L_{eq} versus D. (d) C_s versus D.

the inductance can be calculated by

$$L_1 = \frac{V_g D}{\Delta I_{L1} f_s} = \frac{DR}{r_{L1} G^2 f_s} \tag{35}$$

where r_{L1} is ripple factor of the input current. At rated power generally take the value of 0.2–0.25.

The turns ratio n_1 and n_2 of the three-winding build-in transformer are determined by compromising leakage inductance and voltage gain. The magnetizing inductance is determined after choosing an operating point where the switch of the converter can achieve ZVS-ON. The selection of this operating point is given by (34) and Fig. 8. The value of the magnetizing inductance L_m can be obtained as

$$L_m = \frac{L_1 L_{eq}}{(1-n_1)^2(L_1 - L_{eq})}. \tag{36}$$

Note that the value of the magnetizing inductance should not be too small to avoid saturation of the core. The core size can be selected by AP method

$$\mathrm{AP} = A_e A_w = \frac{V_{Lm(\mathrm{on})} I_{N1(\mathrm{rms})} D}{J K_w B_{\max} f_s} \times 10^4 \tag{37}$$

where A_e and A_w are the core cross-sectional area and core window area, respectively, which are expressed in cm^2. J is the current density expressed in A/cm^2. K_w is the winding fill factor. B_{max} is the maximum operating flux density expressed in T. $V_{Lm(on)}$ is the voltage applied on L_m during the switch is ON time and $I_{N1(rms)}$ is rms value of the current through winding N_1.

The number of turns of the windings are given by

$$N_1 = \frac{I_{Lm(\max)} L_m}{B_{\max} A_e} = \frac{D(1-D)RI_o}{2(1-n_1+n_2)B_{\max} A_e f_s} \tag{38}$$

TABLE I
DESIGN PARAMETERS OF THE PROPOSED CONVERTER

Parameter	Value
Input voltage V_g	36-48 V
Output voltage V_o	380 V
Rated power P_o	500 W
Frequency f_s	50 kHz
Inductor L_1	200 μH
Build-in transformer L_m / L_k	80 and 50 μH / 1.2 μH
Turns of windings	N_1=8, N_2=4, N_3=16
MOSFET S	IRFP4668PBF
Capacitors (C_1, C_{o1}, and C_{o2}) / C_{o3}	10 μF / 68 μF
Diodes D_1 / (D_2 and D_3)	STTH6003CW / STTH6004W

TABLE II
PARASITIC PARAMETERS OF THE PROPOSED CONVERTER

Parameter	Description
R_S	Static drain-to-source on-resistance of the MOSFET
R_{Ci}	Equivalent series resistance (ESR) of the capacitor
R_{Di}	ESR of the diode
R_{L1}	ESR of the input inductor
R_{N1}, R_{N2}, R_{N3}	ESR of the windings of build-in transformer
C_s	Equivalent drain-to- source capacitance of the MOSFET
V_{FDi}	Forward voltage drop of the diode
t_{on}, t_{off}	Turn-on and turn-off transition time of the MOSFET

$$\begin{cases} N_2 = n_1 N_1 \\ N_3 = n_2 N_1 \end{cases}. \tag{39}$$

The output capacitor C_{oi} (i = 1, 2, 3) can be calculated as follows by limiting the voltage ripple:

$$\begin{cases} C_{o1} = \dfrac{I_{Co1(on)} D}{\Delta V_{Co1} f_s} = \dfrac{1-n_1+n_2}{r_{Co1} n_2 f_s R} \\ C_{o2} = \dfrac{I_{Co2(on)} D}{\Delta V_{Co2} f_s} = \dfrac{1-n_1+n_2}{r_{Co2} n_2 f_s R} \\ C_{o3} = \dfrac{I_{Co3(on)} D}{\Delta V_{Co3} f_s} = \dfrac{(1-n_1+n_2)(n_2+(1-n_1)D)}{r_{Co3}(1-n_1)^2 f_s R} \end{cases} \tag{40}$$

where r_{Coi} is ripple factor of the capacitor voltage, which usually is considered as 0.02–0.05.

Due to quasi-resonant characteristic, capacitor C_1 resonates with the leakage inductance, and the resonant frequency needs to be similar to the switching frequency. Thus, the capacitor C_1 can be obtained as

$$C_1 \approx \frac{1}{4\pi^2 f_s^2 L_k - \frac{1}{C_{o3}}}. \tag{41}$$

Finally, the calculated parameters of the proposed converter for experiment are listed in Table I.

B. Efficiency Estimation

The power dissipation of the proposed converter mainly consists of switch power losses, diode power losses, capacitor power losses, and magnetic power losses. The main parasitic parameters of the proposed converter are listed in the Table II.

The power losses of the proposed converter are calculated as follows when the converter operates in ZVS-ON condition.

TABLE III
VALUES OF THE PARAMETERS OF THE PROPOSED CONVERTER

Parameter	Value	PARAMETER	Value
R_S	8 (mΩ)	t_{on}, t_{off}	146, 138 (ns)
R_{Ci}	4 (mΩ)	α_L, α_T	1.29, 1.43
R_{D1}, R_{D2}/R_{D3}	8, 3.3 (mΩ)	β_L, β_T	1.78, 2.35
R_{L1}	36 (mΩ)	k_{iL}, k_{iT}	3.41, 0.04
R_{N1}, R_{N2}, R_{N3}	22, 13, 46 (mΩ)	N_L, N_T	52, 8
V_{FD1}, V_{FD2}/V_{FD3}	0.75, 0.8 (V)	A_{eL}, A_{eT}	105, 196 (mm^2)
V_L, V_T	16490, 17260 (mm^3)		

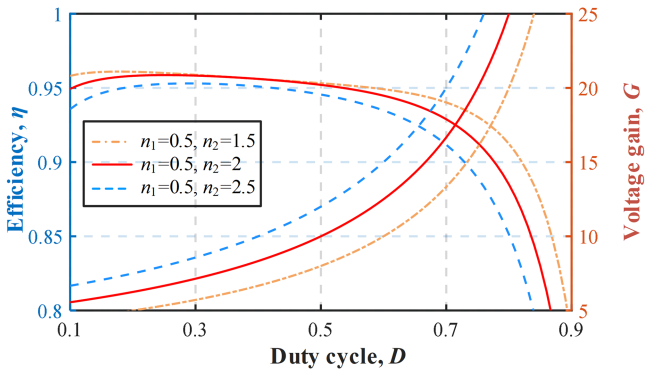


Fig. 9. Theoretical efficiency and voltage gain versus duty cycle at different turns ratio.

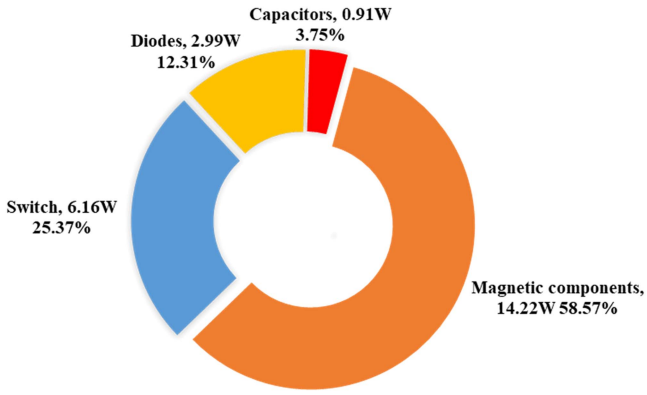


Fig. 10. Power losses distribution of the components at 500 W.

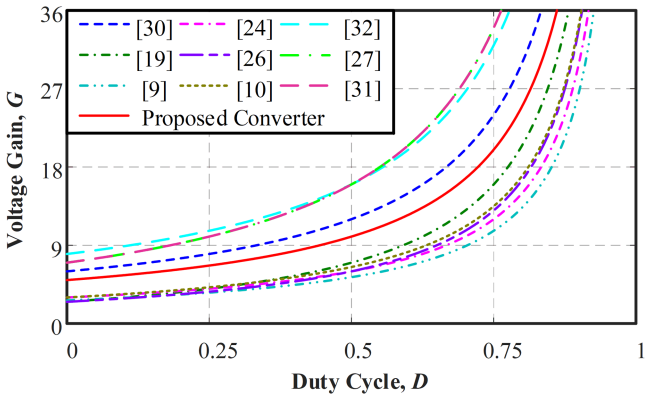


Fig. 11. Voltage gain comparison of converters given in Table IV.

TABLE IV
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER SIMILAR CONVERTERS

Converter	Voltage Gain	Voltage Stress on Main Switch	Total Voltage Stresses on Diodes	Number of Components **S/D/C/CL(BIT)+L/T**	Soft-Switching	Input Current Ripple	Common Ground
[9]	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{(n-1)V_o}{2n-1}$	$\frac{2nV_o}{2n-1}$	2/2/4/1^{2W}+1/10	ZVS	Low	Yes
[10]	$\frac{1+n_1D+n_2}{1-D}$	$\frac{V_o}{1+n_1D+n_2}$	$\frac{(1+n_1+2n_2)V_o}{1+n_1D+n_2}$	1/3/3/1^{3W}+0/8	ZCS	High	Yes
[19]	$\frac{2+n_1+n_2D}{1-D}$	$\frac{V_o}{2+n_1+n_2D}$	$\frac{(2+2n_1+n_2D)V_o}{2+n_1+n_2D}$	2/3/4/1^{3W}+0/10	ZVS	High	No
[24]	$\frac{1+2n_2-n_1}{(n_2-n_1)(1-D)}$	$\frac{(n_2-n_1)V_o}{1+2n_2-n_1}$	$2V_o$	1/4/5/1^{3W}+1/12	ZCS+QR	Low	Yes
[26]	$\frac{n_1+n_2(1+D)-D}{(n_2-1)(1-D)}$	$\frac{(n_2-1)V_o}{n_1+n_2(1+D)-D}$	$\frac{2(n_1+n_2)V_o}{n_1+n_2(1+D)-D}$	1/3/4/1^{3W}+1/10	ZCS+QR	Low	Yes
[27]	$\frac{2+D+n_2-n_1}{(1-n_1)(1-D)}$	$\frac{(1-n_1)V_o}{2+D+n_2-n_1}$	$\frac{(4+2n_2-n_1)V_o}{2+D+n_2-n_1}$	1/4/5/1^{3W}+1/12	ZCS+QR	Low	Yes
[30]	$\frac{3+2n_1+n_2}{1-D}$	$\frac{V_o}{3+2n_1+n_2}$	$\frac{(5+4n_1+2n_2)V_o}{3+2n_1+n_2}$	1/5/5/1^{3W}+0/12	ZCS	High	Yes
[31]	$\frac{1+n_1+n_2+D}{n_1(1-D)}$	$\frac{n_1V_o}{1+n_1+n_2+D}$	$\frac{(3+2n_2+n_1)V_o}{1+n_1+n_2+D}$	1/4/5/1^{3W}+1/12	ZCS	Low	Yes
[32]	$\frac{2+n_2}{(1-n_1)(1-D)}$	$\frac{V_o}{2+n_2}$	$\frac{(3+n_1+2n_2)V_o}{2+n_2}$	1/4/5/1^{3W}+1/12	ZCS	Low	Yes
Proposed Converter	$\frac{1-n_1+n_2}{(1-n_1)(1-D)}$	$\frac{(1-n_1)V_o}{1-n_1+n_2}$	$\frac{(1-n_1+2n_2)V_o}{1-n_1+n_2}$	1/3/4/1^{3W}+1/10	ZVS/ZCS +QR	Low	Yes

Notes: **S** = Switches, **D** = Diodes, **C** = Capacitors, **CL(BIT)** = Coupled Inductors (Build-in Transformers), **L** = Inductors, **T** = Total Components.

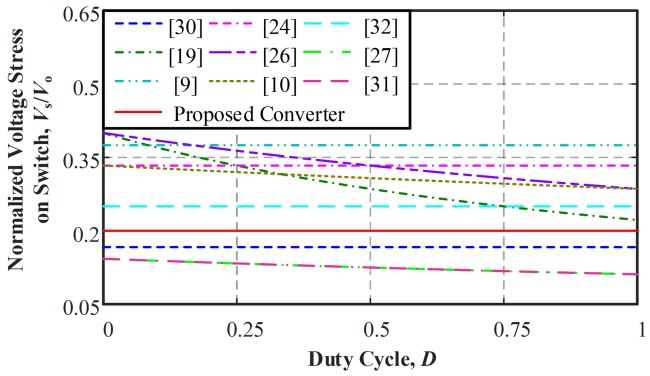


Fig. 12. Comparison of normalized voltage stress on switch.

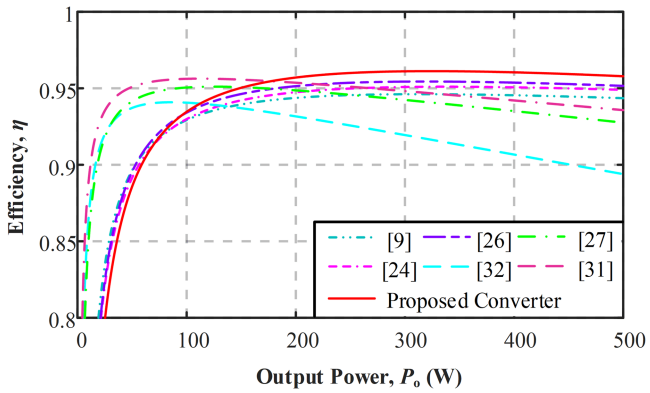


Fig. 13. Efficiency comparison under the same voltage gain ($n_1 = 0.5$, $n_2 = 2$).

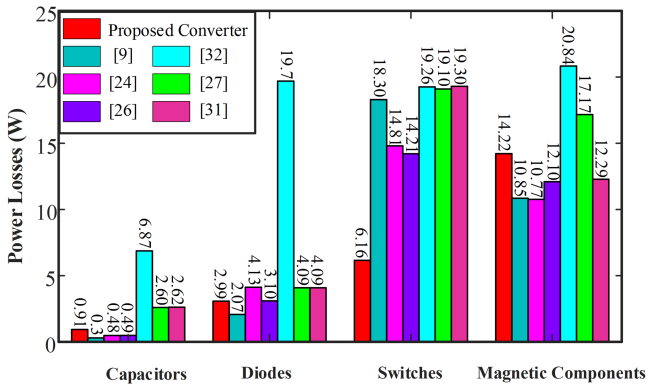


Fig. 14. Power loss distribution of the converters under $P_o = 500$ W.

1) Switch Losses: Due to the ZVS operation, the switch turn-ON power loss is eliminated. We only consider its turn-OFF power loss and conduction power loss, which are expressed by $P_{\mathrm{sw,S}}$ and $P_{\mathrm{cond,S}}$, respectively, as follows:

$$\begin{cases} P_{SW,S} = \frac{1}{T_s}\left(\int_0^{t_{\mathrm{on}}} V_S i_S dt + \int_0^{t_{\mathrm{off}}} V_S i_S dt\right) \\ = \frac{1}{2} f_s V_S i_S(t_2) t_{\mathrm{off}} \\ P_{cond,S} = \frac{1}{T_s}\int_0^{T_s} R_S {i_S}^2 dt = R_S I^2_{S-\mathrm{rms}}. \end{cases} \tag{42}$$

2) Diode Losses: From Section II-B, all diodes of the proposed converter turn-OFF with ZCS. Then, the diode power

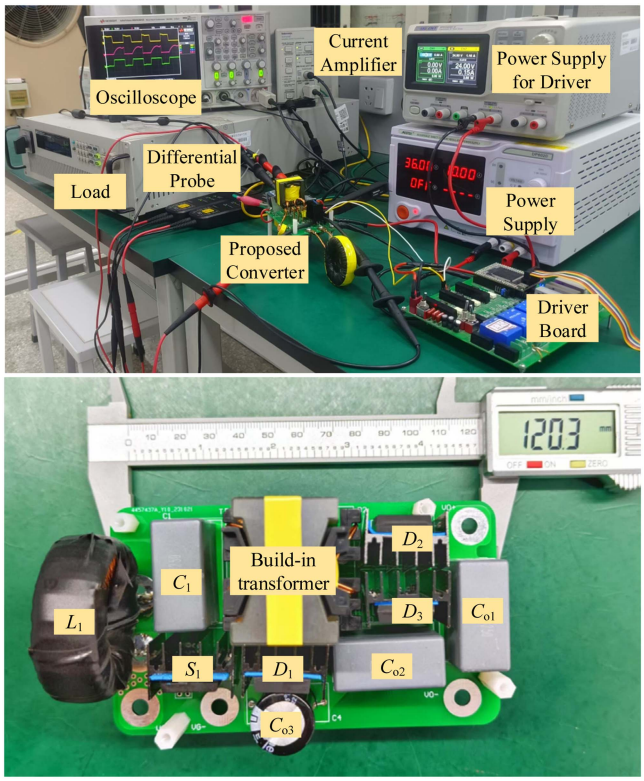


Fig. 15. Experimental setup and prototype.

losses are calculated as

$$P_D = \sum_{i=1}^{3} (V_{FDi} I_o + R_{Di} I_{Di-\text{rms}}^2). \tag{43}$$

3) Capacitor Losses: The capacitor power losses can be estimated as follows:

$$P_C = R_{C1} I_{C1-\text{rms}}^2 + R_{Co1} I_{Co1-\text{rms}}^2 + R_{Co2} I_{Co2-\text{rms}}^2 + R_{Co3} I_{Co3-\text{rms}}^2. \tag{44}$$

4) Magnetic Components Losses: Losses in magnetic components include copper losses P_{Cu} and iron losses P_{Fe} [36], expressed as

$$P_{\text{Cu}} = R_{\text{L1}} I_{\text{L1}-\text{rms}}^2 + R_{\text{N1}} I_{\text{N1}-\text{rms}}^2 + R_{\text{N2}} I_{\text{N2}-\text{rms}}^2 + R_{\text{N3}} I_{\text{N3}-\text{rms}}^2 \tag{45}$$

$$\begin{cases} P_{Fe\_L} = k_{iL} \left(\frac{V_{\text{L1(ON)}} D}{N_L A_{eL} f_s} \right)^{\beta_L - \alpha_L} \\ \times \left(\left(\frac{V_{\text{L1(ON)}}}{N_L A_{eL}} \right)^{\alpha_L} D + \left(-\frac{V_{\text{L1(OFF)}}}{N_L A_{eL}} \right)^{\alpha_L} (1-D) \right) V_L \\ P_{Fe\_T} = k_{iT} \left(\frac{V_{\text{Lm(ON)}} D}{N_T A_{eT} f_s} \right)^{\beta_T - \alpha_T} \\ \times \left(\left(\frac{V_{\text{Lm(ON)}}}{N_T A_{eT}} \right)^{\alpha_T} D + \left(-\frac{V_{\text{Lm(OFF)}}}{N_T A_{eT}} \right)^{\alpha_T} (1-D) \right) V_T \end{cases} \tag{46}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{47}$$

where α, β, and k are Steinmetz parameters. k_{i} is modified Steinmetz parameter in order to adapt square voltage excitation. N is the winding turns of magnetic component. A_{e} is the core cross-sectional area. The subscripts L and T represent the inductor and the build-in transformer, respectively.

The power losses of the switch in the ZCS-ON are different from those in the ZVS-ON condition. When the converter operates in the ZCS state, we consider the turn-ON loss and parasitic capacitance loss of the switch. The loss estimation of switch for the converter operating in the ZCS state is given as

$$\begin{cases} P_{SW,S} = \frac{1}{2} f_s V_S (i_S(t_6) t_{\text{on}} + i_S(t_2) t_{\text{off}}) \\ P_{cond,S} = \frac{1}{T_s} \int_0^{T_s} R_S i_S{}^2 dt = R_S I_{S-\text{rms}}^2 \\ P_{Cs,S} = \frac{C_S V_S^2 f_s}{2}. \end{cases} \tag{48}$$

Therefore, the theoretical efficiency η of the proposed converter can be expressed as

$$\eta = \frac{P_o}{P_o + P_S + P_D + P_C + P_{Cu} + P_{Fe}} \times 100\%. \tag{49}$$

The values of the parameters of the proposed converter are shown in Table III.

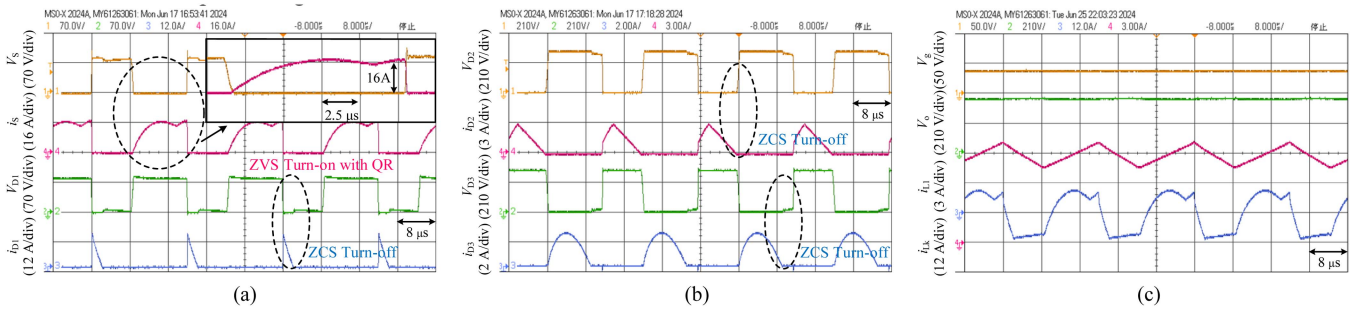
Fig. 9 depicts theoretical efficiency along with the voltage gain of the proposed converter as a function of the duty cycle with different turns ratio n_2 at $V_{\text{g}} = 36$ V, $R = 300\ \Omega$. It can be seen that the efficiency decreases with increasing turns ratio n_2 at a certain duty cycle. Moreover, an increase in duty cycle also leads to a decrease in efficiency. Taking efficiency and voltage gain into account, the optimum duty cycle range is between 0.4 and 0.6.

Fig. 10 shows the losses distribution of the components at rated output power. The main losses come from the magnetic components, which reaches 14.24 W, accounting for 62.76% of the total loss. It is followed by switch and diodes with a share of 19.53% and 13.57%, respectively. The losses of capacitors, which are the lowest, are less than 1 W.

IV. Comparative Study

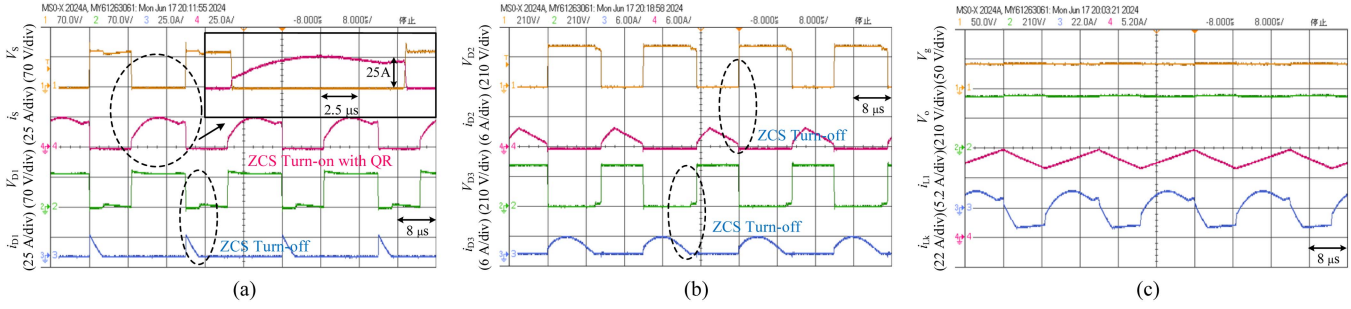
In order to highlight the advantages of the proposed converter, an analytical comparison is presented in this section. Table IV compares the properties of the proposed converter with other existing high voltage gain dc–dc converters, including voltage gain, voltage stress of the switch, total voltage stress of diodes, number of components, soft-switching characteristic, input current ripple, and common ground. To ensure fairness, all comparisons of the converters listed in Table IV are with the same conditions of turns ratios, as $n_1 = 0.5$, $n_2 = 2$ (for converters with three-winding coupled inductor/build-in transformer), $n = 2.5$ (for converters with two-winding coupled inductor/build-in transformer).

Fig. 11 shows the voltage gain comparison of the converters. It can be observed that the proposed converter has a medium voltage gain among the compared converters, which is lower than the converters in [27], [30], [31], and [32], while the number of components is less than theirs. The converter in [30] has a discontinuous input current and needs additional input



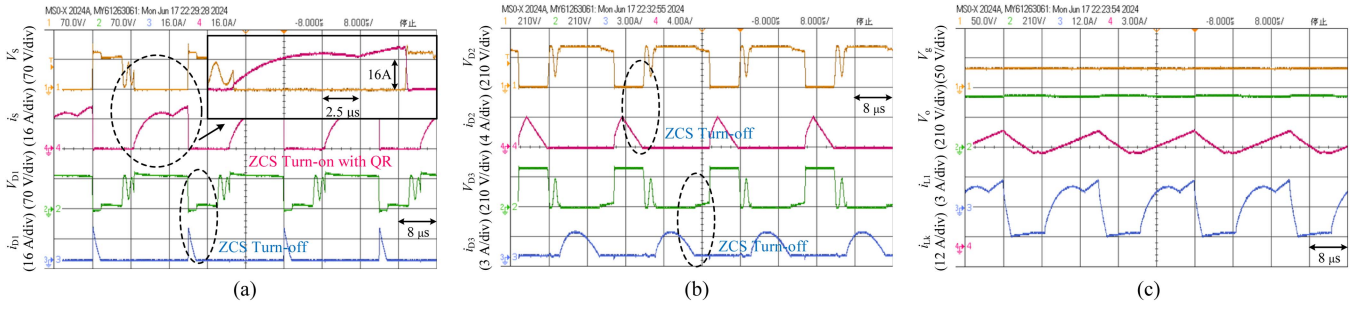
(a) (b) (c)

Fig. 16. Experimental results of the proposed converter under ZVS condition ($L_{\rm m} = 80$ μH, $P_{\rm o} = 300$ W). (a) Waveforms of the switch S and diode D_1. (b) Waveforms of diodes D_2 and D_3. (c) Voltages of input and output, and currents of input inductor and leakage inductance.



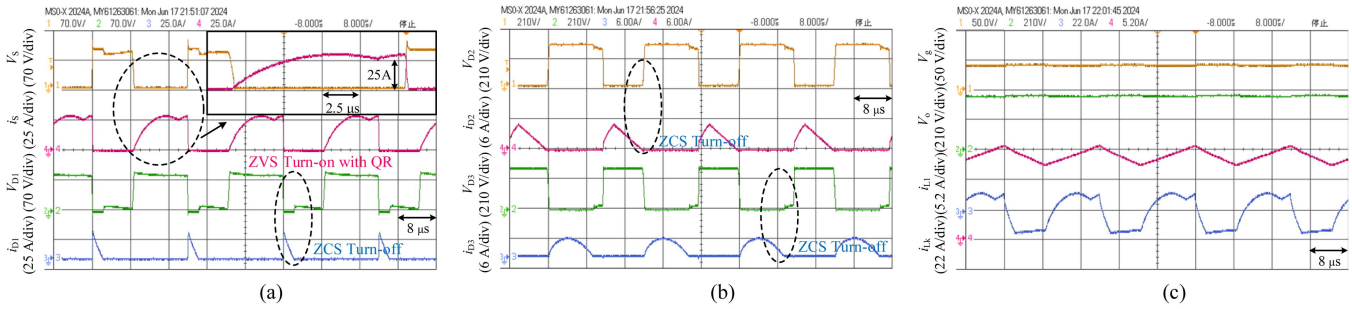
(a) (b) (c)

Fig. 17. Experimental results of the proposed converter under ZCS condition ($L_{\rm m} = 80$ μH, $P_{\rm o} = 500$ W). (a) Waveforms of the switch S and diode D_1. (b) Waveforms of diodes D_2 and D_3. (c) Voltages of input and output, and currents of input inductor and leakage inductance.



(a) (b) (c)

Fig. 18. Experimental results of the proposed converter under ZCS condition ($L_{\rm m} = 50$ μH, $P_{\rm o} = 300$ W). (a) Waveforms of the switch S and diode D_1. (b) Waveforms of diodes D_2 and D_3. (c) Voltages of input and output, and currents of input inductor and leakage inductance.



(a) (b) (c)

Fig. 19. Experimental results of the proposed converter under ZVS condition ($L_{\rm m} = 50$ μH, $P_{\rm o} = 500$ W). (a) Waveforms of the switch S and diode D_1. (b) Waveforms of diodes D_2 and D_3. (c) Voltages of input and output, and currents of input inductor and leakage inductance.

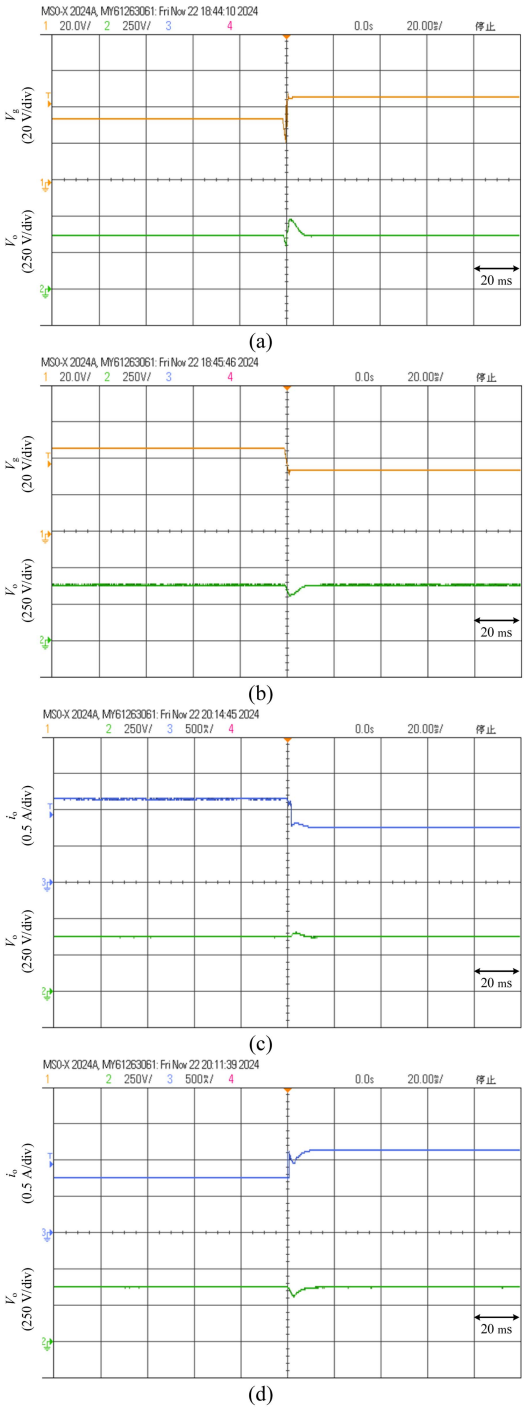


Fig. 20. Input and output voltage waveforms of the closed-loop experiment. (a) Input voltage changes from 36 V to 48 V. (b) Input voltage changes from 48 V to 36 V. (c) Load changes from 320 Ω to 500 Ω. (d) Load changes from 500 Ω to 320 Ω.

filtering to fulfill the continuous input current. Furthermore, the normalized voltage across the switch is compared in Fig. 12. It can be seen that the voltage stress on the switch of the proposed converter is at a low level. Therefore, MOSFET with lower rated voltages can be selected to improve efficiency and reduce costs of the converter. In addition, the soft-switching characteristic of the proposed converter and the small number of components further reduce the power losses. The theoretical efficiency comparison of the converters is depicted in Fig. 13. The proposed converter has the highest efficiency in operation above 200 W among the competitors. Fig. 14 illustrates the power loss distribution of the converters. From Fig. 14, the power losses of the proposed converter are at a low level when operating at 500 W.

The comparison results show that the introduced converter possesses advantages of low switch voltage stresses and low number of components. Thus, MOSFETS with lower rated voltages can be chosen to reduce costs. And the soft-switching characteristics provides an improvement in efficiency.

V. Experimental Results

In order to verify the validity of the theoretical analysis of the converter, an experimental prototype rated at 500 W is constructed in laboratory, as shown in Fig. 15. The parameters of the converter are shown in Table I.

First, the proposed converter is tested with $D = 0.55$, $L_{\rm m} = 80\ \mu$H, and $P_{\rm o} = 300$ W, and the results are illustrated in Fig. 16. Fig. 16(a) shows the waveforms of the switch S and diode D_1. The current of switch S rises from zero and varies as a sinusoidal waveform after the switch voltage drops to zero. Thus, the switch S achieves ZVS and QR turn-ON. The current of diode D_1 drops to zero linearly before D_1 turns OFF. Therefore, D_1 can be considered to turn OFF with ZCS. Because of the clamp of capacitor $C_{\rm o3}$, the voltage stresses of switch S and diode D_1 are both about 77 V, which are closed to the theoretical value of 80 V. Fig. 16(b) shows the waveforms of the diodes D_2 and D_3. As it can be seen, the currents of D_2 and D_3 both decrease to zero naturally before turning OFF. Hence, ZCS turn-OFF are also achieved for D_2 and D_3, which helps to reduce the reverse recovery loss of diodes. The input and output voltages of the proposed converter are illustrated in Fig. 16(c). With an input of 36 V and a duty cycle of 0.55, the output voltage reaches about 380 V. The voltage gain is about 10.56, which is slightly lower than the theoretical value of 11.11. This is a result of the parasitic parameters in the converter. The currents $i_{\rm L1}$ and $i_{\rm Lk}$ are also shown in Fig. 16(c). The input current ripple is about 30% at the output power is 300 W. At the moment of the switch-OFF, the values of $i_{\rm L1}$ and $i_{\rm Lk}$ are about 10.2 A and 8.4 A.

Then, the proposed converter is tested with $D = 0.55$, $L_{\rm m} = 80\ \mu$H, and $P_{\rm o} = 500$ W, and the results are illustrated in Fig. 17. Because the load becomes heavy, the current through diode D_2 has not dropped to zero by the time the switch receives a gate signal. The switch S conduct under ZCS-ON condition due to the leakage inductance $L_{\rm k}$. However, as shown in Fig. 17(a) and (b), all diodes can also achieve ZCS turn-OFF under this test condition. To ensure that the output voltage is about 380 V, the input voltage under this test condition is 38 V and the input current ripple is now about 27%, as shown in Fig. 17(c). This is because the actual inductance value decreases as the dc component of the inductor current increases.

In order to verify that the proposed converter is able to achieve ZVS-ON at different loads by designing proper parameters, the converter is tested with $D = 0.55$, $L_{\rm m} = 50\ \mu$H. Figs. 18 and

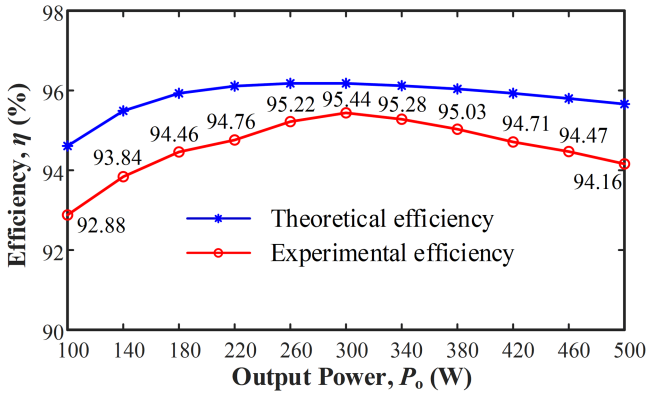


Fig. 21. Experimental and theoretical efficiency with $D = 0.55$, $V_g = 36$ V, $V_o = 380$ V.

19 show the results operating at 300 W and operating at 500 W, respectively. According to Figs. 18 and 19, we can see that by only changing the value of L_m, the converter is able to achieve ZVS turn-ON at 500 W. In this test condition, the converter enters in TW-ZCM mode when operating at 300 W, and the switch achieve ZCS turn-ON. Due to the TW-ZCM operation, the voltage gain is higher than in TW-CCM operation. To ensure that the output voltage is about 380 V, the input voltage under this condition is about 30 V. From Figs. 16, 17, 18, and 19, all waveforms match the theory analysis very well.

Fig. 20 shows the closed-loop experimental waveforms of the converter. Fig. 20(a) shows the waveform when the input is switched from 36 V to 48 V. Fig. 20(b) shows the waveform when the input is switched from 48 V to 36 V. Fig. 20(c) shows the waveform when the load is switched from 320 Ω to 500 Ω. Fig. 20(d) shows the waveform when the load is switched from 500 Ω to 320 Ω. From the view of power supply disturbance and load disturbance response, the proposed converter has better dynamic response and antidisturbance characteristics.

Moreover, the experimental and theoretical efficiency of the proposed converter as a function of output power P_o are depicted in Fig. 21. The efficiency reaches 95.44% at 300 W and the efficiency at rated power is 94.16%.

VI. Conclusion

This article has presented a new single-switch high step-up dc–dc converter for renewable energy system application. It provides high voltage gain, continuous input current with low ripple, low voltage stresses on switch, and output capacitors. The low number of components gives the converter a simple structure, low cost, and high efficiency. In addition, the converter realizes ZVS turn-ON of the switch and ZCS turn-OFF of the diodes around the rated load without adding any other components, which improves the EMC and efficiency.

A detailed theoretical analysis of soft-switching of proposed converter is presented in this article. Finally, a prototype with a rated power of 500 W is constructed, and the experimental results show that the converter achieves soft-switching turn-ON by designing appropriate elements' parameters without adding any other components, which fully utilized the parasitic parameters and made the converter as simple as possible.

References

[1] C. Sun, X. Zhang, and X. Cai, "A step-up non-isolated modular multilevel DC-DC converter with self-voltage balancing and soft switching," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13017–13030, Dec. 2020, doi: 10.1109/TPEL.2020.2993298.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017, doi: 10.1109/TPEL.2017.2652318.

[3] R. Rahimi, S. Habibi, M. Ferdowsi, and P. Shamsi, "A three-winding coupled inductor-based interleaved high-voltage gain DC–DC converter for photovoltaic systems," *IEEE Trans. Power Electron*, vol. 37, no. 1, pp. 990–1002, Jan. 2022, doi: 10.1109/TPEL.2021.3099486.

[4] T. Sutikno et al., "A review on non-isolated low-power DC-DC converter topologies with high output gain for solar photovoltaic system applications," *Clean Energy*, vol. 6, no. 4, pp. 557–572, Jul. 2022, doi: 10.1093/CE/zkac037.

[5] H. Tarzamni, H. S. Gohari, M. Sabahi, and J. Kyyrä, "Non-isolated high step-up DC–DC converters: Comparative review and metrics applicability," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 582–625, Jan. 2024, doi: 10.1109/TPEL.2023.3264172.

[6] G. G. Kumar, K. Sundaramoorthy, V. Karthikeyan, and E. Babaei, "Switched capacitor-inductor network based ultra-gain DC-DC converter using single switch," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10274–10283, Dec. 2020, doi: 10.1109/TIE.2019.2962406.

[7] S. Miao, W. Liu, and J. Gao, "Single-inductor boost converter with ultra-high step-up gain, lower switches voltage stress, continuous input current, and common grounded structure," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7841–7852, Jul. 2021, doi: 10.1109/TPEL.2020.3047660.

[8] Y. Zheng and K. M. Smedley, "Analysis and design of a single-switch high step-up coupled-inductor boost converter," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 535–545, Jan. 2020, doi: 10.1109/TPEL.2019.2915348.

[9] A. Mirzaee and J. S. Moghani, "Coupled inductor-based high voltage gain DC-DC converter for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7045–7057, Jul. 2020, doi: 10.1109/TPEL.2019.2956098.

[10] C. Albuquerque Caldeira, M. Lucio da Silva Martins, M. C. Cavalcanti, A. D. D. de Almeida, E. A. O. Barbosa, and L. R. Limongi, "High voltage step-up boost converter based on a three-winding-coupled inductor with voltage multiplier cell," *IEEE Access*, vol. 12, pp. 70117–70128, 2024, doi: 10.1109/ACCESS.2024.3401718.

[11] R. Fani, Z. Akhlaghi, and E. Adib, "High step-up DC-DC converter by integration of active switched inductors, built in transformer, and multipliers," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2468–2477, Feb. 2024, doi: 10.1109/TPEL.2023.3335391.

[12] T. Nouri, N. Vosoughi Kurdkandi, and M. Shaneh, "A novel ZVS high-step-up converter with built-In transformer voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12871–12886, Dec. 2020, doi: 10.1109/TPEL.2020.2995662.

[13] M. F. Guepfrih, G. Waltrich, and T. B. Lazzarin, "Unidirectional step-up DC–DC converter based on interleaved phases, coupled inductors, built-In transformer, and voltage multiplier cells," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2385–2395, Mar. 2023, doi: 10.1109/TIE.2022.3170639.

[14] T. Nouri, N. V. Kurdkandi, and O. Husev, "An improved ZVS high step-up converter based on coupled inductor and built-in transformer," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13802–13816, Dec. 2021, doi: 10.1109/TPEL.2021.3088092.

[15] N. A. Madiseh, E. Adib, and M. R. Amini, "A novel soft switching non-isolated bidirectional DC-DC converter without any extra auxiliary switch," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1875–1882, Apr. 2024, doi: 10.1109/JESTPE.2023.3250435.

[16] A. Mondzik, R. Stala, S. Piróg, A. Penczek, P. Gucwa, and M. Szarek, "High efficiency DC-DC boost converter with passive snubber and reduced switching losses," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2500–2510, Mar. 2022, doi: 10.1109/TIE.2021.3063874.

[17] H. M. Jazi, R. R. Khorasani, E. Adib, P. Zanchetta, G. Velasco-Quesada, and H. Martínez-García, "A high-efficient single-switch, soft-switching high step-up DC-DC converter with a simple structure and continuous input current for renewable energy integration," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9814–9826, Aug. 2024, doi: 10.1109/TPEL.2024.3391064.
[18] M. Heidari, H. Farzanehfard, and M. Esteki, "A single-switch single-magnetic core high conversion ratio converter with low input current ripple and wide soft-switching range for photovoltaic applications," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7226–7234, Jul. 2020, doi: 10.1109/TPEL.2019.2958839.
[19] X. Zhang et al., "Novel high step-up soft-switching DC-DC converter based on switched capacitor and coupled inductor," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9471–9481, Sep. 2020, doi: 10.1109/TPEL.2020.2972583.
[20] B. Poorali and E. Adib, "Soft-switched high step-up quasi-Z-source DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4547–4555, Jun. 2020, doi: 10.1109/TIE.2019.2922948.
[21] X. Ding, F. Wang, M. Zhou, Y. Cao, and Z. Wei, "Soft switching high voltage gain quasi-Z-source DC-DC converter with switched-capacitor technique," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11231–11241, Nov. 2022, doi: 10.1109/TIE.2021.3125649.
[22] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016, doi: 10.1109/JESTPE.2016.2532930.
[23] J. Wang, X. Wu, Z. Liu, X. Cui, and Z. Song, "Modified SEPIC DC-DC converter with wide step-up/step-down range for fuel cell vehicles," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2022.3203151.
[24] S. Hasanpour, M. Forouzesh, Y. P. Siwakoti, and F. Blaabjerg, "A novel full soft-switching high-gain DC/DC converter based on three-winding coupled-inductor," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12656–12669, Nov. 2021, doi: 10.1109/TPEL.2021.3075724.
[25] S. Hasanpour, "New structure of single-switch ultra-high-gain DC/DC converter for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12715–12728, Oct. 2022, doi: 10.1109/TPEL.2022.3172311.
[26] S. Hasanpour, Y. P. Siwakoti, and F. Blaabjerg, "Analysis of a new soft-switched step-up trans-inverse DC/DC converter based on three-winding coupled-inductor," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2203–2215, Feb. 2022, doi: 10.1109/TPEL.2021.3103978.
[27] S. Hasanpour, Y. P. Siwakoti, and F. Blaabjerg, "A new high efficiency high step-up DC/DC converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1489–1500, Feb. 2023, doi: 10.1109/TIE.2022.3161798.
[28] S. Hasanpour, T. Nouri, F. Blaabjerg, and Y. P. Siwakoti, "High step-up SEPIC-based trans-inverse DC-DC converter with quasi-resonance operation for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 485–497, Jan. 2023, doi: 10.1109/TIE.2022.3150103.
[29] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1290–1297, Feb. 2018, doi: 10.1109/TIE.2017.2733421.
[30] M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "A high voltage gain DC-DC converter based on three winding coupled inductor and voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4558–4567, May 2020, doi: 10.1109/TPEL.2019.2944518.
[31] M. Yang, Y. Weng, H. Li, J. Lin, X. Yan, and T. Jin, "A novel three-winding coupled inductor-based high-gain DC-DC converter with low switch stress and continuous input current," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15781–15791, Dec. 2023, doi: 10.1109 /TPEL.2023.3313796.
[32] T. Jin, X. Yan, H. Li, J. Lin, Y. Weng, and Y. Zhang, "A new three-winding coupled inductor high step-up DC-DC converter integrating with switched-capacitor technique," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 14236–14248, Nov. 2023, doi: 10.1109 /TPEL.2023.3301869.
[33] T. Jin, J. Lin, H. Li, X. Yan, Y. Weng, and X. Mao, "A novel three-winding coupled inductor-based high step-up DC-DC converter for renewable energy application," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 4, pp. 4477–4490, Aug. 2023, doi: 10.1109/JESTPE.2023.3260899.
[34] S. B. Santra, D. Chatterjee, Y. P. Siwakoti, and F. Blaabjerg, "Generalized switch current stress reduction technique for coupled-inductor-based single-switch high step-up boost converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1863–1875, Apr. 2021, doi: 10.1109/JESTPE.2020.2998487.
[35] X. Ding, K. Jiang, Y. Yu, B. Li, Y. Sun, and L. Quan, "A high step-up DC–DC converter integrated with modified sepic network," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2024.3511082.
[36] H. Matsumori, T. Shimizu, X. Wang, and F. Blaabjerg, "A practical core loss model for filter inductors of power electronic converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 29–39, Mar. 2018, doi: 10.1109/JESTPE.2017.2761127.

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