Letters

A Seamless Thermal Balance Control Strategy for Asynchronous Parallel Half-Bridge Circuit

Jinghao Zheng, *Graduate Student Member, IEEE*, Junfeng Liu, Renjun Hu, Ningrui Yang, Yue Li, Jun Zeng, Wentao Ge, and Zhixing Yan, *Graduate Student Member, IEEE*

***Abstract*—The asynchronous parallel half-bridge circuit has the characteristics of reliable capacity expansion and easy realization of zero-voltage switching, which can be a promising candidate for large capacity converters using wide bandgap devices. However, it has the issue of heat concentration, which leads to severe thermal imbalance and high thermal stress, posing a challenge to thermal design. In this letter, thermal balance control strategy is utilized by exchanging the drive signals of two-phase circuits, which can periodically change the loss distribution among the switches, suppressing the above problem. By compensating for the current variation, it effectively eliminates current overshoot and oscillation during transition, thereby mitigating inductor saturation and enhancing the reliability of the system. Furthermore, a thermoelectric coupling analysis method is proposed to evaluate the performance of the converter and provide guidance for converter design. Experimental and simulation results have been presented to demonstrate the effectiveness of the proposed solution.**

***Index Terms*—DC–DC converter, modulation, nonisolated converter, soft-switching techniques.**

I. Introduction

WIDE bandgap (WBG) devices have been penetrated into many applications taking place of traditional Si counterparts due to its exceptional characters. However, popularizing large-capacity WBG devices is limited by low fabrication rates and large variance of parameters, which result in high costs and low reliability. Therefore, it brings some challenge to apply WBG devices to some high-power applications [1], [2]. In order to meet the requirements of higher power levels, the parallel connection of small-capacity devices can be a cost-effective and inevitable solution. A common approach is to parallel device at the die level or circuit level, which means paralleling dies in a single package or paralleling discrete devices as a single switch unit. However, parameter mismatch on devices or layout may cause current imbalance and oscillation, which needs some inefficient snubber circuits or complicated active gate drive methods [3], [4]. To further increase power capacity, parallel at converter level is utilized, since it is difficult to ensure reliable parameters match of layout in large-scale device parallel. By increasing the number of devices, the above methods can significantly increase the power capacity, while these also lead to higher junction capacitance, which causes high switching loss for those hard-switching topologies, especially at partial load where switching loss is dominant for efficiency.

To optimize the performance for these configurations, many solutions have been studied from the aspects of control scheme and topology [5], [6], [7]. Among them, the asynchronous modulation of parallel half-bridge circuits, shows the potential to solve the above problems by taking into account the global efficiency optimization, circuit complexity, and control complexity well [8], [9], [10], [11]. As shown in Fig. 1, half-bridge circuit, in which a small auxiliary inductor is added to its intermediate port, constitutes an circuit unit, and several units can be divided into two phases, then a slight time delay is introduced between two phases to create differential-mode current for achieving zero-voltage switching. With this configuration, converter can work in asynchronous modulation mode when switching loss is dominant and work in continue current mode when conduction loss is dominant, thus the global efficiency can be optimized.

Nevertheless, it faces the problem of thermal imbalance, which means the main loss will be concentrated on part of the devices, resulting in higher thermal stress, which may become the limiting factor for thermal design and need bulky heatsink that affects the power density. In the previous studies, a scheme of exchanging drive signals between phases is proposed to

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Jinghao Zheng, Junfeng Liu, and Yue Li are with the School of Automation Science and Engineering, South China University of Technology, Guangzhou 510641, China (e-mail: 202221017777@mail.scut.edu.cn; jf.liu@connect.polyu.hk; 202320116134@mail.scut.edu.cn).

Renjun Hu is with the College of Engineering, South China Agricultural University, Guangzhou 510640, China (e-mail: rjhu@scau.edu.cn).

Ningrui Yang is with the University of Macau, Taipa 999078, Macau (e-mail: ningruiyang@um.edu.mo).

Jun Zeng and Wentao Ge are with the School of Electric Power Engineering, South China University of Technology, Guangzhou 510641, China (e-mail: junzeng@scut.edu.cn; 202120115121@mail.scut.edu.cn).

Zhixing Yan is with the AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: zhya@energy.aau.dk).

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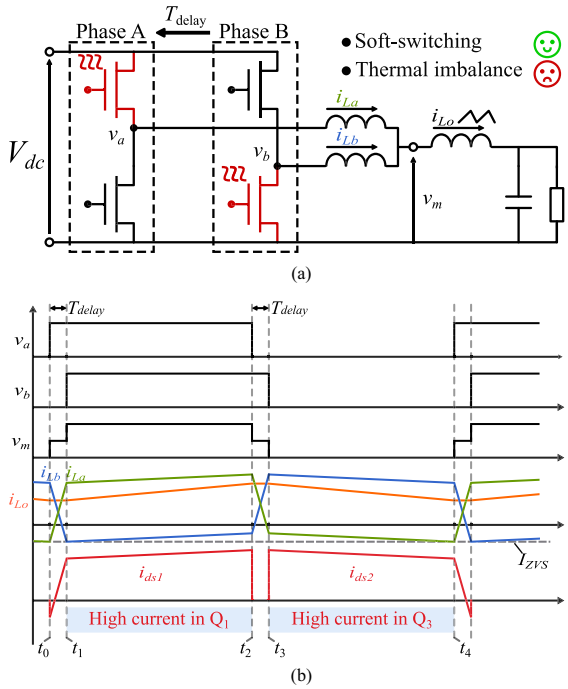

Fig. 1. (a) Schematic of the asynchronous parallel half-bridge circuit. (b) Key waveform of the asynchronous parallel half-bridge circuit.

balance the thermal stress [8], [9]. But direct transition will lead to current overshoot and oscillation, which may saturate the inductor and affect the reliability of the system.

To tackle this issue, a seamless thermal balance strategy is proposed to achieve smooth transition of exchanging driving signals. By compensating for the current variation during the transition, the current overshoot and oscillation of the inductor can be eliminated. Furthermore, a thermoelectric coupling analysis method is proposed to estimate the extreme thermal stress that is not easily obtained from existing solutions, providing guidance for the iterative design of the converter.

The contributions of this work can be summarized as follows.

1) The proposal control strategy can achieve seamless thermal balance control without current overshoot and oscillation. Due to the seamless operation, the proposed control strategy can reduce the transition period to the ms level, effectively suppress the thermal imbalance and eliminate the extreme thermal stress.
2) A thermoelectric coupling analysis is proposed to estimate the junction temperature variation and worst-case scenario of the converter, which provides design guidance for reducing the design iterations and speeding up the design process.

The following section will illustrate the proposed solution in detail.

II. Optimal Thermal Balance Control Strategy and Thermoelectric Coupling Analysis

A. Issues With Conventional Strategy

Fig. 1(a) shows the schematic of the asynchronous parallel half-bridge circuit, and an auxiliary inductor is inserted to the intermediate port of half-bridge circuit. Then, the another port of inductors is connected to the output inductor. By introducing a slight phase delay between the two-phase circuits, differential mode current is generated to achieve zero-voltage switching (ZVS) of all switches in the converter.

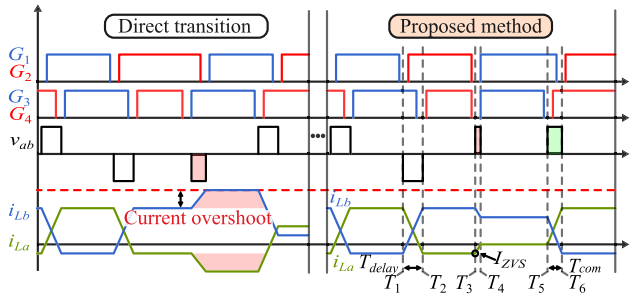

Fig. 2. Key waveform of the proposed control strategy.

This method can effectively increase the power capacity of the converter without sacrificing the efficiency of partial load, showing advantages in high-power applications. However, most of the current flows through upper switch of leading phase and lower switch of lagging phase when operating in asynchronous parallel mode; thus, the main loss will be concentrated on part of the devices, resulting in extreme thermal stress. Fig. 1(b) shows the example that large current is mainly conducted in Q_1 and Q_3 when phase A is leading, which may cause these switches to overheat. This problem may bring challenge to thermal design, and a bulky heat sink limits the improvement of power density.

B. Optimal Thermal Balance Control Strategy

From the previous instructions, we can know that some switches bear most of the loss, while the power capacity of other switches is not fully utilized.

To suppress the high thermal stress, a thermal balance control strategy can be adopted by exchanging the drive signals of two-phase circuits. With this operation, the phase-delay time of the two-phase circuits is periodically interchanged, resulting in corresponding changes in the distribution of losses. This allows all switches to alternatively bear the loss, thereby mitigating extreme thermal stress, which means all switches are fully utilized.

However, if only the drive signal is directly exchanged, it may lead to current overshoot and oscillation, which may saturate the inductor and affect the reliability of the system. Thus, a seamless thermal balance control strategy is proposed in this article, and its operating waveform is shown in Fig. 2.

As shown in the figure, direct transition refers to the direct change of gate driver signals between two-phase circuits. An unexpected differential voltage V_{ab} of the same polarity as in the previous interval is applied to the auxiliary inductor. This means that the inductors cannot be demagnetized in time, that is, the volt–second balance principle is not satisfied, which causes the inductor current overshoot.

To tackle this issue, a seamless transient method is proposed by inserting a transient interval between two sets of phase-delay modes, and the operation procedure is as follows: The transition begins when the lower switch of the leading phase is turned OFF, and the signals of two-phase circuits shift from being

asynchronous to synchronous. Through this operation, the current in each phase circuit will be transferred from the conducting switch to its complementary switch, which provides appropriate phase-delay relationship and differential current for next steady state. Then, the duty cycle of the phase that was leading in previous steady state is increased to provide appropriate differential current to achieve ZVS and allow the circuit to enter steady state.

It must be noted that the current commutation process ([T_3-T_4]) will apply a differential voltage to the auxiliary inductors, resulting in a change in differential current, which should be compensated in the next switching process ([T_5-T_6]) to achieve a seamless transition.

In order to avoid current overshoot and oscillation, and to quickly enter the next steady state after the transition, the voltage–second balance principle should be satisfied on auxiliary inductors, which can be expressed as

$$\int_{T_0}^{T_1} v_{ab}dt = \int_{T_2}^{T_3} v_{ab}dt + \int_{T_5}^{T_6} v_{ab}dt \tag{1}$$

where the time of interval [T_0-T_1] T_{delay} is the phase-delay time to achieve ZVS in steady state, and the time of interval [T_3-T_4] is the time for current commutation from the lower switch to the upper switch. The calculation of the time of interval [T_5-T_6] is the key to achieve seamless transition. Since T_{delay} has been calculated in asynchronous parallel half-bridge circuit control, and voltage–second product of interval [T_3-T_4] can be derived according to the linear MOSFET switching model [12], which can be written as

$$\int_{T_2}^{T_3} v_{ab}dt = V_i \cdot \frac{2Q_{\text{oss}}}{I_{\text{ZVS}}} = 2V_i \cdot \sqrt{\frac{L_{\text{aux}}Q_{\text{oss}}}{V_i}} \tag{2}$$

where Q_{oss} is the equal capacitance of the switches and L_{aux} is the inductance of auxiliary inductors.

Then the compensation time can be written as

$$T_{\text{com}} = T_{\text{delay}} - 2 \cdot \sqrt{\frac{L_{\text{aux}}Q_{\text{oss}}}{V_i}}. \tag{3}$$

The detailed derivation is presented in the Appendix.

C. Thermoelectric Coupling Analysis

In the proposed control strategy, these devices take turns to withstand main loss, resulting in periodic changes in their temperature. In order to evaluate the effect of thermal balance strategy and provide guidance to thermal and control design, thermoelectric coupling analysis is conducted [13].

The main heat dissipation path is shown in Fig. 3(a), most of the heat is transferred to the air through the bottom thermal pad, printed circuit board (PCB), and heat sink. In addition to self-heating, the loss of device also increases the temperature of other switches, which is called thermal coupling. As shown in Fig. 3, the proposed method is utilized to build up the thermoelectric coupling model, where the thermal impedance can obtain from commercial finite-element analysis software and the power loss can be extracted from datasheet or simulation [14].

Then, we can see that the temperature of these switches variates exponentially, and the transient period can effectively

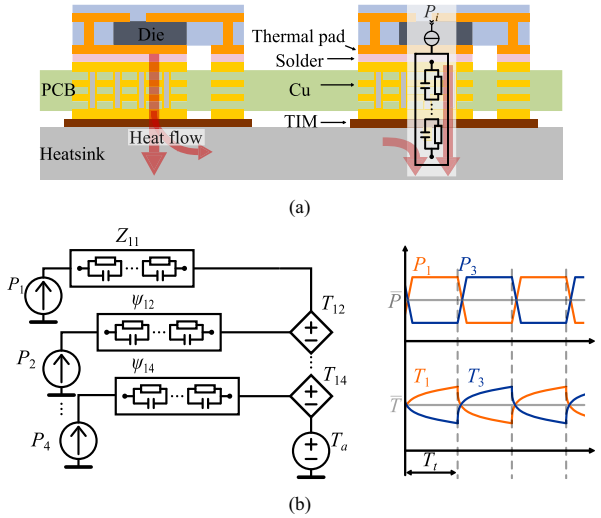

Fig. 3. (a) Physical model of heat dissipation path. (b) Thermoelectric coupling model to estimate junction temperature of devices.

influence the magnitude of the temperature change. The maximum temperature of each switch can be calculated as follows:

$$T_{\max\_i} = T_a + \sum_{j=1}^{4} \overline{P}_{ij} \cdot \sum_{k=1}^{n} R_{jk} + \frac{1}{2} \sum_{j=1}^{4} \Delta P_{ij} \sum_{k=1}^{n} R_{jk} \cdot \left(1 - e^{-\frac{T_t}{\tau_k}}\right). \tag{4}$$

It must be noted that the detection of rapidly changing junction temperatures is difficult, requiring high-speed sampling equipment and intrusive tests that are not easy to implement. The proposed analysis method can estimate the worst condition, which can be complemented with experimental tests to provide guidance for the thermal design of the converter.

D. Implementation of the Proposed Seamless Thermal Balance Control Strategy

As shown in Fig. 4(a), the seamless thermal balance control strategy can be divided into two parts: steady-state control and transition control. The steady-state control includes voltage regulation with PI controller and asynchronous parallel control to achieve ZVS with the calculation of T_{delay} (or lookup table), which has been well demonstrated in [8]. The transition control that is marked with light-yellow background includes the calculation of compensation time T_{com} and corresponding pulsewidth modulation (PWM) signal generation method.

Fig. 4(b) shows an example implementation using two timers in a microcontroller. As shown, the counters in two timers are set to sync and two compare registers in each timer are set to obtain the expected PWM signal. During the steady state, compare values are set to obtain the appropriate phase-delay time. When it operates in phase A leading mode, PWM1 is ahead of PWM2, and vice versa. When time of transition is reached, the first compare values of two timers are set to equal, and then,

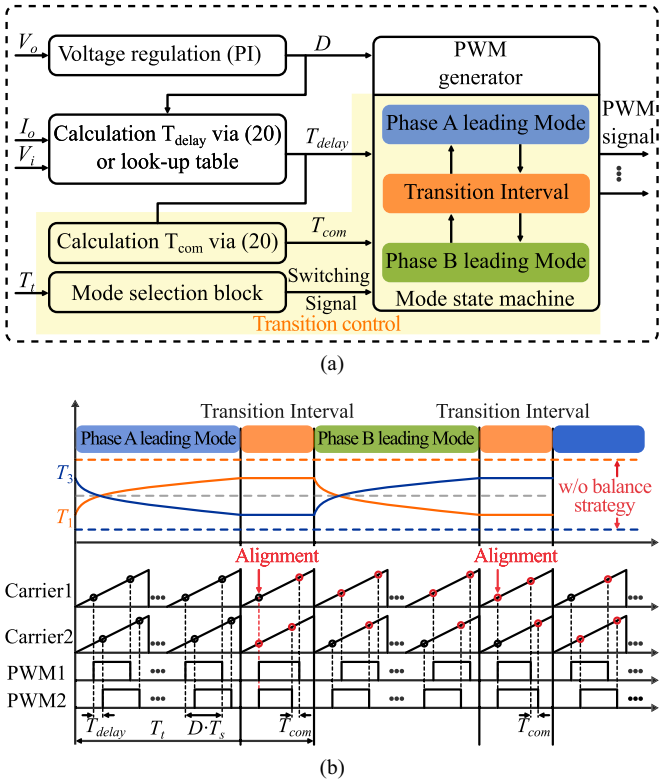

Fig. 4. (a) Control diagram of the proposed method. (b) Implementation and thermal balance effect of the proposed method.

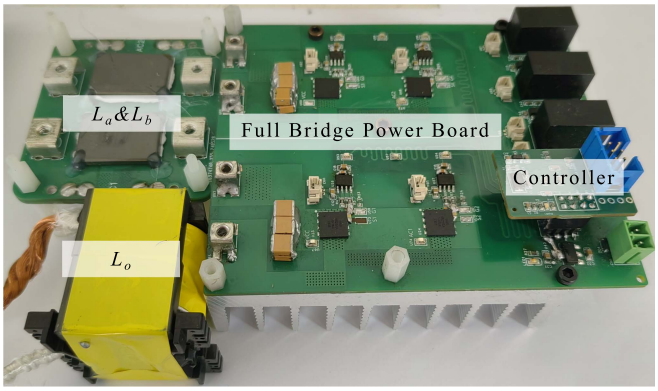

Fig. 5. Experimental prototype.

the second values of two timers are increased and decreased, respectively, based on the require compensation time T_{com}. After this switching cycle, the compare register can be directly set to the value corresponding to the next steady-state mode.

With thermal balance control, the temperature in each switch can be limited to a narrow range, and its temperature stress can be much smaller than without thermal balance control, which reduces thermal design requirements and redundancy.

III. Experimental and Simulation Results

A 600-W two half-bridge parallel prototype is built to validate the proposed method. Fig. 5 presents the experimental prototype and its parameters are listed in Table I.

TABLE I
Parameters of the Prototype

Parameters	Symbols	Values
Input voltage	V_i	250 V
Output voltage	V_o	100-150 V
Output power	P_o	600 W
Differential inductance	L_{aux}	2.5 μH
Output inductance	L_o	96 μH

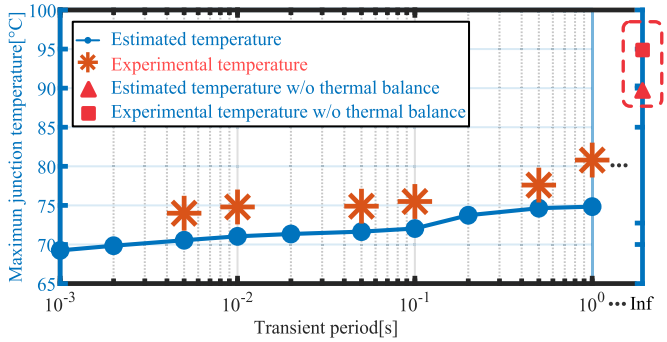

Fig. 6. Estimation of maximum junction temperature and experimental results.

As shown in Fig. 6, the proposed analysis method is carried out to design the transient period of the control strategy and evaluate the extreme thermal stress of the converter. The proposed thermal balance control strategy can effectively reduce the maximum temperature of the switches, and reduction effect is more significant the shortening of the balance time.

Fig. 7 shows comparison experiments between the direct transition and the proposed seamless transition. CH1 and CH2 represent the gate driving signals of the upper switches on each phase, respectively. CH3 and CH4 represent the auxiliary inductor current on each phase, respectively.

Fig. 7(a)–(c) shows the transition waveform of the direct transition under different duty cycle conditions. As seen, direct transition will lead to inductor current overshoot, which may need a redundant design margin to avoid inductors saturation. In addition, the current overshoot also causes oscillations, which make the circuit unable to quickly enter the next steady state and thus deviate from the efficient operation state.

Fig. 7(d)–(f) shows the transition waveform of the proposed seamless transition. During transition, the drive signal of Q_1 and Q_3 is first aligned and the on-time of the switch is adjusted to provide the desired differential voltage to bring the circuit to the next steady state. As seen, the converter smoothly transfer to the next steady state without current overshoot or oscillation, which means that the proposed control strategy has little impact on the operation of the converter and a short transition period can be adopted.

Fig. 8(a) shows the thermal image without thermal balance control, and Fig. 8(b) shows the thermal image with thermal balance control. As shown in Fig. 8(a), without the thermal balance control, the maximum temperature difference is almost 32.4 °C, and the maximum temperature is 95.6 °C on Q_1, where the extreme hot spot may become the limiting factor in thermal design. In contrast, as shown in Fig. 8(b), with the thermal

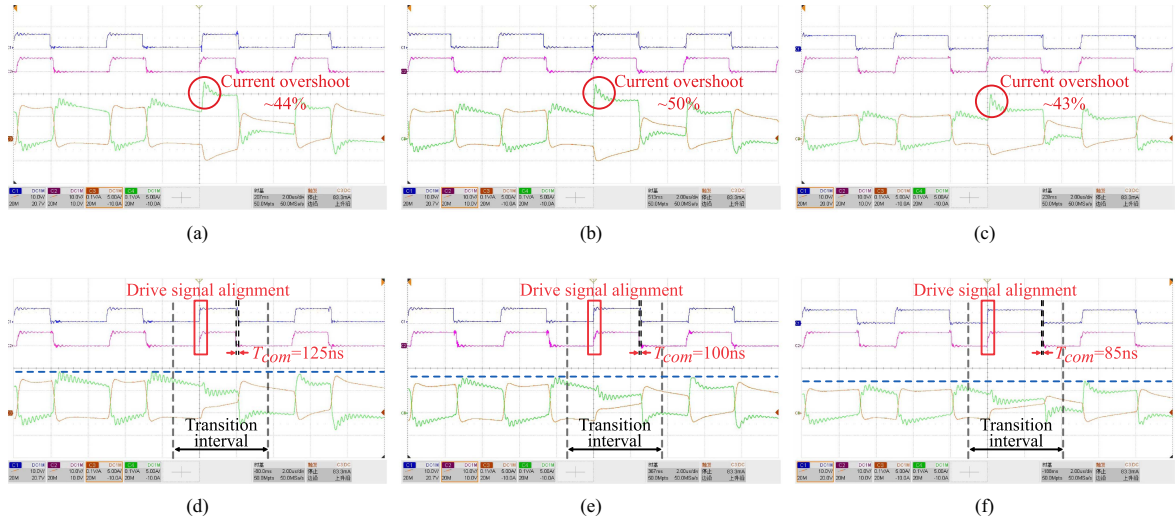

Fig. 7. Experimental waveform. (a) Direct transition, D = 0.4. (b) Direct transition, D = 0.5. (c) Direct transition, D = 0.6. (d) Proposed method, D = 0.4. (e) Proposed method, D = 0.5. (f) Proposed method, D = 0.6.

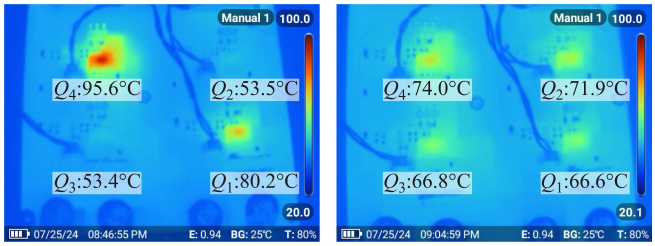

Fig. 8. Thermal images of circuit. (a) Operation without thermal balance control. (b) Operation with thermal balance control (T_t = 5 ms).

balance control, the maximum temperature difference is reduced to about 7.4 °C, and the maximum temperature is reduced to about 74 °C, which shows that the proposed control strategy can effectively suppress the thermal imbalance and extreme thermal stress. It is inevitable that there are errors between the thermal model and the loss model and the actual working condition, but the experimental results are still in good agreement with the proposed analysis method, which proves that the method can provide guidance for the thermal design of the converter.

IV. Conclusion

Due to the limited process of WBG devices, the production of high-capacity devices is not a cost-effective solution compared with parallel devices. Among several technical solutions, asynchronous parallel half-bridge exhibits good performance for its ability of achieving ZVS to reduce switching loss and improve partial load efficiency. However, it has the problem of loss concentration, resulting in serious thermal imbalance and high thermal stress, which poses challenge to thermal design. To tackle this issue, an optimal thermal balance strategy is proposed, which can smoothly transfer between two modes that have different loss distribution and these devices take turns to withstand main loss, thus suppressing thermal imbalance and high thermal stress. Furthermore, the thermoelectric coupling analysis method is proposed to estimate the worst condition of the converter, which can provide a guidance for the design of the converter.

The proposed methods fill the research gap of asynchronous parallel half-bridge circuit and make it a more potential solution.

Appendix

To achieve transition control (calculation of compensation time T_{com}), the closed-form solution for asynchronous parallel control should be derived, which will be simply presented here, and a more detailed derivation can be found in [8].

For simplification, the linear MOSFET switching model is applied [12], where the parasitic capacitance of the switch is assumed to be constant C_{oss} and the switching node voltage remains unchanged until Q_{oss} is injected or ejected. It must be noted that the total electric charge should be injected or ejected is $2Q_{\text{oss}}$.

For ease of understanding, the topology schematic is showed again in Fig. 9(a). Fig. 9(b) shows the waveform using the simplified model.

Generally, the upper switches can easily achieve ZVS with high current at switching instant t_2 or t_3. While ZVS condition for lower switches should be well designed. Considering the time interval after the voltage change from 0 to V_i, there is still Q_{oss} that should flow out the switching node, and the current in that phase will increase from $-I_{\text{ZVS}}$ to zero, which can be written as

$$\frac{2Q_{\text{oss}}}{I_{\text{ZVS}}} = \frac{2L_{\text{aux}}I_{\text{ZVS}}}{V_i}. \tag{5}$$

Then, the I_{ZVS} can be derived as

$$I_{\text{ZVS}} = \sqrt{\frac{Q_{\text{oss}}V_i}{L_{\text{aux}}}}. \tag{6}$$

In asynchronous parallel control, one switching period can be divided into four intervals.

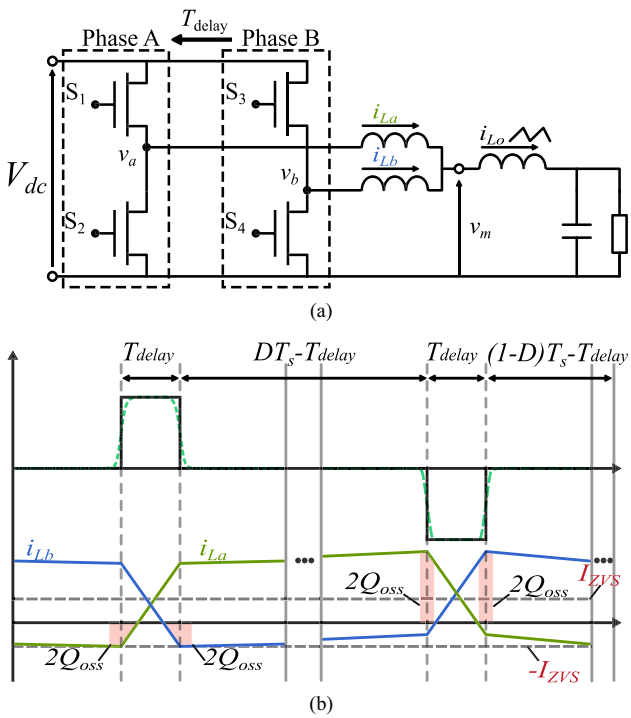

Fig. 9. (a) Schematic of the topology. (b) Simplified waveform for asynchronous parallel half-bridge circuit based on linear MOSFET switching model.

Interval 1 [t_0-t_1]: Q_1 turns ON while the Q_4 remains ON, and the positive differential voltage V_{ab} is applied on auxiliary inductors, which makes i_{Lb} decrease and i_{La} increase. This interval ends when i_{Lb} reaches I_{ZVS}. The inductors current can be written as

$$i_{La}(t) = I_{La,t_0} + \left(\frac{1-2D}{4L_0} + \frac{1}{2L_{\text{aux}}}\right) V_i(t-t_0) \tag{7}$$

$$i_{Lb}(t) = I_{Lb,t_0} + \left(\frac{1-2D}{4L_0} - \frac{1}{2L_{\text{aux}}}\right) V_i(t-t_0). \tag{8}$$

Interval 2 [t_1-t_2]: Q_3 turns ON while the Q_1 remains ON, and no differential voltage V_{ab} is applied on auxiliary inductors. The auxiliary inductors current increase equally. The inductors current can be written as

$$i_{La}(t) = I_{La,t_1} + \frac{1-2D}{2L_0} V_i(t-t_1) \tag{9}$$

$$i_{Lb}(t) = I_{Lb,t_1} + \frac{1-2D}{2L_0} V_i(t-t_1). \tag{10}$$

Interval 3 [t_2-t_3]: Q_2 turns ON while the Q_3 remains ON, and the negative differential voltage V_{ab} is applied on auxiliary inductors, which makes i_{La} decrease and i_{Lb} increase. The inductors current can be written as

$$i_{La}(t) = I_{La,t_2} + \left(\frac{1-2D}{4L_0} - \frac{1}{2L_{\text{aux}}}\right) V_i(t-t_2) \tag{11}$$

$$i_{Lb}(t) = I_{Lb,t_2} + \left(\frac{1-2D}{4L_0} + \frac{1}{2L_{\text{aux}}}\right) V_i(t-t_2). \tag{12}$$

Interval 4 [t_3-t_4]: Q_4 turns ON while the Q_2 remains ON, and there is no differential voltage V_{ab} is applied on auxiliary inductors. The auxiliary inductors current decrease equally. When this interval ends, i_{La} will decrease to I_{ZVS}, where the next switching period begins. The inductors current can be written as

$$i_{La}(t) = I_{La,t_3} - \frac{D}{2L_0} V_i(t-t_3) \tag{13}$$

$$i_{Lb}(t) = I_{Lb,t_3} - \frac{D}{2L_0} V_i(t-t_3). \tag{14}$$

In the steady state, we can obtain the following:

$$I_{La}(t_0) = I_{La}(t_0+T_s) = -I_{\text{ZVS}} \tag{15}$$

$$I_{Lb}(t_1) = I_{Lb}(t_1+T_s) = -I_{\text{ZVS}}. \tag{16}$$

Substituting (6)–(14) into (15), (16) yields the delay time

$$T_{\text{delay}} = \frac{2L_{\text{aux}}[2L_o(I_o+2I_{ZVS}) - (1-D)DT_sV_i]}{V_i(2L_0 - L_{\text{aux}})}. \tag{17}$$

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