A Novel SVM Strategy With Carrier-Based Implementation for Three-Level Simplified Neutral-Point-Clamped-Inverters

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***Abstract*—The three-level simplified neutral point clamped (3L-SNPC) inverter has been studied in recent years to unlock its potential for electrical drives and smart grids. Unfortunately, nearly all the existing papers on the 3L-SNPC inverter focus on control development. The carrier-based implementation of space vector modulation scheme and its associated converter loss analysis under various operating conditions are missing. In practice, these two points are paramount for industry applications. To fill such a research gap, this article proposes a simple carrier-based implementation of space vector modulation strategy for the 3L-SNPC inverter, which contributes to reducing the implementation cost and complexity. Furthermore, important performance metrics, including execution time, loss, and total harmonic distortion of the 3L-SNPC inverter under the proposed modulation strategy, are experimentally compared with those of the state-of-the-art modulation strategies for the 3L-SNPC inverter to validate the efficiency of the proposed modulation strategy. Comparative analysis is carried out in the full modulation range.**

***Index Terms*—Carrier-based implementation, converter loss, neutral point voltage balancing, space vector modulation, three-level simplified neutral point clamped (3L-SNPC) inverter.**

I. Introduction

THREE-LEVEL neutral point clamped (3L-NPC) inverters have been widely used in low to medium voltage applications [1], such as electric machine drives [2], grid integrated solar photovoltaic system [3], ship propulsion [4] and microgrid [5], owing to their low total harmonic distortion (THD), reduced voltage stress, and good voltage handling capacity. Nevertheless, two key issues of the conventional 3L-NPC inverter are known as the employment of a large number of power semiconductors and high losses [6], [7].

To reduce the number of semiconductors and the associated losses in low voltage applications, Kolar et al. [8] proposed the three-level T-type inverter. It not only eliminates the six clamping diodes but also offers higher overall efficiency in a wide modulation range. In practice, the semiconductor count can be further driven down when the three-level simplified NPC (3L-SNPC) inverter topology is used [9], [10]. Compared to the three-level T-type inverter, the 3L-SNPC inverter further removes two active switches together with their driver circuits, resulting in lower cost. It has also alleviated neutral point voltage (NPV) fluctuations due to the absence of medium voltage vectors (VVs) in its space vector diagram [11], [12].

Unfortunately, even though some research papers have been published on the control of 3L-SNPC inverter [13], [14], [15], [16], [17], the literature on the carrier-based implementation of space vector modulation (CBSVM) and loss analysis for the 3L-SNPC inverter is very sparse. Common modulation methods for multilevel inverters like [10], [18], [19], [20], and [21] are not directly applicable due to the absence of medium VVs. For instance, a modulation scheme for the 3L-SNPC inverter is proposed in [10]. It suffers from the inability to balance the NPV under a high modulation index. Due to the three-phase asymmetric structure of the 3L-SNPC inverter, common carrier-based implementation of space vector modulation method such as [21] is not directly applicable. An enhanced space vector modulation (SVM) scheme is introduced in [22], which uses a lookup table of different switching sequences to reduce NPV fluctuations. It encounters the problems of variable switching frequency, high design complexity, and increased hardware cost.

A two-stage model predictive control was proposed to regulate the grid-connected 3L-SNPC inverter in [23]. Despite its effective NPV balancing, this method applies only one VV in each sampling cycle, leading to variable switching frequency and high current harmonics. In the same year, a deadbeat based model predictive control was proposed for the 3L-SNPC inverter fed motor drives [15].

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The SVM method proposed in [22] introduced an approach where each sector was divided into two regions, exploring various VV sequence combinations. This method provided significant theoretical insights but lacked hardware validation, as it required FPGA implementation due to the complexity of noncarrier-based SVM. The refinements made in [24] further improved this approach by optimizing voltage sequencing, also utilizing field programmable gate arrays (FPGA) for implementation. Despite these advancements, both methods rely on noncarrier-based SVM, necessitating complex programmable logic devices (CPLD) or FPGA, which adds to the hardware complexity and cost. Noticeably, the loss of 3L-SNPC inverter is rarely studied.

In [14] and [15], an enhanced SVM approach was introduced by dividing each sector into four regions, improving duty cycle calculations and voltage vector sequence selection. These refinements addressed some of the limitations in earlier methods by simplifying the region determination process and streamlining duty cycle computation, which enabled the implementation on CPLD rather than FPGA. However, the reliance on additional hardware components remains a challenge, hindering the broader industrial adoption of 3L-SNPC inverters. In contrast, the CBSVM methods for the conventional 3L-NPC inverters can be directly implemented on digital signal processors (DSP), offering a more accessible solution for industrial applications without the need for extra hardware.

This article addresses these limitations by introducing a novel modulation technique for the 3L-SNPC inverter that further enhances region partitioning and duty cycle calculations while employing a simplified carrier-based implementation. This approach eliminates the need for FPGA or CPLD, thereby reducing system complexity and cost. The proposed method aligns with industry preferences for DSP-based solutions, potentially facilitating broader adoption of 3L-SNPC inverters in practical power electronics applications.To the best of the authors' knowledge, there is no paper on the CBSVM for the 3L-SNPC inverter that guarantees NPV balance in the full modulation range. Moreover, a comprehensive inverter loss analysis under the CBSVM is necessary as it serves as a guideline for power electronic engineers. For industry applications, these two points are of great importance. Notably, the proposed CBSVM ensures the NPV balance and excellent current performance in full modulation range. Its conduction and switching losses are thoroughly analysed and compared with those of the existing modulation schemes in full modulation range.

The key contributions of this article are summarized below.

1) For the first time, a carrier-based implementation of SVM strategy is proposed for the 3L-SNPC inverter that enables low cost and simple real-time implementation.
2) Compared to the existing modulation schemes for the 3L-SNPC inverter, the proposed modulation strategy achieves comparable results with a significantly reduced hardware cost.
3) A comprehensive analysis on the efficiency and harmonics performance of the 3L-SNPC inverter under the CBSVM is provided, clearly demonstrating the advantages and limitations of the proposed modulation strategy.

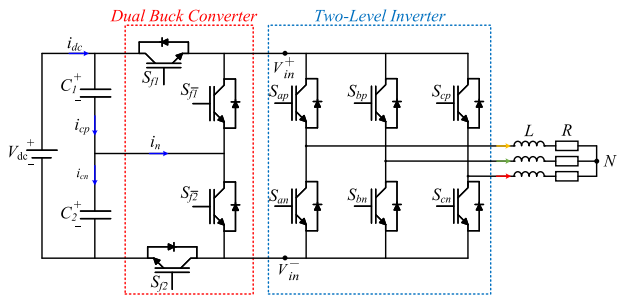


Fig. 1. Circuit topology of 3L-SNPC inverter.

TABLE I
SWITCHING LOGIC OF DUAL BUCK CONVERTER

Switching logic	S_{f1}	1	1	0	0
	S_{f1}^-	0	0	1	1
	S_{f2}	0	1	1	0
	S_{f2}^-	1	0	0	1
Terminal voltage	V_{in}^+	V_{dc}	V_{dc}	$V_{dc}/2$	$V_{dc}/2$
	V_{in}^-	$V_{dc}/2$	0	0	$V_{dc}/2$

The rest of this article is organized as follows. Section II describes the operating principle and system modeling of the 3L-SNPC inverter. The proposed strategies are detailed in Section III. Section IV presents experimental results and comparison with state-of-the-art methods. Finally, Section V concludes this article.

II. SYSTEM MODELING

The circuit topology of 3L-SNPC inverter is shown in Fig. 1. It comprises a dual buck converter connected with a conventional two-level voltage source inverter (2L-VSI). Two capacitors with equivalent capacitance are connected to the neutral point of the front-end dual buck converter. Table I summarizes the switching logic of the front-end dual buck converter, where S_{f1}, S_{f1}^-, S_{f2}, and S_{f2}^- represent the switching combinations of corresponding switches. V_{in}^+ and V_{in}^- represent the positive and negative terminal voltage of the dual buck converter. Based on this, the space vector diagram of 3L-SNPC inverter can be derived as presented in Fig. 2.

The space vector diagram of 3L-SNPC inverter comprises 21 VVs, which are either large, small, or zero VVs. Notably, in 3L-SNPC inverter, six medium VVs are missing compared to the traditional 3L-NPC and T-type topologies. Each VV is represented by three digit notation, where "2," "1," and "0" denote the three voltage levels: $V_{dc}, V_{dc}/2$, and 0, respectively.

Vector synthesis in 3L-SNPC inverter can only use the available 21 VVs. Among them, all large vectors V_{1-6} are associated with only "2" and "0," which means full dc voltage. Consequently, the switching combination for the dual buck converter $(S_{f1}, S_{f1}^-, S_{f2}, S_{f2}^-)$ is consistent as 1010 for all large VVs. Apparently, large VVs will not cause the NPV imbalance.

According to the space vector diagram, in order to output large VV, for instance, $V_1(200)$, the above switching combination applies. Subsequently, the switching state of 2L-VSI can be

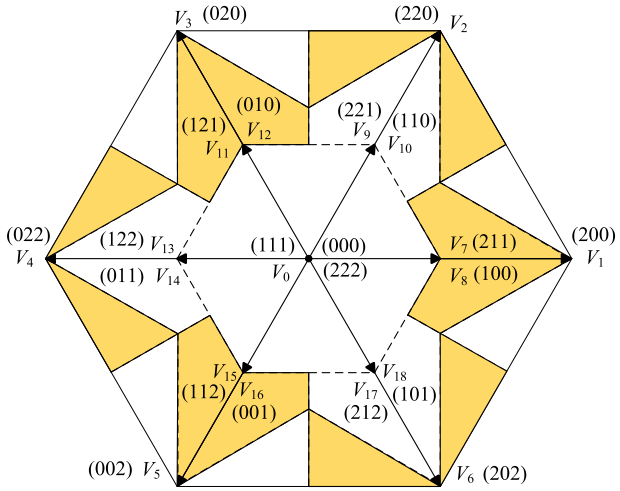


Fig. 2. Space vector diagram of 3L-SNPC inverter with full region division, where highlighted regions indicate the use of both convex and concave carriers, and nonhighlighted regions use only the concave carrier.

TABLE II
SWITCHING SEQUENCE FOR V_9, V_{10}

Voltage vectors	Dual buck converter S_{f1-2}	2L-VSI $S_{a,b,c}$	Neutral point current i_n
$V_9(221)$	10	110	i_c
$V_{10}(110)$	01	110	$-i_c$

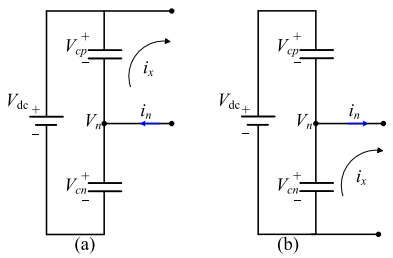


Fig. 3. Effect of the small VV on NPV, where (a) indicates $V_{7,9,11,13,15,17}$ and (b) indicates $V_{8,10,12,14,16,18}$.

determined as "100" for $S_a = 1$, $S_b = S_c = 0$. The capacitor currents can be expressed as

$$\begin{cases} i_{cp} = C_1 \frac{dV_{cp}}{dt} \\ i_{cn} = C_2 \frac{dV_{cn}}{dt} \end{cases} \tag{1}$$

where i_{cp} and i_{cn} represent the currents flowing through capacitors $C_1$and C_2, respectively.

Moreover, the neutral point current can be modeled as follows:

$$i_n = (-|S_a - 1|)\, i_a + (-|S_b - 1|)\, i_b + (-|S_c - 1|)\, i_c \tag{2}$$

where i_a, i_b, i_c, and i_n represent current produced by each phase leg and the neutral point current. S_a, S_b, and S_c stand for the switching states of the corresponding phase leg. The gate signal combinations from front-end dual buck converter determines which capacitor provides i_n as shown in Table II and Fig. 3, where equivalent small VV, $V_{9/10}$ are selected.

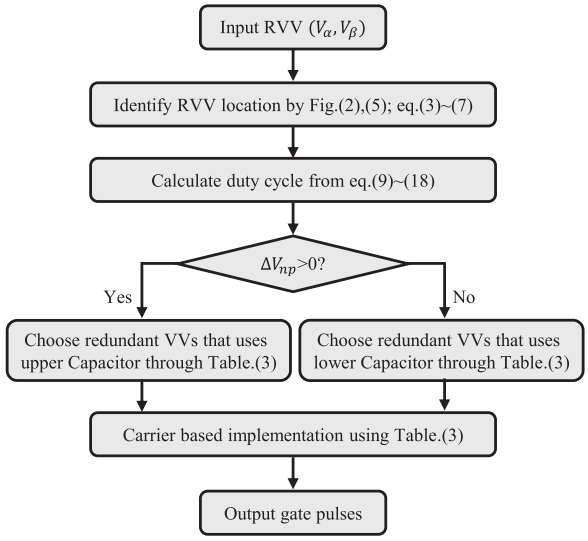


Fig. 4. Flowchart of the proposed modulation method.

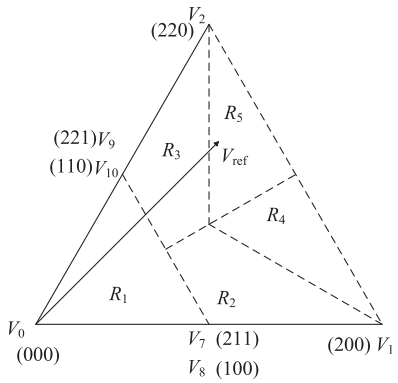


Fig. 5. Region determination in the first sector.

In Fig. 3, the activation of V_9 results in $i_n = i_x = -i_a - i_b = i_c$, which corresponds to the discharging current from capacitor C_1 and consequently diminishes the NPV V_{cp}. Similarly, for V_{10}, $i_n = i_x = -i_c$, which signifies the discharging current from capacitor C_2, thereby diminishing V_{cn}. Thus, the redundancy of small VVs contributes to balancing the NPV.

III. PROPOSED MODULATION FOR 3L-SNPC INVERTER

Building upon previous studies [15] and [24], the proposed method firstly introduces improved region division and duty cycle calculations to facilitate carrier-based implementation. Flowchart of the proposed scheme is depicted in Fig. 4.

A. Region Determination

In three-level inverter, voltage levels are typically restricted to change only once during each VV switching action to minimize the impact on switching frequency and output harmonic distortion. Based on this constraint and using Sector 1 as an example, the sector can be divided into five regions, as illustrated in Fig. 5. The other sectors are divided following the same principle.

For a given reference VV, it can be decomposed into its α and β components, i.e., V_α, V_β, where $V_\alpha = |V_{\text{ref}}| \cdot \sin\theta$, and$V_\beta = |V_{\text{ref}}| \cdot \cos\theta$. The specific region can be determined based on the values of V_α and V_β. The boundaries between regions are defined as follows:

$$R_1 : \begin{cases} V_\beta \le -\sqrt{3}V_\alpha - \frac{\sqrt{3}}{3}V_{dc} \\ 0^o \le \theta < 30^o \end{cases} \tag{3}$$

$$R_2 : \begin{cases} -\sqrt{3}V_\alpha - \frac{\sqrt{3}}{3}V_{dc} < V_\beta \le -\frac{\sqrt{3}}{3}V_\alpha + \frac{2\sqrt{3}}{9}V_{dc} \\ 0^o \le \theta 30^o \end{cases} \tag{4}$$

$$R_3 : \begin{cases} -\sqrt{3}V_\alpha - \frac{\sqrt{3}}{3}V_{dc} < V_\beta \le \frac{1}{3}V_{dc} \\ \&30^o \le \theta < 60^o \end{cases} \tag{5}$$

$$R_4 : \begin{cases} -\frac{\sqrt{3}}{3}V_\alpha + \frac{2\sqrt{3}}{9}V_{dc} < V_\beta \le -\sqrt{3}V_\alpha + \frac{2\sqrt{3}}{3}V_{dc} \\ 0^o \le \theta < 30^o \end{cases} \tag{6}$$

$$R_5 : \begin{cases} \frac{1}{3}V_{dc} < V_\beta \le -\sqrt{3}V_\alpha + \frac{2\sqrt{3}}{3}V_{dc} \\ 30^o \le \theta < 60^o \end{cases}. \tag{7}$$

B. Duty Cycle Calculation

The corresponding dwelling times can be calculated based on the selected VVs. In Sector 1, for reference VV synthesis, there are total 5 VVs, where each small voltage vector contains two redundant switching states. Consequently, five unique duty cycles can be identified. d_0 denotes the duty cycles of zero VV, V_0, d_1 and d_2 are the duty cycles of small VVs V_1 and V_2, respectively, where d_3 and d_4 signify the duty cycles of large VVs, $V_{7/8}$ and $V_{9/10}$. Notably, each duty cycle must be within 0 and 1, and the sum of all duty cycles must be 1

$$\begin{cases} 0 \le d_0, d_1, d_2, d_3, d_4 \le 1 \\ d_0 + d_1 + d_2 + d_3 + d_4 = 1. \end{cases} \tag{8}$$

Adhering to the aforementioned constraints, the duty cycle of each voltage vector can be uniquely determined after identifying the specific region of V_{ref}, within each sector, in accordance with the voltage-second balance principle.

1) Region R_1: If V_{ref} enters region R_1, VVs $V_0, V_{7/8}$ and $V_{9/10}$ will be applied with the duty cycles d_0, d_3, and d_4 correspondingly. As V_1 and V_2 are not used in this region, $d_1 = d_2 = 0$. The relationship between duty cycles and V_α, V_β can be derived

$$R_1 : \begin{cases} V_\alpha = \frac{V_{dc}}{3}d_3 + \frac{V_{dc}}{6}d_4 \\ V_\beta = \frac{\sqrt{3}V_{dc}}{6}d_4. \end{cases} \tag{9}$$

Consequently, solving (7) and (8) gives

$$\begin{cases} d_3 = \frac{3}{V_{dc}}V_\alpha - \frac{\sqrt{3}}{V_{dc}}V_\beta \\ d_4 = \frac{2\sqrt{3}}{V_{dc}}V_\beta \\ d_0 = 1 - \frac{3}{V_{dc}}V_\alpha - \frac{\sqrt{3}}{V_{dc}}V_\beta. \end{cases} \tag{10}$$

2) Region R_2: If V_{ref} is positioned in region R_2,VVs $V_1, V_{7/8}$, and $V_{9/10}$ will be applied with duty cycle d_1, d_3, and d_4, respectively. As a result, $d_0 = d_2 = 0$ yields

$$R_2 : \begin{cases} V_\alpha = \frac{2V_{dc}}{3}d_1 + \frac{V_{dc}}{3}d_3 + \frac{V_{dc}}{6}d_4 \\ V_\beta = \frac{\sqrt{3}V_{dc}}{6}d_4. \end{cases} \tag{11}$$

Solving (10) subject to the constraints in (7) yields

$$\begin{cases} d_1 = \frac{3}{V_{dc}}V_\alpha + \frac{\sqrt{3}}{V_{dc}}V_\beta - 1 \\ d_3 = 2 - \frac{3}{V_{dc}}V_\alpha - \frac{3\sqrt{3}}{V_{dc}}V_\beta \\ d_4 = \frac{2\sqrt{3}}{V_{dc}}V_\beta. \end{cases} \tag{12}$$

3) Region R_3: If V_{ref} is situated in region R_3,VVs $V_2, V_{7/8}$, and $V_{9/10}$ will be applied with duty cycle d_2, d_3, and d_4, respectively. In this case, $d_0 = d_1 = 0$ leads to

$$R_3 : \begin{cases} V_\alpha = \frac{V_{dc}}{3}d_2 + \frac{V_{dc}}{3}d_3 + \frac{V_{dc}}{6}d_4 \\ V_\beta = \frac{\sqrt{3}V_{dc}}{3}d_2 + \frac{\sqrt{3}V_{dc}}{6}d_4. \end{cases} \tag{13}$$

Solving (12) with respect to the constraints in (7) results in

$$\begin{cases} d_2 = \frac{3}{V_{dc}}V_\alpha + \frac{\sqrt{3}}{V_{dc}}V_\beta - 1 \\ d_3 = \frac{3}{V_{dc}}V_\alpha - \frac{\sqrt{3}}{V_{dc}}V_\beta \\ d_4 = 2 - \frac{6}{V_{dc}}V_\beta. \end{cases} \tag{14}$$

4) Region R_4: If V_{ref} is located in region R_4,VVs V_1, V_2, and $V_{7/8}$ will be applied with duty cycle d_1, d_2, and d_3, respectively. In this case, $d_0 = d_4 = 0$. The following relationship can be formed:

$$R_4 : \begin{cases} V_\alpha = \frac{2V_{dc}}{3}d_1 + \frac{V_{dc}}{3}d_3 + \frac{V_{dc}}{3}d_2 \\ V_\beta = \frac{\sqrt{3}V_{dc}}{3}d_2. \end{cases} \tag{15}$$

Corresponding duty cycle can be determined through (7) and (14)

$$\begin{cases} d_1 = \frac{3}{V_{dc}}V_\alpha - 1 \\ d_2 = \frac{\sqrt{3}}{V_{dc}}V_\beta \\ d_3 = 2 - \frac{3}{V_{dc}}V_\alpha - \frac{\sqrt{3}}{V_{dc}}V_\beta. \end{cases} \tag{16}$$

5) Region R_5: If V_{ref} is found in region R_5,VVs V_1, V_2, and $V_{9/10}$ will be applied with duty cycle d_1, d_2, and d_4, respectively. In this case, $d_0 = d_3 = 0$. The following relationship can be formed:

$$R_5 : \begin{cases} V_\alpha = \frac{2V_{dc}}{3}d_1 + \frac{V_{dc}}{3}d_2 + \frac{V_{dc}}{6}d_4 \\ V_\beta = \frac{\sqrt{3}V_{dc}}{3}d_2 + \frac{\sqrt{3}V_{dc}}{6}d_4. \end{cases} \tag{17}$$

The corresponding duty cycles can be figured out below

$$\begin{cases} d_1 = \frac{3}{2V_{dc}}V_\alpha - \frac{\sqrt{3}}{2V_{dc}}V_\beta \\ d_2 = \frac{3}{2V_{dc}}V_\alpha + \frac{3\sqrt{3}}{2V_{dc}}V_\beta - 1 \\ d_4 = 2 - \frac{3}{V_{dc}}V_\alpha - \frac{\sqrt{3}}{V_{dc}}V_\beta. \end{cases} \tag{18}$$

C. Carrier-Based Implementation of SVM

Once the duty cycles and switching states have been determined, the subsequent step involves generating gate signals for the 3L-SNPC inverter. Existing approaches in [15] and [24], typically rely on complex sequential programming to map each

duty cycle to its corresponding switching state, resulting in high programming complexity and hardware cost. To address this issue, a carrier-based implementation method is proposed.

Due to the inherently asymmetric structure of the 3L-SNPC inverter, directly comparing the reference values with the carrier signal fails to generate the correct gate signals for some cases. To overcome this challenge, both convex and concave type carriers are utilized in the reference VV synthesis.

In each region, three VVs are utilized to synthesize the reference VV. In region R_1, two small vectors and one zero vector are employed, while region R_2 and R_3 utilize two small vectors and one large vector. Regions R_4 and R_5 employ two large vectors and one small vector. Redundant small vectors, such as V_7 and V_8, or V_9 and V_{10}, are used to balance the NPV. Specifically, V_7 and V_9 can be used to discharge C_1, while V_8 and V_{10} can be used to discharge C_2. The NPV deviation is defined as $\Delta V = V_{Cp} - V_{Cn}$.

1) Reference VV Synthesis in R_1: In region R_1, when the ΔV is greater than zero, switches S_{f1} and $S_{\overline{f2}}$ should be activated to balance the NPV as illustrated in Fig. 3. Consequently, the output voltages of the dual-buck converter, i.e., V_{in+}, V_{in-}, are clamped at V_{dc} and $V_{dc}/2$, respectively. In this instance, vectors V_0, V_7, and V_9 are selected, with their corresponding switching sequence and duty cycles provided in Table III.

When ΔV is less than zero, switches S_{f2} and $S_{\overline{f1}}$ need to be activated to increase ΔV. Accordingly, vectors V_8 and V_{10} are selected, with the corresponding switching sequence and duty cycles determined as in Table III.

The vector synthesis logic used in R_1, which only requires the concave carrier, also applies to other regions where the convex carrier is not needed. The regions where the convex carrier is used are explained in the following sections and illustrated in Fig. 2.

2) Reference VV Synthesie in R_2 and R_3: In regions R_2 and R_3, the reference VV is synthesized using two small vectors and one large vector. The large vector used in R_2 is V_1, while in R_3 it is V_2.

In R_2, when the NPV deviation is greater than zero, C_1 should be discharged, and the vectors V_7, V_9, and V_1 are selected. The duty cycles for each switch can be derived from Table III. In this case, duty cycles of a, b, c and f_1 utilize the concave carrier, while the convex carrier is introduced for f_2 to generate the correct duty cycles, as demonstrated in Table III. If the NPV deviation is less than zero, C_2 should be discharged, and the vectors V_8, V_{10}, and V_1 are selected, with the voltage sequence shown in Table III. In this situation, the convex carrier is applied at f_1. Aside from using V_2 as the large vector, the vector synthesis logic in R_3 follows a similar pattern to R_2. In sector one of R_3, there is no need to introduce the convex carrier. When the NPV deviation is greater than zero, vectors V_7 and V_9 are used, while vectors V_8 and V_{10} are selected when the NPV deviation is less than zero.

3) Reference VV Synthesis in R_4 and R_5: In these two regions, the reference VV is synthesized using two large vectors V_1 and V_2, along with a small vector V_7/V_8 for R_4 and V_9/V_{10} for R_5. The time allocation logic is consistent with that used in other sectors, as detailed in Table III. The method for balancing the NPV remains the same: when the NPV deviation is greater than zero, vectors V_7 and V_9 are selected, and when the NPV deviation is less than zero, vectors V_8 and V_{10} are used. In sector one of R_5, the convex carrier is required, and the implementation follows the same approach as in sector one of R_2, where the convex carrier is used.

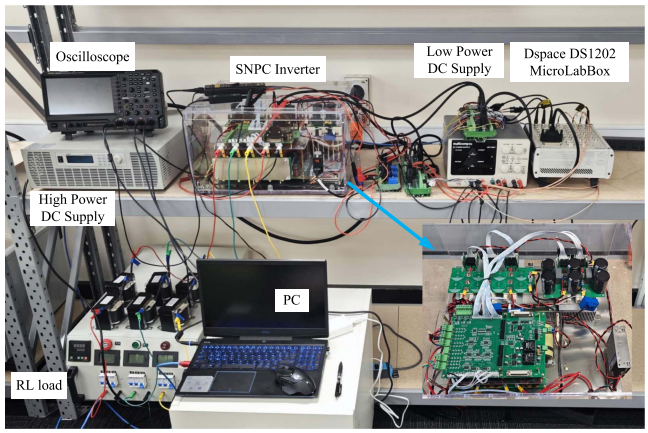


Fig. 6. Experiment system overview.

IV. Experimental Results

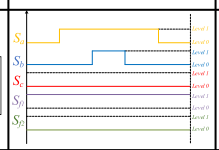
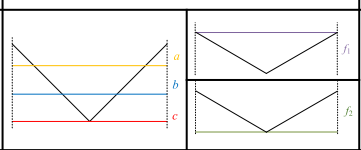
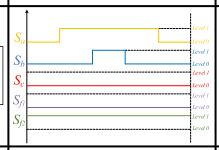
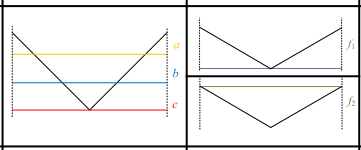
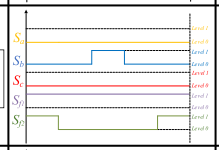
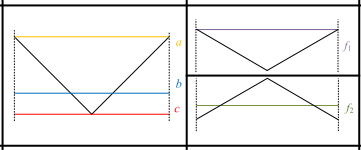
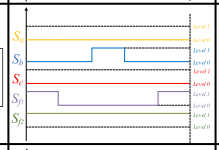
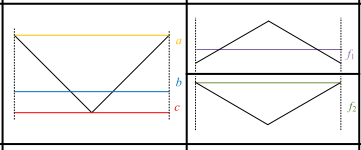
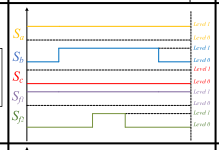
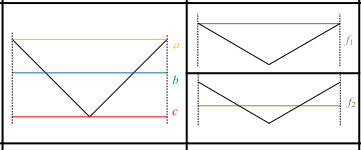
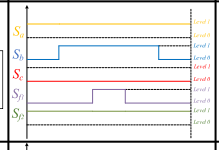
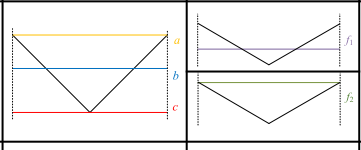
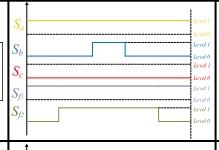
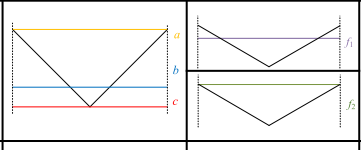
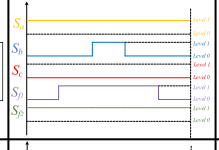
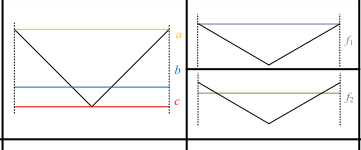
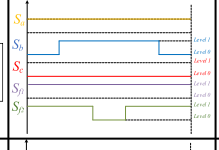
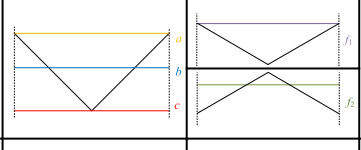
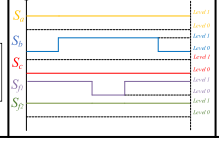
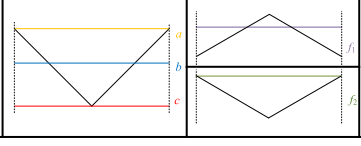
To validate the proposed CBSVM strategy, an experimental setup of the 3L-SNPC inverter is built, as depicted in Fig. 6. The system parameters are provided in Table. IV. The proposed CBSVM strategy is implemented on the NXP QorIQP5020 processor in the dSPACE DS1202 MicroLabBox with a control time period of 200 us. For comparison, two different types of SVM methods [15] and [24] are tested in this experimental setup. Notably, to implement [15] and [24], the NXP QorIQP5020 processor is used for reference VV allocation and duty cycle calculation, while the VV synthesis and gate signals are generated by Xilinx Kintex-7 XC7K325 T in the dSPACE DS1202 MicroLabBox.

A. Computational Performance

The execution time of different methods is first tested to compare their computational complexity. In this case, each modulation scheme is written in C and implemented on a DSP TMS320F28335 with a clock frequency of 150 MHz, and a digital output port is utilized to measure the execution time. Specifically, the level of the digital output port is set to 5 V when the algorithm starts running and reset to 0 V when the modulation scheme execution is finished. The results are shown in Table V.

Compared to the methods in [15] and [24], the proposed method includes VV synthesis and carrier based gate signal generation in the NXP QorIQP5020 processor without utilizing the FPGA. Even with such constrain, the proposed method still reduces the execution time by 43.8% and 23.5%, respectively. This is mainly attributed to the efficient handling of region transitions, where the number of switching sequences in each region remains equal, avoiding unnecessary switching actions during transitions. Additionally, the VV synthesis and duty cycle

TABLE III
CONDITIONS, SWITCHING SEQUENCES, CARRIER FORMS, DUTY CYCLES, AND GATE SIGNALS OF THE PROPOSED METHOD

Region	NPV	Sequence	Gate signal	Carrier compare	Duty cycle
R_1	$\Delta V_{np} > 0$	$V_0\ V_7\ V_9\ V_7\ V_0$			$a = d_3 + d_4$ $b = d_3$ $c = 0$ $f_1 = 1$ $f_2 = 0$
	$\Delta V_{np} < 0$	$V_0\ V_8\ V_{10}\ V_8\ V_0$			$a = d_3 + d_4$ $b = d_3$ $c = 0$ $f_1 = 0$ $f_2 = 1$
R_2	$\Delta V_{np} > 0$	$V_1\ V_7\ V_9\ V_7\ V_1$			$a = 1$ $b = d_4$ $c = 0$ $f_1 = 1$ $f_2 = d_2 + d_3$
	$\Delta V_{np} < 0$	$V_1\ V_8\ V_{10}\ V_8\ V_1$			$a = 1$ $b = d_4$ $c = 0$ $f_1 = d_2 + d_3$ $f_2 = 1$
R_3	$\Delta V_{np} > 0$	$V_7\ V_9\ V_2\ V_9\ V_7$			$a = 1$ $b = d_2 + d_4$ $c = 0$ $f_1 = 1$ $f_2 = d_2$
	$\Delta V_{np} < 0$	$V_8\ V_{10}\ V_2\ V_{10}\ V_8$			$a = 1$ $b = d_2 + d_4$ $c = 0$ $f_1 = d_2$ $f_2 = 1$
R_4	$\Delta V_{np} > 0$	$V_7\ V_1\ V_2\ V_1\ V_7$			$a = 1$ $b = d_2$ $c = 0$ $f_1 = d_2 + d_1$ $f_2 = 1$
	$\Delta V_{np} < 0$	$V_8\ V_1\ V_2\ V_1\ V_8$			$a = 1$ $b = d_2$ $c = 0$ $f_1 = 1$ $f_2 = d_2 + d_1$
R_5	$\Delta V_{np} > 0$	$V_1\ V_2\ V_9\ V_2\ V_1$			$a = 1$ $b = d_2 + d_4$ $c = 0$ $f_1 = 1$ $f_2 = d_4$
	$\Delta V_{np} < 0$	$V_1\ V_2\ V_{10}\ V_2\ V_1$			$a = 1$ $b = d_2 + d_4$ $c = 0$ $f_1 = d_4$ $f_2 = 1$

calculations are performed in the stationary reference frame, further contributing to the reduction in execution time.

B. Steady State Performance

The experimental results, including the line voltage V_{ab}, line currents I_a, and the voltages across both the upper and lower capacitors V_{cp} and V_{cn}, are presented in Fig. 7 The modulation index, defined as $|V_{\text{ref}}|/(2/3\ V_{dc})$, is varied from 0 to 1.

To comprehensively analyze the behavior of the reference VV under varying load conditions, this study examines three representative modulation indices: 0.3, 0.6, and 0.9, corresponding to light, medium, and heavy load conditions, respectively. This selection provides a balanced

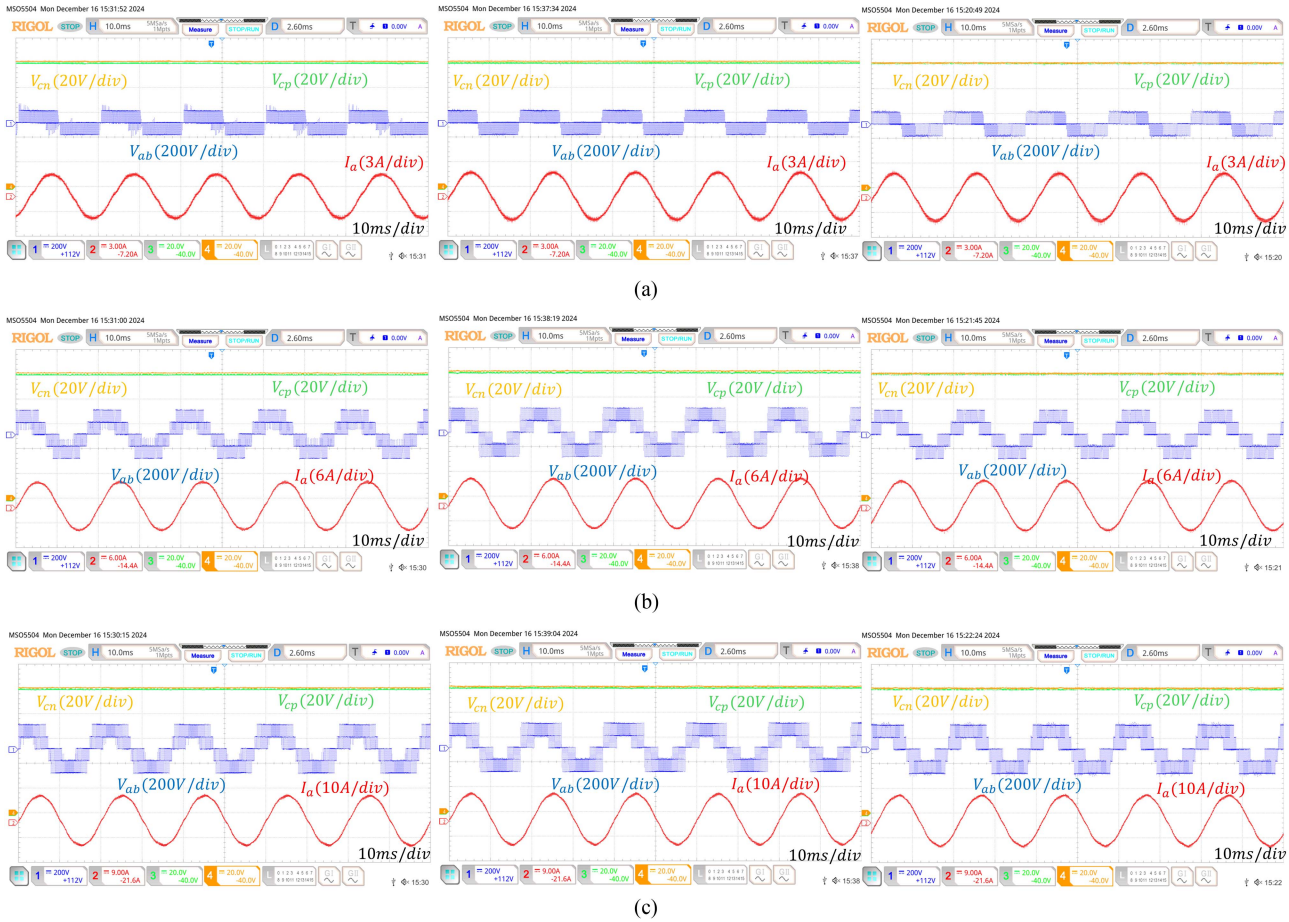


Fig. 7. Experiment results of NPV V_{cp} and V_{cn}, line voltage V_{ab}, line currents I_a, with modulation index at (a) m = 0.3, (b) m = 0.6, (c) m = 0.9. Left column: Method 1 from [15]. Middle column: Method 2 from [24]. Right column: Proposed method.

TABLE IV
EXPERIMENTAL PARAMETERS

Circuit variables	Description	Value
V_{dc}	DC-link voltage	200V
$C_{1/2}$	DC-link capacitance	680 μF
L	Load inductance	10mH
f_s	Switching frequency	5kHz

TABLE V
EXECUTION TIME OF DIFFERENT MODULATION METHODS

Methods	In [15]	In [24]	Proposed
Execution time (μs)	10.05	7.39	5.65

representation across the operational range of the 3L-SNPC inverter.

Fig. 8 demonstrated a zoom-in experimental waveform at m=0.9 for the proposed method. To further assess output waveform quality, the THD of line voltage is calculated for full modulation indices, as illustrated in Fig. 9.

At low modulation index, ranging from 0.1 to 0.5 and representing light load conditions, the reference VV in all three methods, including method 1 and 2 described in [15] and [24], respectively, and the proposed method, exclusively traverses Region 1, the innermost triangular region of the space vector diagram. In this region, the reference VV is synthesized using one zero vector and two small vectors. As shown in Fig. 9, the THD performance trends in this region are notably similar across all methods.

As the modulation index increases to 0.6, indicative of medium load conditions, method-specific behaviors emerge. In the proposed method, the reference VV path extends to encompass regions 2 and 3. Under heavy load conditions, represented by a modulation index of 0.9, the proposed method exhibits a further expanded reference VV trajectory, spanning regions 2, 3, 4, and 5. The proposed method has competitive THD performance at medium load condition with a modulation index ranging from 0.6 to 0.7, and a better performance in heavy load condition for m = 0.8 to 1.0.

Performance of the proposed CBSVM is further examined from the perspective of active NPV balancing capability. The result shown in Fig. 12 demonstrated that all three methods exhibit comparable performance in achieving NPV balance.

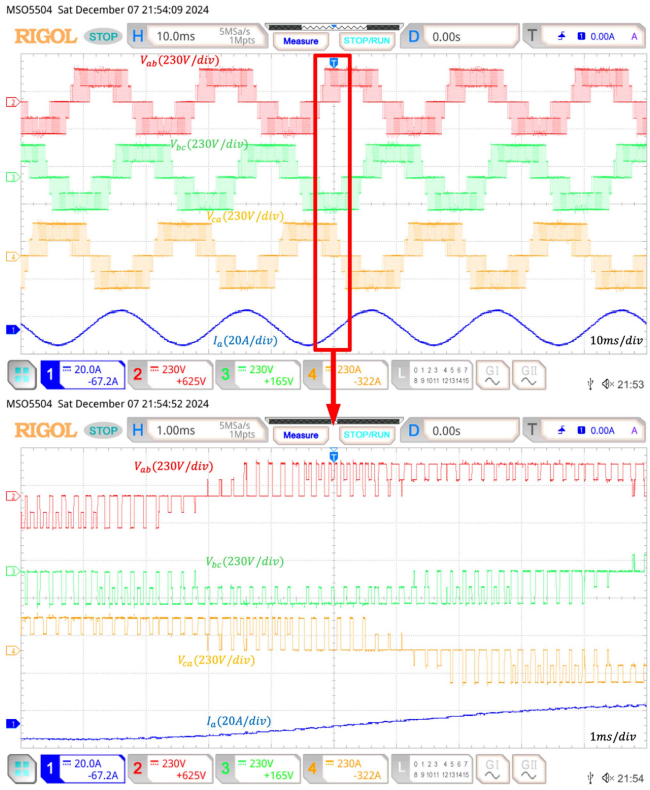


Fig. 8. Zoom-in experimental waveform of the proposed method at m = 0.9.

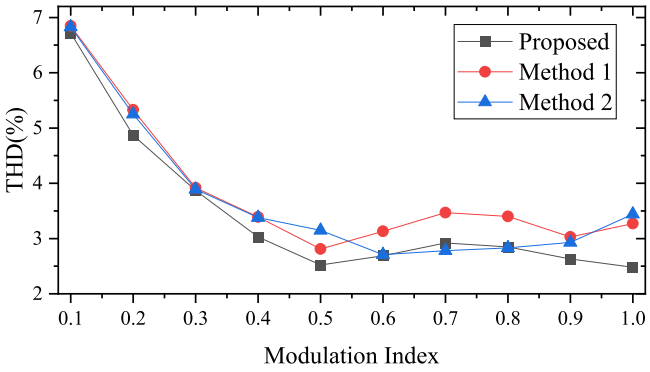


Fig. 9. Comparison of the current THD of the 3L-SNPC Inverter.

This observation suggests that the steady-state NPV balancing capability of proposed CBSVM method aligns closely with that of the other state-of-the-art methods tested.

The selection of specific modulation indices (0.3, 0.6, 0.9) facilitates a systematic comparison of the methods across a wide operational range, highlighting the transitions in reference VV behavior and the associated implications for inverter performance and modulation strategies.

C. Overmodulation Performance

The minimum phase error approach is adopted in the overmodulation region of the proposed method as shown in Fig. 10. The waveform at m=1.15 is presented in Fig. 11, where the

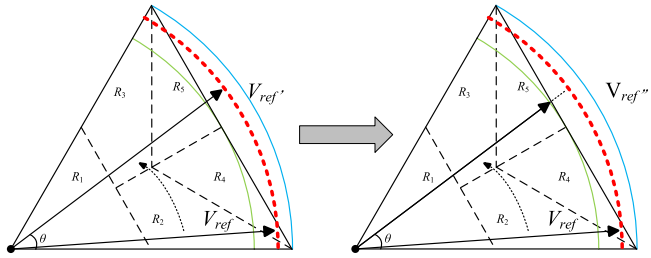


Fig. 10. Minimum phase angle error-based scheme for operating in the overmodulation region.

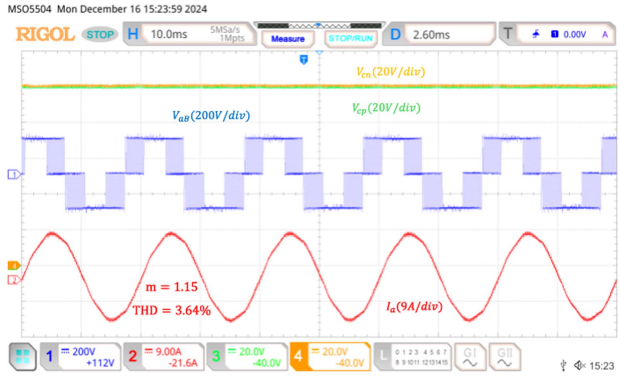


Fig. 11. Overmodulation performance of the proposed method at m = 1.15.

THD of the line current is measured to be 3.64%. These results demonstrate that the proposed method maintains acceptable harmonic performance under overmodulation conditions.

D. Transient Performance

To study the transient NPV balancing performance of the proposed method, an experiment in Fig. 13 was conducted in which the modulation index was linearly varied from 0 to 1 over a period of 0.5 s. This test illustrates the NPV balancing capability of the proposed algorithm, with comparative analysis against method 1 [15] and method 2 [24]. It is seen from this figure that the NPV in all modulation range are well balanced during transients. Three methods have shown similar NPV balancing capabilities in this test.

To evaluate the response capability of the proposed algorithm to sudden changes in the modulation index, the experiment shown in Fig. 14 was conducted. The results demonstrate that the proposed CBSVM exhibits good responsiveness to modulation index transitions, with dynamic response characteristics closely resembling those of state-of-the-art methods. However, a noticeable distinction can be observed in the common mode voltage (CMV): while the CMV performance is comparable to other methods at low modulation indices, the proposed method achieves a significantly sparser CMV pattern at higher modulation indices, indicating a potential advantage in reducing CMV under these conditions.

E. Loss and Efficiency Analysis

A prototype 3L-SNPC inverter was constructed using Infineon IGBT half-bridge modules. The front-end dual-buck converter

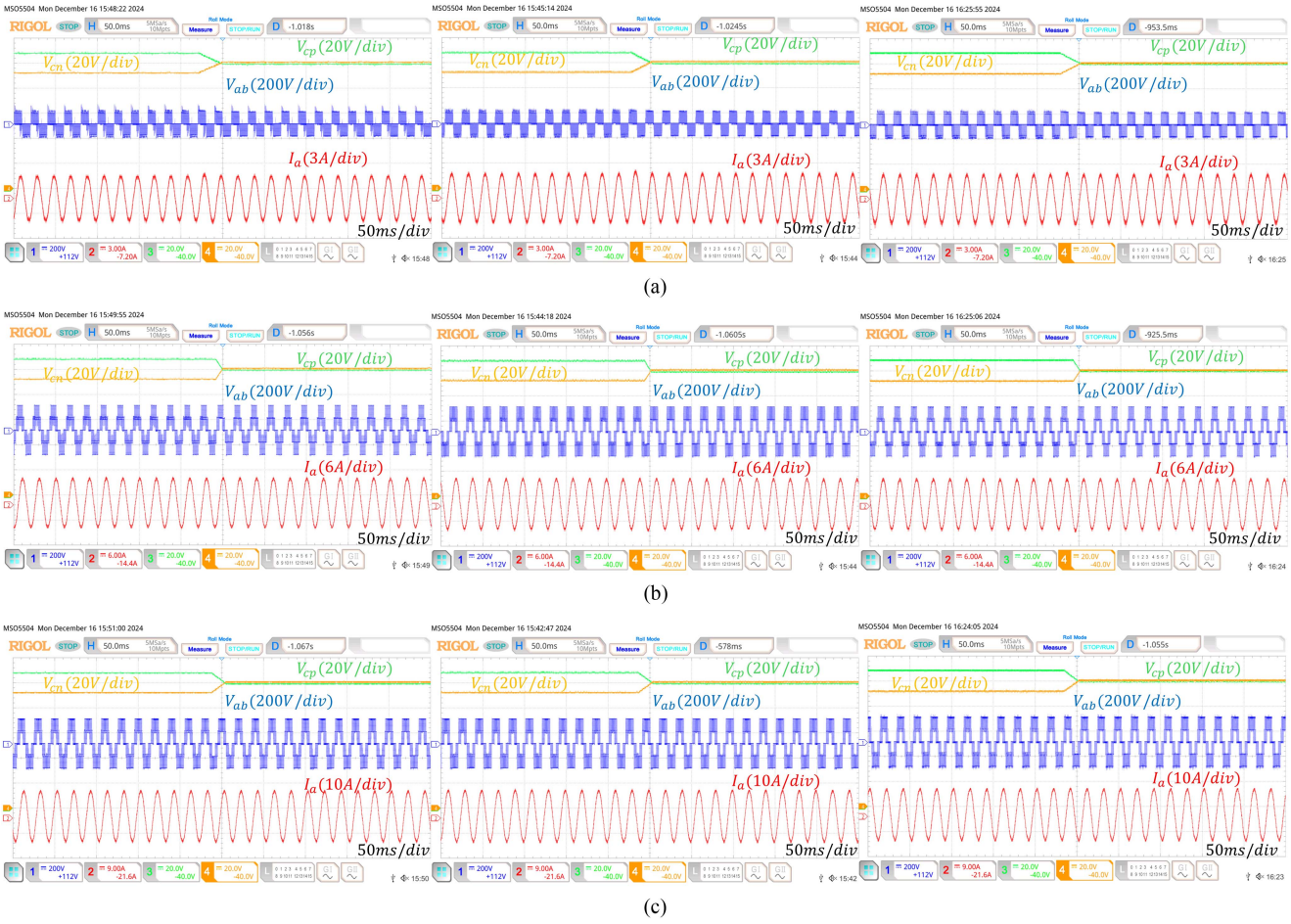


Fig. 12. Active NPV balance capability: Transition from unbalanced ($\Delta V = 20$V) to balanced ($\Delta V = 0$V) condition. NPV V_{cp} and V_{cn}, line voltage V_{ab}, line currents I_a, with modulation index at (a) m = 0.3, (b) m = 0.6, and (c) m = 0.9. Left column: Method 1 from [15]. Middle column: Method 2 from [24]. Right column: Proposed method.

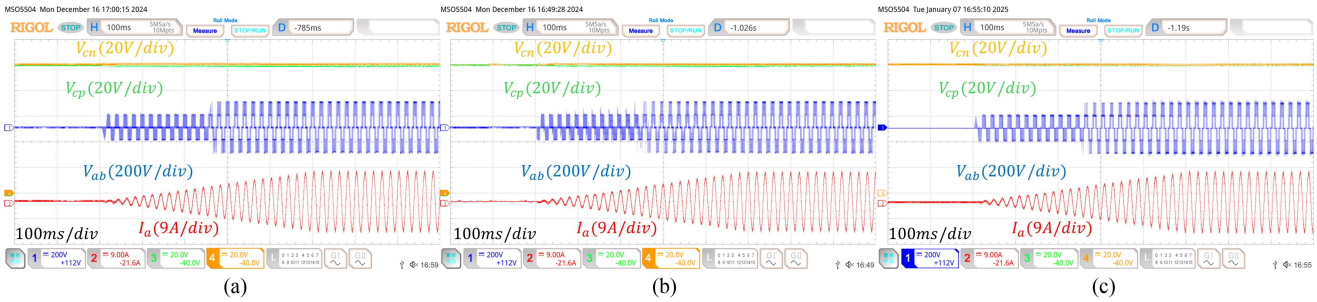


Fig. 13. Dynamic response of NPV balancing under linear modulation index transition from 0 to 1 over 0.5 s. (a) Method 1 from [15]. (b) Method 2 from [24]. (c) Proposed method.

utilized two FF200R06KE3 modules, while the back-end two-level VSI employed three FF200R12KE3 modules. IGBT loss modeling has been thoroughly investigated in many previous studies. The switching loss, total loss, and efficiency for method 1, method 2, and the proposed CBSVM method are shown in Figs. 15, 16, and 17, respectively.

Switching losses were assessed using double-pulse test (DPT) experiments, which included a half-bridge module identical to that used in the inverter, a variable air-core inductor, and a function generator. Following the methodology outlined in [7], the switching and conduction losses were quantified under various operating conditions, with voltages ranging from 100 to 200 V and currents from 1 to 10 A. The losses were further evaluated using the method from [20].

Infrared thermal images of the 3L-SNPC inverter under different methods and load conditions are presented in Fig. 18,

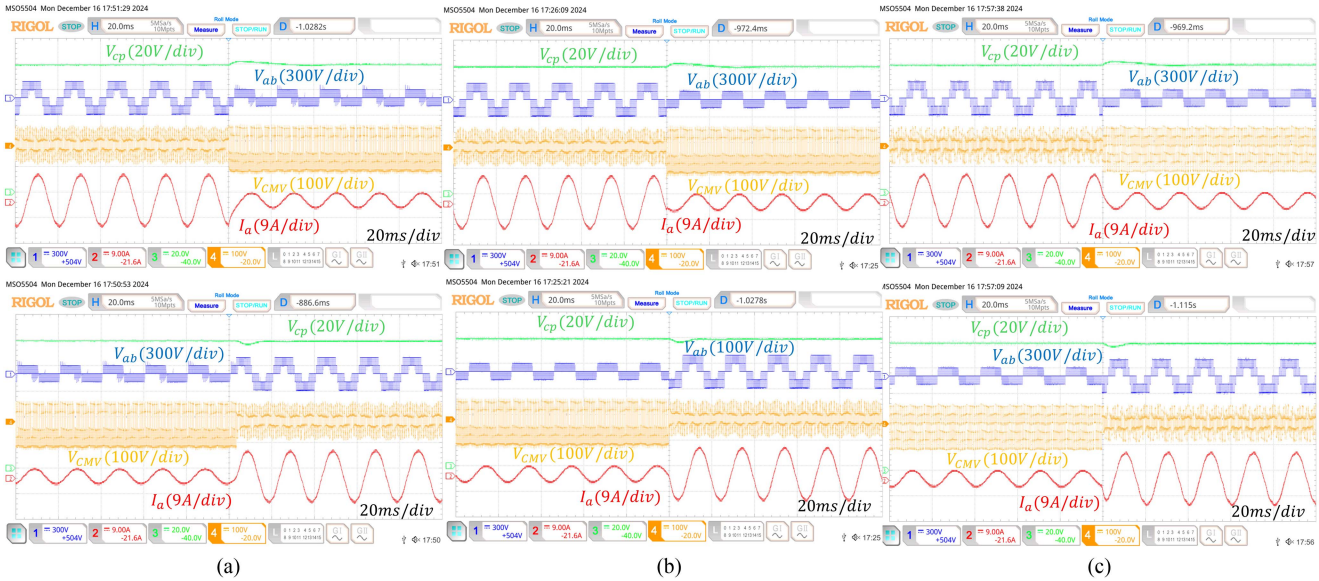


Fig. 14. Transient response of V_{cp}, V_{ab}, common mode voltage (CMV), and I_a during modulation index transitions from 0.9 to 0.3 and 0.3 to 0.9. (a) Method 1 from [15]. (b) Method 2 from [24]. (c) Proposed method.

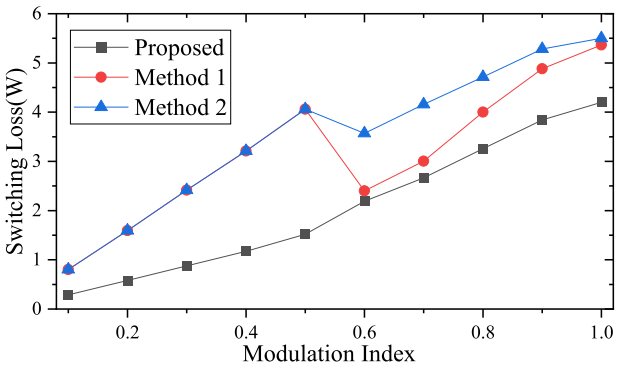


Fig. 15. Switching loss comparison of the 3L-SNPC inverter.

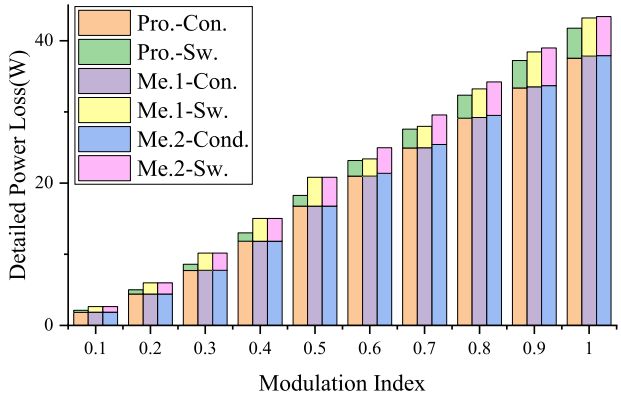


Fig. 16. Comparison of conduction and switching losses across different methods at varying modulation indices for the 3L-SNPC inverter.

where P1–P3 represent the back-end two-level inverter, and P4–P5 represent the front-end dual buck converter. The results have clearly shown that under all tested conditions, the proposed method consistently achieves the lowest temperature. Specifically, at m = 0.9, the proposed method demonstrates a temperature reduction of 4.24% compared to Method 1 [15] and 5.53% compared to Method 2 [24].

This improvement is due to reduced number of switching actions in the proposed modulation, which lowers switching losses. The proposed modulation also achieves even distribution of switching actions within each region, which ensures more balanced temperatures across all modules. In contrast, methods in [15] and [24] clearly show higher temperatures in P4 and P5 due to more frequent switching in the front-end dual buck converter.

As shown in Fig. 15, the proposed method achieves significantly lower switching losses across the full modulation range compared to method 1 [15] and method 2 [24]. Since conduction losses are nearly identical for all three methods within the same circuit topology, as demonstrated in Fig. 16. These reduced switching losses contribute directly to higher overall efficiency, as shown in Fig. 17. This improvement is due to the carrier-based implementation of the proposed method, which consistently synthesizes the reference VV using three VV with five switching sequences in each region.

In contrast, method 1 [15] and method 2 [24] vary their switching sequences across regions, as detailed in [15] and [24]. Method 1 uses seven sequences in Region 1, reduced to five in Regions 2 and 3, then increased to six in Region 4, which corresponds to Regions 4 and 5 combined in the proposed method. Similarly, method 2 applies seven sequences in Region 1, but Region 2 which is equivalent to Regions 2, 3, 4, and 5 combined in the proposed method, is able to utilize 6, 8, or 10 sequences depending on the specific needs. For this analysis, six switching sequences were chosen for Region 2 in Method 2 for a fair comparison and balanced efficiency and performance.

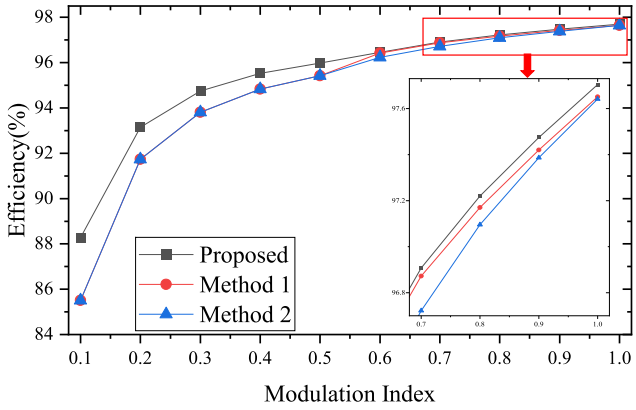


Fig. 17. Efficiency comparison of the 3L-SNPC Inverter.

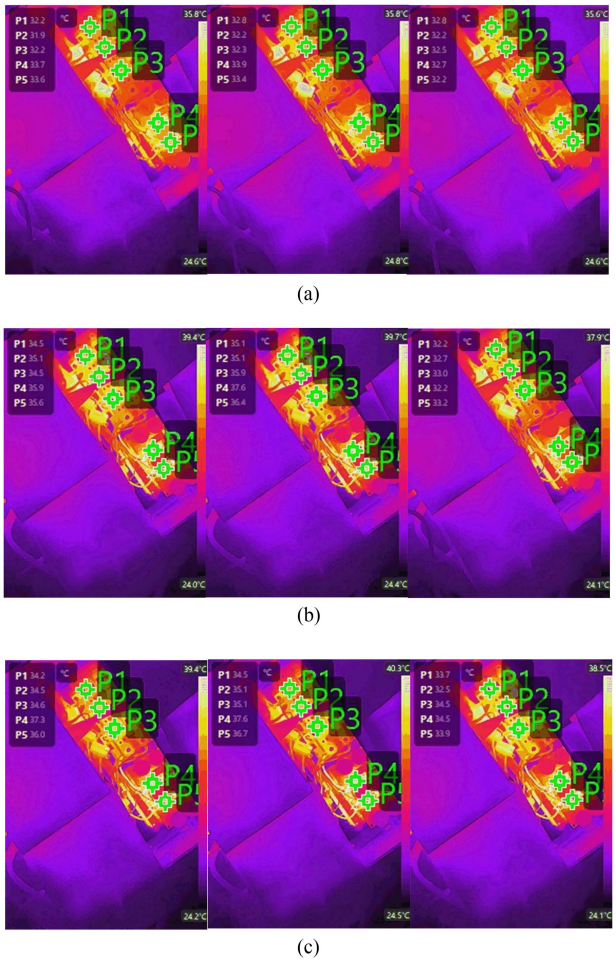


Fig. 18. Infrared thermographs of power devices under different methods with a modulation index at (a) m = 0.3, (b) m = 0.6, and (c) m = 0.9. Left column: Method 1 from [15]. Middle column: Method 2 from [24]. Right column: Proposed method.

The impact of these differences is evident in the switching loss trends. From modulation indices of m = 0 to 0.5, the proposed method consistently shows lower switching losses, following the same upward trend as the other methods as the modulation index increases, highlighting its efficiency across the entire range.

TABLE VI
SUMMARY OF ADVANTAGES OF PROPOSED METHOD

Modulation methods	Execution time	Hardware Requirement	Cost	Loss
Method 1 in [15]	Medium	DSP+FPGA required	High	Medium
Method 2 in [24]	High	DSP+CPLD required	Medium	High
Proposed Method	Low	DSP only	Low	Low

Method 1 experiences a drop in switching loss at m = 0.6 due to a reduction from seven to five switching sequences, but losses increase again from m = 0.8 to 0.9 as the sequence count returns to six, causing the switching loss to approach those of method 2.

For method 2, switching losses drop at m = 0.6 as it shifts from Region 1 to Region 2, reducing the sequence count from seven to six. Beyond m = 0.6, however, switching losses increase with the modulation index, consistent with power demands.

This trend underscores the advantage of the proposed method's consistent approach, maintaining lower switching losses across all modulation indices and achieving higher efficiency. A table is put together that summarized advantages of proposed method below.

The advantages of the proposed method are summarized in Table VI. The proposed CBSVM for the 3L-SNPC inverter significantly reduces execution time by 43.8% compared to method 1 and 23.5% compared to method 2, lowering computational complexity. The proposed method requires only a DSP, eliminating the need for FPGA or CPLD, which reduces hardware costs. In terms of switching loss, the proposed method outperforms other methods across the full modulation range, particularly at medium and high modulation indices. For instance, at m = 0.5, switching losses are reduced by 62.5%, at m = 0.6, by 8.8% and 38.7%; and at m = 0.9, by 21.3% and 27.3% compared to methods 1 [15] and 2 [24]. These advantages are achieved without any compromise on steady-state or transient performance, such as THD or NPV balancing, making the proposed method an efficient and cost-effective solution for 3L-SNPC inverters.

V. CONCLUSION

This article introduces a novel CBSVM for the 3L-SNPC inverter. The proposed CBSVM significantly reduces the implementation costs and complexity, thereby addressing a notable deficiency in the existing literature. Moreover, this work pioneers a comprehensive inverter loss and performance analysis of the 3L-SNPC inverter under the CBSVM. Experimental comparisons with the existing SVM methods for the 3L-SNPC inverter unequivocally affirm the efficacy of the proposed method from the perspectives of superior efficiency and lower THD. This positions the proposed CBSVM strategy as a viable, cost-efficient, and efficacious solution for the 3L-SNPC inverter.

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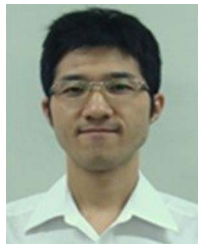

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