A High-Efficiency MHz-Integrated Three-Phase Interleaved Boost–*LLC* Converter With Voltage Regulation

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***Abstract*—Three-phase interleaved *LLC* can achieve high-efficiency and low-ripple conversion, but it is difficult to reach a wide voltage regulation range due to the difficulty of synchronous rectification. Based on the principle of bridge arm multiplexing, this article proposes a three-phase interleaved boost and three-phase interleaved *LLC* integrated topology. The integrated topology adopts a modulation strategy in which the duty and frequency change cooperatively, which can achieve decoupling of boost and *LLC* and smooth gain. Among them, the boost works in the forced continuous conduction mode, using the inductor current to realize zero-voltage turn-ON of all switching devices, which can realize an air-gap-free transformer design and help reduce winding losses. Based on the modal analysis, this article gives the switching function of the proposed topology to achieve synchronous rectification in the voltage regulation range. Furthermore, this article analyzes the effect of the transformer ratio on device stress and provides an optimization strategy for integrated transformers. Finally, a prototype with a switching frequency of 1 MHz, 40–60-V input, and 400-V at 1.5-kW output was designed to verify the proposed topology and the modulation strategy, achieving a full-load efficiency of 97.7% and a power density of 159 W/in^3.**

***Index Terms*—High frequency, integrated converter, three-phase interleaved *LLC*, voltage regulation.**

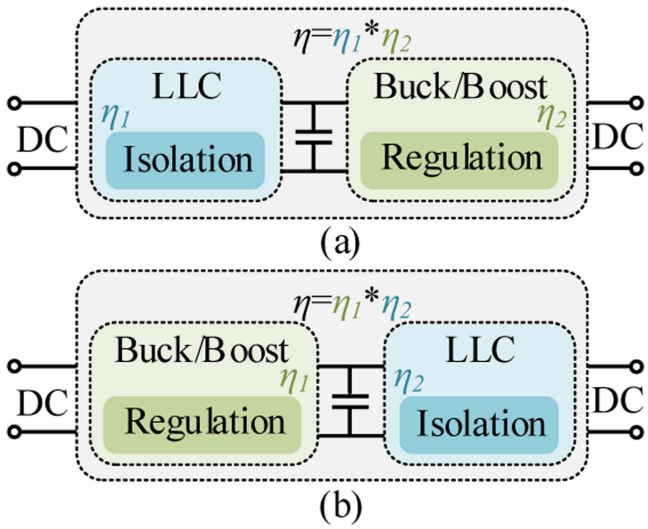

Fig. 1. Two two-stage voltage regulation structures. (a) *LLC* + buck/boost. (b) Buck/boost + *LLC*.

I. Introduction

TO INCREASE power density, the switching frequency can usually be increased to reduce the size of passive components. However, the higher the switching frequency, the greater the switching losses. To achieve high-efficiency and high-power-density conversion, *LLC* is widely used because it can realize soft switching of primary- and secondary-side devices [1], [2], [3], [4], [5], [6], [7]. Furthermore, to improve power capacity and reduce current ripple, three-phase interleaved *LLC* is widely used [8], [9], [10], [11], [12], [13], [14]. However, three-phase interleaved *LLC* also needs to adjust the gain by changing the frequency, which makes it difficult to achieve a wide voltage regulation range. There are two main reasons for this: 1) when the switching frequency changes, it is difficult to implement synchronous rectification on the secondary side; and 2) the wide frequency variation range is not conducive to designing magnetic components.

Therefore, many studies adopt a two-stage structure to achieve voltage regulation (see Fig. 1). Many studies use buck or boost as the voltage regulation stage, and *LLC* works in the quasi-resonant mode [15], [16], [17], [18], [19], [20]. In [18], the front stage uses *LLC* to work at a fixed frequency, and buck is used to realize voltage regulation. Similarly, Jin et al. [19], [20] added a four-phase interleaved buck circuit after three-phase interleaved *LLC* to achieve a wide voltage regulation range. The two-stage structure can achieve power decoupling and simple control. However, this voltage regulation method requires many power devices. Moreover, the wide bus voltage is not conducive to the design of the transformer, and there may be a large magnetizing current that increases losses.

Received 13 September 2024; revised 9 November 2024 and 29 December 2024; accepted 28 January 2025. Date of publication 3 February 2025; date of current version 20 March 2025. This work was supported by the Fundamental Research Funds for the Central Universities, HUST under Grant 2024JYCXJJ044. Recommended for publication by Associate Editor H. S. Krishnamoorthy. *(Corresponding author: Cai Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3537657.

Digital Object Identifier 10.1109/TPEL.2025.3537657

In the two-stage structure, three-phase interleaved *LLC* operates in the quasi-resonant mode, the switching frequency is fixed, and the voltage regulation stage achieves a wide voltage regulation range. However, the two-stage structure has too many energy processing stages, which will greatly affect the cost and efficiency.

To improve the efficiency of the converter and reduce the number of components, some studies have proposed an integrated topology based on the principle of bridge arm multiplexing. Jeong et al. [21] and York et al. [22] proposed an integrated boost–*LLC* structure for single-phase *LLC*, reducing the number of devices by multiplexing the boost and *LLC* bridge arms. Integrated two-phase interleaved parallel boost *LLC* (IIBLLC) is proposed in [23] and [24], which uses two-phase interleaved boost as the regulating stage and multiplexes the primary-side bridge arm with full-bridge *LLC*, which can reduce the number of switching devices. However, when the duty is not equal to 0.5, *LLC* will work in the over-resonant mode, which is not conducive to achieving synchronous rectification. In [25], the duty cycle is fixed to 0.5, which can achieve zero input current ripple. However, *LLC* has a wide frequency range, and it is difficult to achieve high efficiency. To reduce the size of passive components, Deng et al. [26] proposed a method of integrating high-frequency passive components, which can greatly improve the power density. To solve the problem of dead time asymmetry caused by IIBLLC soft-switching current asymmetry, Wen et al. [27] proposed an iterative calculation dead time compensation strategy. Based on IIBLLC, Wu et al. [28] added an inductor, which not only improved the power reverse transmission characteristics but also achieved smooth gain adjustment. However, since boost operates in the continuous current mode (CCM), a large magnetizing current is still required to achieve soft switching of the lower switching device. To optimize the loss and soft-switching characteristics, Xu et al. [29] proposed digital adaptive frequency modulation. However, limited by parameter design, the power density and efficiency of the prototype are low. The authors in [30], [31], and [32] proposed integrating buck–boost with half-bridge *LLC* and adjusting the gain through phase shifting. However, there are problems with soft-switching current and secondary-side current asymmetry under the proposed modulation. Furthermore, Wang et al. [33] proposed a two-phase buck–boost and full-bridge *LLC* integrated topology, which solved the current asymmetry problem in single phases by interleaving.

Although the integrated topology can reduce the number of devices, it will introduce new modulation problems. Different modulation strategies impact the secondary-side synchronous rectification, soft-switching characteristics, and gain characteristics greatly.

Based on the principle of bridge arm multiplexing, to achieve wide voltage regulation range of three-phase interleaved *LLC*, this article proposes an integrated three-phase boost–*LLC* topology (as shown in Fig. 2). After adding the three-phase interleaved boost circuit, the primary-side bridge of three-phase interleaved *LLC* and the bridge of three-phase interleaved boost can be multiplexed. Therefore, it is equivalent to adding only three inductors to achieve a wide voltage regulation range. Furthermore, this

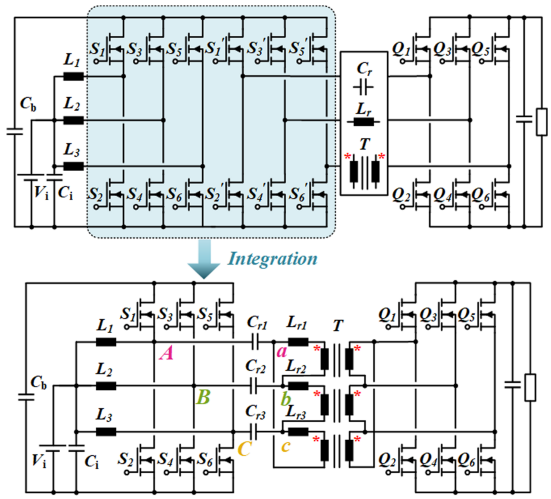

Fig. 2. Proposed three-phase integrated boost–*LLC* topology.

article proposes a modulation strategy for the proposed topology with coordinated changes in frequency and duty. The implementation method of synchronous rectification, soft-switching characteristics, and gain characteristics of the proposed topology are analyzed. The characteristics of the proposed modulation are as follows.

1) The time of the positive half-cycle or negative half-cycle of the resonant current is always equal to half of the resonant period, and the sum of the two times is equal to the resonant period. This means that even if the switching frequency changes, three-phase interleaved *LLC* always works in a quasi-resonant mode and has high efficiency.
2) Since three-phase interleaved *LLC* operates in a quasi-resonant mode, it is easy to achieve synchronous rectification of the secondary-side devices. However, unlike traditional integrated boost *LLC*, the secondary- and primary-side drive timings are the same. The synchronous rectification timing of integrated three-phase interleaved boost *LLC* is different from the primary side. Combined with the switching mode of the primary side, this article analyzes the timing sequence of synchronous rectification under different input voltages and gives the switching function.
3) Boost works in the forced continuous conduction mode (FCCM) using inductor current to achieve soft switching of switching devices. No magnetizing current is required to achieve zero-voltage switching (ZVS), so the transformer does not require an air gap, which can further reduce winding losses [31]. It is worth noting that when there is no magnetizing current, the resonant part is equivalent to a series-resonant converter. Considering that the magnetizing current can also be used to assist in soft switching, this article still calls it *LLC*.
4) Due to the large magnetizing inductance, the gain of three-phase interleaved *LLC* can be approximately 1 under all operating conditions through appropriate design. Therefore, the overall gain of the topology is only related to the

duty cycle of the three-phase boost, which is conducive to continuous and smooth voltage regulation.

To reduce current stress, this article provides optimization methods for the transformer ratio and chopper inductance. Furthermore, to improve the efficiency and power density of the prototype, this article uses a three-phase integrated transformer. The volume and loss of the integrated transformer are optimized based on the loss model and the size model.

Finally, a 1.5-kW prototype with a switching frequency of 1 MHz was designed to verify the proposed topology and the modulation strategy. Soft switching is achieved in the full voltage range, and synchronous rectification of the secondary side is also achieved. The prototype achieved a full-load efficiency of 97.7% and a power density of 159 W/in^3. The prototype can be used in photovoltaic power generation. The output voltage and power of photovoltaic panels are not stable and are affected by many factors. Therefore, an isolated dc/dc is needed to achieve a stable output voltage.

The rest of this article is organized as follows. Section II introduces the modulation strategy of cooperatively changing duty and frequency and analyzes the synchronous rectification strategy. Section III analyzes the soft-switching characteristics and the system gain. Section IV gives the transformer ratio and the current stress optimization method, proposes a three-phase integrated transformer structure and optimization model, and verifies it through simulation. Section V gives the experimental results of the 1.5-kW prototype, which verifies the previous theoretical analysis. Finally, Section VI concludes this article.

II. Modulation Strategy and Synchronous Rectification

After the three-phase boost is integrated with three-phase *LLC*, the number of switching devices can be reduced by one-third. However, the duty needs to be changed to achieve voltage regulation, which will affect the working mode of three-phase interleaved *LLC*. Assuming that the switching frequency is constant and equal to the resonant frequency. When the duty is 0.5, the operating mode of three-phase interleaved *LLC* is no different from that without integration [12]. When the duty cycle is not 0.5, the operating mode of three-phase interleaved *LLC* will be changed.

Taking the duty less than 0.5 as an example, the key waveform is shown in Fig. 3. The driving waveforms of the three half-bridges have a phase difference of 120°, and the driving waveforms of the upper and lower switches on the same bridge are complementary. The resonant period of the resonant element is T_r. Taking phase A as an example, in the positive half-period, due to the reduction in the duty cycle, the high-level time is less than $0.5{*}T_r$. The resonant current does not have a complete half-resonant period $[t_0, t_1]$. After the upper switch is turned OFF, the resonant current quickly drops to zero within the dead time $[t_1, t_3]$. At this time, it is equivalent to being in the over-resonant mode, and the turn-OFF current of the secondary-side device is large. In the negative half-period, the low-level time is greater than $0.5{*}T_r$; the resonant current will

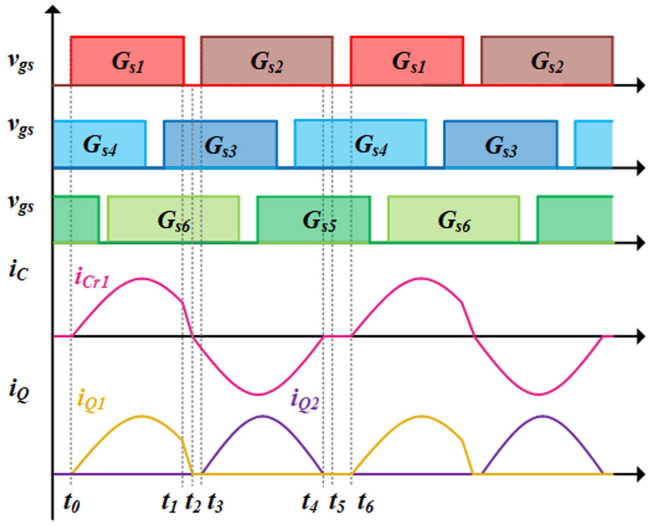

Fig. 3. Key waveforms of three-phase interleaved *LLC* when the duty is less than 0.5.

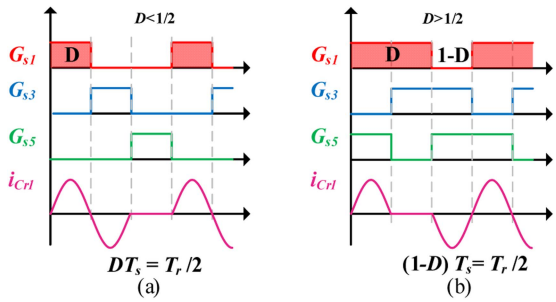

Fig. 4. Modulation of frequency as a function of the duty cycle. (a) $D < 1/2$. (b) $D > 1/2$.

have a complete half-resonant cycle $[t_3, t_4]$ and then be in the current discontinuous mode $[t_4, t_6]$. At this time, it is equivalent to the under-resonant mode, and it is also difficult to achieve better synchronous rectification. It can be seen that when the duty cycle is not equal to 0.5, three-phase interleaved *LLC* operates in the under-resonant mode or the over-resonant mode, which is not conducive to achieving high-frequency and secondary-side synchronous rectification.

A. Frequency and Duty Cycle Coordinated Modulation Strategy

According to the previous analysis, when the switching frequency is unchanged, changes in the duty will cause changes in the resonant mode, which is not conducive to achieving high-frequency work. When the duty changes, three-phase interleaved *LLC* is under-resonant mainly because the high-level time is less than $0.5{*}T_r$. Therefore, this article proposes a modulation strategy in which the duty and frequency change cooperatively. Taking the duty cycle less than 0.5 as an example, as shown in Fig. 4(a), when the duty cycle changes, the switching frequency changes accordingly to ensure that the high-level time is equal to

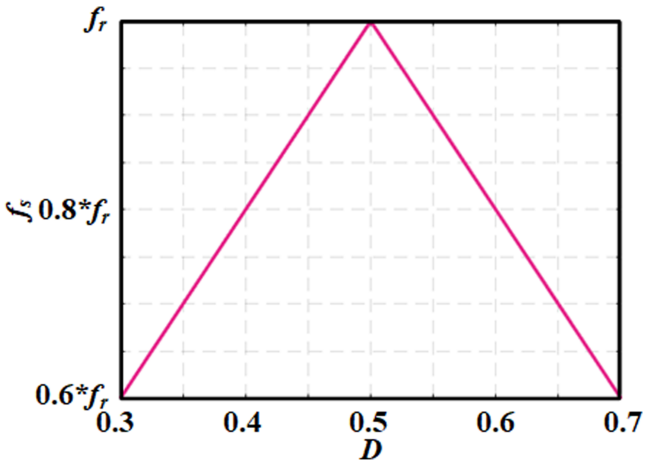

Fig. 5. Relationship between switching frequency and duty.

the half-resonant period (1). Among them, T_s is the switching period, and f_r is the resonant frequency. Therefore, the relationship between switching frequency and duty, as shown in Fig. 5, can be obtained (2). When the duty is 0.5, the switching frequency is equal to the resonant frequency. Three-phase interleaved *LLC* operates in the resonant mode, and the resonant element has a complete resonant period. When the duty cycle is not equal to 0.5, the switching frequency can be changed so that the resonant element still has a complete resonant period (2). This means that even if the duty changes, three-phase interleaved *LLC* still operates in the quasi-resonant mode, which is beneficial to the secondary side to achieve synchronous rectification. It can be seen that the proposed modulation is equivalent to inserting a certain length of zero-level time based on the resonance period

$$\begin{cases} DT_s = 0.5T_r = 0.5/f_r, & D \le 0.5 \\ (1-D)T_s = 0.5T_r = 0.5/f_r, & D > 0.5 \end{cases} \tag{1}$$

$$\begin{cases} f_s = 2Df_r, & D \le 0.5 \\ f_s = 2(1-D)f_r, & D > 0.5. \end{cases} \tag{2}$$

B. Analysis of Synchronous Rectification

The difference between the proposed modulation and three-phase interleaved *LLC* operating in the quasi-resonant mode is that a certain length of zero-level time is inserted. Therefore, the zero-level time in each mode can be calculated, and the ON–OFF signal of the secondary side can be adjusted to achieve synchronous rectification. Depending on the duty, the driving signal of the secondary-side switching device needs to be discussed in four cases: [0, 1/3], [1/3, 1/2], [1/2, 2/3], and [2/3, 1]. The key waveforms for each case are shown in Fig. 6. To simplify the analysis, the following analysis takes the duty cycle less than one-third and phase A as an example (as shown in Fig. 7), ignoring the influence of dead time.

Mode I (t_0, t_1): S_1, S_4, and S_6 are turned ON. C_{r1} starts to charge, and C_{r3} has been charged at the previous moment. Since S_6 is turned ON, C_{r3} starts to discharge. $i_{Cr1} = -i_{Cr3}$. Therefore,

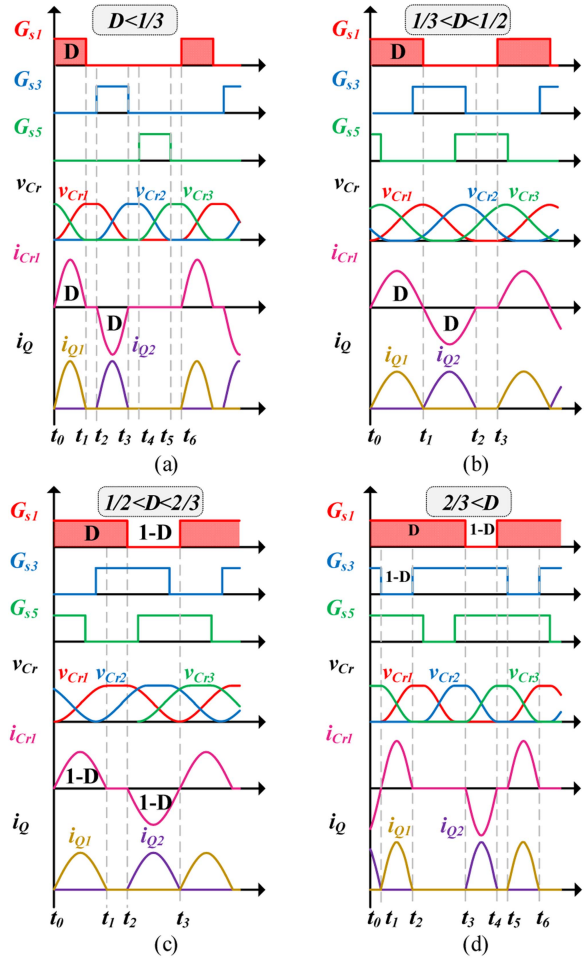

Fig. 6. Key waveforms under different duty cycles. (a) $D < 1/3$. (b) $1/3 < D < 1/2$. (c) $1/2 < D < 2/3$. (d) $2/3 < D$.

there is no current in phase B, and the capacitor voltage remains at 0. Due to the change of switching frequency, $DT_s = 0.5*f_r$, so the resonant current of phase A has a complete half-resonance cycle.

Mode II (t_1, t_2): S_2, S_4, and S_6 are turned ON. The resonant current of phase A enters the discontinuous mode, and the capacitor voltage remains unchanged. The zero-level time at this stage is $(1/3\text{-}D)*T_s$.

Mode III (t_2, t_3): S_2, S_3, and S_6 are turned ON. The resonant capacitor of phase A begins to discharge, and the resonant current enters the negative half-cycle, $DT_s = 0.5*f_r$, so the resonant current of phase A has a complete half-resonant cycle.

Mode IV (t_3, t_4): S_2, S_4, and S_6 are turned ON. This mode is the same as Mode II, where the resonant current enters the discontinuous mode, and the capacitor voltage remains unchanged. The zero-level time at this stage is $(1/3\text{-}D)*T_s$.

Mode V (t_4, t_5): S_2, S_4, and S_5 are turned ON. This mode is similar to Mode I. C_{r3} charges, C_{r2} discharges, and the currents are equal. There is no current in phase A, so the capacitor voltage remains unchanged. The zero-level time in this stage is $D*T_s$.

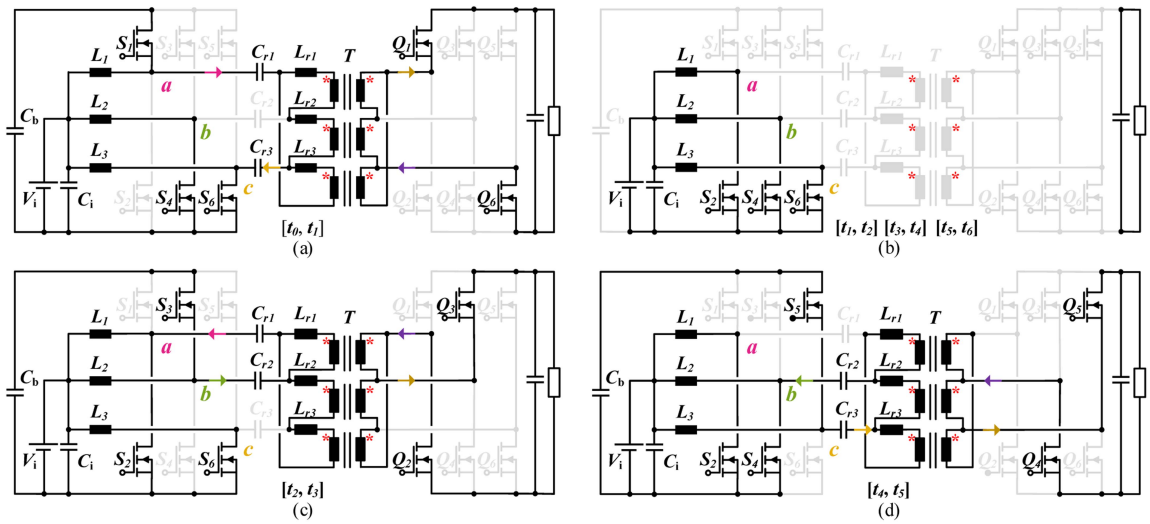

Fig. 7. Equivalent circuits in different working modes. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$, $[t_3, t_4]$, $[t_5, t_6]$. (c) $[t_2, t_3]$. (d) $[t_4, t_5]$.

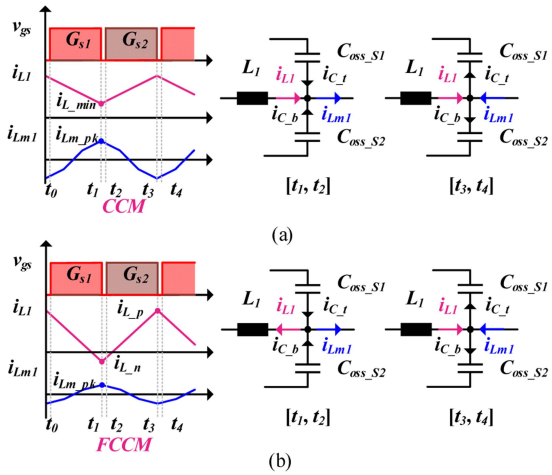

Fig. 8. Comparison of soft-switching currents under different modulations. (a) CCM. (b) FCCM.

Mode VI (t_5, t_6): S_2, S_4, and S_6 are turned ON. This mode is the same as Modes II and IV. The resonant current enters the discontinuous mode, and the capacitor voltage remains unchanged. The zero-level time at this stage is (1/3-D)$*T_s$.

Based on the aforementioned analysis, the synchronous rectification switching function of phase A can be obtained (3). Based on the same method, the zero-level time inserted in different stages can be calculated to obtain the synchronous rectification functions in the other three cases (4)–(6)

$$\text{when} \quad D \in \left(0, 1/3\right]$$

$$\begin{cases} G_{\mathrm{Q1\_on}} = G_{\mathrm{S1\_on}} \\ G_{\mathrm{Q1\_off}} = G_{\mathrm{S1\_off}} \end{cases}$$

$$\begin{cases} G_{\mathrm{Q2\_on}} = G_{\mathrm{S2\_on}} + (1/3 - D)Ts \\ G_{\mathrm{Q2\_off}} = G_{\mathrm{S2\_off}} - (2/3 - D)Ts \end{cases} \tag{3}$$

$$\text{when} \quad D \in \left(1/3, 1/2\right]$$

$$\begin{cases} G_{\mathrm{Q1\_on}} = G_{\mathrm{S1\_on}} \\ G_{\mathrm{Q1\_off}} = G_{\mathrm{S1\_off}} \end{cases}$$

$$\begin{cases} G_{\mathrm{Q2\_on}} = G_{\mathrm{S2\_on}} \\ G_{\mathrm{Q2\_off}} = G_{\mathrm{S2\_off}} - (1 - 2D)Ts \end{cases} \tag{4}$$

$$\text{when} \quad D \in \left(1/2, 2/3\right]$$

$$\begin{cases} G_{\mathrm{Q1\_on}} = G_{\mathrm{S1\_on}} \\ G_{\mathrm{Q1\_off}} = G_{\mathrm{S1\_off}} - (2D - 1)Ts \end{cases}$$

$$\begin{cases} G_{\mathrm{Q2\_on}} = G_{\mathrm{S2\_on}} \\ G_{\mathrm{Q2\_off}} = G_{\mathrm{S2\_off}} \end{cases} \tag{5}$$

$$\text{when} \quad D \in \left(2/3, 1\right)$$

$$\begin{cases} G_{\mathrm{Q1\_on}} = G_{\mathrm{S1\_on}} + (D - 2/3)Ts \\ G_{\mathrm{Q1\_off}} = G_{\mathrm{S1\_off}} - (D - 1/3)Ts \end{cases}$$

$$\begin{cases} G_{\mathrm{Q2\_on}} = G_{\mathrm{S2\_on}} \\ G_{\mathrm{Q2\_off}} = G_{\mathrm{S2\_off}}. \end{cases} \tag{6}$$

III. Soft Switching and Gain Analysis

A. Analysis of the Soft-Switching Strategy

The front stage is boost, and the latter stage is three-phase interleaved *LLC*. The soft switching is realized differently depending on the boost operating mode: 1) boost works in the CCM; and 2) boost works in the FCCM.

1) Boost Works in the CCM, and the Key Waveforms are Shown in Fig. 8(a): Mode I ($[t_1, t_2]$): During the dead time

after the upper switch is turned OFF, the current of the boost inductor flows into the switch node, and the magnetizing current flows out of the switch node. According to Kirchhoff's law, it can be known that the inductor current is not conducive to realizing soft switching. The equivalent soft-switching current is the difference between the magnetizing current and the boost inductor current (7) and (8). Therefore, a large magnetizing current is required to achieve soft switching, which will increase winding loss. In addition, a large magnetizing current means a small magnetizing inductance. This requires a large air gap, which increases losses due to fringing flux (9)

$$i_{Lm1} = i_{L1} + i_{C\_t} + i_{C\_b} \tag{7}$$

$$i_{\text{soft\_sw}} = i_{Lm1} - i_{L1} = i_{Lm\_pk} - i_{L\_\min} \tag{8}$$

$$L_m = \frac{\mu_r \mu_0 N^2 A_e}{l_g}. \tag{9}$$

Mode II ([t_3, t_4]): During the dead time after the lower switch is turned OFF, the current of the boost inductor flows into the switch node, and the magnetizing current flows into the switch node. According to Kirchhoff's law, the current of the boost inductor is conducive to realizing soft switching, and the equivalent soft-switching current is the sum of the magnetizing current and the inductor current as follows:

$$i_{\text{soft\_sw}} = i_{Lm1} + i_{L1}. \tag{10}$$

2) Boost Works in the FCCM, and the Key Waveforms are Shown in Fig. 8(b): Mode I ([t_1, t_2]): During the dead time after the upper switch is turned OFF, the magnetizing current flows out of the switch node. Since the current of the boost inductor is reversed, the current flows out of the switch node. According to Kirchhoff's law, the current of the boost inductor is conducive to realizing soft switching, and the equivalent soft-switching current is the sum of the magnetizing current and the boost inductor current as follows:

$$i_{\text{soft\_sw}} = i_{Lm\_pk} + |i_{L\_n}|. \tag{11}$$

Mode II ([t_3, t_4]): This mode is the same as when boost works in the CCM. The current of the boost inductor is conducive to achieving soft switching, and the equivalent soft-switching current is the sum of the magnetizing current and the inductor current (10).

According to the previous analysis, after the boost operates in the FCCM, the current of the boost inductor during the dead time is conducive to achieving soft switching. Furthermore, to reduce the winding losses caused by the magnetizing current and the eddy losses caused by the fringe flux, this article adopts an air-gap-free transformer design and uses the boost inductor current to achieve zero-voltage turn-ON of all devices.

During the dead time after the lower switch is turned OFF, the inductor current reaches the positive peak value (I_{L_p}). The current freewheels through the body diode of the upper switch, and the upper switch can achieve zero-voltage turn-ON. During the dead time after the upper switch is turned OFF, the boost inductor current reaches the negative peak value (I_{L_n}), charging and discharging the junction capacitor. According to (12)–(14), the absolute value of I_{L_p} is always greater than that of I_{L_n}. Therefore, the charge that the inductor can provide (Q_{td}) during the dead time (t_d) needs to be greater than the charge required to achieve soft switching (Q_{tot}) (15). According to (12)–(15), the maximum inductance value that meets the soft-switching conditions can be obtained (16)

$$I_{L\_\text{avg}} = \frac{P}{3V_i} \tag{12}$$

$$\Delta I = \frac{V_i(1-D)}{Lf_s} \tag{13}$$

where I_{L_avg} is the average current of the inductor, P is the input power, V_i is the input voltage, ΔI is the ripple current of the boost inductor, and L is the boost inductance

$$\begin{cases} I_{L\_p} = I_{L\_\text{avg}} + 0.5\Delta I \\ I_{L\_n} = I_{L\_\text{avg}} - 0.5\Delta I \end{cases} \tag{14}$$

$$\begin{cases} Q_{td} = \int_0^{td} -I_{L\_n} dt \\ Q_{\text{tot}} = 2C_p V_b + 2C_s V_b / n^2 \end{cases} \tag{15}$$

where C_p is the output junction capacitance of the primary-side switching device, C_s is the output junction capacitance of the secondary-side switching device, V_b is the bus voltage, and n is the transformer ratio.

$$\begin{aligned} L &< \frac{V_i(1-D)t_d}{2f_s(Pt_d/(3V_i) + 2C_pV_b + 2C_sV_b/n^2)} \\ \Rightarrow L &< \frac{3D(1-D)t_d n^2 {V_i}^2}{2Df_sPt_dn^2 + 12f_sC_pn^2{V_i}^2 + 12f_sC_s{V_i}^2}. \end{aligned} \tag{16}$$

B. Gain Analysis of the Topology

The system gain can be analyzed based on the two-stage structure. To simplify the analysis, the normalized gains G_{bb}, G_{LLC}, and G_{tot} are defined as follows:

$$\begin{cases} G_{bb} = V_b/V_i \\ G_{LLC} = nV_o/V_b \\ G_{\text{tot}} = nV_o/V_i = G_{bb}G_{LLC}. \end{cases} \tag{17}$$

The gain of boost working in the FCCM is the same as that of the CCM. Its gain can be obtained according to the inductor volt–second balance

$$G_{bb} = 1/D. \tag{18}$$

When the three phases are balanced, one of the phases can be taken out for analysis after star–delta transformation [12] (as shown in Fig. 9). When boost works in the FCCM, the magnetizing inductor can be designed to be large. At a high inductance ratio (the ratio of magnetizing inductance to resonant inductance), the relationship between the fundamental gain of the resonant tank and the switching frequency is shown in Fig. 10.

It can be seen that when the switching frequency is not higher than the resonant frequency, the normalized gain of the resonant tank does not change with the switching frequency in a wide

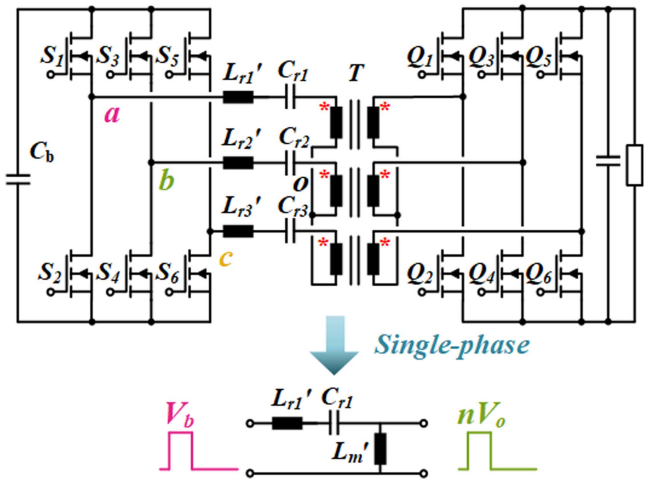

Fig. 9. Single-phase equivalent circuit of the resonant tank.

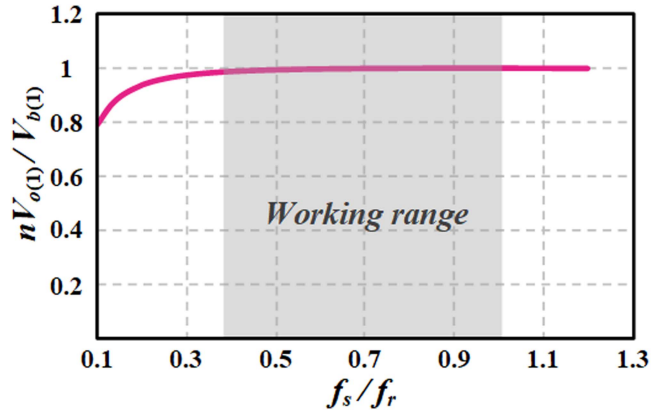

Fig. 10. Resonant tank gain under high inductance ratio.

range (shaded part in the figure). Therefore, the gain of the resonant part can be considered as 1, i.e.,

$$G_{LLC} = 1. \tag{19}$$

Therefore, the normalized gain of the converter can be obtained as follows:

$$G_{\text{tot}} = \frac{1}{D}. \tag{20}$$

Fig. 11 shows the comparison between the calculated gain and the simulated gain. It can be seen that the simulated gain is consistent with the calculated gain. In a wide frequency range, the normalized gain of the resonant tank is unchanged.

IV. Optimization of the Current Stress and the Integrated Transformer

A. Optimization of the Transformer Ratio and Current Stress

When boost works in the FCCM, the negative current of the inductor is used to implement soft switching on the lower side. Section III gives the boundary inductance value for soft switching, but it is not intuitive. The value of the inductor is

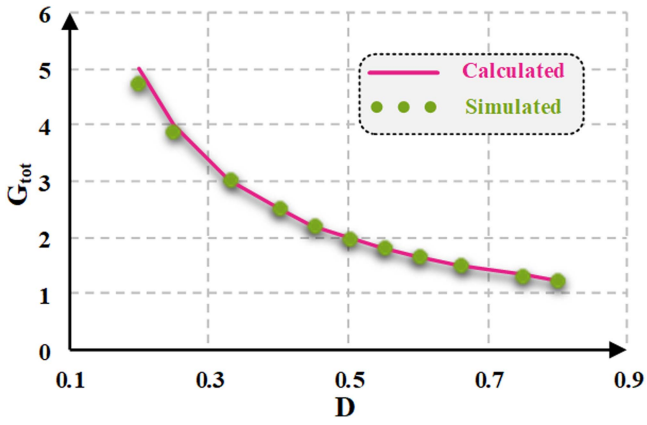

Fig. 11. Comparison of simulation gain and calculation gain.

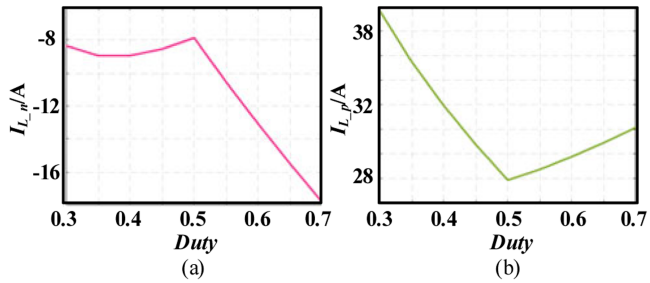

Fig. 12. Peak value of inductor current. (a) Peak value of negative current. (b) Peak value of positive current.

related to both the duty cycle and the switching frequency. To ensure that soft switching can be achieved in the full voltage range, it is necessary to find the peak value of the negative current under different duty cycles. According to (2) and (12)–(14), the relationship between the peak value of the inductor current and the duty can be obtained [see (21) and (22)]. Fig. 12 shows the variation curve of inductor current with the duty. As shown in Fig. 12(a), whether soft switching can be realized mainly considers two design points: the minimum duty and the duty equal to 0.5. In these two cases, soft switching can be achieved, which ensures that soft switching can be achieved in the full range

$$I_{L\_p} = \begin{cases} \frac{P}{3V_{\text{in}}} + \frac{V_{\text{in}}(1-D)}{4LDf_r}, & D \le 0.5 \\ \frac{P}{3V_{\text{in}}} + \frac{V_{\text{in}}}{4Lf_r}, & D > 0.5 \end{cases} \tag{21}$$

$$I_{L\_n} = \begin{cases} \frac{P}{3V_{\text{in}}} - \frac{V_{\text{in}}(1-D)}{4LDf_r}, & D \le 0.5 \\ \frac{P}{3V_{\text{in}}} - \frac{V_{\text{in}}}{4Lf_r}, & D > 0.5 \end{cases} . \tag{22}$$

Therefore, it is necessary to determine the minimum duty of the converter, which is related to the ratio of the transformer. When the output voltage is fixed, different ratios correspond to different bus voltages and different duties (17). In addition, different ratios also affect the voltage and current stress and losses of the device. Therefore, the boost inductance and current can be optimized based on different transformer ratios.

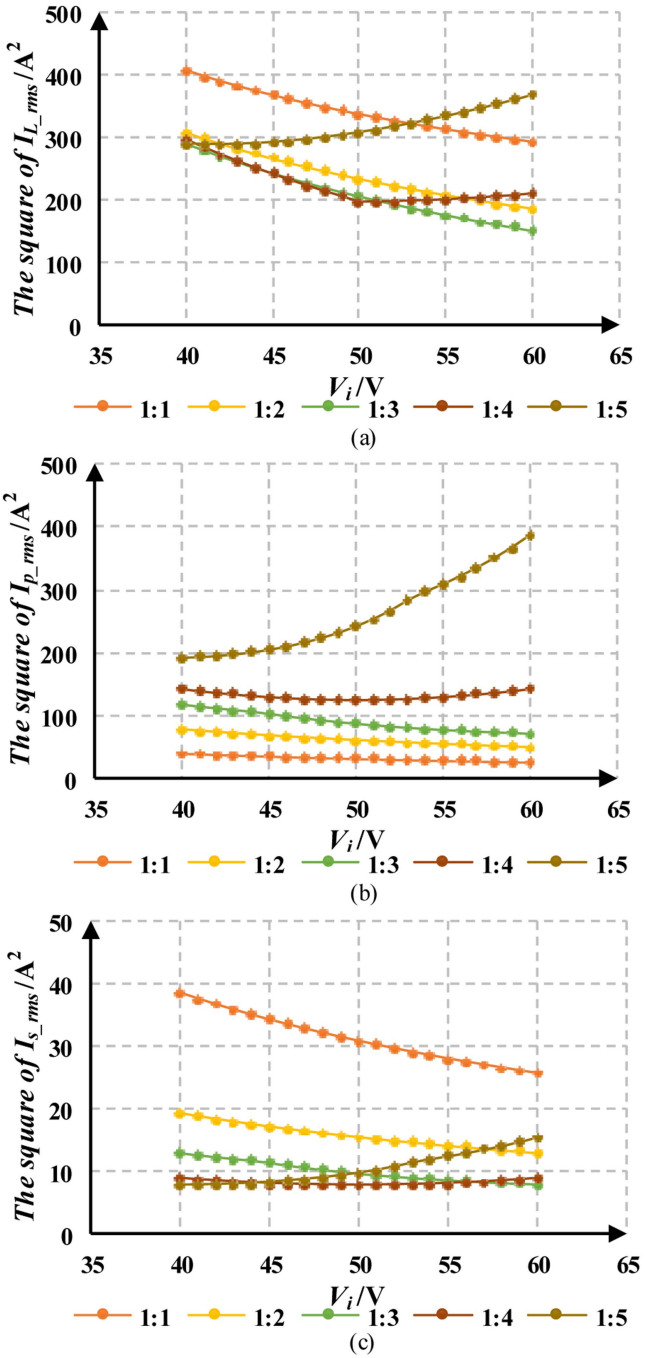

Fig. 13. Square of the current RMS value changes with the duty cycle under different transformer ratios. (a) Current of the inductor. (b) Current in the primary side of the transformer. (c) Current in the secondary side of the transformer.

The RMS value of the inductor current can be calculated according to (23). According to the output charge balance, the peak value and the RMS value of the resonant current of the Y-type connection of the primary and secondary sides under different duty cycles can be calculated in (24)–(27)

$$I_{L\_\mathrm{rms}} = \sqrt{\frac{{I_{L\_p}}^2 + {I_{L\_n}}^2 + I_{L\_p} I_{L\_n}}{3}} \tag{23}$$

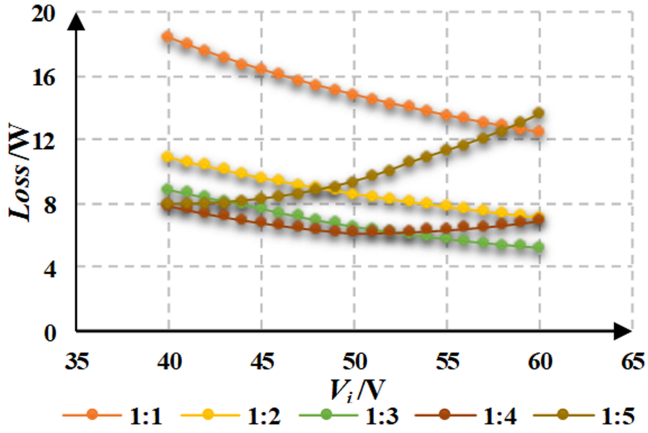

Fig. 14. Device loss changes with the duty cycle under different transformer ratios.

TABLE I
CIRCUIT DESIGN PARAMETERS

Parameters	Symbol	Value
Input voltage	V_i	40–60 V
Output voltage	V_o	400 V
Output power	P_o	1.5 kW
Resonant frequency	f_r	≈1 MHz
Primary device	S_n	EPC2305
Secondary device	Q_n	GS66508T
Drive	–	1EDB7275
Controller	–	STM32G474rbt6

$$I_{s\_pk} = \begin{cases} I_o \Big/ \left(\dfrac{3D\int_0^{\pi} \sin x dx}{\pi} \right), & D \in (0, 1/3] \\ I_o \Big/ \left(\dfrac{\int_{\left(D-\frac{1}{3}\right)*2\pi}^{\left(\frac{1}{2}-\left(D-\frac{1}{3}\right)\right)*2\pi} \sin x dx}{\pi - 2\left(D-\frac{1}{3}\right)*2\pi} \right), & D \in \left(1/3, 1/2\right] \\ I_o \Big/ \left(\dfrac{\int_{\left(1-D-\frac{1}{3}\right)*2\pi}^{\left(\frac{1}{2}-\left(1-D-\frac{1}{3}\right)\right)*2\pi} \sin x dx}{\pi - 2\left(1-D-\frac{1}{3}\right)*2\pi} \right), & D \in \left(1/2, 2/3\right] \\ I_o \Big/ \left(\dfrac{3(1-D)\int_0^{\pi} \sin x dx}{\pi} \right), & D \in (2/3, 1) \end{cases} \tag{24}$$

$$I_{s\_\mathrm{rms}} = \begin{cases} \sqrt{\dfrac{D\left({I_{s\_\mathrm{pk}}}^2 \int_0^{2\pi} (\sin x)^2 dx\right)}{\pi}}, & D \in \left(0, 1/2\right] \\ \sqrt{\dfrac{(1-D)\left({I_{s\_\mathrm{pk}}}^2 \int_0^{2\pi} (\sin x)^2 dx\right)}{\pi}}, & D \in (1/2, 1) \end{cases} \tag{25}$$

$$I_{p\_\mathrm{pk}} = I_{s\_\mathrm{pk}}/n \tag{26}$$

$$I_{p\_\mathrm{rms}} = I_{s\_\mathrm{rms}}/n. \tag{27}$$

Since soft switching can be achieved, device losses are primarily related to the square of the RMS current. Based on the parameters in Table I, Fig. 13 shows the comparison of the square of the current RMS value under different transformer ratios. Table II shows the maximum inductance that can achieve

TABLE II
MAXIMUM INDUCTANCE FOR SOFT SWITCHING

Ratio	$L_1/L_2/L_3$
1:1	3.3 μH
1:2	1.9 μH
1:3	1.2 μH
1:4	0.7 μH
1:5	0.5 μH

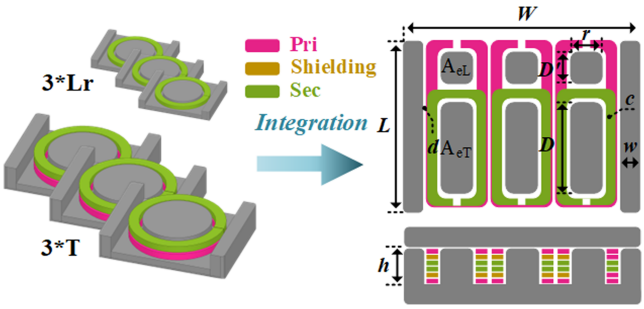

Fig. 15. Three-phase integrated transformer.

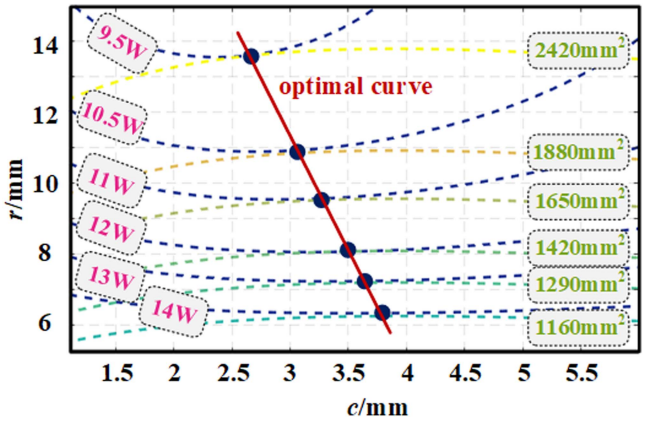

Fig. 16. Transformer optimization curve.

soft switching under different transformer ratios. It can be seen that the larger the transformer ratio, the larger the secondary current, and the larger the loss of the secondary switching device. If the transformer ratio is too small, the primary current will be large, and the loss of the primary switching device will be large. Regardless of whether the transformer ratio is too large or too small, the RMS value of the inductor current will be large, which will greatly increase the inductor loss.

Furthermore, the loss of the switching device can be calculated according to (28) and (29). Fig. 14 shows the comparison of device losses as the input voltage changes under different transformer ratios. It can be seen that different transformer ratios have a great impact on device loss. To achieve high-efficiency operation within the full voltage regulation range, it is necessary to select an appropriate transformer ratio according to the required voltage regulation range. After comprehensive consideration, the transformer ratio in this article is

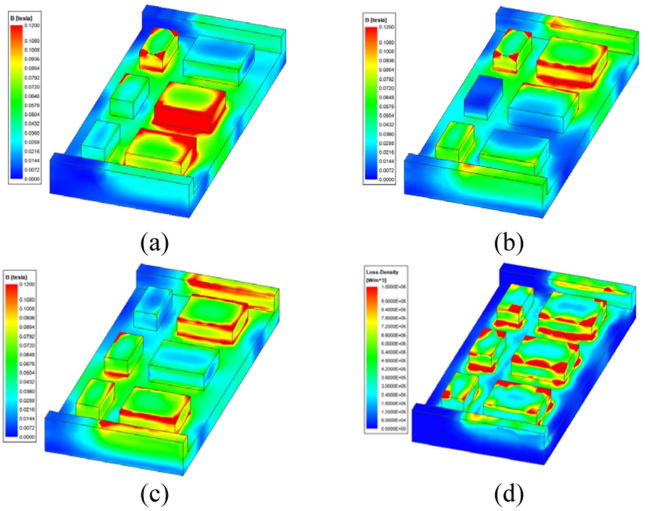

Fig. 17. Magnetic core simulation results. (a) 0°. (b) 120°. (c) 240°. (d) Core loss density.

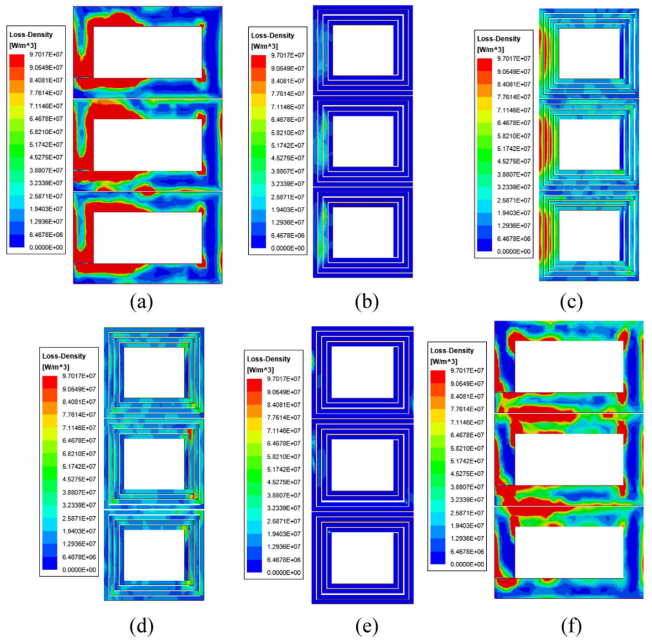

Fig. 18. Winding simulation results. (a) Top layer. (b) Middle layer 1. (c) Middle layer 2. (d) Middle layer 3. (e) Middle layer 4. (f) Bottom layer.

chosen as 1:4

$$P_{\text{sw\_con}\_p} = 3\left(I_{L\_\text{rms}}{}^2 + I_{p\_\text{rms}}{}^2\right) R_{dson\_p} \tag{28}$$

$$P_{\text{sw\_con}\_s} = 3 I_{s\_\text{rms}}{}^2 R_{dson\_s}. \tag{29}$$

B. Optimization of the Three-Phase Integrated Transformer

Three-phase interleaved *LLC* has a large number of magnetic components, three resonant inductors, and three transformers. To reduce the number of magnetic components and improve the power density, this article uses the three-phase integrated transformer shown in Fig. 15. To reduce the parasitic capacitance

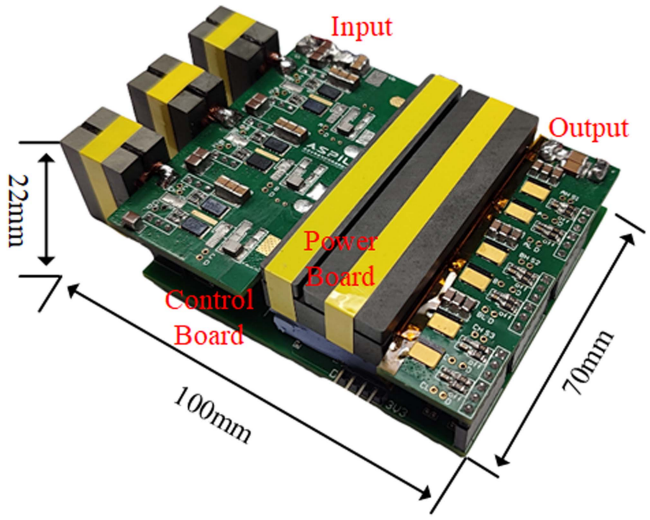

Fig. 19. Prototype of the three-phase integrated boost–*LLC* converter.

of the primary and secondary windings, two layers of shielded windings are added. The three magnetic columns on the upper (A_{eL}) provide a low reluctance path for leakage flux, resulting in leakage inductance, which is used as a resonant inductor. The magnetic column on the lower (A_eT) provides a magnetic path for the main magnetic flux. Ignoring the reluctance of the magnetic core, the resonant inductance L_r can be derived based on the reluctance relationship as follows:

$$\begin{cases} L_r = N_p\varphi_L/i_p \\ \varphi_L = \varphi_p - \varphi_s \\ \varphi_p = A_{e\_L}B_L + A_{e\_T}B_T \\ \varphi_s = A_{e\_T}B_T \\ B = \mu Ni/l \end{cases} \tag{30}$$

$$L_r = \mu_0 {N_p}^2 A_{e\_L}/l_g \tag{31}$$

where φ_L is the leakage inductance flux, i_p is the primary current, φ_p is the total primary magnetic flux, φ_s is the main magnetic flux of the transformer, and l_g is the equivalent air gap length of the leakage inductance magnetic column.

Furthermore, the size model of the integrated transformer can be obtained according to the variables in Fig. 15 [see (32)]. The window height (h) of the transformer is 3 mm, and the insulation distance (d) of the winding is 0.25 mm

$$\begin{cases} D' = A_{eL}/r \\ D = A_{eT}/r \\ w = A_{eT}/(2D + 4d + 4c) \\ L = D + D' + 4d + 3c \\ W = 2w + 6c + 3r + 10d \\ \text{Footprint} = L * W \\ V_T = \text{Footprint} * (h + 2w). \end{cases} \tag{32}$$

To simplify the design, the volume loss (P_v) of the core is set to 200 mW/cm^3, and the material is DMR53 from DMEGC. According to the loss curve, the magnetic flux density (B_m) can be obtained as approximately 70 mT (33). The transformer winding ratio is 2:8, and the required A_{eT} and A_{eL} can be calculated (33) and (34), respectively. Therefore, the core loss, winding loss, and footprint of the transformer under rated working conditions can be expressed by r and c [4]

$$A_{eT} = \frac{V_o}{6Nf_sB_m} \tag{33}$$

$$A_{eL} = \frac{L_rI_{p\_pk}}{NB_m}. \tag{34}$$

According to (32), the loss curve and the area curve shown in Fig. 16 can be obtained. The optimized design points can be selected based on the optimal curve in Fig. 16. Fig. 17(a)–(c) shows the magnetic flux density distribution of the core at different phase angles. Fig. 17(d) shows the average loss density distribution of the core. It can be seen that the loss distribution of the three-phase integrated transformer is even. Fig. 18 shows the ohm loss distribution of the winding, where the top layer and bottom layer are the primary windings, Middle layer 1 and Middle layer 4 are the shielding layers, and Middle layer 2 and Middle layer 3 are the secondary windings. It can be seen that since the main magnetic column is designed with no air gap, the ohm loss of the surrounding group is distributed evenly. Since the leakage inductance column has an air gap, the losses around it are concentrated. In addition, it can be seen that the loss density of the shielding layer is low, and the loss is almost negligible. Table III shows that the calculated losses of the transformer are consistent with the simulated losses. Table IV shows the dimension parameters of the integrated transformer.

Table V shows the comparison between integrated and non-integrated transformers. According to the results, high power density and high efficiency can be achieved using the proposed magnetic integrated transformer.

TABLE III
TRANSFORMER LOSS COMPARISON

Parameters	Calculation	Simulation
Core loss	2.6 W	2.7 W
Winding loss	7.7 W	8.1 W
Total loss	10.3 W	10.8 W

TABLE IV
DIMENSIONAL PARAMETERS OF THE INTEGRATED TRANSFORMER

Parameters	Value	Parameters	Value
D	12 mm	c	3.5 mm
D'	5 mm	w	4 mm
r	10 mm	h	3 mm

V. EXPERIMENTAL VERIFICATIONS

To verify the proposed topology and the modulation strategy, this article designed a 1.5-kW prototype (see Fig. 19). The key parameters of the prototype are shown in Table I. The size of the prototype is 100 mm × 70 mm × 22 mm, the switching frequency is 1 MHz at 50-V input, and the power density of

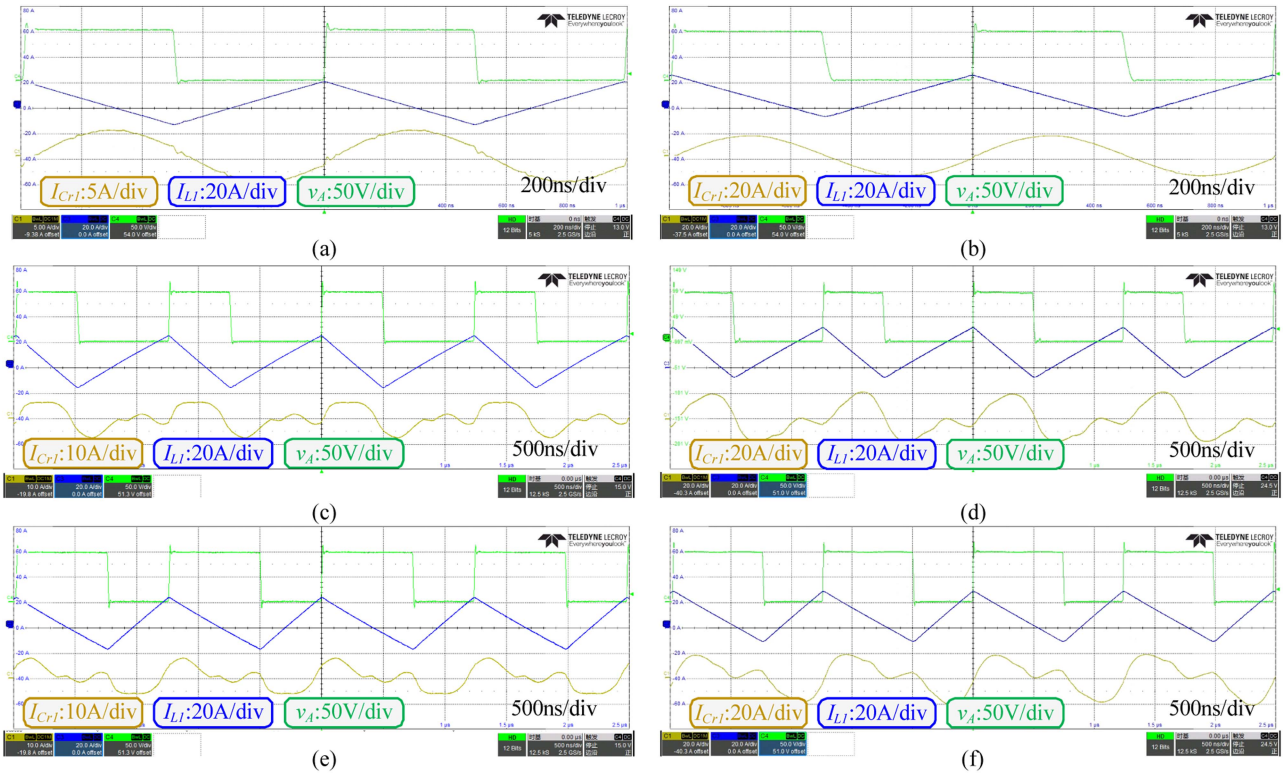

Fig. 20. Waveforms under different input voltages and loads. (a) Light load at 50 V. (b) Full load at 50 V. (c) Light load at 40 V. (d) Full load at 40 V. (e) Light load at 60 V. (f) Full load at 60 V.

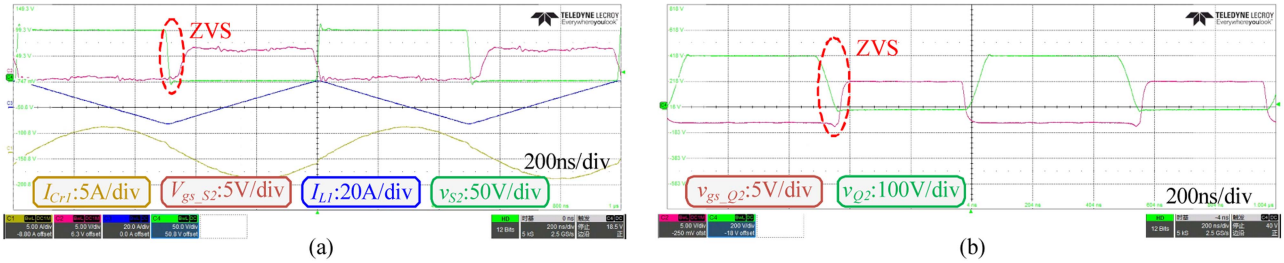

Fig. 21. Soft switching waveforms of phase A at 50-V input. (a) Primary. (b) Secondary.

TABLE V
COMPARISON BETWEEN THE INTEGRATED TRANSFORMER AND THE NONINTEGRATED TRANSFORMER

	Ref.	Power density*	Loss ratio*
Nonintegrated	[12]	32.7 W/cm^3	1.03%
	[14]	11 W/cm^3	–
Integrated	[9]	–	0.92%
	[13]	3.23 W/cm^3	–
	[17]	–	0.69%
	This work	75.7 W/cm^3	0.72%

* The power density of the magnetic component is the ratio of the total power to the total volume of the magnetic component. The higher the power density, the smaller the magnetic component.
* The loss ratio of the magnetic components is the ratio of the loss of magnetic components to the total power. The smaller the value, the smaller the loss of magnetic components.

159 W/in^3 is achieved. The prototype includes a power board and a control board. Low-voltage devices, such as driver chips and control chips, are on the control board, and high-voltage devices, such as power devices, are on the power board. The power board and the control board are connected through connectors. The advantage of this is that the space in the height direction can be fully utilized to improve space utilization while reducing the interference of high-voltage circuits on low-voltage signals.

Fig. 20 shows the half-bridge midpoint voltage, chopper inductor current and resonant current waveforms of phase A at different loads and input voltages. The switching frequency is 1-MHz at 50 V input. It can be seen that boost works in FCCM, and the current of the chopper inductor is bipolar. The negative current at the light load is large and the half-bridge midpoint

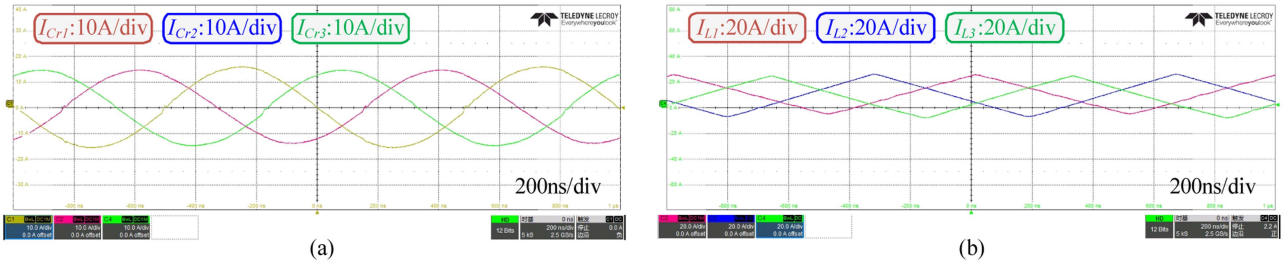

Fig. 22. Three-phase current waveforms at 50-V input. (a) Three-phase resonant current. (b) Three-phase inductor current.

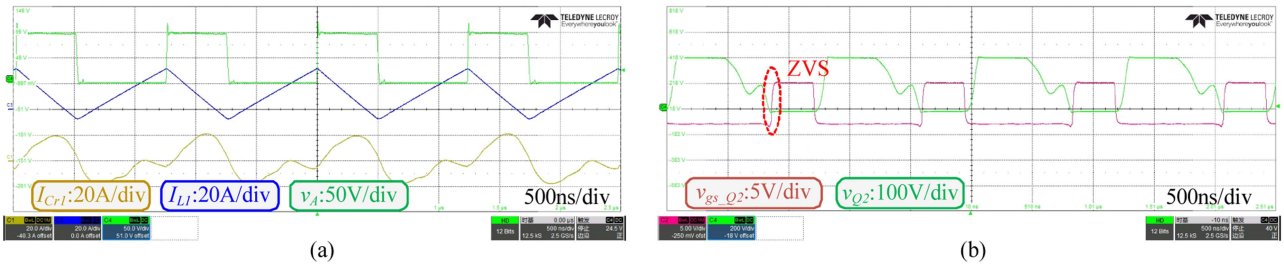

Fig. 23. Full-load waveforms at 40-V input. (a) Voltage and current waveforms of the primary side. (b) Voltage waveforms of the secondary side.

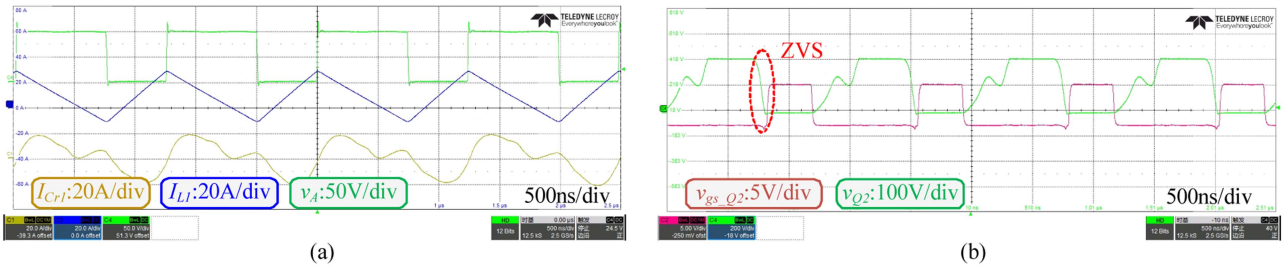

Fig. 24. Full-load waveforms at 60-V input. (a) Voltage and current waveforms of the primary side. (b) Voltage waveforms of the secondary side.

voltage (v_{ds}) drops quickly; the negative current at the full load is small and the v_{ds} drop slowly.

Fig. 21(a) shows the primary-side soft-switching waveform, and Fig. 21(b) shows the secondary-side soft-switching waveform. The proposed modulation can achieve ZVS of the primary- and secondary-side switches. Fig. 22(a) shows the three-phase resonant current at full load, and Fig. 22(b) shows the three-phase chopper inductor current at full load. The three-phase circuit has good symmetry, and the three-phase current is balanced.

Fig. 23(a) shows the half-bridge midpoint voltage, chopper inductor current, and resonant current waveforms at full load with 40-V input. The switching frequency is about 800 kHz, and the current waveform is consistent with the theoretical analysis. Fig. 23(b) shows the midpoint voltage and driving waveform of the secondary half-bridge. Consistent with the previous theoretical analysis, the secondary side can achieve ZVS.

Fig. 24(a) shows the half-bridge midpoint voltage, chopper inductor current, and resonant current waveforms at full load with 60-V input. The switching frequency is about 800 kHz, and the current waveform is consistent with the theoretical analysis. Fig. 24(b) shows the midpoint voltage and driving waveform of the secondary half-bridge. Consistent with the previous theoretical analysis, the secondary side can achieve ZVS.

Fig. 25 shows the thermal test results at full load. The ambient temperature is 25 °C, and a 2850-r/min fan is used to assist the heat dissipation. The temperature rise is the largest at 40-V input, because the input voltage is low and the input current is large, so the loss is the highest. It should be noted that the cooling fan is not included when calculating the power density of the prototype. In addition, the prototype designed in this article is only used to verify the proposed topology and modulation in the laboratory, and there are some shortcomings in the consideration of thermal management. In industrial applications, a heat sink with better heat dissipation performance or liquid cooling can be used to reduce the device temperature.

Fig. 26 shows the experimental waveforms when the input voltage changes between 40 and 60 V. In the zoomed-in waveform, the change in the inductor current shows that the closed-loop control changes the duty cycle, verifying that the closed-loop control works. It can be seen that after adding

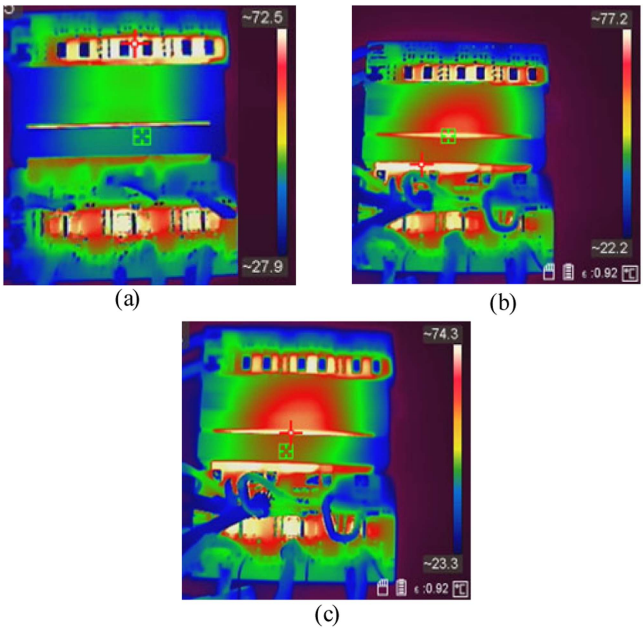

Fig. 25. Thermal test under full load. (a) 50 V. (b) 40 V. (c) 60 V.

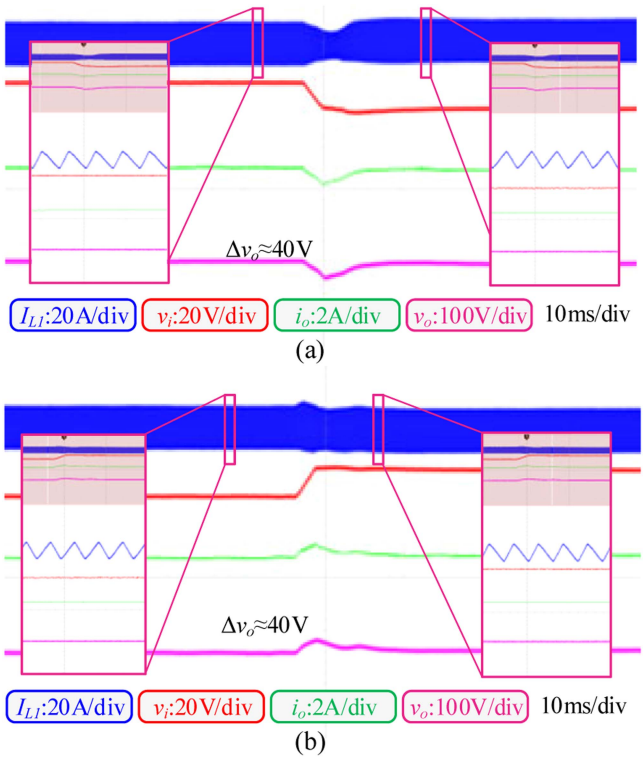

Fig. 26. Waveform when the input voltage changes. (a) From 60 to 40 V. (b) From 40 to 60 V.

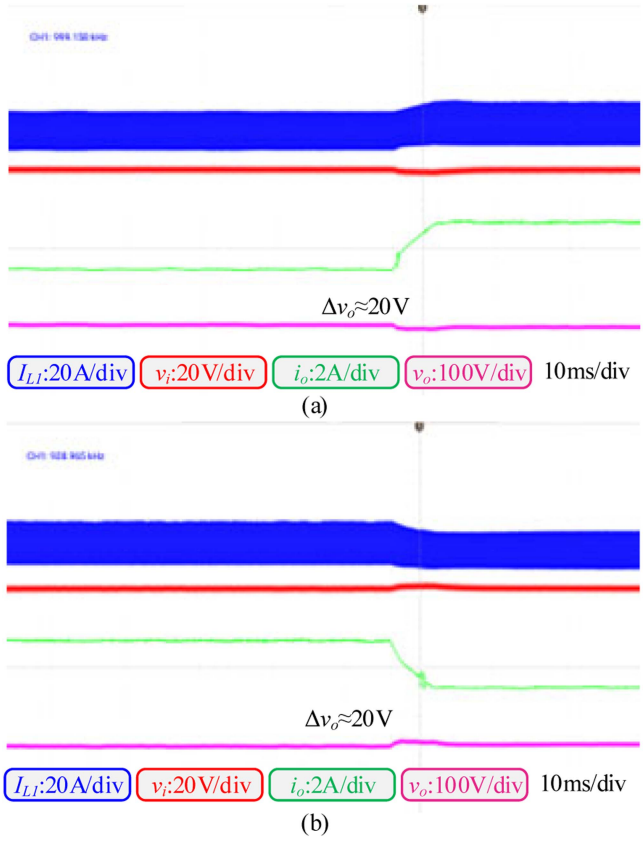

Fig. 27. Waveform when the load changes. (a) From 0% to 50%. (b) From 50% to 0%.

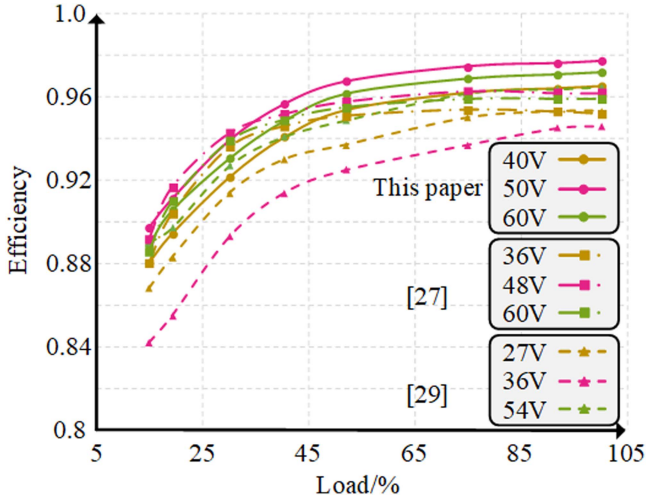

Fig. 28. Efficiency curve and comparison.

closed-loop control, when the input voltage changes, the output voltage has an overshoot or drop of about 40 V, and the output voltage can be stabilized after proportional–integral (PI) control. Fig. 27 shows the experimental waveforms when the load changes between half-load and no load. It can be seen that the load change will cause the output voltage to overshoot or drop by about 20 V, and the output voltage can be stabilized after PI control.

Fig. 28 shows the efficiency comparison of this article, [27], and [29] under different input voltages. At the lowest input voltage, the full-load efficiency of this article is 96.5%, which is higher than 95.2% in [27] and 95.3% in [29]. Under rated voltage, the full-load efficiency of this article is 97.7%, which

TABLE VI
COMPARISON OF DIFFERENT STRUCTURES

	This work	[18]	[21]	[24]	[33]
Topology	Boost–*LLC*	Two–stage	Boost–*LLC*	Boost–*LLC*	Boost–*LLC*
Regulation method	PWM+PFM	PWM	PWM	PWM	Phase shift
Frequency	800 kHz to 1 MHz	400 kHz	100 kHz	100 kHz	1 MHz
Gain	0.8–1.2	0.83–1.16	0.67–1.33	0.67–1.33	0.91–1.12
Efficiency	97.7%	96.5%	93.9%	96%	95.7%
Power density	High	Medium	-	Low	High
Reliability	Medium	Medium	High	High	Low
Cost	Low	High	Medium	Medium	High
Manufacturability	High	Low	Medium	Medium	Low

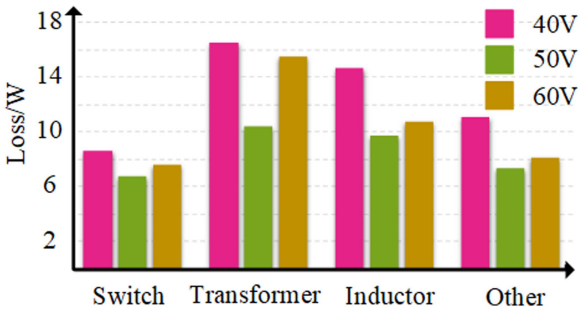

Fig. 29. Loss distribution at full load.

is higher than 96.2% in [27] and 94.6% in [29]. At the highest input voltage, the full-load efficiency of this article is 97.2%, which is higher than 95.9% in [27] and 96.5% in [29]. Within the full input voltage range, the prototype of this article has the highest efficiency, verifying the proposed modulation and the transformer optimization strategy.

Fig. 29 shows the full-load loss distribution of the prototype at different input voltages. The switching device loss includes conduction loss and turn-OFF loss, and the influence of temperature on ON-state resistance is taken into account in the calculation. Inductor loss and transformer loss include core loss and winding loss. The impact of temperature on winding loss is taken into account in the calculation. The remainder after subtracting the losses mentioned earlier from the total tested losses is other losses, including capacitor losses, printed circuit board copper losses, and auxiliary circuit losses. Since soft switching can be achieved, the loss is mainly related to the RMS value of the current, so the loss is highest at 40-V input. When the input voltage is 50 V, three-phase *LLC* operates in the resonant mode, and the reactive current is the smallest, so the loss is the lowest, and the efficiency is the highest.

Furthermore, Table VI gives a comparison of different structures. Overall, the topology and modulation proposed in this article can achieve the highest efficiency at high switching frequency and has high power density and a wide voltage regulation range.

VI. CONCLUSION

This article proposes a three-phase interleaved boost and three-phase interleaved *LLC* integrated topology that can achieve wide-range voltage regulation. Using the collaborative control strategy of the duty and frequency, smooth voltage gain and secondary-side synchronous rectification can be achieved. Boost works in the FCCM, and the bipolar inductor current can realize soft switching of all switching devices. No magnetizing current is required to achieve soft switching, so a gapless transformer design can be achieved, which is beneficial for reducing winding losses. To reduce device losses, this article compares the effects of different transformer ratios on voltage and current stress. A three-phase integrated transformer was designed to optimize efficiency and power density based on the size model and the loss model. Finally, the designed prototype with a switching frequency of 1 MHz can achieve synchronous rectification over a wide input voltage range (40–60 V) and has a peak efficiency of 97.7%.

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