# Letters

# A Full-Range Soft-Switching Class-E Inverter Achieving Quasi-Constant Voltage Output

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***Abstract*—In this letter, a novel parameter design methodology is proposed to achieve a full-range soft switching for the Class-E inverter with a quasi-constant voltage (CV) output. The metal-oxide-semiconductor field-effect transistor's (MOSFET's) body diode conduction in advance and the shunt capacitor recharging phenomenon during the switch-OFF period are analyzed by proposing a more precise modeling method. With the optimized resonant parameters, hard switching due to recharging of the MOSFET's shunt capacitor can be avoided. Thus, the load-independent zero voltage switching is extended to the whole load range. Moreover, a quasi-CV output, tailored to the varying load, is obtained within a certain range with the proposed parameter design methodology. An experimental setup is fabricated at 1 MHz and the feasibility of the proposed method has been verified through experimental results.**

***Index Terms*—Body diode conduction, class-E inverter, full-range soft switching, quasi-constant voltage (CV) output, shunt capacitor recharging.**

## I. Introduction

In a traditional Class-E inverter, the input inductor is designed with an ideally infinite inductance to achieve zero voltage switching (ZVS) [1]. However, it only works for a specific load, which results in reduced efficiency under varying load conditions and poses a challenge for practical applications [2].

To address this issue, an auxiliary compression network has been proposed to ensure load insensitivity, independent of the inverter topology [1]. However, the overall circuit structure is complex with an increasing cost. A Class-E inverter with a constant output voltage (CV) is discussed in [3] and one with a constant output current (CC) in [4], or both [5] and [6]. Utilizing the resonant technique, the CV or CC structure is simple and low-cost, achieving a stable output as well as soft switching over a wide load range [7].

However, when the load resistance falls below a critical threshold value in the CV-output Class-E inverter in [3], the metal-oxide-semiconductor field-effect transistor's (MOSFET's) body diode conducts in advance. Due to the shunt capacitor's recharging, it would lead to non-ZVS, which impedes the safe operation of the circuit [8]. Thus, this topology cannot be used in applications with large load variations. In this letter, a novel parameter design methodology is proposed to extend the ZVS range of the Class-E inverter. By establishing a novel parametric design flow that employs a normalization technique and considers inequality constraints, a parameter optimization procedure is proposed, leveraging the conventional design values as reference values. With the proposed parameter optimization method, the shunt capacitor recharging phenomenon can be avoided, thereby achieving a load-independent ZVS throughout the entire load range. It is the main novelty of this letter. Moreover, a quasi-CV characteristic within a relatively broad load range can still be achieved. An experimental setup has been fabricated to verify the reliability of the full-range ZVS parameter design method.

## II. Analysis of the Conventional CV-Output Class-E Inverter

The Class-E inverter circuit is depicted in Fig. 1, featuring a dc source $V_{\rm in}$, an input inductor $L_1$ with the current $i_{\rm in}$, and a composite capacitor $C_1$ comprising the MOSFET $S_1$'s $C_{\rm oss}$ and an external capacitor $C_{\rm add}$. The series resonant tank is composed of $L_2$ and $C_2$, with $L_2$ conceptually divided into $L_{2\rm x}$ and $L_2'$. The output voltage across the load resistor $R_{\rm o}$ is $v_{\rm o}$, and the current flowing through $R_{\rm o}$ is $i_{\rm o}$. The switching frequency is $f$ (the period $T = 1/f$) and the angular frequency is $\omega$ ($\omega = 2\pi f$). The MOSFET's switching signal has a constant duty cycle $D_{\rm const}$, with $D$ representing the actual cycle. When the body diode conducts in advance, $D$ is larger than $D_{\rm const}$. In the conventional CV Class-E parameter design method, introduced in [7], it is assumed that $D = D_{\rm const}$ [5].

The equivalent circuit can be deduced from the assumptions outlined in Fig. 1. The series resonant tank can be conceptually substituted with a sinusoidal current source, as shown in Fig. 1, where $\varphi$ represents the phase angle of the current.

Received 9 October 2024; revised 24 November 2024 and 11 January 2025; accepted 8 February 2025. Date of publication 13 February 2025; date of current version 20 March 2025. This work was supported by the National Natural Science Foundation of China under Grant 52307044. *(Corresponding author: Chenwen Cheng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3541206.

Digital Object Identifier 10.1109/TPEL.2025.3541206

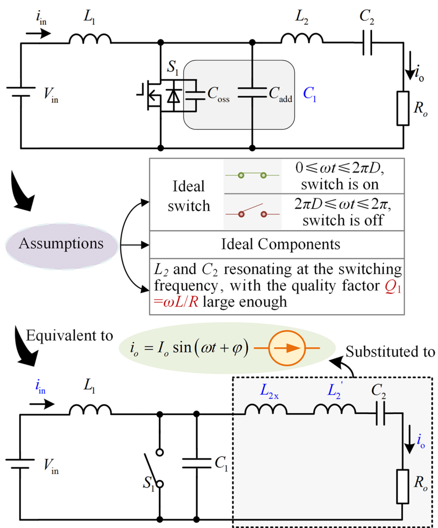


Fig. 1. Circuit topology of the Class-E inverter and the equivalent circuit based on assumptions.

Ignoring the high-order harmonics, the fundamental sinusoidal component $V_{\mathrm{o,res}}$ and the fundamental cosine component $V_{\mathrm{x,res}}$ of the switch voltage $v_{\mathrm{ds}}$ are obtained by Fourier decomposition, as shown in the following:

$$V_{\mathrm{o}} = \frac{1}{\pi}\int_0^{2\pi} v_{\mathrm{DS}}(\omega t)\sin(\omega t + \varphi)\, d\omega t = X_1(V_{\mathrm{in}}, I_o) \quad (1)$$

$$V_{\mathrm{x}} = \frac{1}{\pi}\int_0^{2\pi} v_{\mathrm{DS}}(\omega t)\cos(\omega t + \beta)\, d\omega t = X_2(V_{\mathrm{in}}, I_o). \quad (2)$$

To ensure the load-independent ZVS and CV output, the constraints below should be satisfied in the conventional CV Class-E parameter design method [3], [4]

$$v_{\mathrm{DS}}(2\pi D_{\mathrm{const}}) = 0 \quad (3)$$

$$\frac{\partial X_1}{\partial I_o} = 0 \quad (4)$$

$$\frac{\partial X_2}{\partial I_o} = 0. \quad (5)$$

The load-independent conditions listed in Table I are obtained by solving (3) and (4). Using the load-independent conditions, the parameter design equations ($I_{o,\max}$, $R_{o,\min}$, $L_1$, $C_1$, $L_2$, $C_2$, $L_{2\mathrm{x,res}}$, *and* $L_2'$) for the conventional CV Class-E inverter in [8] are constructed and serve as base values for further discussions in the proposed design method. Load-independent conditions and parameters are presented in Table I. $Q_{\max}$ refers to the quality factor of the series resonant tank formed by $L_2'$ and $C_2$. $L_{2\mathrm{x,\ res}}$ is the compensation inductance in the conventional CV Class-E design, compensating for the cosine component of $v_{\mathrm{DS}}$. $h$ is a function of $D_{\mathrm{const}}$ and $q$ (see Table I), serving as intermediate variables for parameter calculations [5].

Two possible scenarios are analyzed in [8] and are illustrated in Fig. 2(a).

1) The body diode remains nonconductive when $S_1$ is switched on, fulfilling $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}\omega t|_{\omega t=2\pi(1+D-D_{\mathrm{const}})} <= 0$, and $D = D_{\mathrm{const}}$.

TABLE I
CONVENTIONAL PARAMETER DESIGN EQUATIONS WITH LOAD-INDEPENDENT CONDITIONS

| Load-independent condition | Parameter (base value) | |
|---|---|---|
| $\tan[\pi(D_{\mathrm{const}}-1)q]=\pi D_{\mathrm{const}}q$ <br> $q$ is the ratio of the input switching frequency to the resonant frequency, $q=\frac{1}{\omega\sqrt{L_1C_1}}$. | $I_{o,\max}$ | $\frac{V_{\mathrm{in}}h}{mL_1\omega}$ |
| | $R_{o,\min}$ | $\frac{m^2L_1\omega}{h}$ |
| $\varphi=(3/2-D_{\mathrm{const}})\pi$ <br> $\varphi$ is the phase of the current. | $L_1$ | $\frac{R_{\mathrm{o,min}}h}{m^2\omega^2}$ |
| | $C_1$ | $\frac{m^2}{q^2\omega R_{\mathrm{o,min}}h}$ |
| $\begin{cases}V_{\mathrm{o}}=mV_{\mathrm{in}}\\ V_{\mathrm{x}}=n\omega L_1I_{\mathrm{o}}\end{cases}$ <br> $m$ and $n$ are functions of $D_{\mathrm{const}}$ and $q$. | $L_2'$ | $\frac{Q_{\max}R_{\mathrm{o,min}}}{\omega}$ |
| | $C_2$ | $\frac{1}{\omega Q_{\max}R_{\mathrm{o,min}}}$ |
| | $L_{2\mathrm{x,res}}$ | $\frac{nR_{\mathrm{o,min}}h}{m^2\omega}$ |

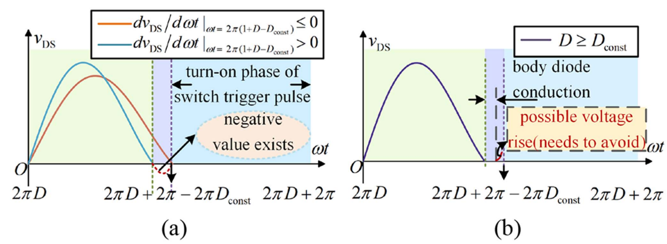


Fig. 2. $v_{\mathrm{DS}}$ waveform illustration. (a) Two possible waveforms of the calculated $v_{\mathrm{DS}}$. (b) Real waveform of $v_{\mathrm{DS}}$ while $D > D_{\mathrm{const}}$.

2) The calculated $v_{\mathrm{DS}}$ is negative, satisfying $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}\omega t|_{\omega t=2\pi(1+D-D_{\mathrm{const}})} > 0$, which implies $D > D_{\mathrm{const}}$. In reality, because the body diode of the MOSFET conducts, $v_{\mathrm{DS}}$ will be clamped to zero.

In [8], the critical load current $I_{\mathrm{o,max}}$ and the resistance $R_{\mathrm{o,min}}$ that prevent MOSFET body diode conduction were determined under the condition $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}\omega t|_{\omega t=2\pi} <= 0$. However, most of the existing studies did not consider body diode conduction as well as the shunt capacitor's recharging, which occurs when $R_{\mathrm{o}} < R_{\mathrm{o,min}}$, potentially leading to a non-ZVS condition.

This letter introduces a new parameter design approach based on a more precise and comprehensive mathematical model incorporating the body diode conduction. This design ensures ZVS throughout the entire load range and sustains a quasi- CV output across a broad load domain.

## III. Proposed Design Method

### A. Circuit Modeling and Analysis

As shown in Fig. 2(b), the waveform of $v_{\mathrm{DS}}$ is re-established, considering the body diode conduction case, which describes the variation of the switching voltage $v_{\mathrm{DS}}$ throughout a cycle. Specifically, when $D = D_{\mathrm{const}}$, the design adheres to the conventional parameters, with which the body diode remains nonconductive. Before the turning-ON instant of the switching signal, the shunt capacitor $C_1$ may be recharged, causing $v_{\mathrm{DS}}$ to rise and the power switch to lose its ZVS characteristic. To avoid this phenomenon, a constraint inequality will be added in the following system analysis. In this case, when $0 \leq \omega t \leq 2\pi D$, the switch is ON.

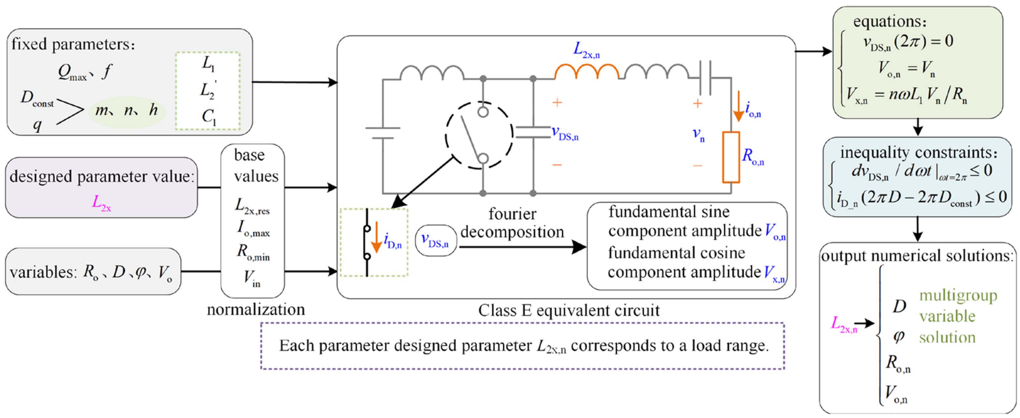


Fig. 3. Flowchart of the novel parameter design.

When $2\pi D \leq \omega t \leq 2\pi$, the switch is OFF. The differential equation of the Class-E inverter using kirchhoff's current law (KCL) and kirchhoff's voltage law (KVL) is formulated as follows:

$$\omega C_1 \frac{d^2 v_{\mathrm{DS}}(\omega t)}{d(\omega t)^2} = \frac{1}{\omega L_1}\left(V_{\mathrm{in}} - v_{\mathrm{DS}}(\omega t)\right) - I_{\mathrm{o}} \cos(\omega t + \varphi). \tag{6}$$

Boundary conditions to solve the differential equation are as follows.

1) The voltage of the switch at the instant of switching OFF is 0

$$v_{\mathrm{DS}}(2\pi D) = 0. \tag{7}$$

2) The average voltage of the switch during a cycle is equal to $V_{\mathrm{in}}$.

$$V_{\mathrm{in}} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{DS}}(\omega t) d\omega t. \tag{8}$$

The expression of $v_{\mathrm{DS}}$ can be obtained with (6)–(8). The expression of $i_{\mathrm{in}}$ can be obtained from the relationship between the voltage and current of $L_1$ and $C_1$

$$i_{\mathrm{in}}(\omega t) = \begin{cases} \frac{1}{\omega L_1} V_{\mathrm{in}} \omega t + i_{\mathrm{in}}(2\pi), & 0 \leq \omega t \leq 2\pi D \\ \omega C_{\mathrm{s}} \frac{dv_{\mathrm{DS}}(\omega t)}{d\omega t} + I_{\mathrm{o}} \sin(\omega t + \beta), & 2\pi D \leq \omega t \leq 2\pi \end{cases}. \tag{9}$$

To simplify the calculation process and establish a generalized design methodology, normalized values are used with the base values in Table I. The normalized load current $I_{\mathrm{o,n}}$ is based on $I_{\mathrm{o,max}}$. The normalized load resistance $R_{\mathrm{o,n}}$ is based on $R_{\mathrm{o,min}}$. The normalized compensation inductance $L_{\mathrm{2x,n}}$ is based on $L_{\mathrm{2x,res}}$. The switch voltage $v_{\mathrm{DS,n}}$, the output voltage $V_{\mathrm{n}}$, the fundamental sinusoidal component $V_{\mathrm{o,n}}$, and the fundamental cosine component $V_{\mathrm{x,n}}$ are all normalized with respect to the input voltage $V_{\mathrm{in}}$. All the base values can be referred to in Table I.

## *B. System Design*

The flowchart outlining the proposed parameter design methodology is presented in Fig. 3. It illustrates the design process of the optimal circuit parameters to ensure that the inverter maintains ZVS across the whole load range, while also sustaining a quasi-constant output voltage characteristic within a considerable range. The following conditions are satisfied when $L_{\mathrm{2x,n}}$ and $R_{\mathrm{o,n}}$ change.

1) To ensure ZVS, the voltage at the instant of switch conduction (including the case of body diode conduction) is 0

$$v_{\mathrm{DS,n}}(2\pi) = 0. \tag{10}$$

2) Due to the filter network, the output current is the fundamental component. The output voltage amplitude equals the sinusoidal component of $v_{\mathrm{DS}}$

$$V_{\mathrm{o,n}} = V_{\mathrm{n}}. \tag{11}$$

3) Likewise, the output voltage amplitude equals the cosine component of $v_{\mathrm{DS}}$

$$V_{\mathrm{x,n}} = n\omega L_1 V_{\mathrm{n}}/R_{\mathrm{n}}. \tag{12}$$

There are two solutions to the system of equations associated with (10)–(12), the incorrect one causes $v_{\mathrm{DS,n}}$ to have a negative waveform during $2\pi D \leq \omega t \leq 2\pi$, whereas the power switch's voltage within $2\pi D \leq \omega t \leq 2\pi$ can only be positive or zero. To avoid the invalid solutions, the inequality constraint below must be satisfied

$$dv_{\mathrm{DS,n}}/d\omega t|_{\omega t=2\pi} \leq 0. \tag{13}$$

Before the trigger instant of the switching signal, the shunt capacitor $C_1$ may be charged again, resulting in a positive $v_{\mathrm{DS}}$ and the non-ZVS of the switch. To avoid the recharging of $C_1$, the following constraints are added:

$$i_{\mathrm{D,n}}(2\pi D - 2\pi D_{\mathrm{const}}) \leq 0. \tag{14}$$

Fig. 4 is obtained by solving (10)–(14). Fig. 4(a) presents a series of designed parameters $L_{\mathrm{2x,n}}$, each associated with a distinct load range. The solutions delineate the operational boundaries of the Class-E inverter. It reveals that if the inequality constraints are not met, the Class-E inverter works in a nonZVS region. $D$ is used to determine whether the body diode conducts the duration of the body diode conduction. It is observed that increasing $L_{\mathrm{2x}}$ effectively broadens the load range. Theoretical ZVS operation across the entire load spectrum, including from zero load, is attainable when $L_{\mathrm{2x,n}}$ exceeds the threshold value of 1.72.

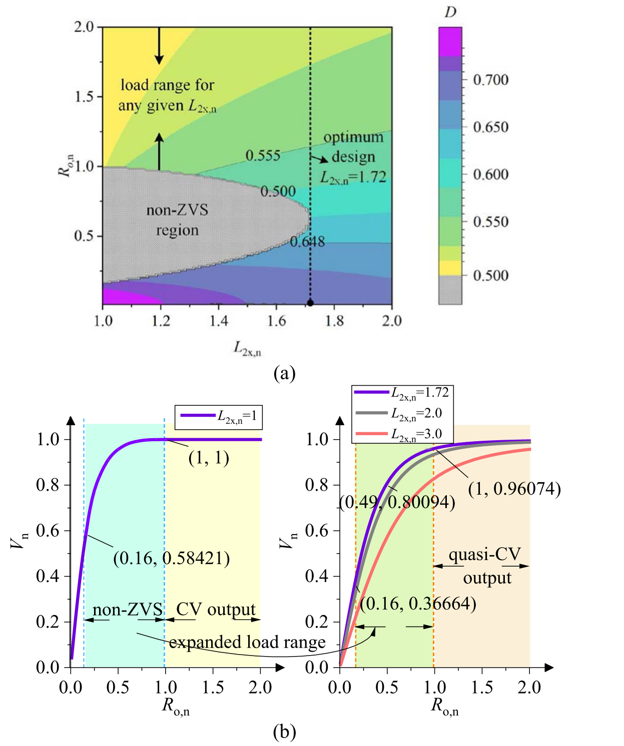


Fig. 4. Optimum compensation inductance value $L_{2x,n}$ design. (a) Output numerical solutions of load range and $D$ related to various $L_{2xn}$. (b) Output voltage characteristics and load range at the optimum design point ($L_{2x,n} = 1.72$) compared to the previous design ($L_{2x,n} = 1$) and the nonoptimal designs ($L_{2x,n} = 2.0$, $L_{2x,n} = 3.0$).

To ensure ZVS, optimizations of the resonant parameters are necessary, which means that the theoretical strict CV output is no longer guaranteed. Fig. 4(b) compares the proposed design with the conventional one, revealing that the revised design not only maintains quasi-CV characteristics across the original load range but also ensures the circuit's ZVS operation under small load conditions. It is found that the voltage deviation of the proposed design is small and the quasi-CV characteristics can still be maintained.

Comparing the quasi-CV characteristics at the optimum design point $L_{2x,n} = 1.72$ with larger design values ($L_{2x,n} = 2.0$, $L_{2x,n} = 3.0$), it can be seen that the quasi-CV characteristics deteriorate as $L_{2x,n}$ increases and deviates from the optimum design point. Therefore, $L_{2x,n} = 1.72$ is selected as the compensation inductance value in this letter. In fact, by adjusting the compensation inductance $L_{2x}$ of the circuit, the load becomes inductive. This is equivalent to adjusting the phase angle of the current source to maintain ZVS.

## IV. Experimental Results and Discussion

### A. Parameter Design Results and System Setup

All the circuit parameters as well as the intermediate parameters used in parameter calculation are presented in Table II. The switching frequency $f$ is designed as 1 MHz. The proposed design can be used for higher frequencies as well. The input voltage is 12V. $D_{\text{const}}$ is chosen to be 0.5 in order to achieve a large output capacity. The quality factor $Q_{\max}$ of the series

TABLE II
Circuit Parameters

| Parameters | Values | Parameters | Values | Parameters | Values |
|---|---|---|---|---|---|
| $q$ | 1.29 | $Q_{\max}$ | 10 | $C_2$ | 0.80 nF |
| $m$ | 1.59 | $D_{\text{const}}$ | 0.5 | $L_1$ | 3.30 $\mu$H |
| $n$ | 0.27 | $V_{\text{in}}$ | 12 V | $L_2'$ | 31.83 $\mu$H |
| $h$ | 2.62 | $f$ | 1 MHz | $L_{2x\_1}$ | 0.88 $\mu$H |
| $R_{o,\min}$ | 20 Ω | $C_1$ | 4.60 nF | $L_{2x\_2}$ | 1.51 $\mu$H |

resonant is set as 10. $L_1$, $L_2'$, $C_1$, and $C_2$ can be obtained according to Table I.

The compensation inductance $L_{2x}$ was set to the traditional parameter value $L_{2x\_1} = L_{2x,\text{res}} = 0.88\,\mu\text{H}\,(L_{2x,n} = 1)$ and the optimal design value $L_{2x\_2} = 1.51\,\mu\text{H}\,(L_{2x,n} = 1.72)$, for two sets of experiments to make a comparison. The specific values are shown in Table II. The data in the table is theoretical values obtained by the design equations, and the actual parameters used in experiments may have deviations. However, as long as the errors are within a certain range, they have a minimal impact on system performance

### B. Experiment Results

The waveforms of the conventional design and the proposed design of this letter at different loads are shown in Fig. 5. In the conventional design, the recharging of $C_1$ appears when the load resistance is less than $R_{o,\min}$. The peak voltage at the turning-on instant of the switching signal is 20 V and 8 V for loads of 4 Ω and 8 Ω, respectively, resulting in non-ZVS. As a contrast, the proposed design eliminates the recharging phenomenon and ensures ZVS at small loads (such as 4 Ω and 8 Ω). When the load resistance decreases, the load power increases and the voltage stress will also increase accordingly. When $R_{\text{o}}$ is 8 Ω, the voltage stress reaches 59.2 V, which is 4.93 $V_{\text{in}}$.

Fig. 6 illustrates the load voltage and efficiency characteristics of the proposed design. In Fig. 6, the maximum efficiency reaches 93.17%. When $R_{\text{o}} > R_{\text{omin}}$, the efficiency of the proposed design is slightly lower than the conventional CV design. With smaller load resistance, which refers to the non-ZVS range of the conventional design, the proposed design is more efficient than the conventional CV design. Moreover, because of the realization of ZVS, compared to the conventional CV design, the proposed design reduces the gate-level oscillations caused by electromagnetic interference, and relieves switch heating, thus prolonging the service life of the switch. Compared to the conventional design, the proposed design exhibits a diminished CV characteristic. However, it is still capable of sustaining a quasi-cCV characteristic over a wide load range. In practice, an increase in $R_{\text{o}}$ leads to a decrease in the quality factor and an increase in the harmonic content of the output. That is why the measured rms value of the load voltage increases a little.

Basically, wherever the traditional CV can be used, the design proposed in this letter can also be applied. In a practical design, the critical value of the load range under the normal operation can be set near $R_{\text{o},\min}$ as seen in Fig. 6. Using the proposed

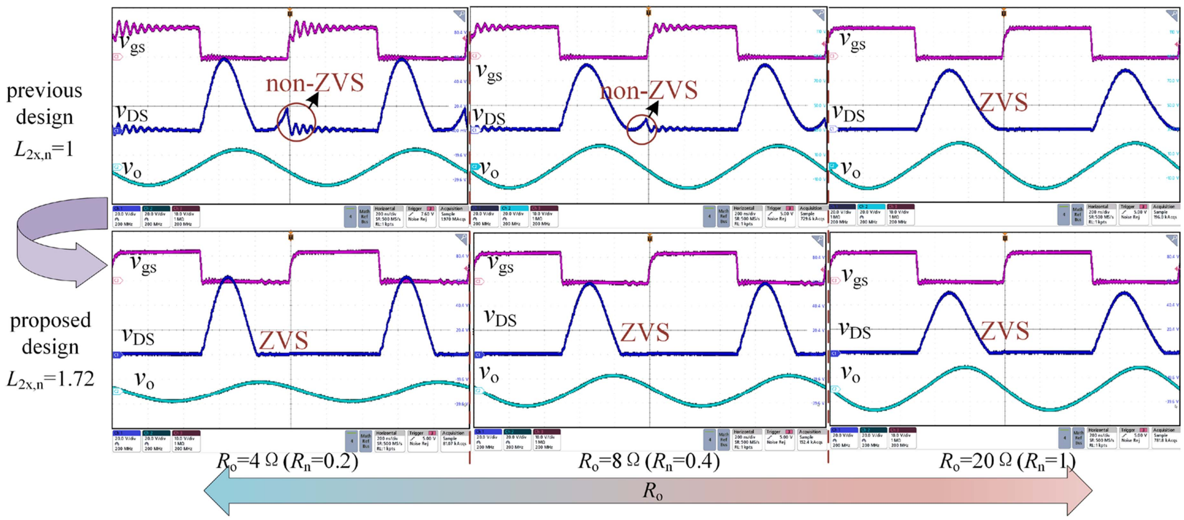


Fig. 5. ZVS characteristics with the output voltage of the previous design and the proposed design of this letter ($L_{2x,n} = 1$ and $L_{2x,n} = 1.72$). At different loads ($R_n = 0.2$, $R_n = 0.4$, and $R_n = 1$).

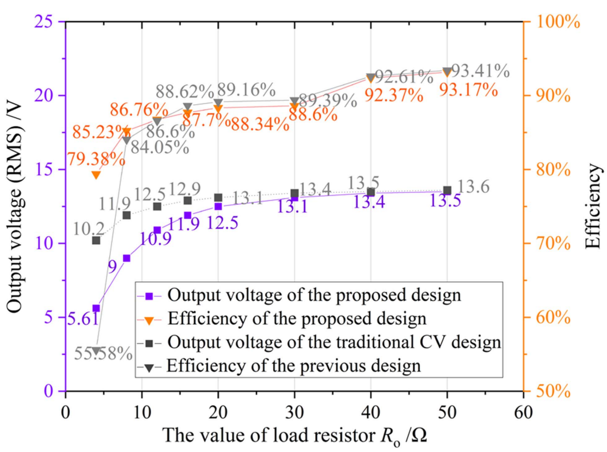


Fig. 6. Efficiency and output voltage under different loads.

design method it can be ensured that when the load resistance is within the normal operation range, larger than $R_{o,\,min}$ (20 Ω), the circuit can maintain a quasi-CV output and ZVS.

## V. Conclusion

A novel parameter design method for the Class E inverter has been proposed in this letter, which achieves a full-range soft switching and quasi-CV characteristic. Thus, the proposed design method is suitable for applications with large load fluctuations. The following conclusions can be summarized.

1) The ZVS has been extended to the whole load range, so that the safe operation of the power switch can be ensured.
2) The quasi-constant load voltage characteristic is achieved, which makes the proposed design method suitable for varying load applications.
3) The effectiveness of the proposed design has been verified on a 1 MHz class-E inverter hardware. The maximum system efficiency reaches 93.17%.

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