Topology Construction, Modeling, and Control of Multilevel Inverters Without Shoot-Through Problem

Xinxin Zheng, Jingwen Hu, Xintian Liu, *Fellow, IEEE*, Yao He, Weihan Li, Yanan Zhou, and Lin He, *Member, IEEE*

***Abstract*—Shoot-through is an inherent topology defect of bridge-type inverters. Especially for multilevel inverters, the addition and compensation of dead-time have higher requirements for control strategies. This article proposes a topology construction regulation of three-phase inverters, which can convert any existing two-level or multilevel bridge-type inverter into a new topology without shoot-through problem. Also, the new topology makes it easier to achieve capacitor balance. With the proposed regulation, two typical multilevel topologies are given, and their working principles are analyzed. They have new switching modes that are not available in conventional bridge topologies and help to achieve dc capacitor balance. Because the filtering plant is coupled in the topology, the traditional inverter transfer function is unsuitable for the newly generated topology. Therefore, power bond graph method is applied to establish the topology mathematical model. A new switching model called switch-diode combined junction is proposed, which is suitable for both discrete and continuous control signals. Based on this, the control system complex vector model in synchronous rotating frame is established and the multiconstrained complex coefficient controller is designed to improve the dynamic performance of inverters. Finally, the simulation and experimental results are given to verify the correctness of the theoretical analysis.**

***Index Terms*—Capacitor balance, complex vector model, power bond graph method, switch-diode combined junction.**

I. Introduction

MULTILEVEL inverters are widely used in high-voltage situations [1]. Similar to two-level topology, multilevel topology also has a shoot-through problem [2]. In order to solve the problem, dead-time should be added to the driving signals. However, dead-time is unable to fundamentally solve the shoot-through problem. During the debugging process of the experimental prototype, it is easy to cause hardware damage due to unreliable software settings. What is more, dead-time introduces additional harmonics, harmonic compensation strategies, or higher requirement filters are needed. A small-scale high-precision digital closed-loop modulation method is presented in [3], which can eliminate the influence of dead time by using a resistive voltage divider to collect the state information. The strategy outlined in [4] involves optimizing the output waveforms of the bridge arms as a means to counteract the effects of dead time. With the proposed method, current sensing or additional control loops are not required but quantization and sampling circuit is still needed. It can be seen that in order to solve the shoot-through problem by control strategies, two steps are needed, one is to add a dead-time, and the other is to eliminate the dead-time effects [5], [6], [7]. As a result, the software and hardware of the control system both require corresponding solutions. In addition, if the dead-time effects cannot be effectively eliminated, the design and optimization of ac filters also need to consider the harmonics introduced by dead-time [8]. The effect of dead time on the voltage harmonic content is scrutinized in [9]. An optimal inductance ratio for the LCL filter, taking into account lower-order harmonics, is provided in [10]. The dead-time effects would increase filter specifications and design difficulty of the inverter.

In order to fundamentally solve the shoot-through problem, the topology of the inverter needs to have antishoot-through capabilities, which means that shoot-through branches cannot exist in the topology. The Z-source network can be combined with bridge topology to eliminate shoot-through branches so it can be applied to two-level and multilevel inverters [11]. It is a typical inverter topology without shoot-through problem [12]. However, Z-source inverters have some drawbacks, such as start-up shocks, large capacitor volumes, and high costs, which necessitate the consideration of improved topologies and control strategies, as discussed in [13]. A five-level inverter structure featuring dual quasi-Z-source networks and a switched capacitor is suggested in [14]. In [15], a novel series of magnetically coupled impedance source inverters is introduced, characterized by a clamped dc-link voltage and reduced shoot-through current. An advanced amplitude-domain technique aimed at reducing inductor current ripple in three-phase quasi-Z-source inverters is discussed in the study reported in [16]. The abovementioned techniques help to solve the problems of Z-source inverters but increase the complexity of the inverter system. What is more, in order to the realize multiquadrant operation of the inverter, additional bidirectional power switches need to be added to the topology in [17].

Received 9 August 2024; revised 31 October 2024 and 16 December 2024; accepted 17 January 2025. Date of publication 22 January 2025; date of current version 26 February 2025. This work was supported by the Research Fund for the National Natural Science Foundation of China under Grant 52207232. Recommended for publication by Associate Editor M. Narimani. *(Corresponding author: Xintian Liu.)*

The authors are with the Automotive and Transportation Engineering, Hefei University of Technology, Hefei 230000, China (e-mail: xinxin.zheng@hfut.edu.cn; 2023171577@mail.hfut.edu.cn; 2012800118@hfut.edu.cn; yao.he@hfut.edu.cn; liweihan@hfut.edu.cn; yanan.zhou@hfut.edu.cn; helin09@tsinghua.org.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3532675.

Digital Object Identifier 10.1109/TPEL.2025.3532675

In addition to Z-source topology, there are still some other topologies without shoot-through problem, such as the combinational power circuit, which consists of the half-bridge circuit proposed in [18] and the dual-buck topology described in [19], [20], [21], and [22]. They are both two-level inverters and can be extended to the modular multilevel converter structure through cascading. Dual-buck topology has a simpler structure than other topologies without shoot-through problem. It can be equivalent to the bridge-type inverter in an ideal condition and has no dead-time effects [20]. In [21], the evolutionary three-level and five-level topologies of dual-buck-type inverters are also provided, however, these topologies still require improvement.

In terms of modeling and control of the inverter, bridge-type inverters can easily obtain the transfer function from the control signal to the output of bridge legs [23]. The Z-source-type inverter can be split into the Z-source network and inverter bridge. They can be modeled separately [24]. Dual-buck-type inverters do not have fixed output points of the bridge legs, so they are usually equivalent to bridge-type inverters, as described in [20]. But, it is only suitable for ideal situations. The inverter model is inaccurate and the controller designed based on the model cannot achieve the desired effect. Small-signal modeling can solve this problem but it is only applicable to system analysis and optimization near steady-state operating points [25], [26].

For the abovementioned reasons, this article proposes a topology construction regulation of three-phase inverters without shoot-through problem. With the proposed regulation, any of the existing two-level or multilevel bridge-type topologies can be converted into a more reliable topology, and dead-time is not required. The newly constructed inverters have a new working mode, which helps to achieve balance of dc capacitors. Similar to bridge-type inverters, they also have the ability to operate in four quadrants. However, the filtering plant is coupled in the topology, the traditional inverter transfer function is not suitable for newly generated topology. The power bond graph (PBG) method is applied, which can obtain an accurate inverter model to design control systems [27]. PBG is a universal modeling method applicable to electrical, mechanical, and hydraulic systems simultaneously. But, it is difficult to characterize power semiconductor devices. A localized model of the inverter, concentrating on the segment without power switches, is constructed using PBG as detailed in [28]. In [29], the concept of switched power junctions is proposed, and it is suitable for modeling power electronic converters, as mentioned in [30]. In [31], the P-cell and N-cell were introduced as the basic switching units that form the foundation of most power electronic circuits. These cells, each comprising a switching device and a diode, offer a new perspective on circuit topology and facilitate the systematic design and evolution of power conversion circuits. In [32], a switching equivalent model of PBG is proposed, which is only applicable to discrete switch control signals. After solving switch modeling, PBG is suitable for pure circuit modeling, and its modeling process is more concise compared to small signal modeling. Especially for inverter circuits where the output points of the bridge arms are not fixed, PBG is able to build a unified circuit model without frequent model adjustments due to the switching of the output points of the bridge arms.

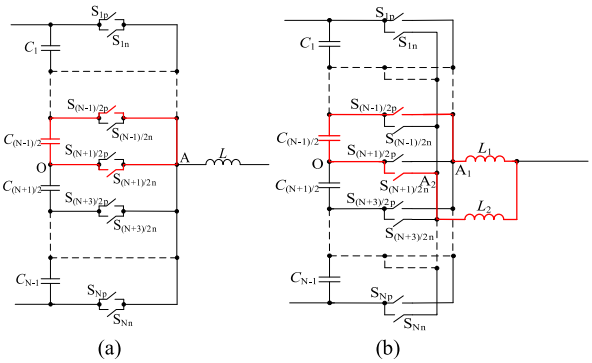


Fig. 1. Construction regulation of single bridge leg to eliminate the shoot-through branches. (a) Simplified structure of single bridge leg for multilevel bridge-type inverters. (b) Construction principle of single bridge leg without shoot-through problem.

Since the filters are coupled in the topology, the traditional inverter transfer function is not suitable for the newly generated topology. Using the PBG method, an accurate inverter model can be obtained for designing the control system. In order to establish an accurate PBG model, this article proposes a new switching junction applied to PBG, which is suitable for both discrete and continuous control signals. It contains a switch and a diode with alternating conduction, which is called switch-diode combined junction (SDJ). With the proposed SDJ, the transfer function within a continuous domain of the inverter can be derived easily. Based on this, the control system complex vector model in synchronous rotating frame (SRF) can be established. A multiconstrained complex coefficient controller is designed to improve the dynamic performance of inverters.

The rest of this article is organized as follows. Section II analyses the topology construction regulation of inverters without shoot-through problem, and the working principle and dc capacitors balance are discussed. Taking two kinds of typical multilevel inverter as an example, the process of topology regulation is given. Section III introduces the proposed SDJ and derives the inverter transfer function with the PBG method. Section IV establishes the control system complex vector model in SRF and designs the multiconstrained complex coefficient controller. Section V gives the simulation and experimental results to verify the correctness of the theoretical analysis. Finally, Section VI concludes this article.

II. Topology Construction Regulation

A. Elimination of Shoot-Through Branches of Single Bridge Leg

The bridge legs of the traditional bridge-type inverter have shoot-through branches, the elimination of which is necessary. Fig. 1 shows the construction regulation of a single bridge leg to eliminate the shoot-through branches. Fig. 1(a) shows the simplified structure of a single bridge leg for multilevel bridge-type inverters. O is the midpoint of dc voltage. A is the output point of the bridge leg. L is the ac side filter. Taking the dc capacitor $C_{(N-1)/2}$ for example, the power devices $S_{(N-1)/2p}$ and $S_{(N-1)/2n}$, respectively, from the forward and reverse pathways

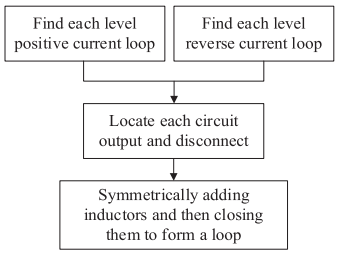


Fig. 2. Construction regulation of flowchart.

from the positive point of $C_{(N-1)/2}$ to the ac side. $S_{(N+1)/2p}$ and $S_{(N+1)/2n}$, respectively, from the forward and reverse pathways from the negative point of $C_{(N-1)/2}$ to the ac side. $S_{(N-1)/2p}$, $S_{(N-1)/2n}$, $S_{(N+1)/2p}$, and $S_{(N+1)/2n}$ are the combination of single or multiple power devices, such as the diodes, IGBTs, and MOSFETs [33]. Also, the same power device can be multiplexed in different pathways. The unreliable cut-off of the power devices may cause simultaneous conduct of $S_{(N-1)/2p}$ and $S_{(N+1)/2n}$, which would cause the short-circuit fault of $C_{(N-1)/2}$, which is also called the shoot-through fault. Each dc capacitor or their combination would cause shoot-through fault so dead-time is necessary for the bridge-type inverter.

Fig. 1(b) shows the construction principle of a single bridge leg without shoot-through problem. In order to eliminate the shoot-through branches, the ac side filter L is embedded in the branch. The inductive current cannot change suddenly so simultaneously conduct of $S_{(N-1)/2p}$ and $S_{(N+1)/2n}$ will not cause short-circuit fault of $C_{(N-1)/2}$. To ensure the symmetry of the positive and negative half cycle, L is split into L_1 and L_2. To further reduce the volume, L_1 and L_2 can be designed as coupled inductors [21].

Multilevel inverters have the problem of unbalanced dc capacitor voltage. Additional balancing circuits need to be added, or the operating time of the control vectors needs to be adjusted [34]. The topology in Fig. 1(b) allows simultaneous conduct of S(N-1)/2p and S(N+1)/2n. It is a new switching mode that traditional bridge-type inverters do not have, which can be called shoot-through mode. In this mode, $C_{(N-1)/2}$ discharges to L_1 and L_2. In other switching modes, L_1 and L_2 can transfer energy to other capacitors. With this principle, it is easy to achieve the balance of dc capacitors. Fig. 2 illustrates the rules for generating a new topology, visualizing the logical structure of the provision and the implementation steps.

B. Construction of Typical Multilevel Bridge Leg

With the construction regulation, any existing two-level or multilevel bridge-type inverter can be converted into a new topology without shoot-through problem. Fig. 3 shows the regulation process of two typical three-level topologies. Fig. 3(a) and (b) is the leg of the I-type three-level neutral-point-clamped (3L-NPC) inverter. S_{1p} is the combination of S_1 and S_2. S_{1n} is the combination of D_{11} and D_{12}, which can be replaced by a single high-voltage diode. S_{2p} is the combination of D_3 and S_2. S_2 is multiplexed in both S_{1p} and S_{2p}. L is embedded in the branch and split into L_1 and L_2. Fig. 3(c) and(d) is the leg

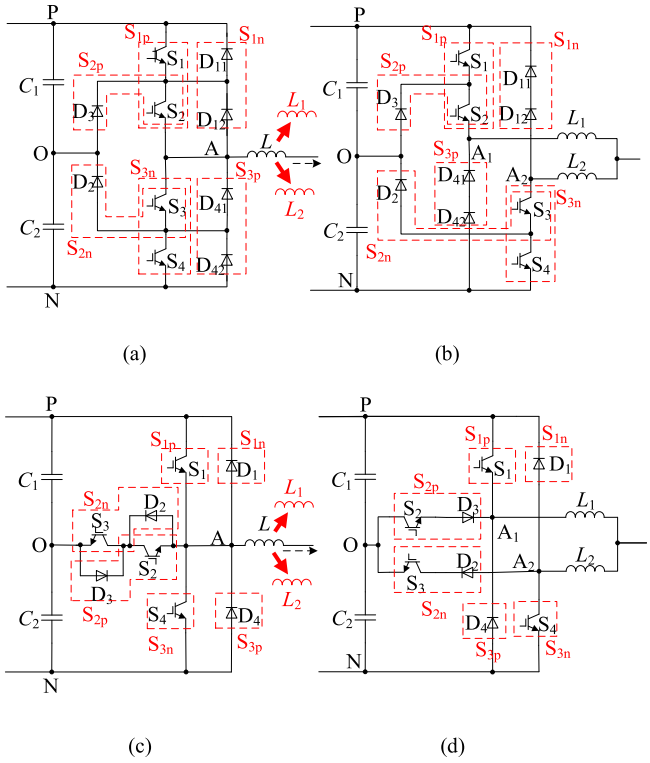


Fig. 3. Construction process of two typical three-level topologies. (a) Leg of I-type 3L-NPC inverter. (b) Newly leg of I-type 3L-NPC inverter. (c) Leg of T-type 3L-NPC inverter. (d) Newly leg of T-type 3L-NPC inverter.

TABLE I
UNIFIED SWITCHING EFFECT OF TWO TYPES OF INVERTERS

Output voltage	S_{1p}VS$_{1n}$	S_{2p}VS$_{2n}$	S_{3p}VS$_{3n}$
U_P	1	0	0
U_O	0	1	0
U_N	0	0	1

of the T-type 3L-NPC inverter. S_{1p} is the single switch S_1. S_{1n} is the single diode D_1. S_{2p} is the combination of S_2 and D_3. S_{2n} is the combination of S_3 and D_2. It can be seen that the I-type and T-type 3L-NPC inverters have a common topology regulation process from bridge-type to the new topology without shoot-through problem.

The output point of the bridge-type 3L-NPC inverter is A. For the newly constructed topology, there are two output points, A_1 and A_2. The unified switching effect of the two kinds of inverters can be obtained, which is shown in Table I.

With the topology construction method, the five-level topologies also can be regulated. Fig. 4 shows the typical topologies. Fig. 4(a) and (b) is the legs of 5L-NPC and its improved topology described in [35]. Fig. 4(c) and (d) is the cascade topologies with single dc source and multiple independent dc sources. It can be seen that the proposed method is applicable to all topologies. But in cascade topologies, more inductors are necessary. The construction method is more suitable for the NPC topologies.

Fig. 5 and 6 show the switching modes of I-type and T-type newly constructed bridge legs without shoot-through problem.

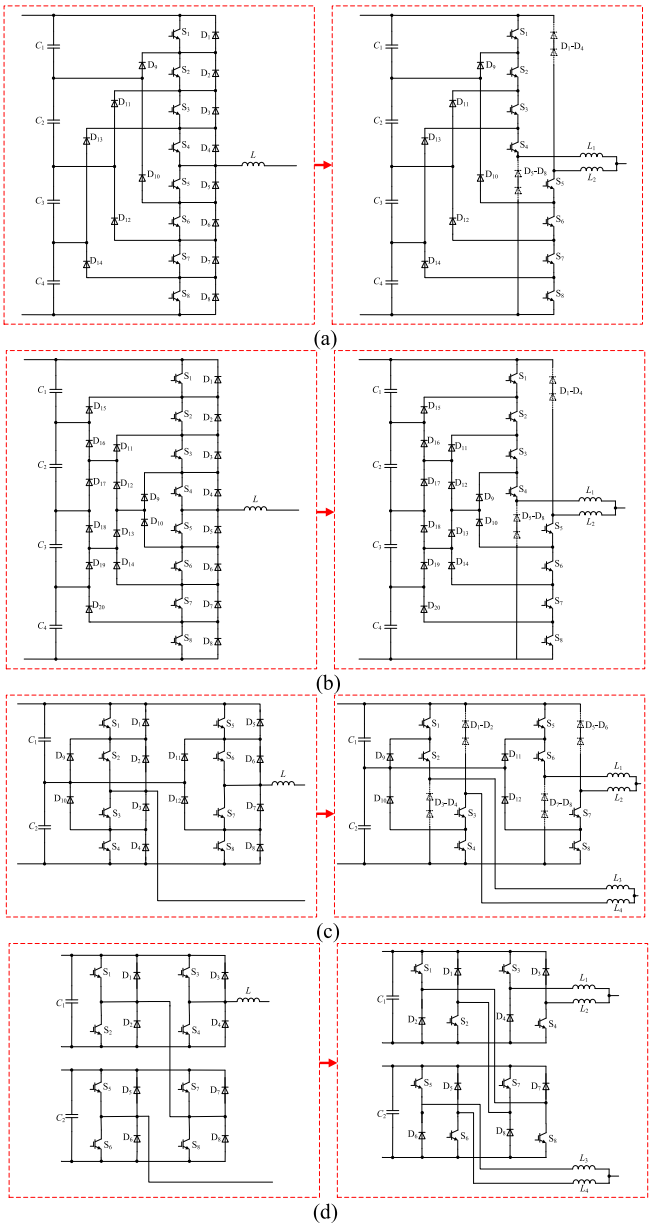


Fig. 4. Construction process of typical five-level topologies. (a) Leg of 5L-NPC inverter. (b) Leg of improved 5L-NPC inverter. (c) Leg of cascade topology with single DC source. (d) Leg of cascade topology with multiple independent DC sources.

The positive direction of ac current is defined in Fig. 3. In the positive half cycle, the output point of the bridge leg is A_1, and in the negative half cycle, the output point of the bridge leg is A_2. As a result, the output point of the bridge leg would switch in each half cycle. The traditional bridge-type inverter transfer function is not suitable for the newly generated topology because the filtering plant is coupled in the topology. In [20], the dual-buck inverter is equivalent to the bridge-type inverter but it is only applicable to the situation where L_1 and L_2 are the same. What is more, the model is affected by control strategies, so a more accurate modeling method needs to be considered.

The A-phase of an I-NPC three-level inverter includes four power switches S_1–S_4 and four diodes D_1–D_4. Assuming that

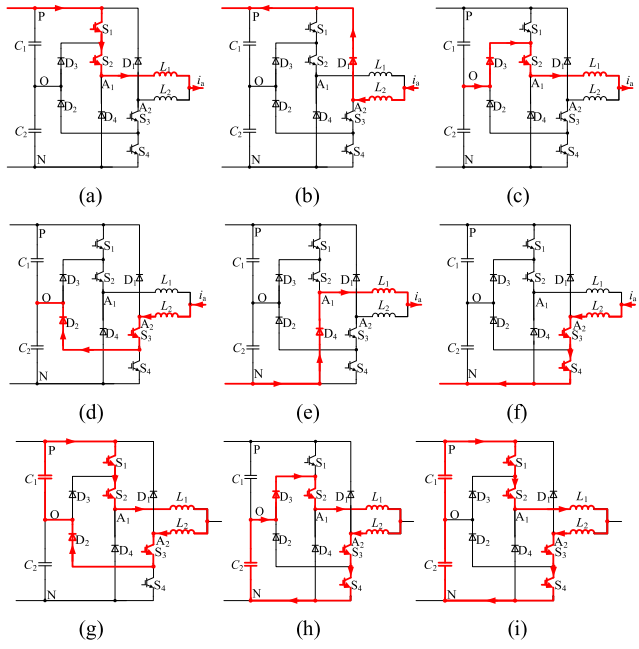


Fig. 5. Switching modes of the I-type newly constructed bridge leg without shoot-through problem. (a) P-level output during the positive half cycle of the AC current. (b) P-level output during the negative half cycle of the AC current. (c) 0-level output during the positive half cycle of the AC current. (d) 0-level output during the negative half cycle of the AC current. (e) N-level output during the positive half cycle of the AC current. (f) N-level output during the negative half cycle of the AC current. (g) Shoot-through mode with capacitor C_1 discharging. (h) Shoot-through mode with capacitor C_2 discharging. (i) Shoot-through mode with capacitors C_1 and C_2 discharging simultaneously.

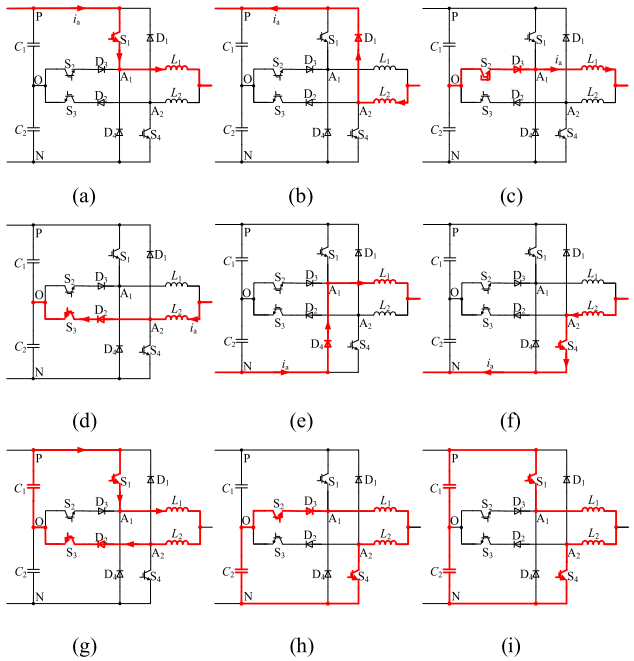


Fig. 6. Switching modes of the T-type newly constructed bridge leg without shoot-through problem. (a) P-level output during the positive half cycle of the AC current. (b) P-level output during the negative half cycle of the AC current. (c) 0-level output during the positive half cycle of the AC current. (d) 0-level output during the negative half cycle of the AC current. (e) N-level output during the positive half cycle of the AC current. (f) N-level output during the negative half cycle of the AC current. (g) Shoot-through mode with capacitor C_1 discharging. (h) Shoot-through mode with capacitor C_2 discharging. (i) Shoot-through mode with capacitors C_1 and C_2 discharging simultaneously.

the current i_a flowing from the dc side to the ac side is defined as positive, when S_1 and S_2 simultaneously turn ON, and S_3 and S_4 turn OFF, the output of the inverter's A-phase is denoted as the potential of P. When the inverter output current $i_a > 0$, as shown in Fig. 5(a), the current flows through S_1 and S_2 from the dc side to the ac side. When $i_a < 0$, as illustrated in Fig. 5(b), the current flows through D_1 from the ac side back to the dc side.

When S_1 and S_4 turn OFF, and S_2 and S_3 turn ON, the output of the inverter's A-phase is denoted as the potential of O. When $i_a > 0$, as shown in Fig. 5(c), the current flows through D_3 and S_2 from the dc side to the ac side. When $i_a < 0$, as depicted in Fig. 5(d), the current flows through S_3 and D_2 from the ac side back to the dc side.

When S_1 and S_2 turn OFF, and S_3 and S_4 turn ON, the output of the inverter's A-phase is denoted as the potential of N. When $i_a > 0$, as shown in Fig. 5(e), the current flows through D_4 from the dc side to the ac side. When $i_a < 0$, as illustrated in Fig. 5(f), the current flows through S_3 and S_4 from the ac side back to the dc side.

The allowable voltage difference between capacitors C_1 and C_2 is ΔU. When the voltage of C_1 is higher than that of C_2, and the voltage difference exceeds the maximum allowable voltage difference ΔU, S_1, S_2, and S_3 will turn ON and S_4 will turn OFF. At this point, C_1 discharges through the shoot-through mode to reduce the voltage difference between C_1 and C_2, as shown in Fig. 5(g). When the voltage of C_1 is lower than that of C_2, and the voltage difference exceeds the maximum allowable voltage difference ΔU, S_2, S_3, and S_4 will turn ON and S_1 will turn OFF. At this point, C_2 discharges through the shoot-through mode to reduce the voltage difference between C_1 and C_2, as shown in Fig. 5(h). When S_1, S_2, S_3, and S_4 all turn ON simultaneously, C_1 and C_2 will discharge through the shoot-through mode, as shown in Fig. 5(i).

Compared to the traditional bridge-type topologies, the newly constructed topologies have a new switching mode called shoot-through mode, which contains three situations: C_1 discharges, C_2 discharges, and C_1 and C_2 discharge together. Utilizing the shoot-through mode that C_1 discharges or C_2 discharges, the dc capacitors can easily achieve balance. For the five-level topologies shown in Fig. 4, the capacitors C_1–C_4 also have shoot-through discharge circuit loop formed by L_1, L_2 and the corresponding power switches, which is similar as the three-level topologies. As a result, all of the proposed multilevel topologies can realize capacitor balance through capacitor discharge in instantaneous shoot-through mode in theory.

Under the same LCL filter parameters, the topology without shoot-through problem exhibits lower total harmonic distortion compared to the conventional topology, mainly because the additional harmonics caused by the dead-time are mainly concentrated in the low-frequency band, whereas the LCL filter has a stronger attenuation capability for high-frequency harmonics. According to the LCL filter parameters in Table II, the overall size and cost of the filter can be reduced despite the increase in the number of inductors. Therefore, when the dead-time is removed, the LCL filter improves the overall system performance more significantly.

TABLE II
DETAILED PARAMETERS FOR THE LCL FILTER

Parameter	Inductor		Capacitor
	Inverter-side	Grid/Load-side	
Proposed	$L_f = 0.5$ mH $M = 0.3$ mH	0.8 mH	20 μF
Traditional	$L_{12} = 1.4$ mH	1.0 mH	20 μF

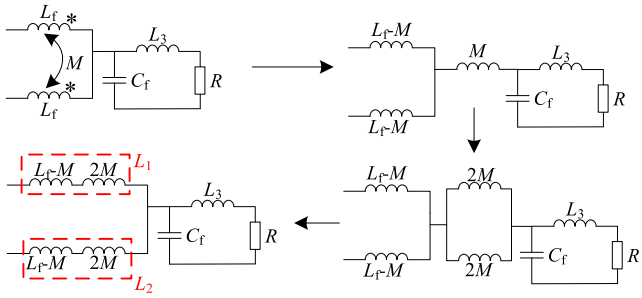


Fig. 7. Equivalent circuit of a-phase with uncomplete-coupled inductors.

As shown in Fig. 7, L_1 and L_2 can be converted to three separate inductors by the equivalent model

$$\begin{cases} L_1 = L_2 = L_f + M \\ L_3 = M \end{cases}. \tag{1}$$

PBG are centered on describing the flow of energy and conversion relationships in a circuit. Although coupled inductors introduce additional magnetic coupling effects, this does not change the basic energy flow laws in the circuit. Therefore, the use of coupled inductors does not interfere with the correctness and validity of the power bonding diagram through appropriate equivalent processing.

Inductors are passive components that can be easily integrated into the inverter design without substantially increasing system complexity. In contrast, implementing software or hardware-based dead time compensation networks often requires additional programming, calibration, and testing, which can be time-consuming and resource-intensive. Inductors help suppress voltage spikes during switching transitions, reducing switching losses. By optimizing the current waveform, inductors can minimize harmonic distortion caused by dead time effects, leading to improved output power quality.

III. PBG OF THE INVERTER

A. SDJ and Its Application

In the newly constructed topology, the filtering plant is coupled in the topology. The output points of the bridge switch between A_1 and A_2. The switches always work in coordination with the corresponding diodes. Under continuous current, once switch S is turned OFF, diode D will conduct freewheeling. S and D conduct alternately. Therefore, they can form a junction together applied to PBG, which is called SDJ. Fig. 8 shows two connection forms of switch and diode. The positive direction of the current is shown in the figures. In Fig. 8(a), the positive

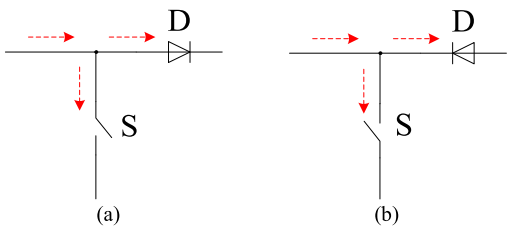


Fig. 8. Two connection forms of switch and diode. (a) Circuit of diversion form. (b) Circuit of confluence form.

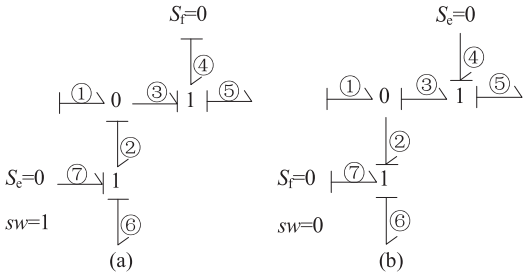


Fig. 9. Unified PBG of combined switch and diode. (a) $sw = 1$. (b) $sw = 0$.

direction is the same as that of the real current. In Fig. 8(b), the positive direction is opposite to that of the real current.

The control signal of S is *sw*. In the condition that $sw = 1$, S turns ON and D turns OFF. S can be seen as a potential source and the potential variable $S_e = 0$. D can be seen as a current source and the current variable $S_f = 0$. In the condition that $sw = 0$, S can be seen as a current source, and $S_f = 0$. D can be seen as a potential source and $S_e = 0$. With the positive direction, the two connection forms can be unified and the PBG of them are the same. Fig. 9 shows the unified PBG of combined the switch and diode. Fig. 9(a) is the PBG in the condition that $sw = 1$ and Fig. 9(b) is the PBG in the condition that $sw = 0$.

It can be seen that there are seven junctions in the PBG. Junctions ②, ③, ④, and ⑦ are the inner junctions. The causal relationships of them change with *sw*. ①, ⑤, and ⑥ are the external junctions. The causal relationships of them are certain, which have no relationship with *sw*.

In the PBG, only one input is allowed as a potential of a "0" node. The potentials of each junction in the "0" node are the same. Only one input is allowed as a current of a "1" node. The currents of each junction in the "1" node are the same. Under the defined energy flow reference direction, the relationships of the junctions are as follows:

$$\begin{cases} u_1 = u_2 = u_3, i_1 = i_2 + i_3 \\ u_5 = u_3 + u_4, i_3 = i_4 = i_5 \\ u_6 = u_7 + u_2, i_2 = i_6 = i_7. \end{cases} \tag{2}$$

In Fig. 9(a), $sw = 1$, $u_7 = 0$, $i_4 = 0$. In Fig. 9(b), $sw = 0$, $i_7 = 0$, $u_4 = 0$. The relationships of the external junctions can be expressed as follows:

$$\begin{cases} i_5 = (1 - sw)i_1 \\ i_6 = swi_1 \\ u_1 = swu_6 + (1 - sw)u_5. \end{cases} \tag{3}$$

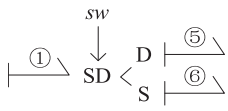


Fig. 10. Model of SDJ.

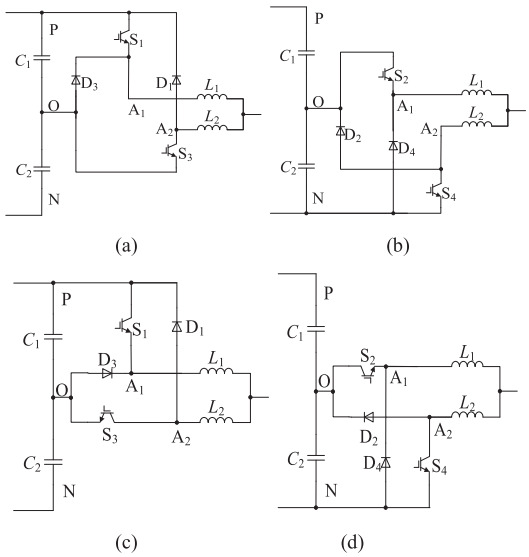


Fig. 11. Equivalence of two-level and three-level inverters constructed by the proposed regulation. (a) Positive half cycle of reference waveform (I-type). (b) Negative half cycle of reference waveform (I-type). (c) Positive half cycle of reference waveform (T-type). (d) Negative half cycle of reference waveform (T-type).

According to the principle of area equivalence, the discrete signal *sw* can be replaced by A continuous signal. In (3), *sw* can be a continuous signal in the range of [0,1]. As a result, the SDJ can be established and it can be represented in the form of Fig. 10. It is universal for both discrete and continuous signals. With SDJ, the inverters based on digital control can be transformed into continuous systems, thereby writing state equations and deriving transfer functions.

Fig. 11 shows the equivalence of two-level and three-level inverters, which are both constructed by the proposed regulation. In the pulsewidth modulation methods of three-level inverters, some power devices would keep normally on for half a cycle [36]. In the positive half cycle of reference waveform, S_2 in the I-type and T-type legs keeps normally on and can be considered as a short circuit. The switch status of D_2 follows that of S_3, it also can be considered as a short circuit. S_4 and D_4 do not work and the branches of them can be ignored. Similarly, in the negative half cycle of the reference waveform, S_3 and D_3 can be regarded as short circuits. The branches of S_1 and D_1 can be ignored.

It can be seen that the equivalent circuits of the I-type inverter and the T-type inverter are the same. In the positive half cycle of the reference waveform, the three-level inverter can is equivalent to a two-level inverter with an input voltage of C_1, while in the negative half cycle, it is equivalent to that with an input voltage of C_2.

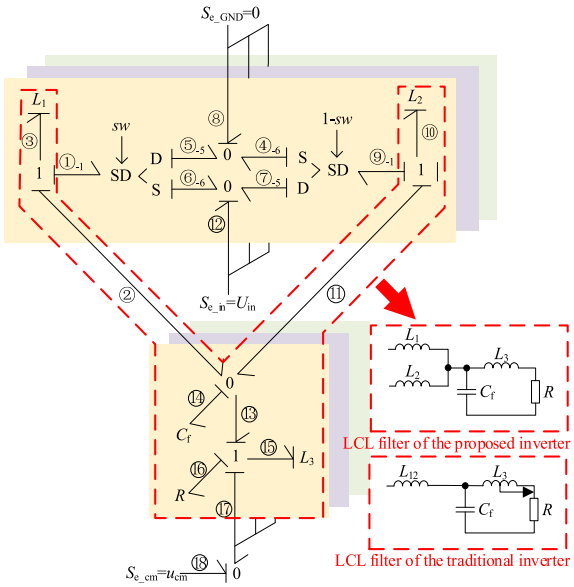


Fig. 12. PBG model of the three-phase inverters without shoot-through peoblem.

As a result, the two-level, I-type and T-type three-level inverters without shoot-through peoblem can share the same PBG model. Fig. 12 shows the common PBG model of the three-phase inverters without shoot-through peoblem. LCL filter is applied, in which L_1 and L_2 are equivalent to the inverter-side inductor. L_3 is the load-side inductor. C_f is the capacitor in the LCL filter. R is the equivalent input impedance on the ac side. U_in is the voltage of C_1 or C_2. u_cm is the common mode voltage. Because the state equation is established in a continuous domain, u_cm is 0.

B. State Equation and Transfer Function Derivation of the Inverter

The state equation of the inverter can be established by Fig. 12. The input variable is

$$u(t) = sw(t). \tag{4}$$

The state variables also are energy variables, which can be expressed as

$$x(t) = \begin{bmatrix} q_{14} & p_{15} & p_3 & p_{10} \end{bmatrix}^T \tag{5}$$

where q_{14} is the capacitor charge of C_f. The current of C_f is i_{14} and it is the differential of q_{14}. p_3, p_{10}, and p_{15} are the flux of L_1, L_2, and L_3. The inductor voltages are the differential of fluxes. Therefore, the differential of the state variables is

$$\dot{x}(t) = \begin{bmatrix} \dot{q}_{14} & \dot{p}_{15} & \dot{p}_3 & \dot{p}_{10} \end{bmatrix}^T = \begin{bmatrix} i_{14} & u_{15} & u_3 & u_{10} \end{bmatrix}^T. \tag{6}$$

The capacitor voltage u_{14}, and inductor current i_{15}, i_3, i_{10} can be expressed as

$$\begin{bmatrix} u_{14} & i_{15} & i_3 & i_{10} \end{bmatrix} = \begin{bmatrix} \frac{q_{14}}{C_f} & \frac{p_{15}}{L_3} & \frac{p_3}{L_1} & \frac{p_{10}}{L_2} \end{bmatrix}. \tag{7}$$

According to the relationship shown in Fig. 12, (6) can be converted as

$$\dot{x}(t) = \begin{bmatrix} 0 & -\frac{1}{L_3} & \frac{1}{L_1} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{R}{L_3} & 0 & 0 \\ -\frac{1}{C_f} & 0 & 0 & 0 \\ -\frac{1}{C_f} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} q_{14} \\ p_{15} \\ p_3 \\ p_{10} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -U_\mathrm{in} \\ -U_\mathrm{in} \end{bmatrix} sw = Ax(t) + Bu(t). \tag{8}$$

The output variable of the inverter is i_{16}, thus, the output equation can be expressed as

$$y(t) = \frac{1}{L_3} p_{15} = \begin{bmatrix} 0 & \frac{1}{L_3} & 0 & 0 \end{bmatrix} \begin{bmatrix} q_{14} \\ p_{15} \\ p_3 \\ p_{10} \end{bmatrix} = C^T x(t). \tag{9}$$

After Laplace transform, (8) and (9) can be transformed as

$$\begin{cases} sX(s) = AX(s) + BU(s) \\ Y(s) = C^T X(s). \end{cases} \tag{10}$$

Ignoring the switching delay, the transfer function from sw to i_{16} can be expressed as

$$G(s) = \frac{Y(s)}{U(s)} = C^T (sI - A)^{-1} B = C^T \frac{(sI - A)^*}{|sI - A|} B. \tag{11}$$

After matrix operation, $G(s)$ can be expressed as (12) shown at the bottom of this page, where the coefficient K_1 is

$$K_1 = \frac{2U_\mathrm{in} L_1 L_2}{L_3}. \tag{13}$$

The LCL filter also has a resonant frequency f_res, which is

$$f_{res} = \sqrt{\frac{L_1 L_2 + L_2 L_3 + L_1 L_3}{L_1 L_2 L_3 C_f}}. \tag{14}$$

With the PBG method, the transfer function of a traditional bridge-type inverter with an LCL filter can also be obtained, which is

$$G'(s) = \frac{U_\mathrm{in}}{L_{12} L_3 C_f s^3 + L_1 C_f R s^2 + (L_{12} + L_3) s + R} \tag{15}$$

where L_{12} is also shown in Fig. 12. In the condition that $L_1 = L_2$, $G(s)$, and $G'(s)$ are exactly the same. In the real condition, L_1 and L_2 would deviation. $G'(s)$ cannot be used as the transfer function of the inverters without shoot-through peoblem. Therefore, (12) should be used in the design process of the controller.

$$G(s) = \frac{K_1}{L_1 L_2 L_3 C_f s^3 + L_1 L_2 C_f R s^2 + (L_1 L_2 + L_2 L_3 + L_1 L_3) s + (L_1 + L_2) R} \tag{12}$$

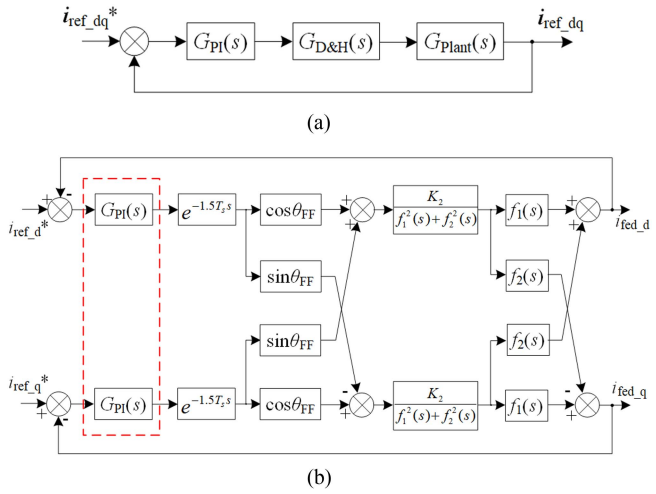


Fig. 13. Control diagram of the inverter system. (a) Complex vector diagram. (b) Coupling relationship of the *dq*-axis.

IV. Control System Design

A. Establish of the Control System Complex Vector Model

Model predictive control (MPC) can be easily realized with (4), (8), and (9). But MPC has the disadvantages of large computation and poor real-time performance [37]. In this article, complex vector control is used to realize the decoupled dynamic performance of the inverter.

In the stationary frame (SF), a synthetic vector of signal can be expressed as

$$x_{\alpha\beta} = A(\cos\omega t + j\sin\omega t) \tag{16}$$

where A is the amplitude of the signal, ω is the angular frequency. After coordinate transformation, the signal in SRF can be expressed as

$$x_{dq} = A\left[\cos\left(\omega-\omega_0\right)t + j\sin\left(\omega-\omega_0\right)t\right] \tag{17}$$

where ω_0 is the fundamental angular frequency. According to (16) and (17), the relationship between the transfer function in SF and SRF is

$$G_{\alpha\beta}(s_{\alpha\beta}) = G_{dq}(s_{dq} + j\omega_0). \tag{18}$$

The transfer function (12) is established in SF, in which s is $s_{\alpha\beta}$. It can be easily converted to that in SRF. Fig. 13 shows the control diagram of the inverter system. Fig. 13(a) is the complex vector diagram. $\boldsymbol{i}_{\mathrm{ref\_dq}}*$ is the reference current vector, which can be can be expressed as

$$\boldsymbol{i}_{ref\_dq}{}^* = i_{ref\_d} + ji_{ref\_q}. \tag{19}$$

The real part is the d-axis current and the imaginary part is the q-axis current. Similarly, $\boldsymbol{i}_{\mathrm{ref\_dq}}$ is the output current vector.

$G_{\mathrm{D\&H}}(s)$ is the time delay introduced by digital control [37], which is

$$G_{D\&H}(s) = e^{-1.5T_s(s+j\omega_0)} = e^{-1.5T_s s}(\cos\theta_{FF} - j\sin\theta_{FF}) \tag{20}$$

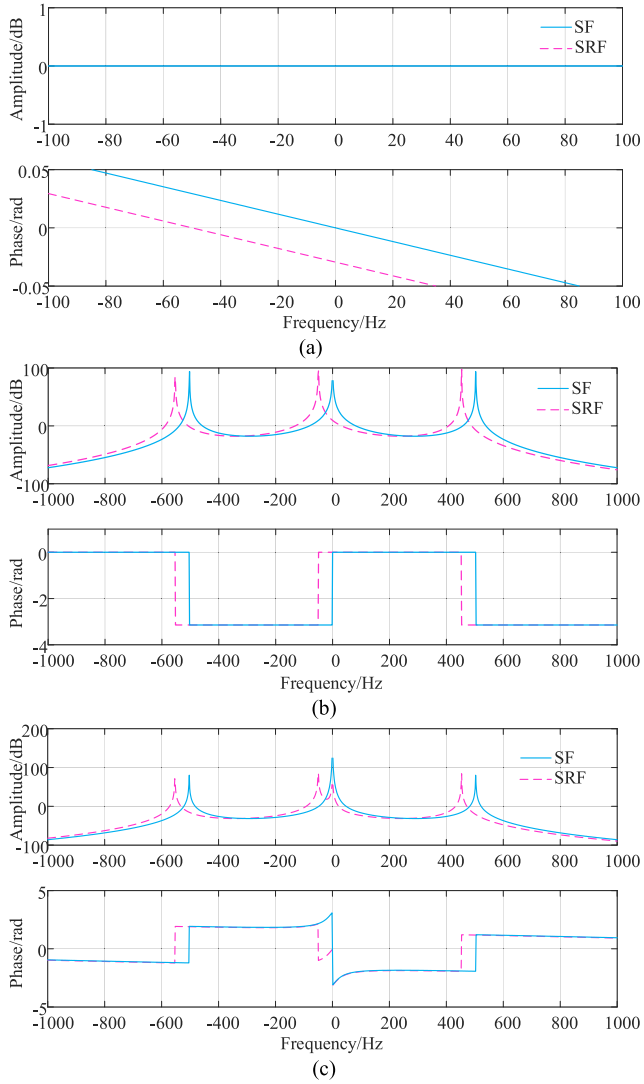


Fig. 14. Comparisons of response curves in different frames ($R = 0$). (a) $G_{\mathrm{D\&H}}(s)$. (b) $G_{\mathrm{Plant}}(s)$. (c) $G_{\mathrm{PI}}(s)G_{\mathrm{D\&H}}(s)G_{\mathrm{Plant}}(s)$.

where T_s is the sampling and calculation period. θ_{FF} is $1.5T_s\omega_0$. $G_{\mathrm{Plant}}(s)$ is the inverter transfer function in SRF, which is

$$G_{\mathrm{Plant}}(s) = \frac{K_2}{f_1(s) + jf_2(s)} \tag{21}$$

in which $K_2, f_1(s)$ and $f_1(s)$ are

$$\begin{cases} f_1(s) = s^3 + \frac{R}{L_3}s^2 + \left(\frac{L_1L_2+L_2L_3+L_1L_3}{L_1L_2L_3C_f} - 3\omega_0^2\right)s \\ \qquad\quad + \left(\frac{L_1+L_2}{L_1L_2L_3C_f} - \frac{\omega_0^2}{L_3}\right)R \\ f_2(s) = 3\omega_0 s^2 + \frac{2\omega_0 R}{L_3}s + \omega_0\left(\frac{L_1L_2+L_2L_3+L_1L_3}{L_1L_2L_3C_f} - \omega_0^2\right) \\ K_2 = \frac{2U_{\mathrm{in}}}{{L_3}^2C_f}. \end{cases} \tag{22}$$

$G_{\mathrm{D\&H}}(s)$ and $G_{\mathrm{Plant}}(s)$ contain imaginary parts, which would introduce coupling of the *dq*-axis. Fig. 13(b) shows the coupling relationship of the *dq*-axis. If a traditional PI controller is applied in the current loop, the coupling of the *dq*-axis is obvious. Fig. 14 shows the comparison of the double-side response curves in

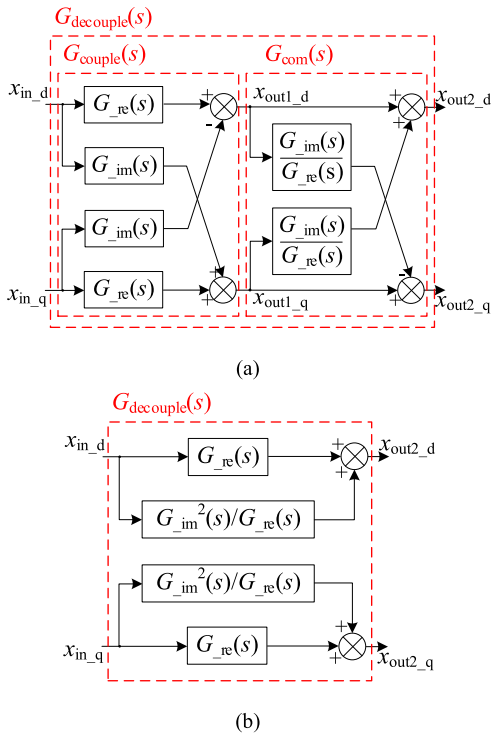


Fig. 15. Unified control diagram of a coupled system and its decoupling method. (a) Decoupling of a coupled transfer function. (b) Decoupled transfer function.

different frames. The negative frequency corresponds to a three-phase negative sequence ac signal. Fig. 14(a) is the comparison of $G_{\mathrm{D\&H}}(s_{\alpha\beta})$ and $G_{\mathrm{D\&H}}(s_{\mathrm{dq}})$. Fig. 14(b) is the comparison of $G_{\mathrm{Plant}}(s_{\alpha\beta})$ and $G_{\mathrm{Plant}}(s_{\mathrm{dq}})$. R is set as 0. In SF, both time delay and inverter models are decoupled, so the response curves of $G_{\mathrm{D\&H}}(s_{\alpha\beta})$ and $G_{\mathrm{Plant}}(s_{\alpha\beta})$ are symmetrical. After coordinate transformation, imaginary parts of the transfer functions are introduced so $G_{\mathrm{D\&H}}(s_{\mathrm{dq}})$ and $G_{\mathrm{Plant}}(s_{\mathrm{dq}})$ are asymmetrical, which implies that the system is coupled. Fig. 14(c) shows the response curves of the current loop. The traditional PI control is applied. The current loop has a serious coupling problem.

B. Design of the Multiconstrained Complex Coefficient Controller

The coupled transfer functions have a unified expression, which is

$$G_{\mathrm{couple}}(s) = G_{\_re}(s) + jG_{\_im}(s) \tag{23}$$

in which the imaginary part is the coupling term. The control diagram is shown in Fig. 15. Fig. 15(a) shows the decoupling of a coupled transfer function. A compensation $G_{\mathrm{com}}(s)$ is added to the control diagram, which can be expressed as

$$G_{com}(s) = 1 - j\frac{G_{\_im}(s)}{G_{\_re}(s)}. \tag{24}$$

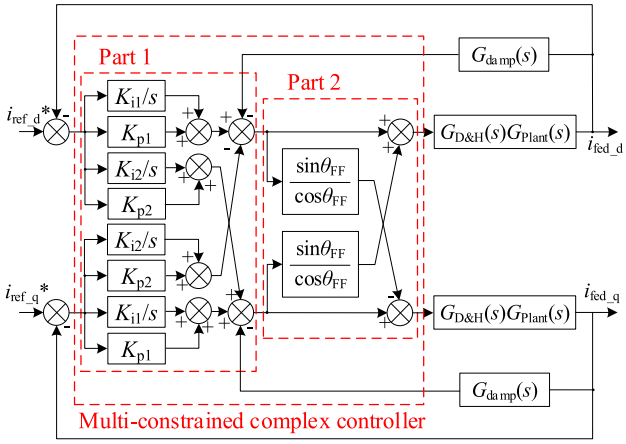


Fig. 16. Multiconstrained complex controller.

After compensation, the decoupled transfer function can be expressed as

$$G_{\mathrm{decouple}}(s) = G_{\_re}(s) + \frac{G_{\_im}(s)^2}{G_{\_re}(s)}. \tag{25}$$

It can be seen that the decoupled transfer function does not have an imaginary part. The control diagram of $G_{\mathrm{decouple}}(s)$ is shown in Fig. 15(b).

Therefore, the traditional PI controller and the decoupling compensation can form a high-order controller, the transfer function of which is

$$\begin{aligned} G_{ctr}(s) &= \left(K_p + \frac{K_i}{s}\right)\left(1 - j\frac{\sin\theta_{FF}}{\cos\theta_{FF}}\right)\left(1 - j\frac{f_2(s)}{f_1(s)}\right) \\ &= G_{ctr\_r}(s) + jG_{ctr\_i}(s) \end{aligned} \tag{26}$$

where $G_{\mathrm{ctr\_r}}(s)$ and $G_{\mathrm{ctr\_r}}(s)$ are

$$\begin{cases} G_{ctr\_r}(s) = \left(K_p + \frac{K_i}{s}\right)\left(1 - \frac{\sin\theta_{FF}}{\cos\theta_{FF}}\frac{f_2(s)}{f_1(s)}\right) \\ G_{ctr\_i}(s) = -\left(K_p + \frac{K_i}{s}\right)\left(\frac{\sin\theta_{FF}}{\cos\theta_{FF}} + \frac{f_2(s)}{f_1(s)}\right). \end{cases} \tag{27}$$

With the new controller $G_{ctr}(s)$, the current loop can be decoupled. However, a high-order controller would introduce more poles, which should be compensated. In order to simplify the controller, a multiconstrained complex controller has been proposed, which is shown in Fig. 16. $G_{damp}(s)$ is the active damping of the LCL filter, which can be expressed as

$$G_{damp}(s) = k\left(1 + j\frac{2\omega_0 s}{\omega_0^2 - s^2}\right)C_f L_3(s + j\omega_0)^2 \tag{28}$$

where k is the damping coefficient. The controller consists of two parts, Part I to compensate for $G_{\mathrm{D\&H}}(s)$ coupling, and Part II to compensate for $G_{\mathrm{Plant}}(s)$ coupling. Part II is just the specific implementation of Fig. 15. Part I is a complex PI controller. It needs to eliminate the poles introduced by coordinate transformation and ensure the symmetry of the response curve to achieve decoupling.

According to (21) and (22), the poles introduced by $G_{\text{plant}}(s)$ can be calculated by the following equation:

$$f_1(s)+jf_2(s)=\sum_{i=0}^{3}k_i s^i=0 \tag{29}$$

where k_0–k_3 are complex coefficients, which can be expressed as

$$\begin{cases} k_1=1 \\ k_2=\frac{R}{L_3}+3\omega_0 j \\ k_3=\frac{L_1L_2+L_2L_3+L_1L_3}{L_1L_2L_3C_f}-3\omega_0^2+\frac{2\omega_0 R}{L_3}j \\ k_4=\left(\frac{L_1+L_2}{L_1L_2L_3C_f}-\frac{\omega_0^2}{L_3}\right)R+\omega_0\left(\frac{L_1L_2+L_2L_3+L_1L_3}{L_1L_2L_3C_f}-\omega_0^2\right)j. \end{cases} \tag{30}$$

In order to compensate the poles, (29) should contain ($K_{\text{p}}s$+K_{i}), so k_0–k_3 have the following relationship:

$$g(K_p,K_i)={K_p}^3k_0-{K_p}^2K_ik_1+K_p{K_i}^2k_2-{K_i}^3k_3=0. \tag{31}$$

According to (30), K_{p} and K_{i} are also complex coefficients. In Fig. 16, K_{p1} and K_{i1} are the real part of the controller, while K_{p2} and K_{i2} are the imaginary part. Therefore, (31) can be transformed into

$$\begin{cases} g_1\left(K_{p1},K_{p2},K_{i1},K_{i2}\right)=\text{Re}\left[g\left(K_p,K_i\right)\right]=0 \\ g_2\left(K_{p1},K_{p2},K_{i1},K_{i2}\right)=\text{Im}\left[g\left(K_p,K_i\right)\right]=0 \end{cases}. \tag{32}$$

In Fig. 14, the response curves in SRF and SF among the high-frequency range are basically symmetrical. In order to realize symmetry during the low-frequency range, the positive and negative cutoff frequencies should be the same. The amplitude gain of the current loop can be expressed as

$$A\left(j\omega\right)=\left|K_{p1}+\frac{K_{i2}}{\omega}-j\left(\frac{K_{i1}}{\omega}-K_{p2}\right)\right|\left|G_{\text{plant}}\left(j\omega\right)\right|. \tag{33}$$

The expected cutoff frequency is ω_{c}, so another constraint condition for the controller coefficients is

$$\begin{cases} A\left(j\omega\right)=1 \\ A\left(-j\omega\right)=1+\varepsilon \end{cases} \tag{34}$$

where ε is the asymmetric threshold. It represents the allowable minor asymmetry. With (33) and (34), the parameters of the controller can be solved by iteration. Fig. 17 shows the response curve of the current loop with the control strategy shown in Fig. 16. It can be seen that the curve is basically symmetrical, and the resonance of the LCL filter can be eliminated. With Part I of the controller, the effective bandwidth changes from 41 Hz to 120 Hz. With Part II, the effective phase margin increases from approximately 39.55° to around 52.16°. The current loop with the proposed controller has a better dynamic performance.

V. Simulation and Experimental Verification

A PBG model based on MATLAB/Simulink has been established. Fig. 18 shows the proposed SDJ model. i_1, u_5, and u_6 are the input signals of SDJ. *sw*, u_1, i_5, and i_6 are the output signals.

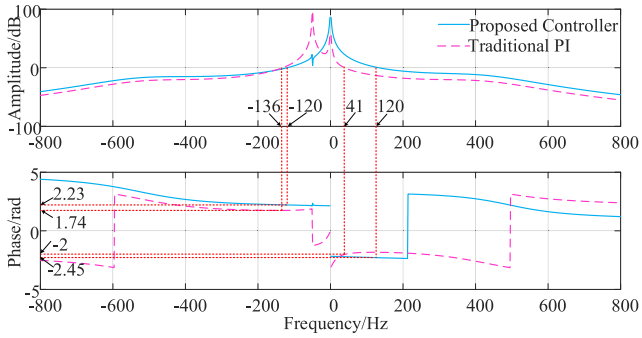


Fig. 17. Response curve of the current loop.

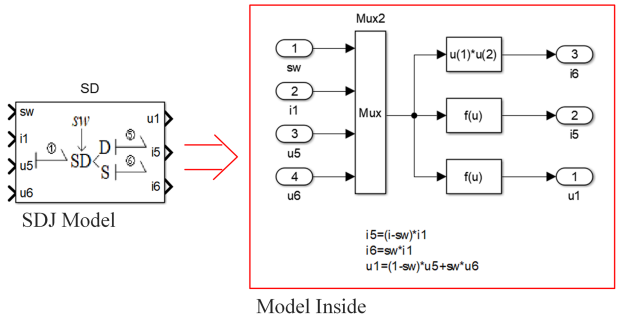


Fig. 18. SDJ simulink model.

Fig. 19 shows the simulation results of the PBG. U_{in} is 800 V. *sw* can be a continuous or discrete signal. The fundamental frequency of *sw* is 50 Hz and the switching frequency of *sw* is 10 kHz. Fig. 19(a) and (b) shows the comparison of the SDJ current with continuous and discrete *sw*. It can be seen that the fundamental waves of the signals in Fig. 19(b) are the same as the signals in Fig. 19(a). Fig. 19(c) and (d) shows the comparison of the SDJ voltages. The relationship of the signals is given in (3). Fig. 19(e) and (f) shows the comparison of the inductor current. With the LCL filter, the harmonic content of output current i_{L3} is low. The effect of continuous *sw* and discrete *sw* is the same.

An 18 kW three-phase I-type three-level newly constructed inverter without shoot-through problem has been established. The parameters are the same as the simulation. The control parameters K_{p1}, K_{p2}, K_{i1}, and K_{i2}, respectively, are 0.1435, −1.4620, 456.2283, and 45.3853. Fig. 20 shows the principle prototype. It contains the main and control circuit, sample and protect circuit, and LCL-type filter.

Fig. 21 shows the balancing effect of the dc capacitors. The voltage of C_1 is U_{up}. The voltage of C_2 is U_{down}. The allowed voltage difference between C_1 and C_2 is ΔU. If the difference between U_{up} and U_{down} is higher than ΔU, C_1 or C_2 should be discharged utilizing shoot-through mode, which is shown in Fig. 5(g) and (h). In Fig. 21, the initial value of U_{up} is higher than U_{down}, so C_1 should be discharged. The discharge process is controlled by the signal $EN_{\text{\_balance}}$, which enables the shoot-through mode of C_1. ΔU and $EN_{\text{\_balance}}$ are output from the DA port of the controller. In the condition that U_{up}-$U_{\text{down}}\geq\Delta U$, $EN_{\text{\_balance}}$ can be 1 or a narrow pulse with fixed frequency and duty cycle. When $EN_{\text{\_balance}}$ is 1, it will not change to 0

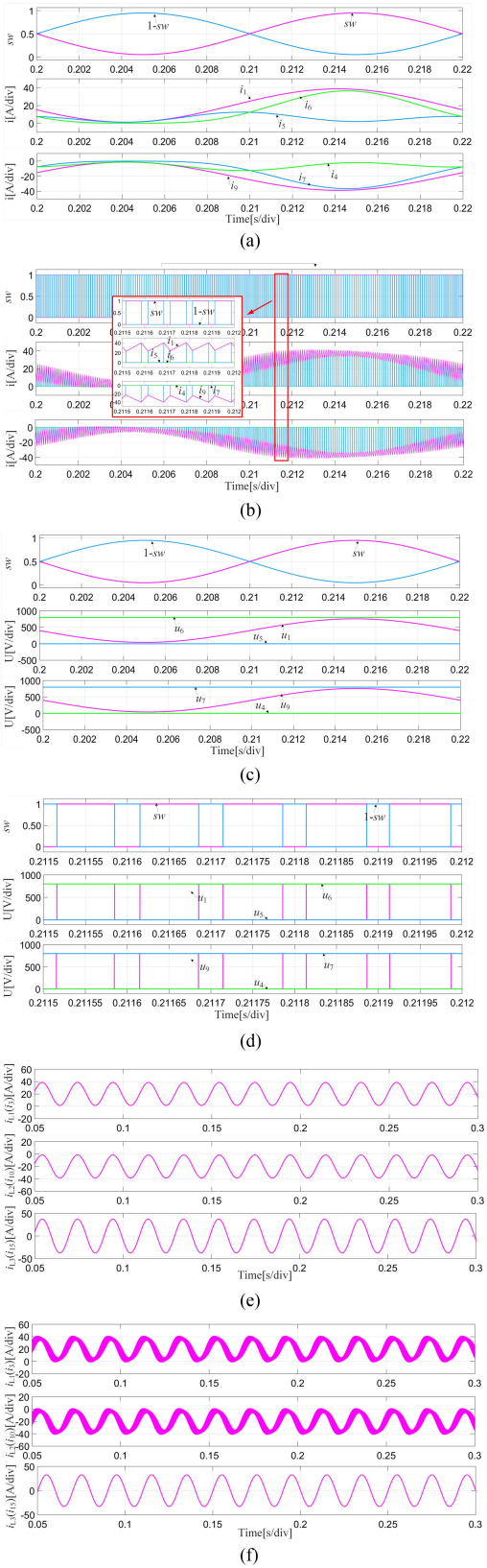


Fig. 19. Simulation results of the PBG. (a) SDJ current (continuous signal *sw*). (b) SDJ current (discrete signal *sw*). (c) SDJ voltage (continuous signal *sw*). (d) SDJ voltage (discrete signal *sw*). (e) Inductor current (continuous signal *sw*). (f) Inductor current (discrete signal *sw*).

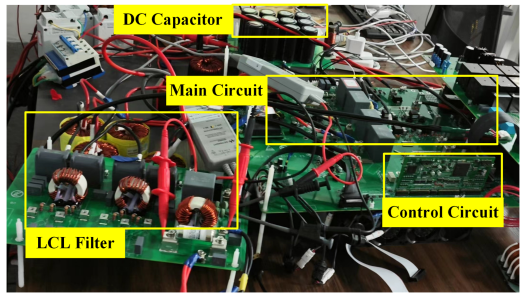


Fig. 20. Principle prototype.

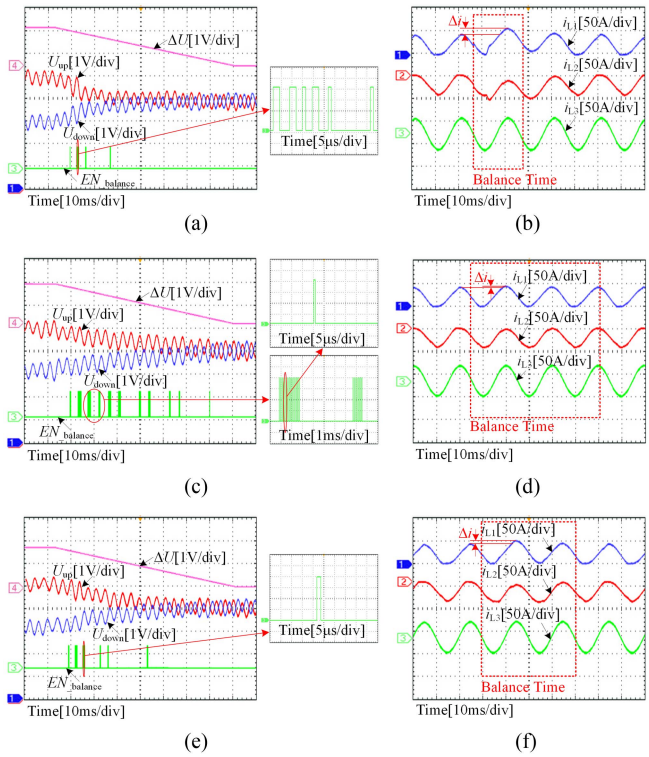


Fig. 21. Balancing effect of DC capacitors. (a) Variation of DC voltages with fixed shoot-through time (10 kHz, 1%). (b) Variation of inductor current with fixed shoot-through time (10 kHz, 1%). (c) Variation of DC voltages with fixed shoot-through time (10 kHz, 2%). (d) Variation of inductor current with fixed shoot-through time (10 kHz, 2%). (e) Variation of DC voltages with changing shoot-through time. (f) Variation of inductor current with changing shoot-through time.

until U_{up}-U_{down} is less than ΔU. As a result, during the balance process, shoot-through time is not fixed. Fig. 21(a) and (b) shows the variation of dc voltages and inductor current with changing shoot-through time. C_1 and C_2 can realize balance quickly, but the inductor currents of L_1 and L_2 would significantly increase. This problem can be solved if $EN_{\_\mathrm{balance}}$ is a narrow pulse. Fig. 21(c)–(f) shows the variation of dc voltages and inductor current with fixed shoot-through time. The frequency of the narrow pulse is 10 kHz. The balance time and current increment are related to the duty cycle. In Fig. 21(c) and (d), the duty cycle is 1%. The current increment is tiny and the balance time is long. In Fig. 21(e) and (f), the duty cycle is 2%. Compared to

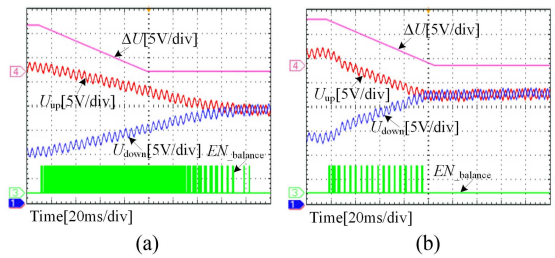


Fig. 22. Effect of the shoot-through time. (a) 1% duty cycle. (b) 2% duty cycle.

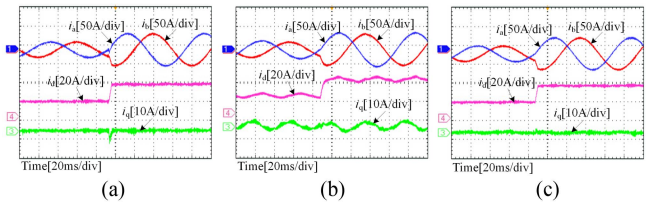


Fig. 23. Effect of the current controller. (a) Traditional PI controller. (b) High-order decoupling controller. (c) Multiconstrained complex coefficient controller.

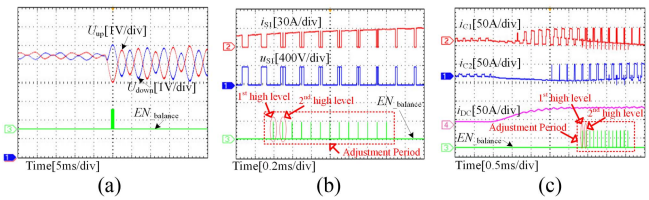


Fig. 24. Experimental results in the dynamic load condition. (a) Change of $U_{\rm up}$ and $U_{\rm down}$. (b) Current and voltage of switch S_1. (c) Effect of shoot-through mode.

Fig. 21(c) and (d), the current increases slightly and the balance time can be shortened. In Fig. 21(b), (d), and (f), the change of $i_{\rm L1}$ and $i_{\rm L2}$ will not affect $i_{\rm L3}$.

It can be seen that changing shoot-through time would lead to a high current increment and is not controllable. So fixed shoot-through time is necessary. Fig. 22 shows the effect of the shoot-through time with a fixed frequency of 10 kHz. Compared to Fig. 21, the initial voltage difference is higher and the change of ΔU is faster. In Fig. 22(a), the duty cycle is 1%. After ΔU stabilizes, the balancing process is not over yet. In Fig. 22(b), the duty cycle is 2%. balancing speed can follow the change of ΔU.

Fig. 23 shows the effect of the current controller. The inverter power jumps from half load to full load. For clearer comparison, the jump time of the active power is set to the reverse zero crossing point of $i_{\rm a}$. In Fig. 23(a), the traditional PI controller is applied, and there is a clear coupling between the current $i_{\rm d}$ and $i_{\rm d}$. Fig. 23(b) employs a higher order controller as described in (26), but without pole compensation. Although the controller can achieve current decoupling, it will cause low-frequency oscillation of the current. The proposed multiconstrained complex coefficient controller is applied in Fig. 23(c). The current $i_{\rm d}$ and $i_{\rm d}$ can basically achieve decoupling.

Fig. 24 shows the experimental results in the dynamic load condition. The load has a sudden change form 2.5 kW to 18 kW. In Fig. 24(a), after the load changes, $EN_{\rm \_balance}$ has a short adjustment period. $U_{\rm up}$ and $U_{\rm down}$ are still able to maintain balance. Fig. 24(b) shows the current and voltage of switch S_1 (as shown in Fig. 5) during the adjustment period. In order to observe the effect of instantaneous shoot-through more clearly, the switching frequency of *sw* is reduced to 5 kHz. Shoot-through occurs when $EN_{\rm \_balance}$ is high level. During the first high level, S_1 is ON, regardless of whether the balancing strategy is added or not. During the second high level, S_1 should be OFF without the balancing strategy, but $EN_{\rm \_balance}$ forces S_1 to turn ON. The effect of shoot-through mode can be seen in Fig. 24(c). The waveforms from top to bottom, respectively, is the charge current of C_1 and C_2, the dc source current and $EN_{\rm \_balance}$. During the first high level, C_1 is already discharging. The discharge caused by through is not obvious. During the second high level, C_1 is originally charging. It switches to discharging in the shoot-through mode, and continues charging after $EN_{\rm \_balance}$ reduces to low level.

VI. Conclusion

The proposed topology construction regulation can convert any of the existing two-level or multilevel bridge-type topologies into a more reliable topology without shoot-through problem. The PBG method is applied to establish the inverter model. Based on this, a multiconstrained complex coefficient controller is designed. The main advantages of the proposed inverter are as follows.

1) *Topological Advantages:* Dead time is not necessary so there are no dead-time effects. The output current harmonics are small and the ac filter specifications can be reduced. The shoot-through modes are able to help achieve the balance of dc capacitors.
2) *Modeling Advantages:* SDJ is suitable for continuous and discrete control signals. With SDJ, the circuit with power semiconductor devices can be modeled easily using the PBG method. It can expand the application of PBG in power electronics.
3) *Control Advantages:* With a more accurate inverter model, the designed current loop controller is capable of achieving expected results, such as effective bandwidth and phase margin. The introduction of imaginary terms can improve the dynamic performance of inverters.

References

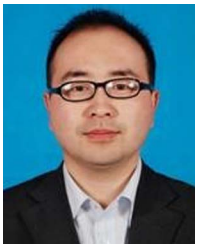
[1] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open J. Power Electron.*, vol. 2, pp. 155–170, Mar. 2021.
[2] A. K. Singh and R. K. Mandal, "A new switched capacitor based multilevel inverter with fewer capacitors," *Int. J. Electron.*, vol. 110, no. 8, pp. 1393–1407, Aug. 2022.
[3] J. Ning, H. Ben, J. Li, X. Wang, and T. Meng, "A small-sized high-precision digital closed-loop modulation method for dead-time compensation for flying capacitor three-level inverters," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 3968–3973, Apr. 2024.
[4] J. Ning, H. Ben, M. Li, T. Meng, and X. Wang, "High-frequency inverter advanced digital modulation strategy and implementation method considering dead time and switching transient effect," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1921–1933, Apr. 2024.

[5] J.-H. Lee and S.-K. Sul, "Inverter nonlinearity compensation through deadtime effect estimation," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10684–10694, Sep. 2021.
[6] A. Sheianov, X. Xiao, and X. Sun, "Adaptive dead-time compensation for high-frequency three-level sparse NPC inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 5169–5182, Oct. 2023.
[7] J. Ye et al., "An accurate dead time compensation method for SPWM voltage source inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4894–4908, Apr. 2023.
[8] M. Bierhoff, R. Soliman, and J. R. Espinoza C, "Analysis and design of grid-tied inverter with LCL filter," *IEEE Open J. Power Electron.*, vol. 1, pp. 161–169, May 2020.
[9] G. Majić, M. Despalatović, and K. Verunica, "Influence of dead time on voltage harmonic spectrum of grid-connected PWM-VSC with LCL filter," in *Proc. 10th Int. Conf. Compat., Power Electron. Power Eng.*, Bydgoszcz, Poland, 2016, pp. 228–233.
[10] Y.-J. Kim and H. Kim, "Optimal inductance ratio of LCL filter for grid connected inverters considering with low order harmonics," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Florence, Italy, 2016, pp. 2355–2360.
[11] X. Ding, Y. Hao, K. Li, H. Li, Z. Wei, and W. Wu, "Extensible Z-source inverter architecture: Modular construction and analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1742–1763, Feb. 2021.
[12] M. F. Elmorshedy, I. J. A. Essawy, E. M. Rashad, M. R. Islam, and S. M. Dabour, "A grid-connected PV system based on quasi-Z-source inverter with maximum power extraction," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6445–6456, Sep./Oct. 2023.
[13] N. Subhani, R. Kannan, A. Mahmud, and F. Blaabjerg, "Z-source inverter topologies with switched Z-impedance networks: A review," *IET Power Electron.*, vol. 14, no. 4, pp. 727–750, Mar. 2021, doi: 10.1049/pel2.12064.
[14] P. Manoj, A. Kirubakaran, and V. T. Somasekhar, "A quasi-switched capacitor based grid-connected PV inverter with minimum leakage current," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5969–5978, Dec. 2023.
[15] A. Nikbahar and M. Monfared, "A Family of high step-up magnetically coupled impedance source inverters with clamped DC-link voltage and low shoot-through current," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 107–111, Jan. 2023.
[16] W. Liang, Y. Liu, Y. Shen, and J. Yin, "An improved amplitude-domain PWM technique with minimum inductor current ripple for three-phase quasi-Z source inverter," *IEEE Trans. Ind. Appl.*, vol. 60, no. 2, pp. 2991–3005, Mar./Apr. 2024.
[17] D. Nanda, K. Mukherjee, and P. Syam, "A simplified control technique for a Z-source PWM rectifier," in *Proc. IEEE Region 10 Symp.*, Mumbai, India, 2022, pp. 1–6.
[18] K. Xu, S. Xie, X. Wang, B. Zhang, and S. Bian, "A combinational power circuit-based submodule topology for MMC with shoot-through and selfbalancing capability," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, Shenzhen, China, 2018, pp. 1–5.
[19] J. Salmon, A. M. Knight, and J. Ewanchuk, "Single-phase multilevel PWM inverter topologies using coupled inductors," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1259–1266, May 2009.
[20] X. Zheng, L. Zhang, X. Liu, Y. He, J. Shi, and C. Wang, "Half-cycle control method of the bidirectional three-phase dual-buck inverter without zero-crossing distortion," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 2088–2097, Apr. 2021.
[21] Z. Yao, "Review of dual-buck-type single-phase grid-connected inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4533–4545, Aug. 2021.
[22] Z. Yao and Y. Zhang, "A doubly grounded transformerless PV grid-connected inverter without shoot-through problem," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6905–6916, Aug. 2021.
[23] M. H. Mahlooji, H. R. Mohammadi, and M. Rahimi, "A review on modeling and control of grid-connected photovoltaic inverters with LCL filter," *Renewable Sustain. Energy Rev.*, vol. 81, no. 1, pp. 563–578, Jan. 2018.
[24] J. Yuan, Y. Yang, P. Liu, and F. Blaabjerg, "Model predictive control of an embedded enhanced-boost Z-source inverter," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, Padua, Italy, 2018, pp. 1–6.
[25] R. Reddivari and D. Jena, "A detailed model of Z-source converter considering parasitic parameters," in *Proc. Int. Conf. Power, Instrum., Control Comput.*, Thrissur, India, 2018, pp. 1–6.
[26] J. Yu, S. Wang, Z. Liu, J. Li, J. Liu, and J. Shang, "Accurate small-signal terminal characteristic model and SISO stability analysis approach for parallel grid-forming inverters in islanded microgrids," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6597–6612, May 2023.
[27] A. Zaidi and Z. B. Ismail, "Bond graphs and Bayesian networks based fault diagnosis: Application to a photovoltaic power supply," in *Proc. IEEE Int. Conf. Artif. Intell. Green Energy*, Sousse, Tunisia, 2023, pp. 1–6.
[28] R. K. Mahapatra, L. Umanand, and K. Gopakumar, "Flux-rate controlled harmonic filtering of an integrated magnetics-based isolated single-phase inverter topology," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6300–6311, Sep./Oct. 2023.
[29] A. C. Umarikar and L. Umanand, "Modelling of switching systems in bond graphs using the concept of switched power junctions," *J. Franklin Inst.*, vol. 342, no. 2, pp. 131–147, Mar. 2005.
[30] P. Ghimire, M. Zadeh, E. Pedersen, and J. Thorstensen, "Dynamic modeling, simulation, and testing of a Marine DC Hybrid Power System," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 2, pp. 905–919, Jun. 2021.
[31] F. Z. Peng, L. M. Tolbert, and F. Khan, "Power electronics' circuit topology - the basic switching cells," in *Proc IEEE Workshop Power Electron. Educ.*, Recife, Brazil, 2005, pp. 52–57.
[32] J. Dai, Y. Shen, and Z. Zhao, "Modeling and Matlab simulation of the inverter based on bond graph," in *Proc. IEEE 16th Conf. Ind. Electron. Appl.*, Chengdu, China, 2021, pp. 588–593.
[33] A. Q. Huang, "Power semiconductor devices for smart grid and renewable energy systems," in *Power Electronics in Renewable Energy Systems and Smart Grid: Technology and Applications*, 1st ed. Hoboken, NJ, USA, Wiley, 2019, ch. 2, pp. 85–152.
[34] W. Zhang, Y. Wang, P. Xu, D. Li, and B. Liu, "DC-bus voltage balancing control for 3-level DC/DC converters in renewable generation systems," *Energy Reps*, vol. 9, no. 10, pp. 210–217, Oct. 2023, doi: 10.1016/j.egyr.2023.05.174.
[35] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 711–718, Jul. 2000.
[36] A. Bıçak and A. Gelen, "Comparisons of different PWM methods with level-shifted carrier techniques for three-phase three-level T-type inverter," in *Proc. 7th Int. Conf. Electr. Electron. Eng.*, Antalya, Turkey, 2020, pp. 28–32.
[37] Y. Elthokaby, I. Abdelsalam, N. Abdel-Rahim, and I. Mohamed, "Simplified three-phase split-source inverter for PV system application controlled via model-predictive control," *Int. J. Circuit Theory Appl.*, vol. 52, no. 5, pp. 2266–2289, May 2024.
[38] J. Shi, J. Shen, Q. Chen, S. Schröder, H. Stagge, and R. W. De Doncker, "Performance evaluation of current control strategies in LCL-filtered high-power converters with low pulse ratios," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, 2014, pp. 3234–3242.

Xinxin Zheng received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2009 and 2015, respectively.

She is currently with the Automotive and Transportation Engineering, Hefei University of Technology, Hefei, China.

Jingwen Hu received the B.S. degree in vehicle engineering from the Taiyuan University of Technology, Taiyuan, China, in 2023. She is currently working toward the M.S. degree in vehicle engineering with the Hefei University of Technology, Hefei, China.



Xintian Liu (Fellow, IEEE) received the Ph.D. degree in automation from the University of Science and Technology of China, Hefei, China, in 2011.

He is the Chief Lecturer for an International Cooperation Project in Anhui Province on power lithium battery lifecycle management system. From 2010 to 2012, he was a General Manager and Chief Engineer of Anhui LIGOO New Energy Technology Company Ltd. He is currently an Associate Professor with the Automotive and Transportation Engineering, Hefei University of Technology, Hefei, China.

Yao He received the B.Sc. and Ph.D. degrees in automation from the University of Science and Technology of China, Hefei, China, in 2007 and 2012, respectively.

He is currently an Associate Professor with the Automotive and Transportation Engineering, Hefei University of Technology, Hefei, China. His research interests include battery management system and battery equalization.

Dr. He was the recipient of the Anhui Science and Technology Award for his achievement on new energy automotive power lithium battery technology and key management systems.

Weihan Li received the Ph.D. degree in vehicle engineering from Hefei University of Technology, Hefei, China, in 2016.

He is currently a Researcher with the Department of Vehicle Engineering, Hefei University of Technology, Hefei, China. From 2012 to 2014, he was a joint Ph.D. student funded by the China Scholarship Council with the GATE Center for Electric Drive Transportation, Department of Electrical and Computer Engineering, University of Michigan, Dearborn, MI, USA, where he was involved in the modeling and design of wireless chargers for electric vehicles (EVs)/plug-in hybrid electric vehicles (PHEVs). His research interests include two areas: 1) New energy vehicle technology, including wireless power transfer, EV/PHEV systems, renewable energy, and 2) decision-making and control for intelligent and connected vehicles.

Yanan Zhou received the B.S. degree in automation from Anhui University of Technology, Maanshan, China, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Hefei University of Technology, Hefei, China, in 2012 and 2018, respectively.

He is currently an Assistant Research Fellow with the Automotive and Transportation Engineering, Hefei University of Technology. His research interests include predictive control and robust control of electrical motor drives.

Lin He (Member, IEEE) received the Ph.D. degree in automotive engineering from Tongji University, Shanghai, China, in 2010.

After that, he entered into the State Key Laboratory of Automotive Safety and Energy, Tsinghua University, Beijing, China, as an Assistant Research Fellow. There into, he does some research on advanced engine control technology for Toyota Motor Corporation with Sophia University, Tokyo, Japan, from 2010 to 2011. He is currently a Professor with Hefei University of Technology. His main research interests include system dynamics models and control for vehicles, electric motors, lithium-ion batteries, steering, and brakes.