Letters

QFT-Based Robust Tracking Control of Nonminimum Phase Boost DC–DC Converter with Sensor Noise Suppression

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***Abstract*—This work addresses the problem of fast and robust tracking of large output voltage set point changes and sensor noise suppression in nonminimum phase (NMP) boost type dc–dc (BTDCDC) converters under voltage mode control. The tracking and sensor noise problems become highly challenging in the presence of the converter model uncertainties, source voltage variations, and control bandwidth limitation due to NMP behavior. To tackle these challenges, in this letter, the frequency domain quantitative feedback theory (QFT) is adapted to systematically design a robust control system for NMP boost type converter. The benefits of the proposed QFT-based design are: first, additional flexibility to achieve the fast tracking of large variation in output voltage setpoint without overshoot in the presence of converter parameter uncertainty and desired robust stability margin; Second, low transient inductor current; third, inclusion of NMP dynamics in the controller loop-shaping design, which respects the bandwidth limitation; fourth, low output voltage deviation from the steady state for a sudden input voltage variation; and finally, suppression of high-frequency sensor noise. To validate the efficacy of the proposed robust control design, experiments are conducted on a BTDCDC converter prototype using only sensed output voltage as feedback. The experimental results obtained with the proposed design demonstrate superior tracking and regulation performance besides sensor noise suppression against the existing designs.**

***Index Terms*—DC–DC converter, nonminimum phase (NMP), quantitative feedback theory, sensor noise, setpoint tracking, voltage regulation.**

I. Introduction

THE design of traditional fixed-voltage power supplies, using the switched-mode dc–dc converters, is carried out to achieve a constant output voltage across a varying load. The applications often demand precise control of voltage levels across the load terminals. Boost type dc–dc (BTDCDC) converters [see Fig. 1] operating in continuous conduction mode (CCM) are in high demand for applications, such as powering RF and analog circuits [1], electric vehicle chargers [2], and LED drivers [3] due to their desirable features. However, the BTDCDC converter exhibits nonminimum phase (NMP) behavior that makes the control design complex, especially for regulating and fast tracking of its output voltage [4], [5]. The challenges include large inductor currents, stability issues during dynamic load and input voltage changes, slow output voltage tracking for large setpoint changes, and sensor noise [3], [4], [5], [6], [7], [8], [9], [10], [11], [12].

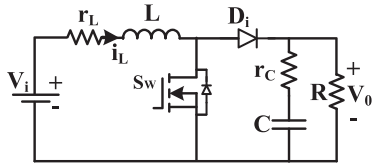

Fig. 1. BTDCDC converter circuit diagram.

Voltage mode control (VMC) is a popular and straightforward method for regulating the output voltage of the converters across the load. Unlike the current mode control [13], the VMC neither suffers from any duty cycle limitation nor does it require an inductor current sensor, making it easier to implement. However, VMC-based BTDCDC converters suffer from a sluggish response due to the latter's NMP characteristics. Further, the performance of the closed-loop controlled BTDCDC converter, is affected by model uncertainties, external disturbances and sensor noise [4], [12]. In the past, VMC has been used in conjunction with PID controller (PIDC), sliding mode controller (SMC) [4], [5], direct synthesis approach (DSA) [9], internal model controller (IMC) [10], and many others. PIDC is widely used in countless applications including the output voltage control of power electronic converters [9], [15], [16]. In fact, more than 90% of the industrial controllers are PID, due to their simplicity, clear functionality, applicability, and ease of use [14]. However, the conventional PIDC tuning does not take RHP zero into account and it results in either overdamped or sluggish response. The tuning of PIDC for a VMC-based BTDCDC converter with NMP behavior was attempted but used an additional phase sensitive device to get phase margin information [16]. When PIDC gains are not systematically tuned, the NMP behavior causes large initial undershoot of output voltage in case of

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large changes in output voltage set point and high sensor noise, thereby reducing the robustness of the system to disturbances and parametric uncertainty.

Majority of robust control techniques implemented under VMC for BTDCDC converters, such as the SMC, DSA, IMC, and scores of others, do not focus on large variations in output voltage set-point tracking and sensor noise issues. In general, limited literature is available that deals with large set-point tracking of the output voltage of an NMP BTDCDC converter [11], [12]. Anti-reset windup methods that focus on improved tracking response during large setpoint changes result in large peak inductor currents [11]. Other methods, like the active disturbance rejection control method involve complex controller design, which is computationally demanding and not so straight forward for naïve designers [12]. The crux is that none of the aforementioned methods effectively addresses sensor noise suppression or reduction in inductor current during large set-point changes. Thus, there is a need for a controller that has transparent tuning and involves easy hardware implementation with only one voltage sensor.

QFT-based robust control technique appears to be a good option due to its simplicity, and transparent design procedure. In addition, the combination of controller with prefilter leads to two degrees of freedom (2-DOF), which gives tremendous tuning flexibility to achieve both accurate tracking and regulation of the output voltage with suppression of sensor noise. In the past, QFT-based PID has been applied to regulate the output voltage of an NMP BTDCDC converter under VMC [17]. However, this design cannot handle both accurate tracking of large output voltage set point changes, and sensor noise suppression.

As the first such instance, to the best of the authors' knowledge, this letter addresses all the aforementioned challenges with simple and systematic selection of PID gains for an NMP BTDCDC converter using QFT approach. During tracking of large setpoint changes, the proposed QFT design does not exhibit overshoot or undershoot in the output voltage, and results in low peak inductor current compared to the existing PID designs [13]. The proposed QFT design exhibits significantly reduced sensor noise amplification on the output voltage.

II. QFT Approach to Robust Control Design

QFT is a frequency domain-based robust design approach that takes into account significant model uncertainties and disturbances [18]. QFT controller, $C(s)$, is designed to achieve improved disturbance rejection with stable closed-loop operation that corresponds to a first DOF structure. Further, a prefilter $(F(s))$ is added to satisfy the robust tracking specifications, that corresponds to a second DOF. The combination of the controller and the prefilter result in a 2-DOF control structure, as shown in Fig. 2. QFT offers a lucid loop-shaping approach to design the controller to make sure that the required specifications are met for the desired frequency set. The QFT bounds put constraints on the nominal loop transmission function $[L_0(s) = C(s)G_0(s)]$ by converting the tracking and disturbance rejection specifications. This is done by means of positioning L_0 on or above the performance (tracking and disturbance rejection) bounds and

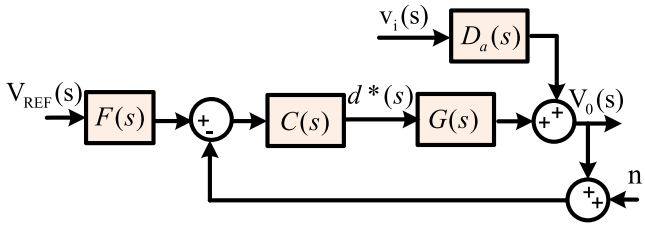

Fig. 2 2-DOF VMC structure for BTDCDC converter with sensor noise.

outside the stability bounds at the respective design frequencies. This completes the design of QFT controller. The design of the prefilter is carried out such that the tracking response of the closed-loop uncertain system lies within the desired tracking limits. The designer has the flexibility to choose the controller and prefilter structure a priori, which meets the specifications. The aim is to design a robust controller and a prefilter to simultaneously meet the following desired specifications.

1) *Robust Tracking Specifications:* The closed-loop tracking response of the uncertain system must lie in between the lower and upper tracking limits (T_L and T_U) as follows:

$$T_L(\omega) \le |F(j\omega)\,T(j\omega)| \le T_U(\omega) \tag{1}$$

where the complementary sensitivity function is given as $|T(j\omega)| = \left|\frac{G(j\omega)C(j\omega)}{1+G(j\omega)C(j\omega)}\right|$.

2) *Robust Disturbance Rejection:* The regulatory response of the uncertain system in the presence of the disturbance must satisfy the following inequality:

$$|S(j\omega)| = \left|\frac{1}{1+G(j\omega)\,C(j\omega)}\right| \le W_d(\omega) \tag{2}$$

where $W_d(\omega)$ denotes the disturbance rejection specification and the magnitude of sensitivity function is denoted by $S(j\omega)$.

3) *Robust Stability Margin:* The robust stability of the closed-loop system is ensured by satisfying the following inequality:

$$\left|\frac{G(j\omega)\,C(j\omega)}{1+G(j\omega)\,C(j\omega)}\right| \le W_s. \tag{3}$$

This inequality depicts the constant M-circle magnitude (W_s), which corresponds to the desired gain and phase margin specs.

III. Application of QFT-Based Robust 2-DOF Design for an NMP Boost Type DC–DC Converter

The nominal values of the converter, operating in CCM mode, are chosen as input voltage (V_i) = 15 V, output voltage (V_0) = 25 V, duty ratio (D) = 0.4, switching frequency (f_{sw}) = 20 kHz, inductor (L) = 3.3 mH, inductor ESR (r_L) = 0.2 Ω, capacitor (C) = 2200 μF, capacitor ESR (r_c) = 0.1 Ω, and load resistance (R) is 50 Ω. The nominal transfer function is as follows [13]:

$$G_0(s) = \frac{39.02 \times \left(-1.87511 \times 10^{-4}s + 1\right) \times \left(2.2002 \times 10^{-4}s + 1\right)}{\left(1.97784 \times 10^{-5}s^2 + 2.7353 \times 10^{-3}s + 1\right)}. \tag{4}$$

Equation (4) shows that the transfer function has a RHP zero. The uncertain BTDCDC converter transfer function is generated by taking 10% parametric uncertainty around the nominal values resulting in

$$G(s)=\frac{[35.12,42.92]\left([-1.68,-2.06]\times10^{-4}s+1\right)\times\left([1.98,2.42]\times10^{-4}s+1\right)}{[1.78,2.17]\times10^{-5}s^2+[2.46,3.00]\times10^{-3}s+1}. \tag{5}$$

The design frequency set (Ω) is chosen as half of the switching frequency (10 kHz), where the switching frequency is 20 kHz. The selected Ω is [1, 2.5, 7.5, 10, 20, 30, 60, 100, 200, 223, 500, 1000, 5000, 10000, 20000, 50000, 65000] rad/s.

The desired requirements of the converter operating in closed-loop (VMC) under 2-DOF control structure are as follows.

A. Robust Output Voltage Setpoint Tracking

The output voltage response of the converter in closed-loop, during setpoint changes, should lie between the desired upper and lower output voltage tracking limits as per (1). The desired tracking limits are specified in the time domain specifications as: 7 ≤ rise time ≤150 ms, over shoot ≤ 15%, and 43 ≤ settling time ≤ 65 ms. Using (1), the corresponding tracking limits are as follows [17]:

$$T_L(\omega)=\frac{0.99}{\left(\frac{(j\omega)^2}{2500}+\frac{2(j\omega)}{50}+1\right)};$$

$$T_U(\omega)=\frac{1.01\left(\frac{j\omega}{100}+1\right)}{\left(\frac{(j\omega)^2}{24414.06}+\frac{1.6(j\omega)}{156.25}+1\right)};\omega\le30\ \text{rad/s}. \tag{6}$$

B. Input Voltage Disturbance Rejection

The sudden change in input voltage causes the output voltage to deviate from its steady state value. The controller is designed such that the output voltage quickly reaches the steady state value in response to input voltage variations. The desired requirement for the input voltage variation (2) with input voltage disturbance dynamics [8], under closed-loop, is chosen as

$$\left|\frac{D_a(j\omega)}{1+C(j\omega)G(j\omega)}\right|\le W_d(\omega)=\left|\frac{s}{s+50}\right|_{s=j\omega};\ \omega\le30\ \text{rad/s}. \tag{7}$$

Here, $D_a(s)=\frac{v_0(s)}{v_i(s)}=\frac{1.63(2.20\times10^{-4}s+1)}{1.97\times10^{-5}s^2+2.73\times10^{-3}s+1}$.

In time domain, the disturbance specification W_d [18] corresponds to $\Delta v_0(t)<0.2$ V with a recovery time of at least 32 ms, once the input voltage disturbance occurs.

C. Robust Stability Margin

The relative stability measures, such as 5 dB gain margin and 60° phase margin, are considered and its equivalent M-circle magnitude (W_s) is 1.2 as per (3).

To achieve the above specifications, the QFT-based 2-DOF design is outlined below:

QFT controller design: The loop-shaping is carried out such that the controller provides high gain at low frequency (improved voltage regulation) and low gain at high frequency (enhanced noise filtering) [18]. This ensures quick recovery of output voltage to the desired value, despite source voltage variations under stable closed-loop converter operation. Also, the effect of high frequency measurement noise is suppressed on the output voltage. For NMP BTDCDC converter, the bandwidth limitation is considered while loop-shaping the controller. Failing to satisfy this limitation may lead to controller overdesign problem [18]. The PID controller parameters can be selected by the designer manually based on the following systematic steps while performing loop-shaping.

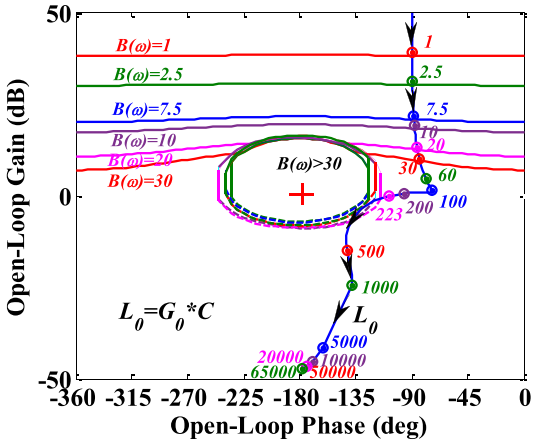

Fig. 3. Loop-shaping of QFT-PID controller.

Step-1: Add the controller gain parameter, *K* with the plant, $G_0(s)$ such that the loop gain ($L_0(s)=KG_0(s)$), increases upto $\omega=30$ rad/s for the performance bounds denoted by $B(\omega)$.

Step-2: Add the integrator (pole at origin) with L_0 brings phase lag of 90° to the loop.

Step-3: Add the two zeros at ω_1 and ω_2 and one pole at ω_3 (for sensor noise suppression) to ensure that the position of L_0 lies on or above the performance (tracking and disturbance rejection) bounds and outside the stability bounds ($B(\omega)>30$) at the respective design frequencies.

The resulting PID controller using QFT design is [see Fig. 3]

$$C(s)=\frac{2.6\left(\frac{s}{250}+1\right)\left(\frac{s}{270}+1\right)}{s\left(\frac{s}{2000}+1\right)}. \tag{8}$$

The obtained gain crossover frequency is around 255 rad/sec. This completes the 1st DOF design in QFT. It is followed by the second DOF that corresponds to the design of prefilter as follows.

QFT prefilter design: Robust prefilter is shaped such that closed-loop tracking response of the converter lies between the desired tracking limits as per (6). This is carried out by integrating the complementary sensitivity functions (minimum and maximum of $T(s)$) with a prefilter to satisfy the desired tracking limits as shown in Fig. 4. The designed prefilter is

$$F(s)=\frac{70}{s+70}=\frac{1}{\left(\frac{s}{70}\right)+1}. \tag{9}$$

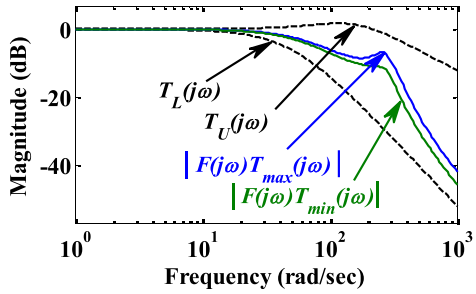

Fig. 4. Prefilter shaping for NMP BTDCDC converter.

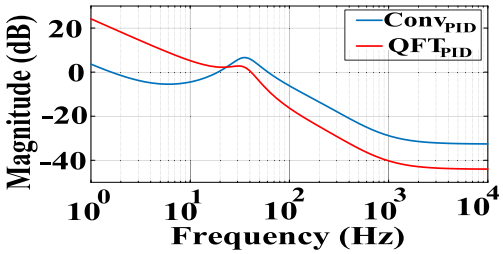

Fig. 5. Loop transfer function (L_0) comparison plot.

To conclude, (8) and (9) constitute the QFT-based robust 2-DOF design. Here onward, the QFT controller *C(s)* and the prefilter *F(s)* are denoted as QFT_{PID} and PF, respectively.

To facilitate a fair comparison, a conventional PID controller described in [13] is selected [10], [17]. The uncompensated NMP BTDCDC converter system, as in (4), demonstrates a phase margin of 8° at a gain crossover frequency of 1500 rad/s. The parameters of the conventional PID controller are chosen to achieve a phase margin of 60° and a gain crossover frequency of 240 rad/s. The conventional PID (Conv_{PID}) parameters are $K_p = 0.0132$, $K_i = 0.235$, $K_d = 1.37 \times 10^{-4}$, $\text{T}_\text{f} = 0.5 \times 10^{-3}$.

In comparison to Conv_{PID}, the gain magnitude of L_0 with the proposed QFT-PID is low at high frequency as shown in Fig. 5. As a consequence, it is expected that the sensor noise is least amplified (better suppressed) with the proposed QFT-PID.

Remark: The loop-shaping has been carried out in such a way that QFT-based PID offers low gain at high frequency to achieve sensor noise suppression. As a result, the proposed work provides accurate and large set-point tracking of output voltage and enhanced sensor noise suppression, as compared to [17], the proposed 2-DOF QFT design offers both accurate and large set-point tracking of output voltage with reduced transient inductor current and enhanced sensor noise suppression.

IV. Experimental Verification

The effectiveness of the proposed QFT 2-DOF design (denoted as QFT_{PID} + PF) discussed in Section III is validated on a hardware prototype as shown in Fig. 6. It consists of a IRFP250N MOSFET, MUR1560 diode, and A3120 gate driver circuit along with a TMS320F28069M DSP controller board.

The following tracking, disturbance rejection and sensor noise suppression scenarios are considered to demonstrate that the proposed QFT design ensures the output voltage lies within the

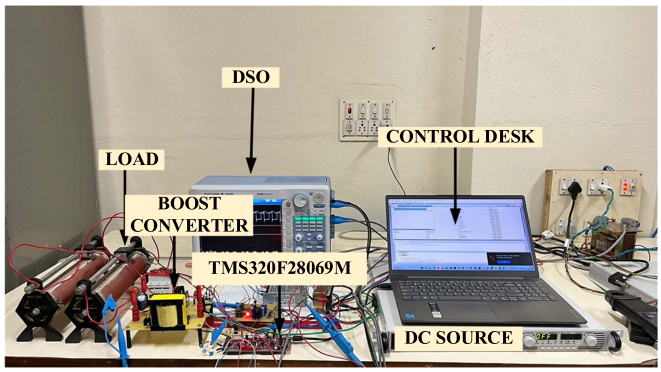

Fig. 6. Laboratory prototype of the experimental setup.

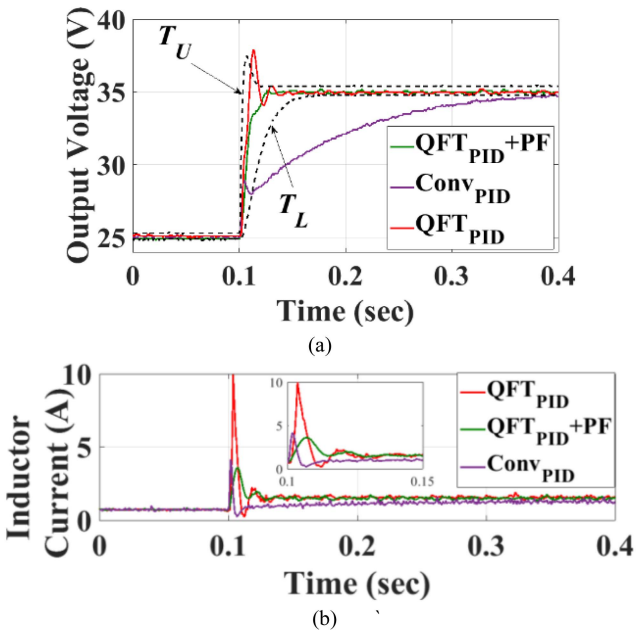

Fig. 7. Tracking performance comparison for output voltage set point change from 25 to 35 V: (a) Output voltage; (b) inductor current.

Tracking scenario: In this case, the tracking of large change in the output voltage setpoint from 25 to 35 V is considered. It is observed here that both 1-DOF designs (QFT_{PID} and Conv_{PID}) violate the desired tracking limits. To remove the overshoot and ensure that the output voltage response lies with in the desirable tracking limits, QFT-based prefilter is added to QFT 1-DOF PID design. The output voltage response in closed-loop with proposed 2-DOF design tracks the large setpoint output voltage satisfactorily without any overshoot and also lies in between the desired tracking limits as shown in Fig. 7(a). With the incorporation of a prefilter in the proposed QFT 2-DOF design, the inductor draws very low current during the large setpoint change [zoomed portion in Fig. 7(b)] as against QFT 1-DOF PID design as shown in Fig. 7(b).

Tracking and disturbance rejection scenario: In this scenario, both the tracking and regulatory performances are validated with the proposed 2-DOF design for tracking of a large setpoint change from 25 to 35 V and source voltage variation from 15 to 18 V at the new operating setpoint voltage of 35 V. The

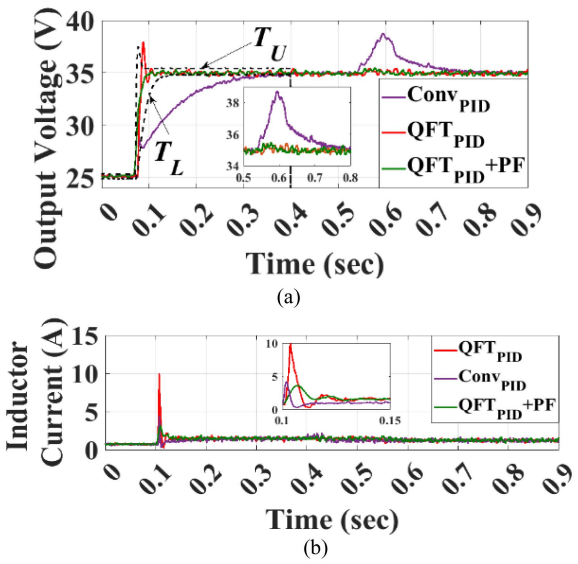

Fig. 8. Tracking and regulatory responses for input voltage change (15–18 V) at a output voltage set-point of 35 V. (a) Output voltage. (b) Inductor current.

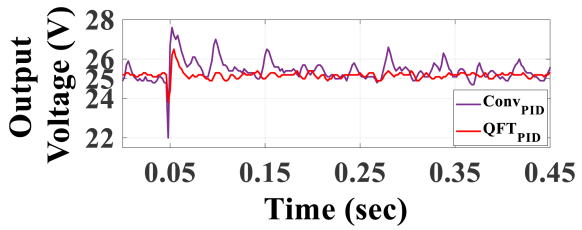

Fig. 9. Output voltage response with voltage sensor noise of Sin (2000πt).

output voltage response, unlike the QFT 1-DOF design, and quickly reaches the new setpoint that lies within the desired tracking limits as shown in Fig. 8(a). The peak value of the inductor current is greatly reduced with the proposed 2-DOF QFT design as against QFT 1-DOF PID design [zoomed portion in Fig. 8(b)] as shown in Fig. 8(b). With the new setpoint of 35 V, the input voltage is suddenly varied from 15 to 18 V. It is observed that both QFT designs allow quick recovery back to 35 V as compared to the conventional 1-DOF PID design [zoomed portion in Fig. 8(a)] as shown in Fig. 8(a).

Sensor noise scenario: In this scenario, the effect of sensor noise supperssion on the output volatge is investigated by injecting a high frequency sinusoidal signal of 1000 Hz externally with the voltgae sensor at t = 0.05 s. Referring to Fig. 5, the proposed QFT-PID design shows an insignificant amplification of the sensor noise on the output voltage [see Fig. 9].

The tracking of setpoint changes, at nominal and perturbed input voltages, with the proposed 2-DOF QFT design exhibits smooth transition to the new setpoint with reduced inductor current and without any overshoot as against 1-DOF designs. The proposed QFT PID design exhibits an insignificant deviation in the output voltage as against conventional 1-DOF PID design for sudden input voltage changes and sensor noise.

To highlight the superiority of the proposed 2-DOF QFT control strategy, a quantitative comparison with 1-DOF QFT [17] is made based on overshoot, settling time, noise suppression, number of voltage, and current sensors used in controller implementation. It is observed that the proposed QFT 2-DOF design exhibits no overshoot in the output voltage and significantly reduces the transient inductor current as compared to [17]. A quantitative comparison is provided between the proposed 2-DOF QFT design and QFT 1-DOF PID [17] in Table I.

TABLE I
QUANTITATIVE COMPARISON-TRACKING SCENARIO

Controller	Over shoot (V)	Settling time (ms)	Inductor Current (A) deviation	Sensor Noise Suppression Capability?	No. of Voltage and Current Sensors
PROPOSED 2-DOF QFT_{PID}	0	23	2.25	YES	1 and 0
1DOF QFT [17]	2.5	36	9	NO	1 and 0

V. CONCLUSION

This work is the first attempt to implement a QFT-based robust 2-DOF design scheme for the tracking, regulation and sensor noise supression of the output voltage of an uncertain NMP BTDCDC converter. From the experiments, it was observed that the output voltage response with the conventional 1-DOF PID design exhibit a sluggish response and fails to achieve the desired tracking specifications for large setpoint changes. Large deviations from the steady state value during sudden variations in the source voltage were also observed. The 1-DOF QFT_{PID} also results in large transient inductor current during large set point changes. With the inclusion of a QFT prefilter, the proposed QFT 2-DOF design could achieve reduced transient inductor current during fast tracking of large output voltage setpoint changes without overshoot. The proposed 2-DOF QFT_{PID} design effectively supresses the sensor noise influence on the output voltage. A smaller output voltage deviation for sudden source voltage variation was achieved along with robust stability. As the future work, it is proposed to focus on optimisation based automatic synthesis of robust 2-DOF design of power converters.

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