Overcurrent Protection Enabled by Broadband Rogowski Coil Current Sensor for Medium-Voltage SiC MOSFET

Jiakun Gong, Yulei Wang, Liang Wang, *Student Member, IEEE*, Mingrui Zou, Peng Sun, *Student Member, IEEE*, Yuxi Liang, Yiming Gong, Huayang Zheng, and Zheng Zeng, *Member, IEEE*

***Abstract*—To guarantee safe switching of the expensive medium-voltage (MV) device with limited durability, the overcurrent protection scheme based on Rogowski coil current sensor (RCCS) is the promising method, featuring fast response and galvanic isolation. However, it is an inherent contradiction to achieve the RCCS with both high noise immunity and high-bandwidth capabilities. In addition, the nonideal dc and low-frequency characteristics of the integrator cause drift and droop errors. In this article, to address the aforementioned challenges, the broadband RCCS is developed and integrated into the overcurrent protection circuit for the MV SiC MOSFET. The novel coil is designed based on the transmission line theory to overcome the constraints imposed by parasitic components on bandwidth. The proposed coil achieves an extra-high bandwidth of approximate 300 MHz with high mutual inductance and shielding layers for high noise immunity. Furthermore, the broadband integrator design method with low-frequency attenuation is proposed to eliminate drift and reduce droop errors significantly. Based on the developed RCCS, the proposed overcurrent protection circuit reacts to both the fault under load and hard switching fault rapidly and softly turns OFF the device within merely 200 ns. Comprehensive experiments demonstrate its exceptional potential in monitoring current and protecting the expensive MV devices.**

***Index Terms*—Drift and droop errors, high bandwidth, medium-voltage (MV) SiC MOSFET, overcurrent protection, Rogowski coil.**

I. Introduction

RECENTLY, the SiC MOSFET has gained significant interest in medium-voltage (MV) applications, thanks to the excellent characteristics of higher blocking voltage, faster switching speed, and better thermal performance compared with the Si insulated gate bipolar transistor (IGBT) [1]. The MV SiC MOSFET with blocking voltage above 3.3 kV has the potential to simplify topology configuration, reduce device number, and decrease switching loss, thereby enhancing the reliability, efficiency, and power density of the MV converter [2], [3], [4]. However, the short-circuit withstand capability of the SiC MOSFET is shorter than that of its Si counterpart, due to the smaller die area and faster current slew. The heat generated during the overcurrent under high voltage would lead to the significant rise in junction temperature, which causes metallization of the bare die, thus resulting in degradation and damage of the expensive MV SiC MOSFET chip [5]. Therefore, fast and reliable overcurrent protection is essential to make full use of the MV SiC MOSFET.

Numerous effective methods have been applied to overcurrent protection for the SiC MOSFET, mainly focusing on drain–source voltage, gate signal, and source current. Concerning the detection of the drain–source voltage, desaturation protection is commonly adopted by measuring the ON-state voltage of the device and evaluating the fault state [6], [7], [8]. Furthermore, faster response can be achieved by combining desaturation and *dv/dt* detection [9], [10]. Concerning the detection of gate signal, the overcurrent fault can be identified by monitoring the anomalies of gate voltage or current [11], [12], [13]. Concerning the detection of source current, integrated current sensors, such as shunt, current transformer, Kelvin inductance, or Rogowski coil current sensor (RCCS), are utilized to obtain the real current of the device, thus detecting the fault quickly and accurately [14], [15], [16], [17]. Previous research has proposed numerous beneficial methods for the overcurrent protection schemes of the SiC devices. With regard to the characteristics of MV SiC MOSFET, higher blocking voltage necessitates additional insulation design for the drain-voltage-based protection scheme, thus increasing the volume of the driver circuit. The detection methods based on the gate signal and source inductance are limited by the characteristics of the protected device, while the shunt and current transformer are not suitable for overcurrent detection in high-current applications. In contrast, the integrated RCCS is a promising method for the overcurrent protection due to its ultrafast response, galvanic isolation, and high-current testing capability.

However, there is a scarcity of integration methods for high-performance RCCS applied to MV SiC MOSFET. The main

Received 26 July 2024; revised 7 December 2024; accepted 29 December 2024. Date of publication 3 January 2025; date of current version 26 February 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52177169, in part by the Natural Science Foundation of Chongqing, China, under Grant CSTB2024NSCQ-JQX0016, and in part by the Graduate Research and Innovation Foundation of Chongqing, China, under Grant CYB240023. Recommended for publication by Associate Editor M. Nawaz. *(Corresponding authors: Yulei Wang; Zheng Zeng.)*

The authors are with the State Key Laboratory of Power Transmission Equipment Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China (e-mail: gonjiakun@cqu.edu.cn; yulei_wang@cqu.edu.cn; wangliangedu@cqu.edu.cn; zoumingrui@cqu.edu.cn; sunpeng_96@cqu.edu.cn; yuxiliang@cqu.edu.cn; 202211131200t@cqu.edu.cn; huayang_z@cqu.edu.cn; zengerzheng@cqu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3525298.

Digital Object Identifier 10.1109/TPEL.2024.3525298

challenges lie in addressing both the high-frequency and low-frequency characteristics of the RCCS. In terms of high frequency, the bandwidth of the coil is limited by its self-inductance and parallel capacitance [18], [19]. The shielding layers for high noise immunity can increase the inherent parasitic parameters of the Rogowski coil, thus decreasing the bandwidth [20], [21]. Moreover, high mutual inductance of the coil is required for the high electromagnetic interference (EMI) environment, which also results in insufficient bandwidth [22], [23]. It is an inherent contradiction to achieve the RCCS with both high noise immunity and high bandwidth. In terms of low frequency, the non-ideal dc and low-frequency characteristics of the RCCS cause severe drift and droop errors, leading to the measured current being severely distorted [24]. While the implementation of a reset switch can mitigate the accumulation of drift errors over multiple cycles, it does not eliminate the errors that occur during the conduction process of the device [22], [25]. The RCCS is a promising embedded current sensor capable of integration into devices and converters, offering both current monitoring and protection. However, the aforementioned challenges caused by insufficient high-frequency and low-frequency characteristics significantly constrain the widespread application of the RCCS.

Motivated by these challenges, the design methodology of integrated RCCS with high performance is proposed and applied for the overcurrent protection of the MV SiC MOSFET in this article. The novel Rogowski coil based on transmission line theory and enhanced integrator is designed to improve the high-frequency and low-frequency performance of the RCCS significantly. The broadband RCCS without drift errors is realized and integrated into the gate driver to monitor current and protect the high-cost MV SiC MOSFET.

The rest of this article is organized as follows. In Section II, the principles and challenges of integrated RCCS applied to overcurrent protection are illustrated. In Section III, considering the aforementioned limitations, the Rogowski coil based on the transmission line theory is designed to realize high bandwidth, and the enhanced integrator design method is proposed to improve the low-frequency characteristics of RCCS. In Section IV, the design of the isolated gate driver integrated with the proposed overcurrent protection circuit is introduced. Comprehensive experiments under different scenarios are presented to demonstrate the advantages of the proposed overcurrent protection scheme in Section V. Finally, Section VI concludes this article.

II. Principles and Limitations of Integrated RCCS in Overcurrent Protection for MV SiC MOSFET

A. Principle of PCB-Embedded RCCS With Broadband Integrator

The Rogowski coil is commonly utilized in current measurement for wide bandgap semiconductor devices [26], [27]. As shown in Fig. 1(a), the coil is composed of spiral-wound turns and an air core, which senses the magnetic field generated by the alternating current, producing a voltage signal proportional to the differential of the current based on Faraday's electromagnetic induction law [28]. The structure of the coil can be replaced by the printed circuit board (PCB) wingdings with fixed parameters, as shown in Fig. 1(b).

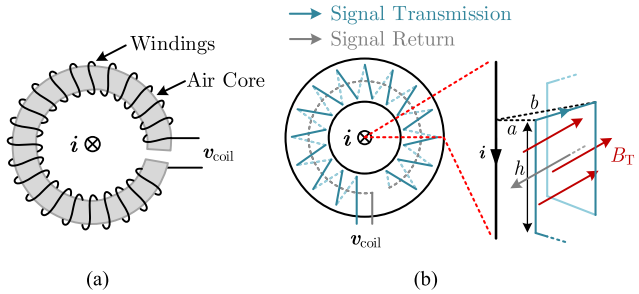

Fig. 1. Configuration of Rogowski coil. (a) Traditional coil. (b) Toroidal PCB coil and cross section of each winding turn.

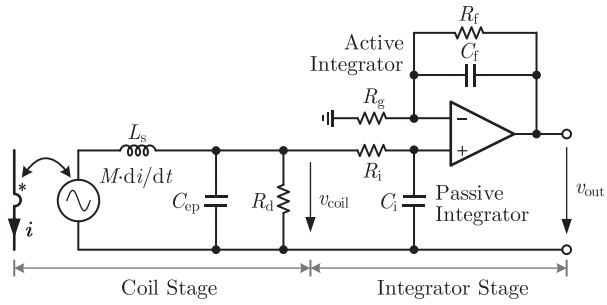

Fig. 2. Equivalent circuit model of RCCS with broadband integrator.

The relationship between the output voltage v_{coil} of a toroidal coil and the measured current i can be expressed as follows:

$$v_{coil} = -N\frac{d\phi}{dt} = -N\frac{\mu_0 h}{2\pi}\ln\frac{b}{a}\frac{di}{dt} = -M\frac{di}{dt} \tag{1}$$

where μ_0 is the permeability of vacuum. M, N, h, a, and b are the mutual inductance, turns, thickness, and internal and external diameters of the coil, respectively [29]. The output voltage of the coil is proportional to the di/dt, with the proportionality constant being the mutual inductance M. To improve the signal-to-noise ratio, the coil with high mutual inductance is preferred in the high EMI environment.

Then, the integrator processes the voltage signal to restore the original current. The equivalent circuit model of the RCCS is depicted in Fig. 2, which is composed of the coil stage and integrator stage. The equivalent circuit of the coil includes the self-inductance L_s and the equivalent parallel capacitance C_{ep}, which limits the bandwidth of the coil under the resonant frequency. Besides, the mutual inductance of the PCB-embedded coil with an air core is typically lower than the current transformer with an iron core [30]. Therefore, the active integrator is preferred to improve the overall gain of the RCCS while combined with a passive RC network to extend its high-frequency characteristics [31], [32]. To achieve smooth and broadband integral characteristics, the active and passive integrators are required to have identical corner frequencies, as shown in Fig. 3. The corner

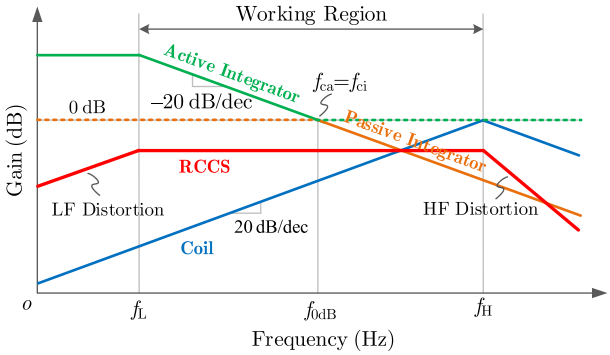

Fig. 3. Frequency characteristics of RCCS.

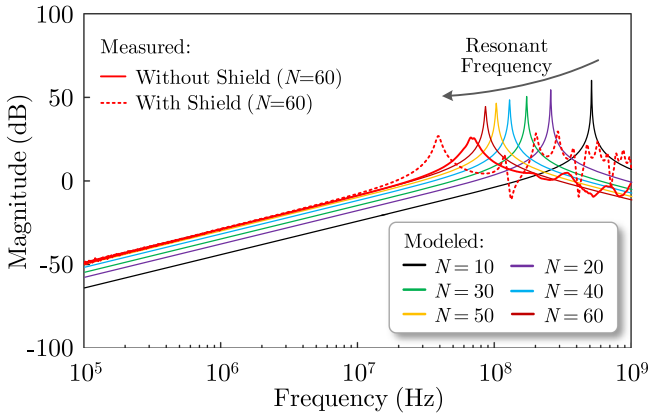

Fig. 4. Impact of number of turns and shielding layers on bandwidth.

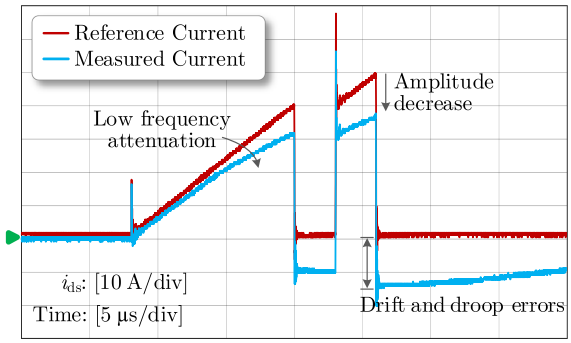

Fig. 5. Drift and droop errors of RCCS.

frequencies of the integrators can be written as

$$f_{\text{ca}} = \frac{1}{2\pi R_g C_f} = f_{\text{ci}} = \frac{1}{2\pi R_i C_i} = f_{0\text{dB}} \tag{2}$$

where f_{ca} and f_{ci} are the corner frequencies of the active and input passive integrators, respectively, and $f_{0\text{dB}}$ is the frequency where the gain of the integrator is 0 dB. Besides, the passive *RC* network is typically placed at the front end of the operational amplification (op-amp) to avoid overdrive of the op-amp under high *di/dt*. Since the gain of the op-amp is limited, the frequency characteristics of the integrator will be distorted in low frequency. The frequency characteristics of the RCCS are depicted in Fig. 3, and the output voltage of the RCCS in the constant gain region between f_L and f_H can be expressed as follows:

$$v_{\text{out}} = K\int v_{\text{coil}}dt = K\int\left(-M\cdot\frac{di}{dt}\right)dt = -MKi \tag{3}$$

$$K = 2\pi f_{0\text{dB}} = \frac{1}{R_g C_f} = \frac{1}{R_i C_i} \tag{4}$$

where *K* is the integral gain. According to (3), the output of the RCCS is proportional to the measured current. The gain of the current sensor can be adjusted by changing the integral gain *K*, thus applied to different current measurement scenarios.

B. Bandwidth Limitation of Integrated Rogowski Coil

The high-frequency characteristics of the coil are determined by the parasitic components. As the frequency gradually approaches the resonant frequency, the coil will no longer reflect the true current signal accurately. The output voltage of the coil can be expressed as follows:

$$v_{\text{coil}}(s) = -sM\cdot i\frac{\frac{1}{sC_{\text{ep}}}\parallel R_d}{sL_{\text{s}}+\frac{1}{sC_{\text{ep}}}\parallel R_d} = \frac{-sMR_d\cdot i}{s^2L_sC_{\text{ep}}R_d+sL_s+R_d} \tag{5}$$

where L_s and C_{ep} are the self-inductance and parallel capacitance of the coil, respectively. R_d is the load resistance of the coil [33].

The self-inductance and parallel capacitance can be written as follows:

$$L_s = N^2\frac{\mu_0 h}{2\pi}\ln\frac{b}{a} \tag{6}$$

$$C_{\text{ep}} = \frac{4\pi^2\varepsilon_0(b+a)}{\lg(b+a)-\lg(b-a)} \tag{7}$$

where ε_0 is the permittivity of vacuum.

The L_s and C_{ep} will lead to the resonance of the signal in the coil. The resonant frequency can be derived as follows:

$$f_R = \frac{1}{2\pi\sqrt{L_sC_{\text{ep}}}} = \frac{1}{2\pi N\sqrt{2\pi h\mu_0\varepsilon_0(b+a)\ln\frac{b}{a}\frac{1}{\lg(b+a)-\lg(b-a)}}}. \tag{8}$$

To achieve high bandwidth for detecting transient current, low self-inductance and parallel capacitance of the coil are required, as indicated by (8). However, when the RCCS is integrated into the MV converter, high number of turns and shielding layers are necessary to enhance noise immunity [20]. This results in increased L_s and C_{ep}, significantly decreasing the bandwidth of the coil, as shown in Fig. 4. Therefore, achieving the RCCS with both high noise immunity and high bandwidth presents an inherent contradiction.

C. Drift and Droop Errors of RCCS

Since the RCCS is a type of probe utilized in measuring ac current, its nonideal dc and low-frequency characteristics will cause drift and droop errors, as shown in Fig. 5. The input dc bias

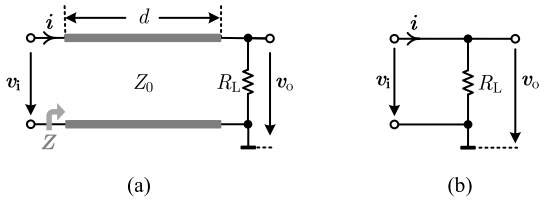

Fig. 6. Equivalent circuit model of transmission line with load. (a) Transmission line model. (b) Simplified model under condition of impedance matching.

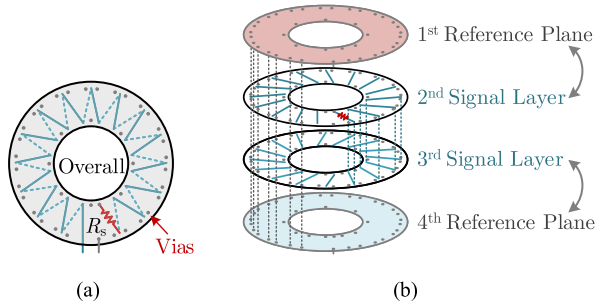

Fig. 7. Structure of transmission line Rogowski coil. (a) Vertical view. (b) Multilayer layout.

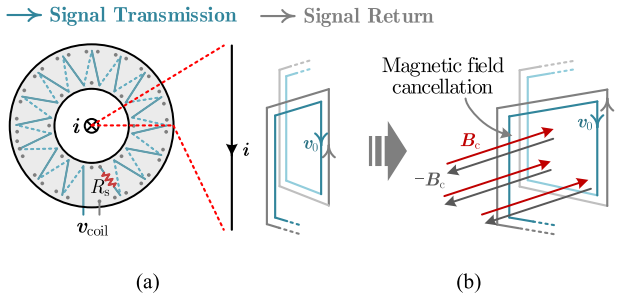

Fig. 8. Operating principle of transmission line *RC*. (a) Signal return path at high frequency. (b) Magnetic field cancelation due to mirror return effect.

will be amplified by the integrator, which may even lead to the saturation of the op-amp. The low-frequency distortion of RCCS results in the signal attenuation in this frequency band and the sag of the overall waveform. Therefore, it is necessary to improve the low-frequency characteristics of the RCCS to eliminate the drift and droop errors for the accurate current detection.

Although the RCCS has the advantages of low invasiveness and ease of integration, applying it to current monitoring and protection for MV SiC MOSFET still faces two major challenges.

1) *Challenge 1:* How to realize the RCCS with both high bandwidth and noise immunity for MV SiC MOSFET?
2) *Challenge 2:* How to improve the low-frequency characteristics to eliminate the drift and droop errors?

III. Performance Enhancement Methods for Integrated PCB RCCS

A. Design of High-Bandwidth Coil With High Noise Immunity Based on Transmission Line Theory

Due to the inherent equivalent self-inductance and parallel capacitance, the impedance of the coil changes with frequency. The high-frequency signal induced by transient switching current will experience distortion when transmitting through the coil. Designs to enhance noise immunity, such as increasing the number of turns and incorporating shielding layers, tend to exacerbate this issue. The Rogowski coil with transmission line structure was developed to pursue bandwidth exceeding gigahertz [34]. Nevertheless, the practicality of the previous design is limited due to low mutual inductance and the neglect of eddy current issues. However, the advantages of transmission line structure can be utilized to overcome the constraint between high bandwidth and high noise immunity, thus achieving a practical RCCS with high performance for the MV SiC MOSFET.

The equivalent circuit model of transmission line with load is shown in Fig. 6(a), and the input signal v_i is transmitted through the transmission line to the load side. The input impedance of the transmission line can be expressed as follows [35]:

$$\boldsymbol{Z} = Z_0 \frac{R_L + jZ_0 \tan(2\pi f d/v_p)}{Z_0 + jR_L \tan(2\pi f d/v_p)} \tag{9}$$

where f is the frequency of the input signals, d represents the length of the transmission line, and v_p is the phase velocity of the electromagnetic waves transmitting on the transmission line. From (9), it can be observed that when R_L equals Z_0, the effect of the entire transmission line with load is equivalent to that of a pure load, and v_o just equals v_i, as shown in Fig. 6(b), which means that the signal no longer distorts with frequency during transmission.

When the signal transmits through the Rogowski coil, the self-inductance and parallel capacitance of the coil cause signal distortion as the frequency increases, especially at the resonance point. To facilitate wideband signal transmission through the coil, reference planes are added for the signal windings, thereby forming the transmission line Rogowski coil, as shown in Fig. 7.

Since the return of signal follows the path with the lowest impedance, the high-frequency signal tends to return via the mirror path of the outgoing signal, as it creates the smallest loop area with the lowest inductance [36]. The reference planes provide return path for the signal, while the vias connecting the first layer and fourth layer are placed close to the vias of signal winding for the purpose of minimizing the return path, as described in Fig. 8(a). Under this condition, the magnetic field $-\boldsymbol{B}_c$ generated by the return signal is the exact opposite of $\boldsymbol{B}_c$ generated by $\boldsymbol{v}_0$, as shown in Fig. 8(b). The central magnetic field of the windings is canceled out, which means that the coil does not exhibit self-induction effect, and the transmission of $\boldsymbol{v}_0$ is no longer affected by L_s.

Moreover, the distributed mutual inductance between the signal routing and the reference plane L_0 still needs to be considered. Similarly, the distributed capacitance between the signal routing and the reference plane C_0 also needs to be taken into account, as explained in the distributed-element model in Fig. 9, where M_0 is the distributed mutual inductance between the circuit under test and the coil. v_0 is the distributed induced

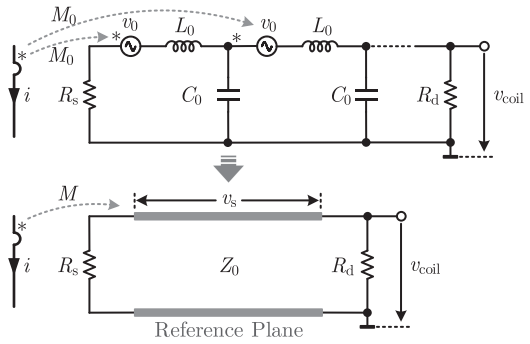

Fig. 9. Distributed-element model of the proposed transmission line Rogowski coil.

voltage in the winding. The characteristic impedance Z_0 of the winding can be written as follows:

$$Z_0 = \sqrt{L_0/C_0}. \tag{10}$$

Since the induced signal v_s is distributed linearly over the transmission line, the coil design needs to satisfy the requirement of double-ended impedance matching to avoid internal signal reflection. In the PCB-embedded Rogowski coil with the multilayer structure, the value of Z_0 is determined by the width of the trace, which can be accurately calculated by using the PCB transmission line field solver, Polar Si9000. The trace width is designed based on the practical considerations, such as coil size and number of turns. To achieve impedance matching, the value of R_s should be consistent with Z_0. However, the matching for R_d is more complex, as R_d is in parallel with the subsequent integrator circuit. Because of the high-impedance input characteristics of the op-amp, the input impedance of the integrator circuit is dominated by the RC network, as shown in Fig. 2. As frequency increases, the input impedance will decrease and eventually approach R_i.

Therefore, the input resistance R_i should be significantly higher than Z_0 to reduce the impact on the impedance matching. Wider trace for lower Z_0 is preferred to achieve better decoupling with the subsequent signal processing circuit. Even though the parasitic capacitance of R_i affects the impedance matching of R_d at frequencies up to hundreds of megahertz, R_d still maintains impedance matching with Z_0 over a broad frequency spectrum. And then, the requirements of double-end impedance matching can be briefly written as follows:

$$R_s = Z_0 = R_d. \tag{11}$$

When the source resistance R_s and load resistance R_d match the characteristic impedance Z_0, the induced voltage v_0 can be transmitted without loss and reflection in the signal winding. The L_0 and C_0 no longer hinder the signal transmission, but rather become essential conditions for the electromagnetic energy conversion, eliminating the constraint between bandwidth and coil parasitic components.

Since the bandwidth of the transmission line coil is decoupled from the self-inductance, increasing the number of turns does not result in bandwidth reduction.

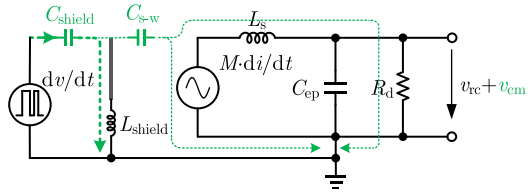

Fig. 10. Principle of shielding.

TABLE I
PARAMETERS OF THE PROPOSED COIL

Parameters	Value	Parameters	Value
a	8 mm	M	5.64 nH
b	12 mm	R_s	40 Ω
h	1.2 mm	R_d	40 Ω
N	60 turns	Z_0	40 Ω

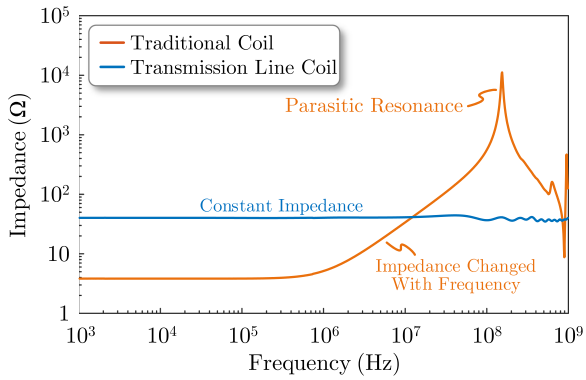

Fig. 11. Input impedance of traditional coil and transmission line coil.

Moreover, the reference planes and vias collectively offer coil the shielding capability, thereby enhancing the noise immunity, as depicted in Fig. 10. The shielding provides a low-impedance path for the common-mode current flowing through the parasitic capacitance between the coil and the circuit under test [21].

In the traditional structures, the insertion of a shielding layer typically introduces parallel capacitance, which subsequently decreases the bandwidth. In contrast, the parallel capacitance introduced is a part of C_0 in the transmission line structure, which is an essential condition to realize high bandwidth. In order to achieve high noise immunity, a 60-turn coil with mutual inductance of 5.64 nH and shielding layers is designed. The structural parameters of the coil are shown in Table I. The outer and inner diameters of the designed coil are 26 mm and 13 mm, respectively. The characteristic impedance of the coil is calibrated as 40 Ω and remains constant as the frequency increases, as shown in Fig. 11.

B. Solution to Eliminate the Impact of Eddy Current

The constant impedance of the coil ensures that the wideband signals can be transmitted without distortion. However, the issue of eddy currents induced by the high-frequency signals received little attention after the implementation of shielding approaches. With the rise of signal frequency, eddy current occurs and flows

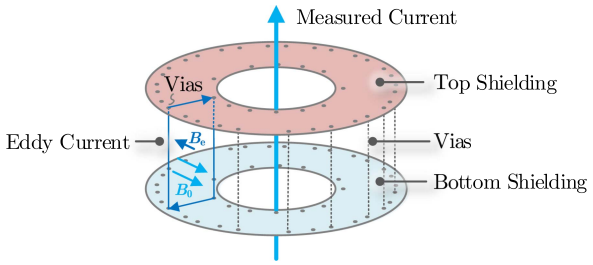

Fig. 12. Eddy current induced by shielding layers and vias.

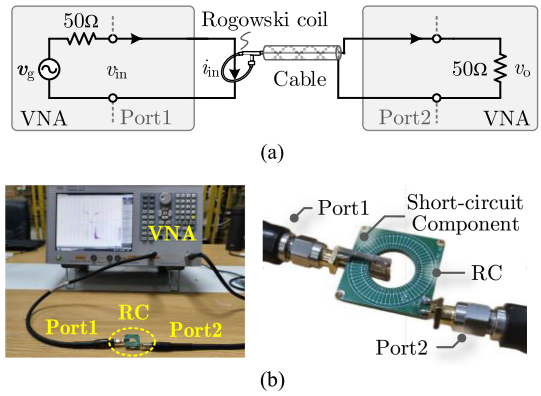

Fig. 13. Principle of calibrating bandwidth and gain of Rogowski coil. (a) Schematic diagram. (b) Test platform for calibration.

through the shielding layers and vias, ultimately impacting the original magnetic field, as shown in Fig. 12.

In order to assess the impact of eddy current, it is necessary to calibrate the frequency characteristics of the coil with a wideband variable-frequency current source. This can be implemented by paralleling the output of the vector network analyzer (VNA) E5061B with a low-inductance short-circuit component, transferring the voltage signal to current signal. The principle of this method is displayed in Fig. 13. The source resistance of the VNA is 50 Ω, which also means that the amplitude of the output current signal is 1/50 (–34 dB) of the original voltage amplitude when the output is short circuited. Then, the gain and bandwidth of the RCCS can be accessed by the VNA forward transmission coefficient S_{21}.

The frequency characteristic of the coil measured by the VNA is displayed in Fig. 14. Distortion occurs at mid-frequency while maintaining differential characteristics at low and high frequency, exhibiting a three-stage feature. To eliminate the effects caused by the eddy current, a method of compensation through the integrator is proposed, and the principle is shown in Fig. 15.

Since the corner frequencies f_1 and f_2 can be identified through the VNA, compensation for the coil characteristics can be achieved by adjusting the corner frequencies of the active and passive integrations, according to the identified f_1 and f_2. The corner frequencies can be written as follows:

$$f_1 = \frac{1}{2\pi R_g C_f}, \quad f_2 = \frac{1}{2\pi R_i C_i}. \tag{12}$$

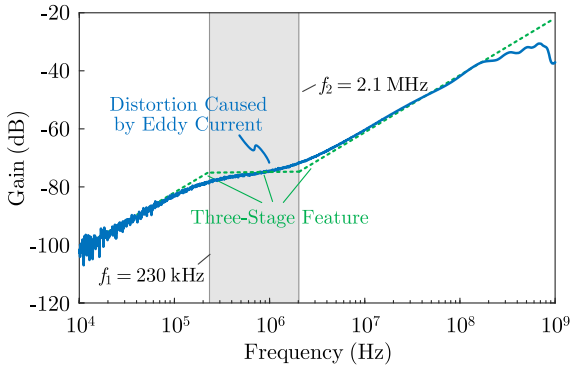

Fig. 14. Frequency characteristics (10 kHz–1 GHz) of the proposed transmission line coil.

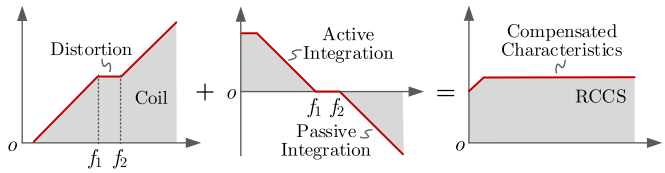

Fig. 15. Principle of compensating coil distortion by integrator.

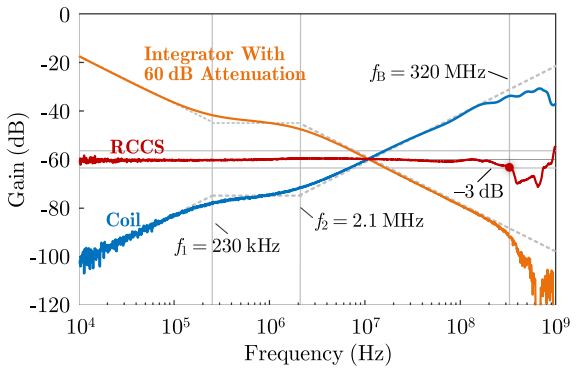

Fig. 16. Frequency characteristics (10 kHz–1 GHz) of the proposed RCCS after compensation.

In this method, the coil characteristics distortion due to the eddy current can be easily and perfectly compensated, and ultimately achieving ultra-high bandwidth of approximate 300 MHz (–3 dB), as shown in Fig. 16.

The parameter comparison between the previous RCCS and the proposed RCCS for integration applications is shown in Table II. Typically, the bandwidth is far lower than the resonant frequency of the coil. It can be found that the high mutual inductance and shielding layers significantly decrease the bandwidth of the coil. The proposed RCCS based on the transmission line theory features the highest bandwidth despite the addition of the shielding layers and the presence of high mutual inductance, which is even much higher than the state-of-the-art commercial product Mini-50HF from power electronic measurements (PEM). Benefiting from the characteristic of bandwidth being decoupled with parasitic components, the proposed structure demonstrates the potential to achieve higher mutual inductance

TABLE II
COMPARISON OF RCCS IN INTEGRATION APPLICATIONS

RCCS	Number of Turns	Mutual-Inductance	Shielding	Resonant Frequency	Bandwidth
[20]	60	1.71 nH	No	115.9 MHz	/
[21]	152	2.54 nH	Yes	42.8 MHz	/
[22]	152	2.54 nH	No	63.1 MHz	28.3 MHz
[24]	116	11.13 nH	No	13.8 MHz	/
Mini-50HF	/	/	No	/	50 MHz
This Work	60	5.64 nH	Yes	/	320 MHz

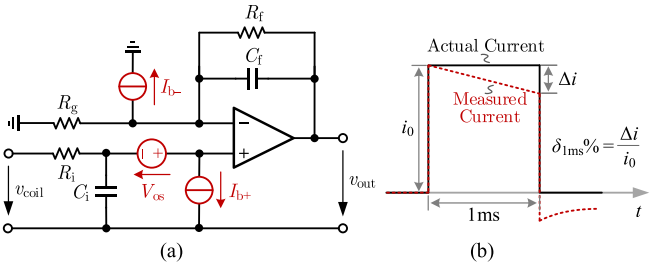

Fig. 17. Drift and droop errors of integrator. (a) Drift errors caused by I_b and V_{os} of op-amp. (b) Droop errors of rectangle current waveform.

without compromising bandwidth while equipped with shielding layers.

C. Mechanism of Integrator With Drift and Droop Errors

Eliminating errors caused by nonideal dc and low-frequency characteristics of the integrator is one of the main challenges in the integration of RCCS. The drift errors are caused by the inherent input bias current I_b and offset voltage V_{os} of op-amp [21], as shown in Fig. 17(a). The continuous charging of the feedback capacitor due to the I_b may lead to saturation of the op-amp. In addition, the V_{os} of the op-amp is also the main source of the drift errors. Typically, the V_{os} varies from tens of microvolts to several millivolts, while the high-speed op-amp usually has higher V_{os}. The tiny dc bias voltage will be amplified thousands of times due to the extremely high dc gain of the active integrator, which will severely impact the output of the RCCS.

To prevent the op-amp from saturation, R_f is connected in parallel with the C_f to provide a discharge path for the bias current I_b. After adding the R_f, the dc gain of the integrating circuit can be expressed as follows:

$$G_d = 20\lg\left(1+\frac{R_f}{R_g}\right) < 20\lg\left(A_{\rm ol}\right) \tag{13}$$

where the $A_{\rm ol}$ is the open-loop gain of the op-amp. The output voltage error V_{eos} caused by the V_{os} can be written as follows:

$$V_{eos} = 10^{\frac{G_d}{20}} V_{os}. \tag{14}$$

In addition, low-frequency attenuation of the RCCS causes droop errors. Taking the rectangular current waveform with a pulsewidth of 1 ms, as shown in Fig. 17(b), as an example, the droop percentage $\delta_{1\rm ms}\%$ can be written as follows:

$$\delta_{1\rm ms}\% = -0.2\pi f_L\% \tag{15}$$

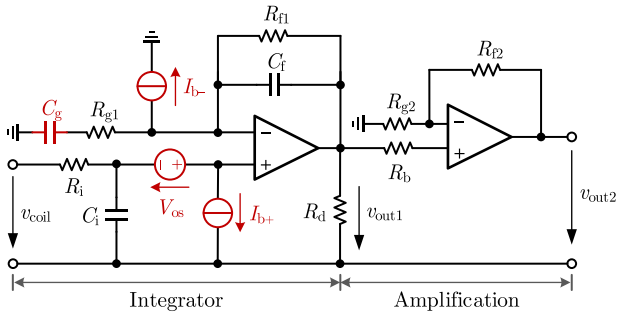

Fig. 18. Improved structure of integrator with low drift and droop errors.

where f_L is the low-frequency cutoff frequency of the RCCS. The f_L is also the first corner frequency of the active integrator after adding the R_f. To minimize the droop errors, the f_L should be designed as low as possible. This frequency is determined by the value of R_f/R_g, at the premise of maintaining the integral gain. The f_L of the integrator with a feedback resistor R_f can be expressed as follows:

$$f_L = \frac{1}{2\pi R_f C_f} = \frac{R_g}{R_f}\cdot\frac{1}{2\pi R_g C_f} = \frac{R_g}{R_f}\cdot\frac{K}{2\pi} \le \frac{K}{2\pi(A_{\rm ol}-1)}. \tag{16}$$

According to (16), increasing the value of R_f/R_g contributes to lower f_L, thus decreasing the impact of droop errors. However, this value is also limited by the open loop gain $A_{\rm ol}$ of the operational amplifier, which is not infinite. This means that the f_L cannot be approached to dc. Moreover, the increased dc gain G_d due to the larger value of R_f/R_g will also cause more severe drift issues according to (14).

D. Solutions to Dealing With Drift and Droop Errors

1) Design of Integrator Without Drift Errors: To avoid the influence of V_{os}, the capacitance C_g is in series with R_{g1} to provide low-frequency attenuation for the integrator, as shown in Fig. 18. After adding the C_g, the transfer function G_i of the integrator is changed as follows:

$$G_i = \begin{cases} 20\lg(1+2\pi R_{f1}C_g f), & f < \frac{1}{2\pi R_{g1}C_g} \\ 20\lg\left(1+\frac{R_{f1}}{R_{g1}}\right), & \frac{1}{2\pi R_{g1}C_g} < f < \frac{1}{2\pi R_{f1}C_f} \\ 20\lg\left(1+\frac{1}{2\pi R_{g1}C_f f}\right), & f > \frac{1}{2\pi R_{f1}C_f}. \end{cases} \tag{17}$$

At low frequency, the gain of the integrator reduces with the frequency decrease and eventually drops to 0 dB at dc. In this way, the impact of V_{os} can be eliminated. The value of the C_g ought to fulfill the subsequent expression so as to preserve the low-frequency capability of the RCCS

$$C_g \ge \frac{1}{2\pi R_{g1} f_L}. \tag{18}$$

However, the input bias current of the op-amp will completely flow through R_{f1}, after adding C_g. The error caused by I_b, i.e., V_{eb} can be expressed as follows:

$$V_{eb} = I_b R_{f1}. \tag{19}$$

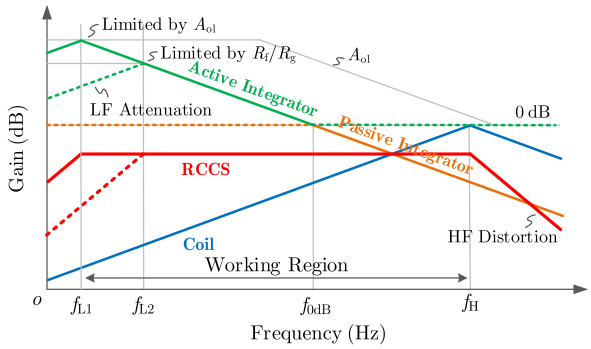

Fig. 19. Characteristics of RCCS with enhanced integrator.

Typically, to ensure sufficient low-frequency characteristics, R_{f1} is selected to be relatively high, which contradicts the requirement of mitigating the error caused by I_b, according to (19). It is important to balance the need for low-frequency performance with the impact of the input bias current. Considering the necessity of using a high R_{f1} in the megohm range, the FET-input op-amp with bias current on the order of picoampere is employed in the integrator, contributing to a negligible output error.

2) Method to Reducing Droop Errors: Benefiting to the enhanced integrator circuit with a dc gain of 0 dB, it is feasible to maximize the value of R_f/R_g and adopt the op-amp with high A_{ol}, thereby achieving superior low-frequency performance, as shown in Fig. 19. However, the nonideal characteristics of the op-amp can also lead to stability issues in the system. Since the closed-loop gain of the active integrator circuit remains unity beyond the corner frequency, it is essential that the selected op-amp exhibits unit gain stability to ensure the overall stability of the circuit. This implies that the op-amp must maintain an adequate phase margin when its open-loop gain is 0 dB.

In summary, the selection of op-amp for the enhanced integrator should satisfy the following requirements:

1) high bandwidth;
2) high open-loop gain to ensure sufficient low-frequency characteristics;
3) FET-input type with extra-low input bias current;
4) Unity-gain stability to avoid instability of the integrator.

In addition, a voltage amplification circuit is connected in series after the integrator to adjust the gain and improve the signal-to-noise ratio. To satisfy the requirements mentioned above, the FET-input op-amp OPA817 with the characteristics of high bandwidth, high A_{ol}, and stability at unity gain is selected as the integrator amplifier [21]. The OPA818 with high output voltage and gain bandwidth product (GBW) of 2.7 GHz is adopted in the voltage amplification circuit [38]. The parameters of the enhanced integrator are listed in Table III.

TABLE III
PARAMETERS FOR ENHANCED INTEGRATOR

Parameters	Values	Parameters	Values
R_{g1}	1.8 kΩ	R_{f1}	10 MΩ
C_f	390 pF	C_g	2.2 μF
f_1	230 kHz	R_{g2}	10 kΩ
R_i	750 Ω	R_{f2}	100 kΩ
C_i	100 pF	f_L	40 Hz
f_2	2.1 MHz	f_H	>100 MHz

IV. Design of Gate Driver Integrated With Proposed Overcurrent Protection Circuit

A. Hardware Design of Overcurrent Protection Circuit With Proposed RCCS

The overcurrent protection circuit includes driving circuit, current monitoring circuit, and soft turn-OFF circuit, as shown in Fig. 20. The totem pole provides sufficient driving current I_{DM} for the devices in normal operation. In addition, the current monitoring circuit includes the proposed RCCS and a high-speed comparator. To avoid insulation issues, the coil is installed at the source of the device under protection, and the output is fed back to the corresponding gate driver. When the device current i_{ds} exceeds the preset threshold, the comparator on the gate driver generates a fault signal, which will be latched by the logic circuit with extra-low propagation delay time (t_d). Then, the p/n channel MOSFETs of the totem pole will be turned OFF at the same time. The gate charge of the device is released through a high-impedance path, decreasing the gate voltage V_g slowly. This approach prevents the device from experiencing severe voltage overshoot caused by rapid turn-OFF current under overcurrent conditions. The turn-OFF speed during this phase can be adjusted by changing the impedance R_H in the turn-OFF path. In addition, upon entering fault mode, the gate voltage of device is monitored and fed into another high-speed comparator. When the gate voltage drops below 5 V, another low-impedance path is activated, completely turning OFF the device.

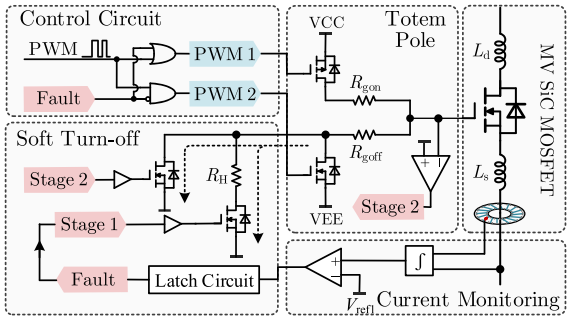

Fig. 20. Circuit structure of gate driver with soft turn-OFF function.

The aforementioned circuit is located in the post isolation stage of the driver, where both the totem-pole and soft turn-OFF circuits are controlled by driver ICs with fast propagation delays, combined with a high-speed signal processing circuit, thus enabling a swift response to fault signals. The components for the overcurrent protection circuit are listed in Table IV. The prototype of the designed gate driver is shown in Fig. 21.

B. Isolation Design of the Proposed Gate Driver

In addition, the high voltage and high *dv/dt* of MV devices impose stringent requirements on the signal and power isolation of the driver when the driver is applied to the upper switch.

TABLE IV
COMPONENTS FOR THE PROPOSED OVERCURRENT PROTECTION CIRCUIT

Components	Part number	Parameters
Comparator	TLV3601	t_d, 2.5 ns
Latch	SN74AHC1G02	t_d, 6.5 ns
Driver IC	UCC27517	t_d, 13 ns
PMOS	FDMC86139	I_{DM}, –30 A
NMOS	CSD15571Q2	I_{DM}, 52 A

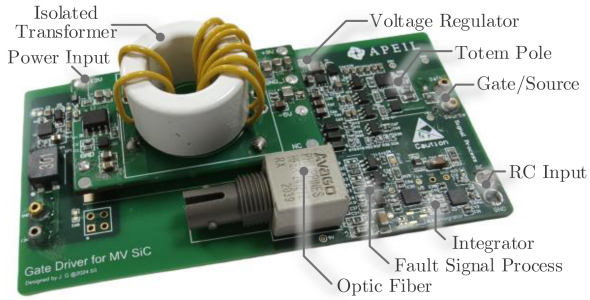

Fig. 21. Prototype of gate driver with the proposed RCCS.

Optical fiber is used for the signal transmission, providing excellent isolation performance. The isolation between the driving circuit and the ground is achieved by the gate driver power supply, which is required to exhibit high insulation performance. Besides, the common-mode current generated during the fast switching transient would flow through the driving circuit and the corresponding signal processing circuit, and ultimately injected into the ground via the isolated power supply. Typically, isolated power supply with extra-low coupling capacitance, or the gate driver with noise-free isolation architecture for signal processing circuit, is adopted to deal with the common-mode issues [22], [39].

In this study, the magnetic isolation is employed, with the transformer windings using the triple-insulated wire to ensure excellent insulation performance. The design features low turns and weak coupling, contributing to low coupling capacitance. The output of the isolated power supply is connected to a high-efficiency power regulation circuit, providing stable and reliable power rails for the gate driver and signal processing circuit. The designed gate driver power supply for the adopted 3.3-kV SiC MOSFETs has dimensions consistent with the MGJ6D052005 from Murata. The coupling capacitance of the gate driver power supply is only 3 pF at 10 MHz, which is lower than that of the commercial product, meeting the common-mode rejection requirements for MV SiC devices, as shown in Fig. 22.

V. EXPERIMENTAL VALIDATION

A. Multipulse Test for the Proposed RCCS

To verify the performance of the proposed RCCS, the multipulse test setup is built with the 3.3-kV, 24-A SiC MOSFET G2R120MT33J. The switching speed of the device can extend to 100 V/ns, which can replicate severe electric field interference in the MV converter. Besides, the low current amplitude and high electric field interference impose stringent requirements

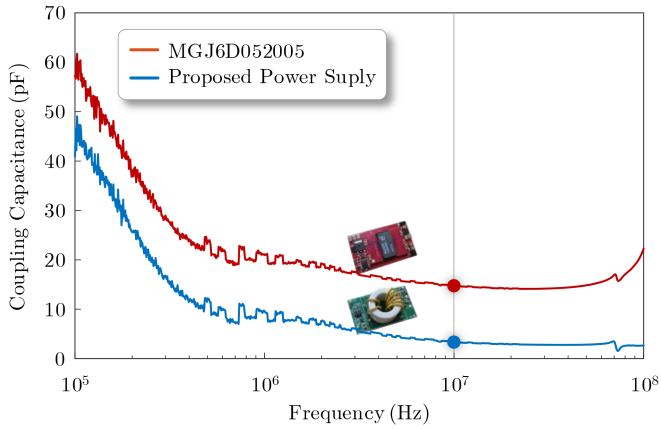

Fig. 22. Coupling capacitance of commercial and designed gate driver power supply.

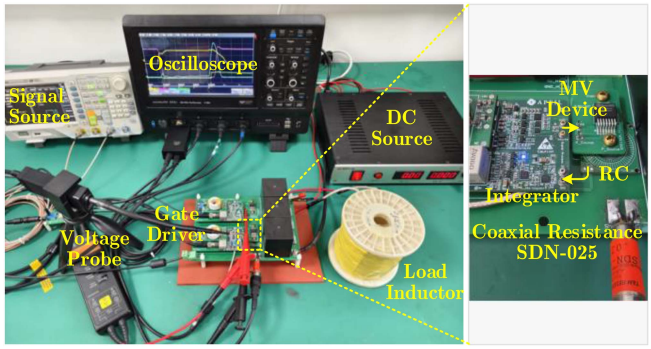

Fig. 23. Developed multipulse setup with the proposed RCCS.

on the noise immunity of the RCCS. In the experiment, the coil is installed at the source terminal of the devices, and the output signal is fed back to the gate driver board, as shown in Fig. 23. To evaluate the real current waveform of the device, the coaxial resistor SDN-025 with a bandwidth of 1.2 GHz is inserted at the return path of the current, which is immune to the interference of electric field.

The gain of the RCCS is configured to 50 mV/A, and the operating voltage of the op-amp is about ±4 V, allowing for precise measurement of the current within ±80 A. The multipulse test results are shown in Fig. 24, where the drift and droop errors were effectively eliminated by adopting the enhanced integrator.

The waveform measured by the developed RCCS is close to that measured by the SDN-025, demonstrating its capability of measuring the switching current of the device. To verify the noise immunity of the developed RCCS, the transient current measurement results under high *dv/dt* are also displayed. It can be found that the measurement errors still persist during switching transients. The accurate measurement of small currents under high electric field interference remains a challenging issue, and even the probes potentially introduce noise. This not only requires the coil to have a high noise immunity but also places demands on the noise immunity of the signal processing circuits.

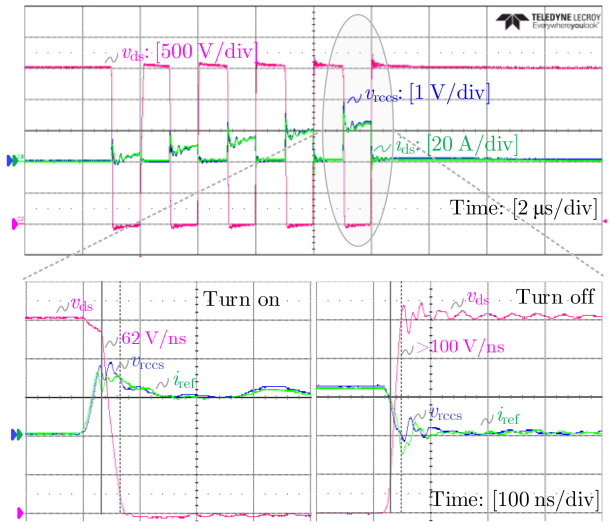

Fig. 24. Measurement result of multipulse test at $V_{dc} = 2.5$ kV.

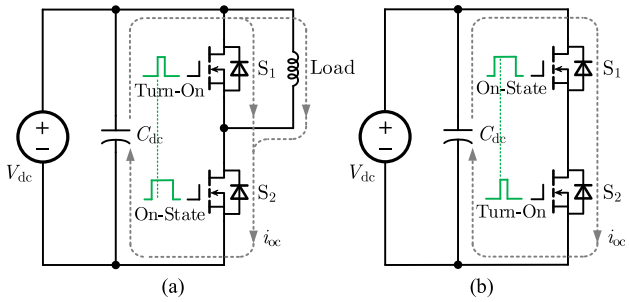

Fig. 25. Overcurrent cases. (a) FUL. (b) HSF.

B. Experimental Evaluation of the Proposed RCCS Under Various Overcurrent Conditions

The overcurrent cases typically include the fault under load (FUL) and hard switch fault (HSF), as shown in Fig. 25. In the case of FUL, current flows through the inductive load and the ON-state switch S_2, while a fault occurs and the switch S_1 is turned ON, leading to surging current. The overcurrent protection circuit is required to turn OFF the device softly when the current exceeds the threshold and avoid excessive voltage overshoot, as shown in Fig. 26(a).

The threshold current for protection is set at 50 A, which is within the measurement range of the RCCS. And the threshold current is approximately twice the rated current of the device, corresponding to an output voltage of 2.5 V for the RCCS. This consideration accounts for reverse recovery current and noise during normal switching operations. When the current exceeds the threshold, the fault signal will be set to "1," and the ON-state switch S_2 is softly turned OFF with a slight overshoot, as displayed in Fig. 26(b). The short-circuit current is accurately measured by the developed RCCS, and the device is reliably turned OFF at approximate 200 ns with a peak current of 125 A.

In the case of HSF, the dc-link voltage is directly applied to the device, which is accidentally turned ON, and the current

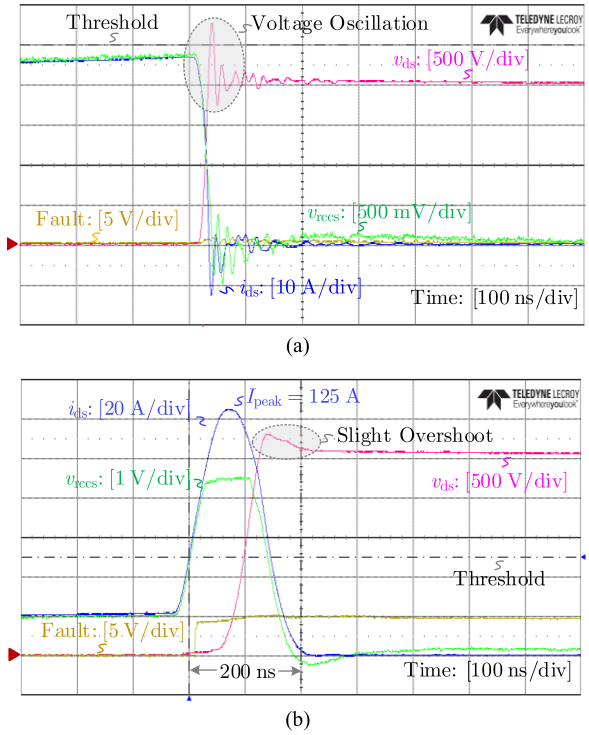

Fig. 26. Experimental results of overcurrent protection test under FUL condition. (a) Normal turn-OFF under approximately twice rated current. (b) Soft turn-OFF under surging current.

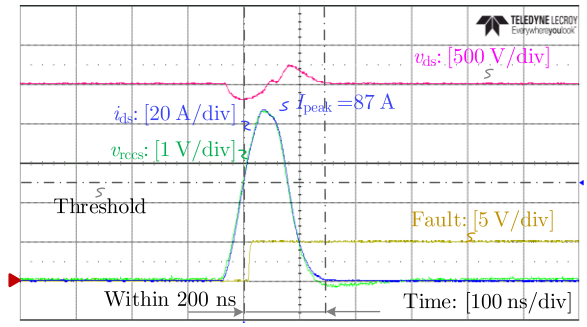

Fig. 27. Experimental results of overcurrent protection test under HSF condition. DC-link voltage: 2.5 kV and gate resistance: 8 Ω.

increases rapidly until saturation, as shown in Fig. 25(b). If the device cannot be turned OFF within a limited time, it may be damaged due to the huge heat generated during the short-circuit period. To verify the proposed overcurrent protection scheme under the HSF condition, the single-pulse test is operated, where the switch S_1 is short circuited, and the switch S_2 is turned ON under the dc-link voltage of 2.5 kV. The results are displayed in Fig. 27. After the device is turned ON, the current increases and exceeds the threshold within 50 ns. The protection circuit reacts quickly and reliably turns OFF the device within 200 ns. The maximum current of the device reaches about 87 A under this condition.

To demonstrate the robustness of the proposed protection circuit, comprehensive FUL and HSF experiments are conducted

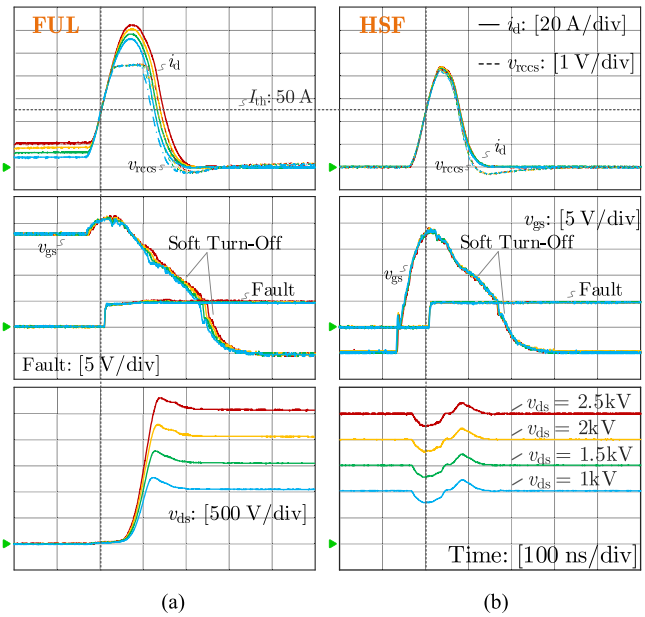

Fig. 28. Overcurrent experiments with DC-link voltage vary from 1 to 2.5 kV. (a) Under FUL conditions. (b) Under HSF conditions.

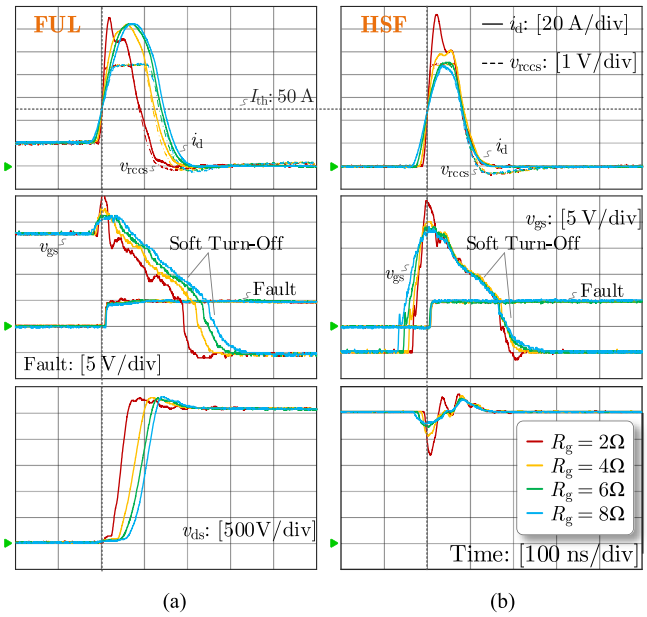

Fig. 29. Overcurrent experiments with gate resistance vary from 2 to 8 Ω. (a) Under FUL conditions. (b) Under HSF conditions.

under different conditions, including various dc voltages, gate resistances, and gate voltages, as presented in Figs. 28–30, respectively. The experimental results indicate that the overcurrent protection circuit detects the fault quickly and the device is safely turned OFF within 200 ns in various overcurrent conditions. The device current i_{ds} and the output voltage of the RCCS v_{rccs} are depicted by the solid and dashed lines, respectively, in the waveforms at the top of Figs. 28–30. Since the operating voltage of the op-amp is typically slightly lower than its supply voltage, which is ±5 V in this design, the RCCS is unable

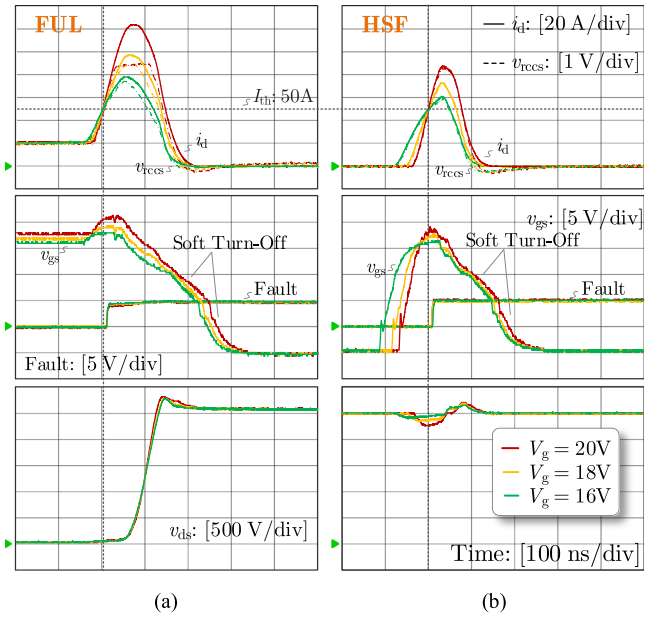

Fig. 30. Overcurrent experiments with gate voltage vary from 16 to 20 V. (a) Under FUL conditions. (b) Under HSF conditions.

to fully replicate the peak short-circuit current, resulting in signal clipping. However, the fault threshold corresponds to an output voltage of 2.5 V for the RCCS, and this voltage can be accurately detected. In addition, the *RC* network at the front end of the op-amp effectively prevents input signal distortion and the potential risk of the failure of the op-amp.

Since the device is already in the ON-state when the fault occurs, the peak short-circuit current generated under FUL conditions is typically higher than that generated under HSF. Among the experiments, the impact of the gate resistance on the overcurrent waveforms is the most significant. With a lower gate resistance, the current rise rate is significantly accelerated, and the peak current reaches 130 A and 133 A under the FUL and HSF conditions, respectively. The proposed protection circuit can still reliably turn OFF the device at the 2 Ω gate resistance while keeping the v_{ds} with oscillation not exceeding 3 kV. Comprehensive experiments demonstrate that the proposed protection circuit can deal with overcurrent faults under various conditions and protect the devices safely and reliably.

VI. Conclusion

The RCCS is a promising embedded current sensor, offering both current monitoring and protection for the devices and converters. However, the insufficient high-frequency and low-frequency characteristics significantly constrain its widespread application. In this article, the design method of broadband RCCS with high performance is proposed and applied to overcurrent protection for MV SiC MOSFET. In the case of high frequency, the novel coil based on the transmission line theory is proposed to overcome the constraint between bandwidth and parasitic components. Benefiting from this feature, the coil with high bandwidth of approximate 300 MHz with high number of turns and shielding layers for high noise immunity is achieved.

The impact of eddy current after inserting the shielding is discussed and eliminated through integrator compensation. In the case of low frequency, the mechanism of drift and droop errors of the integrator is revealed. The drift errors are eliminated by adding low-frequency attenuation of the integrator, and the low-frequency characteristic of the RCCS is improved to minimize the impact of droop error. The overcurrent protection scheme based on the developed RCCS is demonstrated through comprehensive FUL and HSF experiments, exhibiting extra-fast response and reliability. The proposed broadband RCCS based on the transmission line theory shows potential in fast and reliable protection for the MV SiC devices. It could be further integrated into the power electronics system, thus enabling precise current monitoring. Moreover, a more compact design and faster switching speed are prioritized in the power electronics system to enhance the overall performance. This demands the integrated current sensors with improved noise immunity capability so as to achieve seamless operation under extreme electric field environments. Additional techniques are necessary for the coil and its corresponding circuit to further enhance noise immunity while combined with the proposed broadband RCCS to meet the integration requirements for more application scenarios.

REFERENCES

[1] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kV SiC-based medium-voltage ZVS bidirectional single-phase PFC AC/DC stage," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 779–797, Jun. 2019.

[2] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. M. White, and M. Kheraluwala, "Design and implementation of a two-channel interleaved Vienna-type rectifier with >99% efficiency," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 226–239, Jan. 2018.

[3] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019.

[4] K. Vechalapu and S. Bhattacharya, "Performance comparison of 10 kV 15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[5] P. D. Reigosa, H. Luo, and F. Iannuzzo, "Implications of ageing through power cycling on the short-circuit robustness of 1.2-kV SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11182–11190, Nov. 2019.

[6] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design considerations and development of an innovative gate driver for medium-voltage power devices with high d*v*/d*t*," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5256–5267, Jun. 2019.

[7] X. Zhang et al., "A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kV SiC MOSFET," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 946–955, Sep. 2016.

[8] V.-T. Nguyen, V. U. Pawaskar, and G. Gohil, "Isolated gate driver for medium-voltage SiC power devices using high-frequency wireless power transfer for a small coupling capacitance," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10992–11001, Nov. 2021.

[9] X. Huang, D. Li, M. Lin, L. M. Tolbert, F. Wang, and W. Giewont, "Desat protection with ultrafast response for high-voltage SiC MOSFETs with high dv/dt," *IEEE Open J. Ind. Appl.*, vol. 5, pp. 94–105, Jan. 2024, doi: 10.1109/OJIA.2024.3353309.

[10] Z. Guo and H. Li, "D*v*/d*t* sensing-based short-circuit protection for medium-voltage SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10554–10558, Sep. 2023.

[11] M. H. Mohamed Sathik, P. Sundararajan, F. Sasongko, J. Pou, and V. Vaiyapuri, "Short circuit detection and fault current limiting method for IGBTs," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 4, pp. 686–693, Dec. 2020.

[12] T. Horiguchi, S. -i. Kinouchi, Y. Nakayama, and H. Akagi, "A fast short-circuit protection method using gate charge characteristics of SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4759–4764.

[13] Z. Ke, J. Wang, B. Hu, X. Song, Z. Peng, and Y. Dai, "An ultrafast universal short-circuit protection technique based on gate current detection for SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 11931–11936, Oct. 2024, doi: 10.1109/TPEL.2024.3401197.

[14] Texas Instruments, "Understanding the short circuit protection for silicon carbide MOSFETs," 2018. [Online]. Available: www.ti.com/lit/ab/slua863c/slua863c.pdf?ts=1713834481075

[15] D. Rothmund, D. Bortis, and J. W. Kolar, "Highly compact isolated gate driver with ultrafast overcurrent protection for 10-kV SiC MOSFETs," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 4, pp. 278–291, Dec. 2018.

[16] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A d*i*/d*t* feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[17] J.-A. Lee, D. H. Sim, and B. K. Lee, "Short-circuit protection for SiC MOSFET based on PCB-type Rogowski current sensor: Design guidelines, practical solutions, and performance validation," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3580–3589, Mar. 2024.

[18] C. D. M. Oates, A. J. Burnett, and C. James, "The design of high performance Rogowski coils," in *Proc. Power Electron., Drives Conf.*, 2002, pp. 568–572.

[19] W. F. Ray and R. M. Davis, "High frequency improvement in wide bandwidth Rogowski transducers," in *Proc. Elect. Power Eng.*, 1999, pp. 1–9.

[20] X. Zhao et al., "Design of ultracompact gate driver integrated with current sensor and commutation path for a 211-kW three-level SiC aircraft propulsion inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 4, pp. 4077–4094, Aug. 2023.

[21] J. Wang, Z. Shen, R. Burgos, and D. Boroyevich, "Integrated switch current sensor for short circuit protection and current control of 1.7-kV SiC MOSFET modules," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[22] J. Wang, S. Mocevic, R. Burgos, and D. Boroyevich, "High-scalability enhanced gate drivers for SiC MOSFET modules with transient immunity beyond 100 V/ns," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10180–10199, Oct. 2020.

[23] H. Li, Z. Xin, X. Li, J. Chen, P. C. Loh, and F. Blaabjerg, "Extended wide-bandwidth Rogowski current sensor with PCB coil and electronic characteristic shaper," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 29–33, Jan. 2021.

[24] Z. Zhou, Z. Xin, Q. Liu, and C. Li, "A differential compensated air coil current sensor for switching current measurement of power devices," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 5356–5364, May 2023.

[25] S. Mocevic et al., "Comparison and discussion on short-circuit protections for silicon-carbide MOSFET modules: Desaturation versus Rogowski switch-current sensor," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2880–2893, May/Jun. 2020.

[26] Y. Liu, J. Bai, M. Huang, and X. Zha, "An online monitoring method for single aluminum electrolytic capacitor in the DC bank of single-phase inverter based on the Rogowski coil," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12647–12658, Oct. 2022.

[27] S. Fu et al., "Current measurement method of multiple chips using rectangular PCB Rogowski coils integrated in press pack IGBT device," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 96–100, Jan. 2023.

[28] Y. Shi, Z. Xin, P. C. Loh, and F. Blaabjerg, "A review of traditional helical to recent miniaturized printed circuit board Rogowski coils for power-electronic applications," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12207–12222, Nov. 2020.

[29] T. Tao, Z. Zhao, W. Ma, Q. Pan, and A. Hu, "Design of PCB Rogowski coil and analysis of anti-interference property," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 2, pp. 344–355, Apr. 2016.

[30] J. N. Fritz, C. Neeb, and R. W. De Doncker, "A PCB integrated differential Rogowski coil for non-intrusive current measurement featuring high bandwidth and d*v*/d*t* immunity," in *Proc. Power Energy Student Summit*, 2015, Paper S05.2.

[31] W. F. Ray and C. R. Hewson, "High performance Rogowski current transducers," in *Proc. IEEE Ind. Appl. Conf.*, 2000, vol. 5, pp. 3083–3090.

[32] J. A. J. Pettinga and J. Siersema, "A polyphase 500 kA current measuring system with Rogowski coils," *IEE Proc. B (Electr. Power Appl.)*, vol. 130, no. 5, pp. 360–363, 1983.

[33] G. M. Hashmi, M. Lehtonen, and A. Ametani, "Modeling and experimental verification of covered-conductor for PD detection in overhead distribution networks," *IEEJ Trans. Power Energy*, vol. 130, no. 7, pp. 670–678, 2010.
[34] Y. Wang, T. Long, M. Zou, P. Sun, J. Gong, and L. Wang, "Transmission line Rogowski coil: Isolated current sensor with bandwidth exceeding 3 GHz for wide-bandgap device," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13599–13605, Nov. 2023.
[35] R. Ludwig and G. Bogdanov, *RF Circuit Design: Theory and Applications*. Englewood Cliffs, NJ, USA: Prentice Hall, 2010.
[36] D. A. Weston, *Electromagnetic Compatibility: Principles and Applications*. New York, NY, USA: Marcel Dekker, 1992.
[37] Texas Instruments, "OPA817 800-MHz, high-precision, unity-gain stable, FET-input op amp," 2022. [Online]. Available: www.ti.com/lit/ds/symlink/opa817.pdf?ts=1713831701104
[38] Texas Instruments, "OPA818 2.7-GHz, high-voltage, FET-input, low noise, op amp," 2020. [Online]. Available: www.ti.com/lit/ds/symlink/opa818.pdf?ts=1713855341143
[39] H. Li, Z. Gao, and F. Wang, "Medium-voltage isolated auxiliary power supply design for high insulation capability, ultra-low coupling capacitance, and small size," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7226–7240, Jun. 2023.

Jiakun Gong received the B.Sc. degree in electrical engineering in 2022 from Chongqing University, Chongqing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Yulei Wang received the B.Sc. degree from the China University of Mining and Technology, Xuzhou, China, in 2019, and the M.Sc. degree from Chongqing University, Chongqing, China, in 2023, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical and computer engineering with McMaster University, Hamilton, ON, Canada.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Liang Wang (Student Member, IEEE) received the B.Sc. degree from the Chongqing University of Posts and Telecommunications, Chongqing, China, in 2016, and the M.Sc. and Ph.D. degrees from Chongqing University, Chongqing, China, in 2019 and 2024, respectively, all in electrical engineering.

Since May 2023, he has been a Visiting Student with the Department of Engineering, University of Cambridge, Cambridge, U.K. His research interests include advanced packaging and industrial application of wide bandgap power devices.

Mingrui Zou received the B.Sc. degree in electrical engineering from the Kunming University of Science and Technology, Kunming, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with Chongqing University, Chongqing, China.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Peng Sun (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the China University of Petroleum, Beijing, China, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Chongqing University, Chongqing, China.

Since January 2024, he has been a Visiting Student with the Department of Engineering, King's College London, London, U.K. His research interests include advanced packaging and industrial application of wide bandgap power devices.

Yuxi Liang received the B.Sc. and M.Sc. degrees in electrical engineering in 2021 and 2024, respectively, from Chongqing University, Chongqing, China, where she is currently working toward the Ph.D. degree in electrical engineering.

Her research interests include advanced packaging and industrial application of wide bandgap power devices.

Yiming Gong received the B.Sc. degree in electrical engineering from the Kunming University of Science and Technology, Kunming, China, in 2022. He is currently working toward the M.Sc. degree in electrical engineering with Chongqing University, Chongqing, China.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Huayang Zheng received the B.Sc. degree in electrical engineering in 2021 from Chongqing University, Chongqing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include advanced packaging and industrial application of wide bandgap power devices.

Zheng Zeng (Member, IEEE) received the B.Sc. degree from Wuhan University, Wuhan, China, in 2009, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2014, both in electrical engineering.

In July 2014, he joined the School of Electrical Engineering, Chongqing University, Chongqing, China, where he was promoted to an Associate Professor in August 2017 and a Full Professor in August 2022. From July 2018 to July 2019, he was also a Research Fellow with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His research interests include advanced packaging for wide bandgap power device and grid-connected inverter for renewable energy integration.