Influence of Mismatched Gate Loop Inductance on Threshold Dispersity Evolution and Current Sharing of Parallel SiC MOSFETs

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***Abstract*—For high-capacity applications, paralleling multiple silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) is essential. However, it is challenging to achieve complete symmetry in the gate circuits of parallel devices, resulting in mismatched gate inductances, which may lead to the current imbalance. This article focuses on investigating the evolution of threshold voltage dispersity under mismatched gate inductances and its impact on the current sharing evolution. It is found that mismatched gate inductances cause the threshold voltage dispersity to increase with gate stress time, thereby inducing a deterioration in current sharing. A boost converter with two devices in parallel was tested, demonstrating that the difference in the minimum turn-off gate voltage including undershoot is the primary trigger for increased threshold voltage dispersity. Besides, an off-state gate voltage optimization strategy was proposed to effectively mitigate the increase in threshold voltage dispersity and improve the evolution of current sharing under mismatched gate loop inductances. The findings are intended to improve the performance of SiC MOSFETs in parallel applications.**

***Index Terms*—Asymmetric layout, current sharing, parallel connection, silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), stray inductance, threshold voltage.**

I. Introduction

COMPARED to silicon-based insulated gate bipolar transistor, the silicon carbide (SiC)-based power metal oxide semiconductor field effect transistor (MOSFET) excel in high temperature, high voltage, and high frequency [1], [2], [3]. Benefiting from these superior properties, SiC MOSFET can significantly improve the power density and efficiency of converters. Therefore, SiC MOSFETs are commonly used in high-capacity applications such as electric vehicles (EVs) and photovoltaics [4], [5], [6].

SiC MOSFETs face challenges related to long-term reliability. Due to high-density traps in the SiC/SiO_2 system of SiC MOSFETs, the threshold voltage drifts under dynamic gate stress, which is positive and results in the increase of on-state resistance [7], [8]. The increase in on-state resistance causes the device to dissipate more power, subsequently raising the junction temperature [9]. Elevated junction temperatures accelerate the aging process of the device by increasing thermal stress and causing material degradation [10]. Over time, the increase in threshold voltage reduces the long-term reliability of the device.

However, the increase in on-state resistance is not the worst case. The worst case is the diversity of drift in parallel devices, which leads to current imbalance. Current imbalance is typically divided into static and transient imbalance, whereby uneven transient current distribution can increase device current overshoot [11], [12]. If the overcurrent exceeds the safe operating area, the device may experience overcurrent failure [13]. Besides, the current imbalance leads to thermal imbalance, shortening the lifespan of devices with higher temperatures. It takes time for the increase of threshold dispersity [14]. This explains why the Tesla Model 3 failures occurred after being on the road rather than during its laboratory testing phase [15].

For parallel applications, device packaging and printed circuit board (PCB) routing inevitably introduce parasitic inductance, and mismatched parasitic inductance may lead to unbalanced current. It was reported that the mismatch of the parasitic inductance in the gate driver loop leads to current imbalance for the paralleled devices [16]. The gate driver loop parasitic inductance is primarily composed of gate inductance, common source inductance, and driving source inductance. Mismatched common source parasitic inductance is the primary cause of transient current imbalance due to its influence on gate voltage, and device with smaller source parasitic inductance suffers higher transient current [17]. Besides, mismatched gate inductance is believed to have a limited effect on the transient current sharing [17]. Although a higher gate inductance results in a slower charging process of gate voltage, the gate current and its di/dt are usually small during switching. As a result, the influence of gate inductance mismatch on gate voltage values is not as pronounced as that of common source inductance.

Therefore, efforts were put on the matching of the common source inductance by Kelvin source connection and symmetrical layout design to suppress the current imbalance, but the consistency of the gate inductance in parallel devices may be

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sacrificed [18], [19]. The current studies mainly focus on the influence of mismatched gate inductance on current sharing characteristics, and the conclusion is that gate inductance has a limited influence on parallel current sharing, while the effect of threshold voltage drift has not yet been considered [16], [17]. So, there raise some basic questions: does the mismatch of the parasitic inductance in the gate driver loop lead to current imbalance by induce diversely threshold drift, and if yes, how? Besides, the degradation of current sharing over time, caused by the threshold voltage drift differences in parallel devices due to gate loop inductance mismatching, requires additional research for effective suppression.

The main contributions of this article are as follows.

1) Demonstrated that mismatched gate loop parasitic inductance can cause the threshold dispersity to increase with gate stress time, thereby inducing a deterioration of current sharing over time, although the current sharing characteristics are acceptable during the initial parallel operation. This may provide new insights into the potential triggers for the Tesla EVs recall incident.
2) Provided an explanation on why the evolution of current sharing with mismatched gate loop parasitic inductance deteriorates over time.
3) Proposed an OFF-state gate voltage optimization strategy to effectively mitigate the increase in threshold voltage dispersity and improve the evolution of current sharing under mismatched gate loop inductances.

This article tries to answer the above-mentioned questions by experiments based on a boost converter, which is trying to model the real switching conditions.

The rest of this article is organized as follows. The influence of gate inductance on the threshold voltage drift is discussed in Section II. Besides, the influence of gate inductance on the gate voltage waveform is also analyzed. After that, gate inductance mismatch in the TPAK module and gate drive PCB is presented in Section III. Section IV describes the evolution of threshold voltage dispersity and current sharing in the parallel boost converter. Section V investigates the reasons for the increased threshold dispersity. Section VI proposes a method to suppress current sharing degradation. Section VII concludes this article.

II. Influence of the Gate Loop Inductance on the Threshold Voltage Drift

Threshold voltage drift in SiC MOSFETs is a critical issue that impacts device performance and reliability. Threshold voltage drift is influenced by several factors, including the magnitude and slope of the gate voltage. Generally, a higher gate voltage leads to a faster threshold voltage drift. The gate voltage waveform is influenced by the parameters of the gate loop, with higher gate loop inductance causing gate voltage overshoot and undershoot.

To analyze the influence of gate loop inductance on the threshold drift, a test rig based on a boost circuit is developed, as shown in Fig. 1. The test conditions are as follows: $V_{DC} = 100\,\text{V}$, $V_{OUT} = 200\,\text{V}$, $i_{OUT} = 2.5\,\text{A}$, $V_G = 20/-5\,\text{V}$ and $f = 150\,\text{kHz}$. L_{ge} and L_{se} represent the gate loop inductances located external to the device package. L_{gi} and L_{si} are the parasitic gate loop inductances located internal to the device package. R_{ge} and R_{gi} are the external and internal gate resistances, respectively. Four commercial SiC MOSFETs, namely DUT.S and DUT.C, feature a planar gate structure, while DUT.R and DUT.I are trench gate, as shown in Table I.

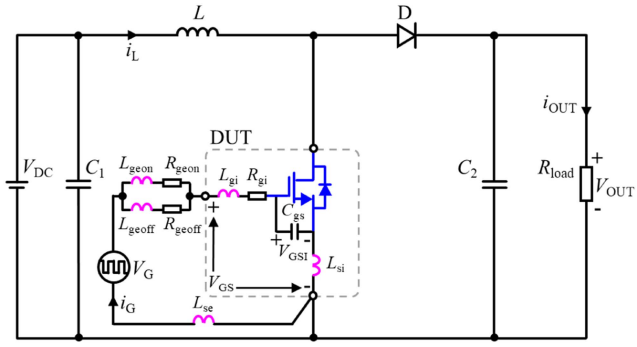

Fig. 1. Test rig using boost circuit to measure threshold voltage drift under different gate loop inductances.

TABLE I
SIC MOSFETs Under Tests

DUT	Gate Structure	Rated current @ $T_c = 25\,°C$	Package	Internal gate resistance R_{gi}
DUT.S	Planar	12 A	TO247-3	8 Ω
DUT.C	Planar	11 A	TO247-3	10 Ω
DUT.R	Trench	21 A	TO247-3	18 Ω
DUT.I	Trench	26 A	TO247-3	9 Ω

A. Influence of Gate Loop Inductance on Gate Voltage

During switching events, the energy stored in the gate loop inductance may lead to gate voltage overshoots and ringing [20]. This overshoot may exceed the gate voltage rating of the device, potentially leading to damage or failure of the gate oxide. Fig. 2 illustrates the gate voltage waveforms of DUT.R and DUT.S under different gate inductances, and the parasitic inductance of the turn-on gate loop L_{gon} ($L_{gon} = L_{geon} + L_{gi} + L_{si} + L_{se}$) is approximately the same as the parasitic inductance of the turn-off gate loop L_{goff} ($L_{goff} = L_{geoff} + L_{gi} + L_{si} + L_{se}$). Adjustable inductors L_{geon} and L_{geoff} are integrated into both the turn-on and turn-off gate loops, for changing the gate loop inductance values. L_{gi} and L_{si} of devices with package of TO247-3 are 6.33 and 4.65 nH respectively.

The parasitic inductance of the gate loop was extracted using the ANSYS Q3D tool, with the extraction frequency set at 10 MHz. The extraction frequency of parasitic inductance typically corresponds to the equivalent frequency during the switching process of power devices, defined as $0.8/(\pi \times t_r)$, where t_r is the current rise time [21]. The typical current rise times for silicon-based and silicon carbide (SiC)-based power devices range from 0.015 to 0.2 μs, with equivalent excitation frequencies between 1.27 and 16.98 MHz, making 10 MHz a suitable choice for the extraction frequency [22].

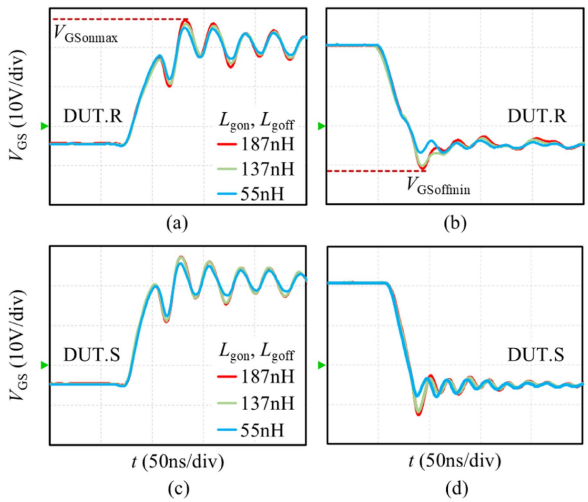

Fig. 2. Turn-ON gate voltage waveform of (a) DUT.R and (c) DUT.S with L_{gon} of 55, 137, and 187 nH. Turn-OFF gate voltage waveform of (b) DUT.R and (d) DUT.S with L_{goff} of 55, 137, and 187 nH. L_{gon} and L_{goff} are the same and change simultaneously. The gate resistance remains constant as the gate loop inductance varies.

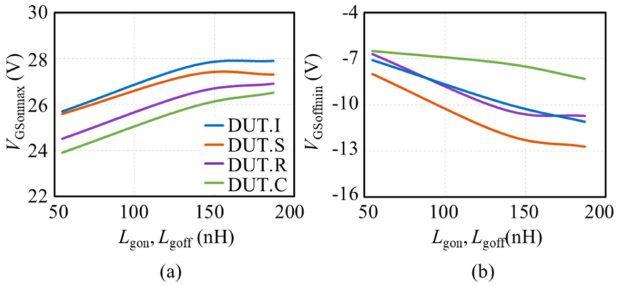

Fig. 3. (a) Maximum turn-ON gate voltage including overshoot and (b) minimum turn-OFF gate voltage including undershoot of four commercial devices under different gate inductance. L_{gon} and L_{goff} are the same and change simultaneously. The gate resistance remains constant as the gate loop inductance varies.

With the increase of parasitic inductance in the gate loop, the overshoot of gate voltage increases, as shown in Fig. 3. When the parasitic inductance in the gate loop increases from 55 to 187 nH, the maximum turn-on gate voltage including overshoot ($V_{GSonmax}$) of DUT.R rises from 24.5 to 26.9 V, while the minimum turn-off gate voltage including undershoot ($V_{GSoffmin}$) decreases from −6.7 to −10.7 V. The internal gate voltage (V_{GSI}) is the direct parameter controlling the device switching, and V_{GSI} is positively correlated with V_{GS}. V_{GSI} is given by

$$V_{GSI} = V_{GS} - (L_{gi} + L_{si}) \times \frac{di_G}{dt} - R_{gi} \times i_G \tag{1}$$

where i_G is the gate current, which is given by [23]

$$i_G = C_{iss} \times \frac{dV_{GSI}}{dt} \tag{2}$$

where the input capacitance C_{iss} is given by $C_{iss} = C_{gs} + C_{gd}$. In addition, based on TCAD simulations, the amplitudes of V_{GSI} overshoot and undershoot were confirmed to be lower than those of the V_{GS}.

For the turn-ON process, i.e., the excitation source is as a step signal, according to the Kirchhoff voltage laws, V_{GSI} is also given by

$$V_{GSI} = \frac{V_{GSon}\omega_0^2}{s\left(s^2 + 2\zeta\omega_0 s + \omega_0^2\right)}. \tag{3}$$

By applying the inverse Laplace transform, (3) can be rewritten as

$$V_{GSI} = V_{GSon}\left[1 - e^{-\zeta\omega_0 t}\left(\cos(\omega_d t) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin(\omega_d t)\right)\right] \tag{4}$$

where the natural oscillation angular frequency ω_0, the damping ratio ζ, and the damped natural frequency ω_d can be expressed as follows:

$$\begin{cases} \omega_0 = \frac{1}{\sqrt{L_{gon}C_{iss}}} \\ \zeta = \frac{R_{geon}+R_{gi}}{2}\sqrt{\frac{C_{iss}}{L_{gon}}} \\ \omega_d = \omega_0\sqrt{1-\zeta^2} \end{cases}. \tag{5}$$

When ζ is less than 1, gate voltage exhibits oscillations. As ζ decreases, the oscillations become more noticeable, and the overshoot increases. According to (5), by keeping the gate resistance unchanged and gradually increasing L_{gon}, the loop time constant rises, ζ decreases, and the overshoot becomes more noticeable. Similarly, the undershoot of V_{GSI} decreases with the increase of L_{goff}.

B. Influence of Gate Loop Inductance on Threshold Drift

As mentioned above, the increase in parasitic inductance within the gate loop results in an increase in the overshoot voltages of V_{GS} and V_{GSI}. An increase in overshoot voltage strengthens the gate oxide electric field, which promotes electron trapping and results in accelerated threshold voltage drift (ΔV_{TH}). As shown in Fig. 4, after 24 h of aging stress, ΔV_{TH} of DUT.R with $L_{gon} = 187$ nH increased by 1.68 V compared to that with $L_{gon} = 55$ nH. The threshold drift of DUT.C, DUT.S, and DUT.I increased by 0.21, 0.14, and 0.08 V, respectively. This means that devices with larger gate loop inductances may exhibit a quicker increase in losses as aging time extends. The initial slower increase in threshold drift for DUT.C is due to the smaller amount of undershoot change from 50 to 100 nH, as shown in Fig. 3(b).

Besides, to avoid the influence of junction temperature on the experimental results, the temperatures of the devices under different gate loop inductances during aging are almost the same. For DUT.I, the aging temperatures of the device under different parasitic inductances are all around 80 °C. DUT.R and DUT.C have aging temperatures near 100 °C, and DUT.S has an aging temperature of roughly 110 °C.

The threshold voltages at the initial aging stage ($t_s = 0$ h) and after 24 h of aging are both tested at room temperature, and the threshold voltage measurement circuit is shown in Fig. 5(a). Short the drain and gate of the device to the positive terminal of the threshold measurement power supply, gradually raising the output voltage while measuring the corresponding output

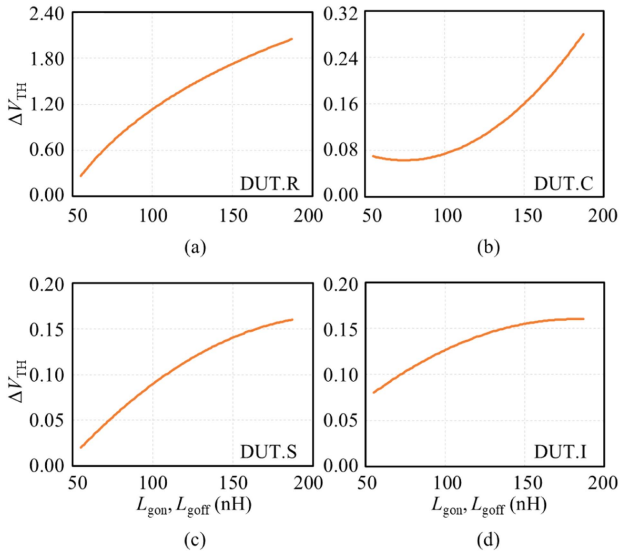

Fig. 4. Threshold voltage drift of (a) DUT.R (b) DUT.C (c) DUT.S, and (d) DUT.I under different gate inductances with $V_{GS} = 20/-5$ V and f of 150 kHz. L_{gon} and L_{goff} are the same and change simultaneously. $\Delta V_{TH} = V_{TH}(24\,h) - V_{TH}(0\,h)$.

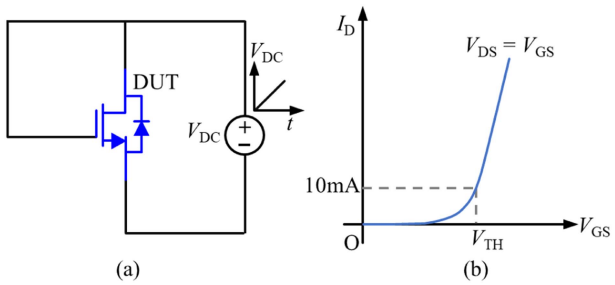

Fig. 5. (a) Threshold voltage measurement circuit. (b) Threshold voltage measurement waveform. The threshold voltages of all devices are measured at room temperature.

current [24]. Due to the low gate leakage current of MOS devices, approximately a few hundred nA, the current through the device is almost equal to the drain current. In this study, the output voltage of the power supply when $I_{DS} = 10$ mA is defined as the threshold voltage of the device, as shown in Fig. 5(b). This threshold measurement method has been experimentally validated, demonstrating good consistency and ensuring the reliability of subsequent experimental results.

III. Gate Loop Inductance Mismatch in Parallel Application

Gate loop inductance is composed of inductance from the PCB, as well as from the terminals and bonding wires of the device module. Typical power stage designs strive to position the gate driver near the switch, creating a compact gate loop to minimize gate loop inductance. However, in applications where space for PCBs and power modules is tightly constrained, designers have to give up on symmetrical layouts, which results in mismatched parasitic inductances in the gate loops of parallel devices.

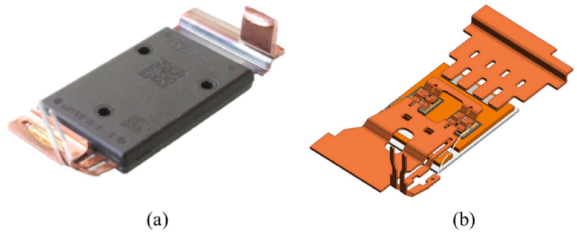

Fig. 6. TPAK SiC MOSFET module of Tesla Model 3. (a) Configuration. (b) Inner interconnection.

TABLE II
General Parameters in TPAK Module

Parameters	Value
Dimensions	20 mm×28 mm×4 mm
Diameter of Al wire	200 μm
AMB's copper thickness	760 μm
Copper lead frame thickness	400 μm

A. Parasitic Gate Loop Inductance in the Module

To investigate the potential factors triggering the Tesla EVs recall incident, i.e., there are no issues arose during initial usage but malfunctions occurred later, an analysis of Tesla's TPAK SiC MOSFET module was undertaken. The TPAK module features four electrical connection terminals, including Kelvin-source connection, as shown in Fig. 6. Each module contains two SiC chips, where the gate terminals of both chips are linked to a common terminal using aluminum wires and copper layers, and the source terminals of the chips are joined together via copper lead frame. The general parameters in TPAK SiC MOSFET module is shown in Table II.

The layout of the gate loop parasitic inductance of the TPAK module is shown in Fig. 7. To simplify the circuit, the internal resistances of the chips have not been shown. The gate loop inductance consists of the gate inductance and the source inductance [25]. For MOS1, the gate inductance includes L_{gi1} and L_{gi2}, and the source inductance consists of L_{si1} and L_{si3}. For MOS2, the gate inductance includes L_{gi1} and L_{gi3}, and the source inductance consists of L_{si2} and L_{si3}. L_{si1} and L_{si2} are the common source inductance, coupling the gate loop and the power loop. L_{si3} is the drive source parasitic inductance. The gate loop of MOS2 is longer than that of MOS1. Compared to L_{gi2}, L_{gi3} contains an extra copper layer trace, and L_{si2} includes an additional portion of copper busbar compared to L_{si1}. The parasitic gate loop inductance of TPAK module was extracted using the ANSYS Q3D tool, with the extraction frequency set at 10 MHz, as shown in Table III. The total gate loop inductance of MOS1 is 39 nH, and that of MOS2 is 51.3 nH.

B. Parasitic Gate Loop Inductance in the Circuit

Four modules are connected in parallel to form a switch in the Tesla Model 3, with each module consists of two chips, as shown in Fig. 8. To accommodate the spatial layout requirements of modules and other components, the gate circuits of the four

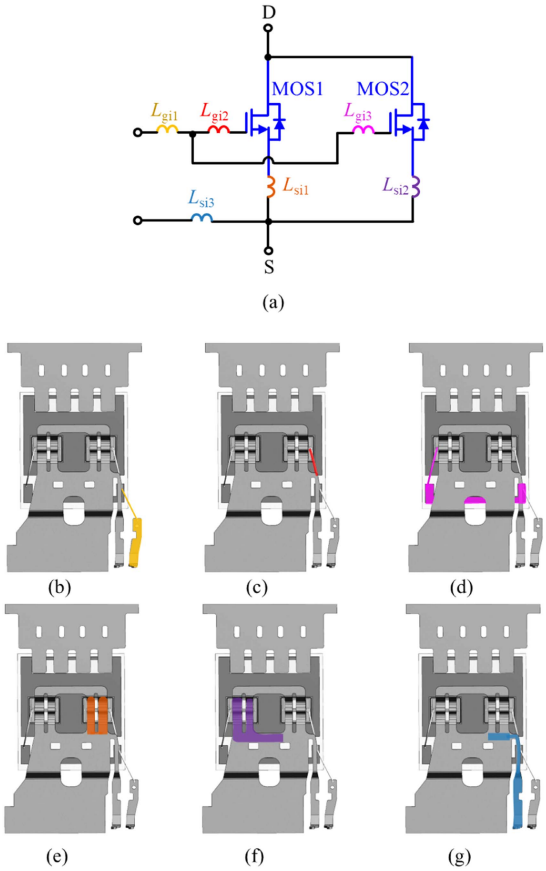

Fig. 7. (a) Schematic showing the intrinsic parasitic inductances of the TPAK module. The corresponding inductance layouts are (b) L_{gi1}, (c) L_{gi2}, (d) L_{gi3}, (e) L_{si1}, (f) L_{si2}, and (g) L_{si3}.

TABLE III
GATE INDUCTANCE OF TPAK MODULE

Inductor	Value (nH)	Inductor	Value (nH)
L_{gi1}	14.7	L_{si1}	3.1
L_{gi2}	5.4	L_{si2}	5.1
L_{gi3}	15.7	L_{si3}	15.8

modules on the PCB are not symmetric. For gate driving in the Model 3, push-pull output is used. As the driving voltage support capacitor is positioned close to the push-pull MOSFETs, the drain and source terminals of the push-pull MOSFETs are selected as the starting and ending points of the gate loop for PCB parasitic inductance extraction. The parasitic inductance of the turn-ON gate loop in the circuit includes L_{geon} and L_{se}. L_{geoff} and L_{se} constitute the inductance in the turn-OFF circuit.

The gate parasitic inductance in the PCB circuit of Tesla Model 3 is extracted by ANSYS Q3D, as shown in Fig. 9. Module 4 has the highest turn-on and turn-off gate loop inductance in the circuit, while Module 2 and Module 1 have the lowest inductance of the turn-on and turn-off gate loop. The difference between the maximum and minimum parasitic inductance of the gate in the turn-ON circuit is 35.7 nH, with the turn-off circuit showing a difference of 41.3 nH, as shown in Table IV.

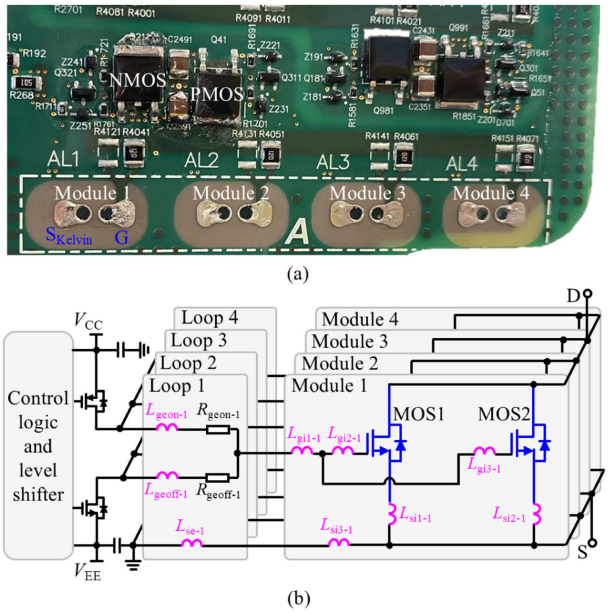

Fig. 8. (a) Printed circuit board of the phase A lower bridge arm drive circuit in the Tesla Model 3. (b) Schematic of the Model 3 drive circuit including gate inductance distribution. Subscript 1 denotes module 1.

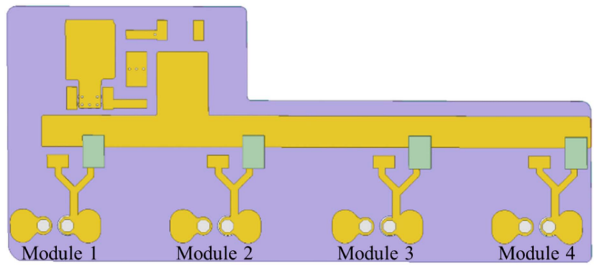

Fig. 9. Simulation of the Tesla Model 3 drive circuit using ANSYS Q3D. The front circuit is turn-ON gate drive circuit, and the back circuit is turn-OFF gate drive circuit.

TABLE IV
GATE INDUCTANCE OF CIRCUIT

Inductor	Value (nH)	Inductor	Value (nH)	Inductor	Value (nH)
L_{geon-1}	6.0	$L_{geoff-1}$	6.7	L_{se-1}	6.6
L_{geon-2}	5.6	$L_{geoff-2}$	10.8	L_{se-2}	5.8
L_{geon-3}	10.9	$L_{geoff-3}$	20.1	L_{se-3}	12.2
L_{geon-4}	24.6	$L_{geoff-4}$	32.1	L_{se-4}	22.5

Compared to the mismatch of gate inductance, although common source parasitic inductance mismatch (L_{si1} and L_{si2}) has a greater impact on parallel current sharing, the TPAK module uses Kelvin connections to minimize the difference in common source parasitic inductance between parallel chips. In the TPAK module of the Tesla Model 3, the common source parasitic inductance difference is minimal, around 2 nH, so its impact on the threshold drift difference and current sharing evolution of parallel devices is limited. Since the mismatch in common

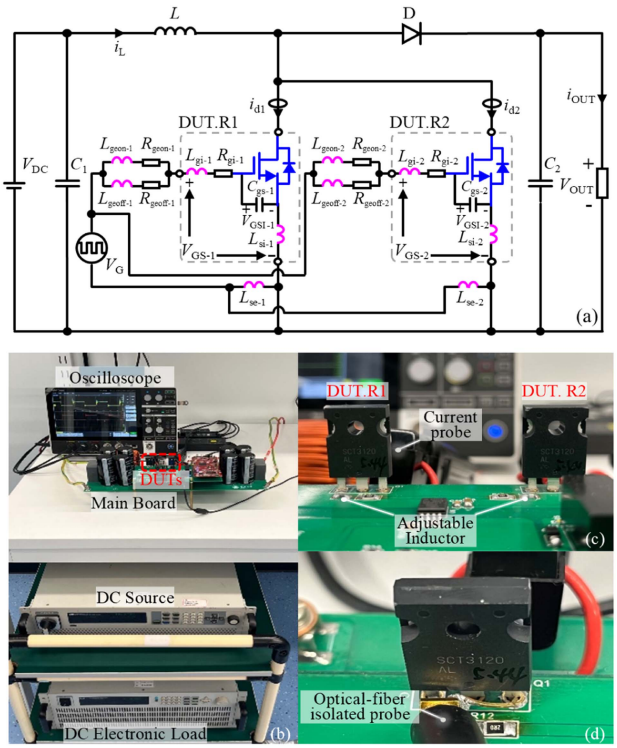

Fig. 10. (a) Boost circuit diagram. (b) Experimental setup of boost. (c) DUT.R1 and DUT.R2 connected in parallel. The driver board and power board are separated, and the common source inductance is small. (d) V_{GS} is measured by optical-fiber isolated probe.

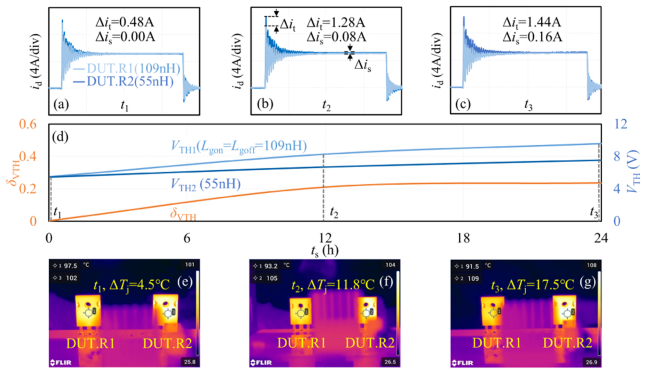

Fig. 11. Evolution of threshold dispersity, current sharing, and temperature imbalance under varying stress time. (a)–(c) represent the current sharing evolution waveforms of the parallel devices at three time points. (d) illustrates the evolution of threshold dispersity over time. (e)–(g) represent the temperature difference evolution at three time points. The total current of DUT.R1 and DUT.R2 is 10 A, and $V_{GS} = 20/-5$ V, $f = 150$ kHz and duty cycle of 50%.

source parasitic inductance is minimal in practical applications, this article does not address its effect on the threshold drift differences and the current sharing evolution of parallel devices.

Mismatched gate inductance is believed to have a limited effect on the transient current sharing. Therefore, designers may sacrifice gate inductance matching to achieve better alignment of other parameters. In the Tesla Model 3, the gate loop inductance mismatch is 53.6 nH, which is much greater than the mismatch in common source parasitic inductance. The current studies mainly focus on the influence of mismatched gate inductance on current-sharing characteristics, with threshold voltage drift not being taken into consideration. However, a mismatch in the parasitic inductance of the gate loop may lead to electrical stress differences between parallel devices, which can trigger an increase in threshold voltage dispersity and subsequently worsen parallel current sharing.

IV. Influence of the Mismatched Gate Loop Inductance on Parallel Application

In parallel applications, it is difficult to achieve strict symmetry in the gate circuits of power devices, which results in differences in the gate loop inductances among parallel devices. To explore the impact of mismatched gate parasitic inductances in parallel applications, a boost circuit test bench with two SiC MOSFETs paralleled was developed, as shown in Fig. 10. The test conditions are as follows: $V_{DC} = 100$ V, $V_{OUT} = 200$ V, $i_{OUT} = 5$ A, $V_{GS} = 20/-5$ V, $f = 150$ kHz and duty cycle of 50%. The total current of paralleled devices is 10 A. Adjustable inductors are connected in the gate circuit. To eliminate the impact of device parameter mismatch, all parallel devices have been screened using a short-time-scale gate stress screening and matching method to ensure the same threshold drift rates under the same gate stress [14].

As mentioned above, the difference between the maximum (105.9 nH) and minimum (52.3 nH) gate loop inductances of the parallel SiC MOSFETs is 53.6 nH in Tesla Model 3. The main factors leading to the parasitic inductance difference in the Model 3 gate loop are the gate parasitic inductance (L_{ge} and L_{gi}) and the driver source parasitic inductance (L_{se}). Since the gate parasitic inductance and driver source parasitic inductance are connected in series in the gate drive circuit, their mismatches have a similar influence on gate voltage and current sharing [16]. Inductance mismatch is mimicked by connecting additional inductors in series within the gate loop, as shown in Fig. 10(c). Adjusting L_{geon} and L_{geoff} to set the gate loop inductance to 109 nH for DUT.R1 and 55 nH for DUT.R2, which is used for simulating the most severe condition of gate loop mismatch in Tesla Model 3.

As shown in Fig. 11(d), mismatched parasitic inductance in the gate loop leads to differences in threshold drift among paralleled devices. V_{TH1} and V_{TH2} are the threshold voltages for DUT.R1 and DUT.R2, respectively. After a stress time of about 24 h, the ΔV_{TH} of DUT.R1 is 4.1 V, and ΔV_{TH} of DUT.R2 is 2.1 V. To investigate the evolution of threshold voltage dispersity under mismatched gate loop inductance, the relative range is used in this paper as a representation of threshold voltage dispersity δ_{VTH} which is given by [14]

$$\delta_{VTH} = \frac{V_{TH\,max} - V_{TH\,min}}{V_{THavg}} \tag{6}$$

where V_{THmax}, V_{THmin}, and V_{THavg} are the maximum, minimum, and average threshold voltage of the paralleled devices, respectively. After nearly 24 h, δ_{VTH} exhibited a 23.3% increment.

Fig. 11(a)–(c) represent the current sharing evolution waveforms of the parallel devices at three time points (t_1, t_2, t_3)

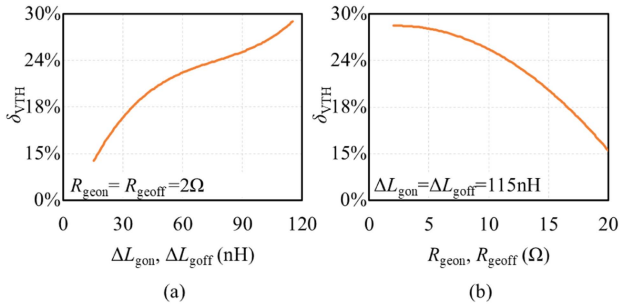

Fig. 12. Influence of (a) gate inductance differences and (b) gate resistance on δ_{VTH}. δ_{VTH} is obtained after 24 h aging stress. ΔL_{gon} and ΔL_{goff} are the same and change simultaneously. R_{geon} is the same to R_{geoff}, and the gate resistance of DUT.R1 and DUT.R2 are the same.

with a gate parasitic inductance difference of 54 nH. At t_1, although the gate parasitic inductance difference between the parallel devices is 54 nH, the current sharing performance is still acceptable, with $\Delta i_t = 0.48$ A and $\Delta i_s = 0$ A. Δi_t is the difference of transient current, and Δi_s is the difference of static current. However, as the stress time increases, Δi_t increases to 1.44 A and Δi_s to 0.16 A at time t_3 due to the increase in threshold voltage dispersity. Current sharing degradation causes temperature differences, and Fig. 11(e)–(g) shows the evolution of temperature difference between parallel devices as stress time increases. The temperature difference increases from 4.5 °C at t_1 to 17.5 °C at t_3, which reduces the stability of the system.

Common source parasitic inductance mismatch also leads to worsening parallel current sharing over time. This is because the difference in common source parasitic inductance causes a mismatch in the gate voltage waveforms of parallel devices, thereby leading to the difference in threshold voltage drift and ultimately worsening current sharing over time. Besides, compared to gate parasitic inductance mismatch, the mismatch of common source parasitic inductance has a greater impact on the deterioration of current sharing evolution caused by threshold voltage drift differences. This is because the common source parasitic inductance is also coupled with the power loop. Given that typical modules such as TPAK and HybridPACK Drive use Kelvin source connections, which minimize common source parasitic inductance differences between parallel devices, this study focuses on the effect of gate inductance mismatch on the evolution of current sharing.

A. Evolution of Threshold Dispersity

The mismatched parasitic gate loop inductances may cause differences in gate voltage waveforms of the paralleled devices. Differences in gate waveforms result in different gate oxide fields in paralleled devices, which induces different threshold drifts. Fig. 12(a) illustrates that with a growing difference in gate loop parasitic inductances ($\Delta L_{gon} = \Delta L_{goff}$) between DUT.R1 and DUT.R2, there is an increase in δ_{VTH}. Since δ_{VTH} is very small at $t_s = 0$ h, approaching zero, $\Delta\delta_{VTH} = \delta_{VTH}(24\,\text{h}) - \delta_{VTH}(0\,\text{h})$ curve is almost identical to δ_{VTH}. The key data points in Fig. 12 are shown in Table V. This is because the differences in gate voltage waveforms of parallel devices are increasing, as

TABLE V
INFLUENCE OF GATE INDUCTANCE AND GATE RESISTANCE DIFFERENCES ON THRESHOLD DISPERSITY

ΔL_{gon}(nH)	ΔL_{goff}(nH)	R_{geon}(Ω)	R_{geoff}(Ω)	δ_{VTH}@24h
15	15	2	2	11.0%
115	115	2	2	29.0%
115	115	20	20	12.4%

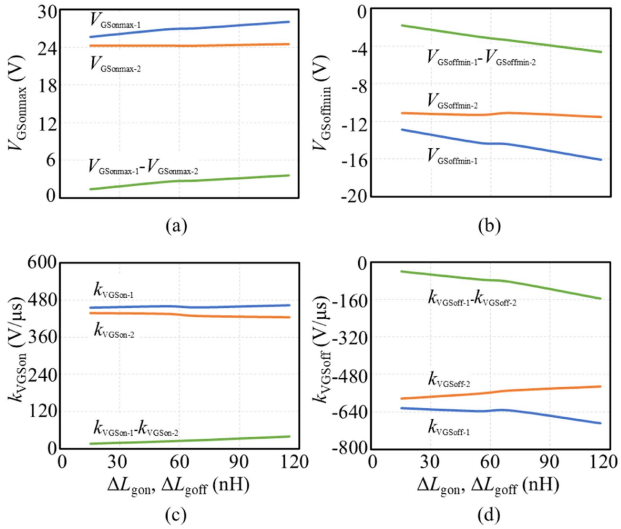

Fig. 13. Influence of mismatched parasitic inductances on (a) gate voltage overshoot, (b) undershoot, (c) turn-ON slope and (d) turn-OFF slope. Subscripts 1 and 2 denote DUT.R1 and DUT.R2, respectively. ΔL_{gon} and ΔL_{goff} are the same and change simultaneously.

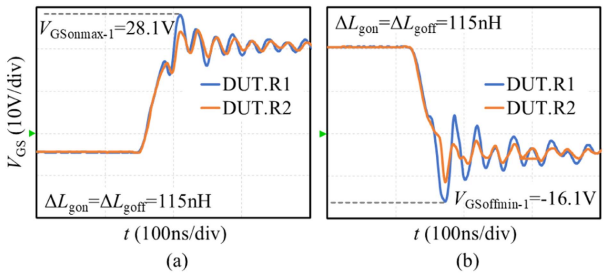

Fig. 14. (a) Turn-ON gate voltage waveform and (b) turn-OFF gate voltage waveform of parallel devices when $\Delta L_{gon} = \Delta L_{goff} = 115$ nH.

shown in Fig. 13. Fig. 14 illustrates the gate voltage waveforms for the parallel devices when $\Delta L_{gon} = \Delta L_{goff} = 115$ nH. Both the difference in the overshoot of gate voltage and the difference in gate slope increase as ΔL_{gon} and ΔL_{goff} increase. Differences in voltage and slope lead to differences in the gate oxide electric field of the parallel devices, i.e., carriers are captured and released by traps at different rates, which means that the parallel devices have different threshold drifts.

B. Evolution of Current Sharing

As mentioned above, mismatched gate parasitic inductances result in different threshold drift between DUT.R1 and DUT.R2,

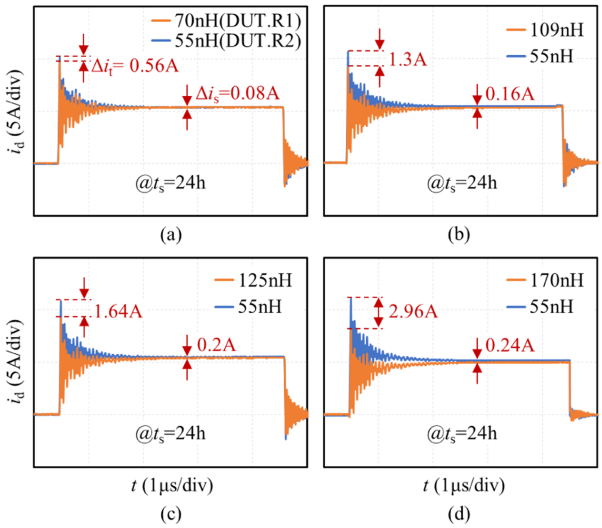

Fig. 15. Influence of mismatched parasitic inductances on current sharing with (a) $\Delta L_{\rm gon} = \Delta L_{\rm goff} = 15$ nH, (b) 54 nH, (c) 70 nH, and (d) 115 nH. The total current of DUT.R1 and DUT.R2 is 10 A, and $V_{\rm GS} = 20/-5$ V, $f = 150$ kHz and duty cycle of 50%. $L_{\rm gon}$ and $L_{\rm goff}$ are the same and change simultaneously.

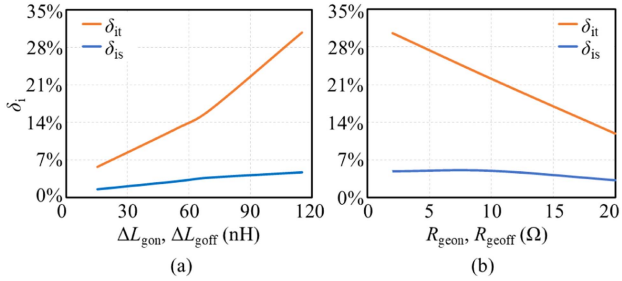

Fig. 16. Influence of (a) mismatched parasitic inductances and (b) gate resistance on current sharing. $\delta_{\rm i}$ is obtained after 24 h aging stress. $\Delta L_{\rm gon}$ and $\Delta L_{\rm goff}$ are the same and change simultaneously. $R_{\rm geon}$ is the same to $R_{\rm geoff}$, and the gate resistance of DUT.R1 and DUT.R2 are the same.

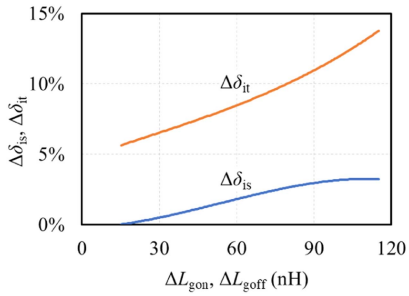

Fig. 17. Changes in current dispersity under different mismatched parasitic inductances. $\Delta\delta_{\rm is} = \delta_{\rm is}\,(24\,{\rm h}) - \delta_{\rm is}\,(0\,{\rm h})$ and $\Delta\delta_{\rm it} = \delta_{\rm it}\,(24\,{\rm h}) - \delta_{\rm it}\,(0\,{\rm h})$.

thereby inducing an increase in threshold dispersity. Threshold dispersity between parallel devices can lead to current mismatch, especially in transient current. After 24 h of aging stress, parallel devices with larger differences in gate loop parasitic inductance demonstrate poor current sharing characteristics, regardless of dynamic or static characteristics, as shown in Fig. 15. In this research, all current waveforms were measured under stable current conditions, where the current does not exhibit significant short-term fluctuations. With a gate loop parasitic inductance difference of 115 nH, the parallel devices exhibit a transient imbalance current of 2.96 A, which is larger than that observed at 15 nH. $\Delta i_{\rm t}$ caused by the threshold difference between DUT.R1 and DUT.R2 can be obtained by [26]

$$\triangle\, i_{\rm t} = \frac{\mu_{\rm ch} C_{\rm OX} Z}{L_{\rm ch}} \left(V_{\rm GS} - V_{\rm TH2}\right)\left(V_{\rm TH1} - V_{\rm TH2}\right) \qquad (7)$$

where $\mu_{\rm ch}$ is the channel mobility, $C_{\rm OX}$ is the gate oxide capacitance per unit area, Z is the channel width, and $L_{\rm ch}$ is the channel length. According to (7), a mismatched gate loop parasitic inductance results in an increase in $V_{\rm TH1}$–$V_{\rm TH2}$ with prolonged stress time, consequently leading to an increase in Δi_t, i.e., the current sharing characteristics deteriorate.

For the boost circuit shown in Fig. 10, the static and transient current imbalances are given by $\delta_{\rm is} = 2\Delta i_s \,/\, (i_{s1} + i_{s2})$ and $\delta_{\rm it} = 2\Delta i_t \,/\, (i_{t1} + i_{t2})$, respectively, as shown in Fig. 16(a). i_{s1} and i_{t1} denote the static and transient currents of DUT.R1, while i_{s2} and i_{t2} denote the static and transient currents of DUT.R2. After operating for 24 h on a boost converter platform with different inductance mismatches, as the difference in gate parasitic inductance increases from 15 to 115 nH, the corresponding $\delta_{\rm it}$ increases from 5.7% to 30.7%, and the corresponding $\delta_{\rm is}$ increases from 1.5% to 4.7%. Besides, the increase in threshold voltage dispersity caused by mismatched parasitic inductance can be suppressed by increasing the gate resistance of parallel devices. As the gate resistance increases, the static and transient current imbalances decrease, as shown in Fig. 16(b).

The degradation in current sharing due to the increase in gate parasitic inductance mismatch shown in Fig. 15 may be caused by the inductance difference itself, rather than by an increase in threshold dispersity over time resulting from inductance mismatch. To verify that the increase in threshold dispersity leads to the degradation of current sharing over time, Fig. 17 compares the current sharing characteristics of parallel devices before and after aging. Fig. 17 illustrates the change in current imbalances $\Delta\delta_i = \delta_i\,(24\,{\rm h})$–$\delta_i\,(0\,{\rm h})$ under different inductance mismatches, $\Delta\delta_i$ is greater than 0 and $\Delta\delta_i$ increases with $\Delta L_{\rm gon}$ and $\Delta L_{\rm goff}$. Since the loop parasitic inductance remains constant over stress time, the degradation of current sharing over time is caused by the increased threshold voltage dispersity, as shown in Fig. 12.

C. Evolution of Temperature Dispersity

Mismatched gate inductances in parallel applications result in different threshold voltage drifts, thereby degrading current sharing characteristics. A current mismatch results in uneven heating of the devices, leading to temperature disparities between DUT R1 and DUT R2. The temperature of the devices is measured using a thermal imager, and measurements are taken when the device temperature has stabilized. With the increasing difference in gate inductance of parallel devices, temperature dispersity $\delta_{\rm Tj}$ increases, and so does the change in temperature

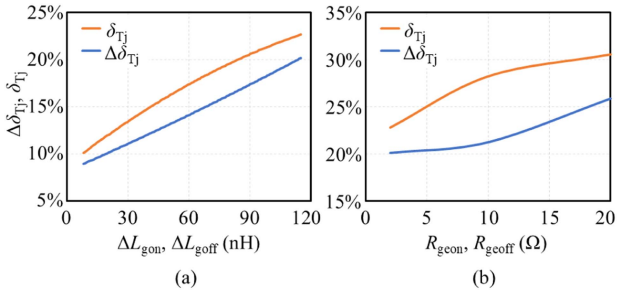

Fig. 18. Influence of (a) mismatched parasitic inductances and (b) gate resistance on temperature dispersity. δ_{Tj} is obtained after 24 h aging stress, and $\Delta\delta_{Tj} = \delta_{Tj}(24\,h) - \delta_{Tj}(0\,h)$. R_{geon} is the same to R_{geoff}, and the gate resistances of DUT.R1 and DUT.R2 are the same.

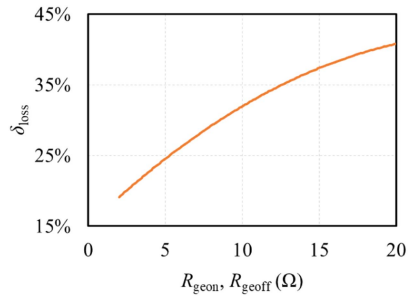

Fig. 19. Influence of gate resistance on switching loss dispersity. δ_{loss} is obtained after 24 h aging stress. R_{geon} is the same to R_{geoff}, and the gate resistances of DUT.R1 and DUT.R2 are the same.

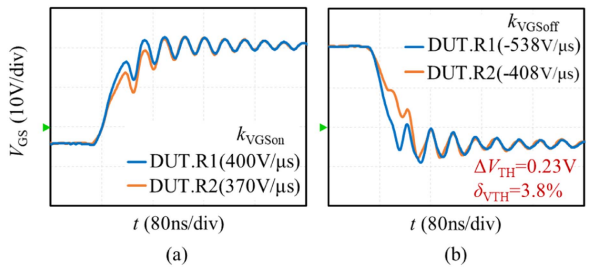

Fig. 20. (a) Turn-ON gate voltage waveform and (b) turn-OFF gate voltage waveform of parallel devices with different slope. $V_{GSonmax}$ of DUT.R1 and DUT.R2 is about 23 V, and $V_{GSoffmin}$ is about −9 V. $V_{GS} = 20\,/\,-5$ V. $\Delta V_{TH} = V_{TH}(24\,h) - V_{TH}(0\,h)$.

dispersity $\Delta\delta_{Tj} = \delta_{Tj}(24\,h) - \delta_{Tj}(0\,h)$, as shown in Fig. 18(a). δ_{Tj} in Fig. 18(a) is obtained after 24 h aging stress. The root cause of the increase of δ_{Tj} stems from the mismatch in gate inductance, which leads to disparate threshold voltage drifts between parallel devices.

As mentioned above, when the gate resistance increases, the increased threshold dispersity induced by mismatched gate inductance is suppressed. Besides, both static and transient current imbalances are improved. When the external gate resistance increased from 2 to 20 Ω, at $t_s = 24$ h, the static current difference decreases from 0.24 to 0.16 A, and the transient current difference decreases from 2.96 to 1.04 A. However, as the gate resistance increases, the temperature dispersity of parallel devices increases, as shown in Fig. 18(b). Due to the switching frequency of boost circuit is 150 kHz, the main factor causing temperature disparity between parallel devices is the difference in switching losses. The difference of switch loss ΔE_{SW} between DUT.R1 and DUT.R2 is given by

$$\triangle E_{SW} = \int_0^{t_{sw}} V_{DS}\,(i_{d2} - i_{d1})\,dt \tag{8}$$

where t_{sw} is the switching time which includes both turn-on and turn-off times, V_{DS} is the drain-to-source voltage, i_{d1} and i_{d2} are the drain current of DUT.R1 and DUT.R2 respectively. According to (8), i_{d2}–i_{d1} decreases with gate resistance, while t_{sw} increases. When the gate resistance is 2 Ω, t_{sw} of devices is 40.8 ns, while it reaches 73.6 ns with a resistance of 20 Ω. Therefore, when the gate inductances of devices are mismatched, increasing the gate resistance may mitigate the increase in threshold dispersity. However, this can lead to a faster rise in the switching loss dispersity δ_{loss}, resulting in increased temperature disparities, as shown in Fig. 19.

V. Analysis of the Increased Threshold Dispersity

Mismatched gate inductance leads to discrepancies in the gate voltage and slope between DUT.R1 and DUT.R2, as shown in Fig. 13. With the increasing disparity in gate inductance, the differences in the overshoot of gate voltage and slope between parallel devices also increase. These differences lead to an increase in threshold voltage dispersity, resulting in different currents and temperatures between parallel devices. However, it remains unclear whether the increase in threshold voltage dispersity is primarily attributed to the difference in the gate voltage overshoot, undershoot, or slope.

By adjusting the gate resistance and inductance, the overshoot, undershoot of gate voltage, and slope are decoupled. The effect of individual variable mismatches on the threshold drift of parallel devices is analyzed. An increase in the undershoot and overshoot amplitudes can accelerate the threshold voltage drift, to shorten the experimental time and study the threshold voltage dispersity under the most severe conditions, the mismatched condition of $\Delta L_{gon} = \Delta L_{goff} = 115$ nH is selected for analysis. The gate voltage overshoot and undershoot of parallel devices are essentially the same, as shown in Fig. 20. Besides, the gate voltage slope differences in Fig. 20 are close to the slope differences in Fig. 13 when $\Delta L_{gon} = \Delta L_{goff} = 115$ nH. When parallel devices gate voltage exhibits only differences in gate voltage slopes, there is no noticeable increase in threshold voltage following 24 h of stress. Fig. 13 shows δ_{VTH} at 29% when $\Delta L_{gon} = \Delta L_{goff} = 115$ nH, but only 3.8% in Fig. 20. This means that differences in slope are not the primary factor contributing to increased threshold dispersity.

As shown in Fig. 13(a) and (b), when $\Delta L_{Gon} = \Delta L_{Goff} = 115$ nH, the differences in $V_{GSonmax}$ and $V_{GSoffmin}$ are approximately 4 and −4 V, respectively. When parallel devices exhibit the same gate voltage slope and $V_{GSoffmin}$, with a maximum turn-on gate voltage including overshoot difference of 4 V, the threshold dispersity is 1.6%, as shown in Fig. 21(a) and (b). This means that differences in $V_{GSonmax}$ are not the primary reason for the increase in threshold dispersity. When the difference in $V_{GSoffmin}$ is −4 V, with the same slope and $V_{GSonmax}$, the threshold

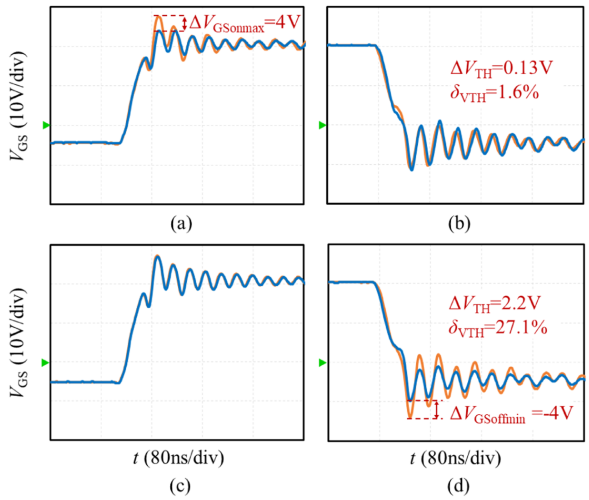

Fig. 21. Gate voltage waveform of DUT.R1 and DUT.R2 with different overshoot and undershoot. (a) and (b) represent the gate voltage waveforms for turn-ON and turn-OFF with different overshoot. (c) and (d) represent the gate voltage waveforms for turn-ON and turn-OFF with different undershoot. k_{VGSon} of DUT.R1 and DUT.R2 is about 437 V/μs, and k_{VGSoff} is about -514 V/μs. $V_{GS} = 20 / -5$ V. $\Delta V_{TH} = V_{TH}(24\,h) - V_{TH}(0\,h)$.

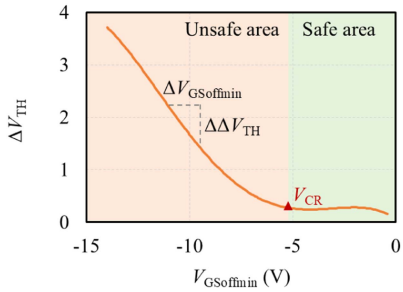

Fig. 22. Threshold voltage drifts under different $V_{GSoffmin}$. $V_{GSonmax}$ and the slope are maintained nearly constant as $V_{GSoffmin}$ decreases from 0 to -15 V. ΔV_{TH} is defined as $V_{TH}(24\,h) - V_{TH}(0\,h)$.

dispersity is 27.1%, as shown in Fig. 21(c) and (d). Thus, the main factor leading to increased threshold voltage dispersity is the difference in the minimum turn-OFF gate voltage including undershoot.

There is a critical voltage (V_{CR}) for the minimum turn-off gate voltage including undershoot, as shown in Fig. 22. When $V_{GSoffmin} > V_{CR}$, the threshold drift rate is slow, marking this area as the safe area. Conversely, when $V_{GSoffmin} < V_{CR}$, the threshold drift rate increases, designating this as the unsafe area. V_{CR} is given by $V_{CR} = \phi_{ms} - Q_{OX}/C_{OX} - Q_{it}/C_{OX}$. Where ϕ_{ms} is the work-function difference between metal and semiconductor, Q_{OX} is the charge density that lie within the gate oxide, and Q_{it} is the interface-trap-charge density.

Because ac bias temperature instability is introduced by the bipolar electric field across the gate interface instead of the bipolar gate stress. Threshold drift becomes significant only when the electric field is bipolar. When V_{GS} switches to positive voltage, the electric field near the SiC/SiO_2 interface (F_{NIT}) is positive. This is because V_{GSon} is typically 15–20 V, which is much greater than V_{CR}. However, when V_{GS} switches to negative voltage, F_{NIT}

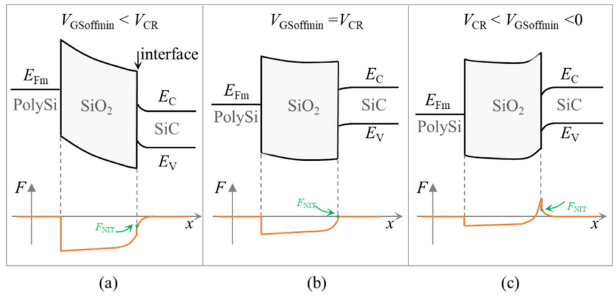

Fig. 23. Electric field across the gate interface. F_{NIT} is the electric field near the SiC/SiO_2 interface. F is the electric field, E_C is the conduction band and E_V is the valence band. (a) $V_{GSoffmin} < V_{CR}$. (b) $V_{GSoffmin} = V_{CR}$. (c) $V_{GSoffmin} < V_{CR} < 0$.

may not be negative. When $V_{CR} < V_{GSoffmin} < 0$ V, although $V_{GSoffmin}$ is less than 0 V, F_{NIT} remains positive, resulting in a unipolar electric field, as shown in Fig. 23(c). F_{NIT} becomes negative only when $V_{GSoffmin} < V_{CR}$, and the bipolar electric field is introduced, as shown in Fig. 23(a).

VI. Off-State Gate Voltage Optimization Strategy

In a parallel SiC MOSFET drive circuit, differences in parasitic inductance cause the threshold voltage dispersity between parallel devices to increase over time, leading to worsening current sharing. By optimizing the drive circuit, the time-dependent degradation of current sharing in parallel SiC MOSFETs can be improved. This optimization can be approached from two directions: first, by improving the layout of the drive circuits for parallel devices to ensure strict symmetry, identical parasitic inductance, and synchronized gate voltage signals. However, this method is challenging in practical applications due to limited layout space and the need to accommodate other components and thermal management. The second method is to suppress the rate of threshold voltage drift by optimizing the gate drive, thereby reducing the increase in threshold voltage dispersity caused by mismatches in the drive circuit.

It can be observed from Fig. 22 that there is critical voltage for the minimum turn-off gate voltage including undershoot in SiC MOSFETs, which is close to -5 V. When $V_{GSoffmin} > V_{CR}$, the threshold drift rate is limited, but when $V_{GSoffmin} < V_{CR}$, the magnitude of dynamic threshold voltage drift increases significantly. Based on the experimental results, by adjusting the off-state gate voltage V_{GSoff} and gate resistance R_{GS} of the devices, current sharing degradation caused by mismatched gate inductance can be suppressed when $V_{GSoffmin}$ of all parallel devices is larger than V_{CR}.

Fig. 24(b) shows the effect of off-state gate voltage optimization strategy based on a parallel boost converter. When $V_{GSoffmin}$ of DUT.R1 is -4.5 V and that of DUT.R2 is -0.5V, after 24 h of aging stress, the threshold voltage difference between DUT.R1 and DUT.R2 is 0.09 V, with a threshold dispersity of 1.5%, lower than the 29% observed in Fig. 24(a). The transient current difference between the parallel devices is 1.18 A, and the static current difference is 0.12 A. The increase in transient current imbalance $\Delta\delta_{it}$ is 3%, lower than the 13.8% observed

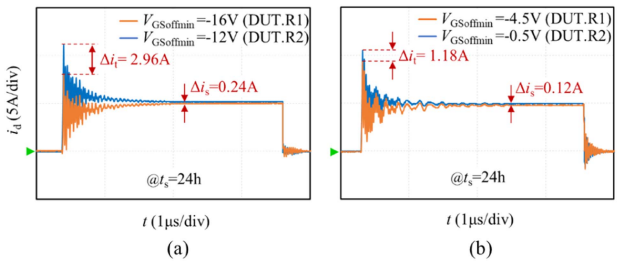

Fig. 24. Effectiveness of OFF-state voltage optimization strategy. (a) $V_{GSoffmin}$ of the parallel devices is in the unsafe region. (b) $V_{GSoffmin}$ of the parallel devices is in the safe region. The total current of DUT.R1 and DUT.R2 is 10 A, and $V_{DS} = 200$ V, $f = 150$ kHz and duty cycle of 50%.

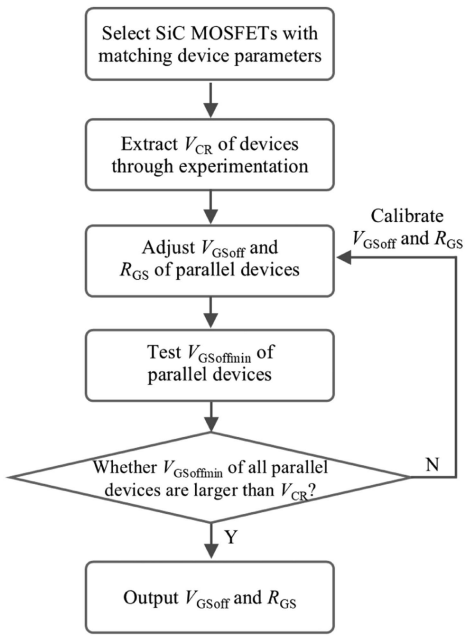

Fig. 25. Flowchart for reducing the time-dependent degradation of current sharing due to gate inductance mismatch.

in Fig. 24(a). The increase in static current imbalance $\Delta\delta_{is}$ is 0.9%, lower than 3.2% in Fig. 24(a).

To better apply this method to practical circuits, Fig. 25 provides a flowchart that offers a systematic approach. The general process for reducing the time-dependent degradation of current sharing due to gate inductance mismatch consists of six main steps.

1) Select SiC MOSFETs with matching device parameters. In parallel applications, it is necessary to ensure that the initial parameters of parallel devices are well matched. These parameters include threshold voltage, conduction resistance, and threshold drift rate under the same stress.
2) Extract the critical voltage V_{CR} of devices through experimentation. There are differences in the critical voltage across different type of devices.
3) Adjust V_{GSoff} and R_{GS} of parallel devices. Adjust V_{GSoff} and R_{GS} in the parallel application based on the critical voltage determined in Step 2.
4) Test $V_{GSoffmin}$ of parallel devices.
5) Confirm whether $V_{GSoffmin}$ of all parallel devices are larger than V_{CR}. If all $V_{GSoffmin}$ are larger than V_{CR}, proceed to the next step. Otherwise, V_{GSoff} and R_{GS} need to be calibrated.
6) Output V_{GSoff} and R_{GS}.

As mentioned above, the degradation in current sharing induced by mismatched gate inductances can be suppressed when the undershoots of all parallel devices are higher than the critical voltage. This study provides guidance for the gate driving strategies of paralleled SiC MOSFETs [27].

VII. Conclusion

This article investigated the evolution of threshold voltage dispersity in parallel SiC MOSFETs under mismatched gate inductance, and its effects on the current sharing in parallel applications were analyzed. It was found that mismatched gate driver loops indeed lead to deteriorated current-sharing characteristics due to increased threshold voltage dispersity, particularly in the transient current. Mismatched gate inductance leads to differences in the gate voltage of parallel devices, such as the maximum turn-on gate voltage including overshoot, minimum turn-off gate voltage including undershoot and slope. These differences increase the threshold dispersity, which, in turn, deteriorates current sharing. Among the three differences, the main cause of degraded current sharing is the difference in undershoot between parallel devices. There is a critical voltage for the undershoot, and the degradation in current sharing induced by mismatched gate inductances can be suppressed when the undershoots of all parallel devices are higher than the critical voltage, which can be achieved by adjusting the off-state gate voltage and gate resistance of the parallel devices. Besides, although the increase in threshold voltage dispersity can be slowed by increasing the gate resistance of parallel devices, it may lead to a faster rise in the temperature dispersity. It is hoped that these findings will be useful for the parallel application of SiC MOSFETs.

References

[1] B. J. Baliga, *Silicon Carbide Power Devices*. Singapore: World Scientific, Jan. 2006.
[2] C. Li, S. Chen, W. Li, H. Yang, and X. He, "An active voltage balancing method for series connection of SiC MOSFETs with coupling inductor," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9731–9736, Sep. 2021.
[3] Q. Wu, M. Wang, W. Zhou, and X. Wang, "Current balancing of paralleled SiC MOSFETs for a resonant pulsed power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5557–5561, Jun. 2020.
[4] X. Ju et al., "Voltage stress calculation and measurement for hairpin winding of EV traction machines driven by SiC MOSFET," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 8803–8814, Sep. 2022.
[5] X. Wang, C. Jiang, B. Lei, H. Teng, H. K. Bai, and J. L. Kirtley, "Power-loss analysis and efficiency maximization of a silicon-carbide MOSFET-based three-phase 10-kW bidirectional EV charger using variable-DC-bus control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 880–892, Sep. 2016.
[6] S. Acharya, X. She, F. Tao, T. Frangieh, M. H. Todorovic, and R. Datta, "Active gate driver for SiC-MOSFET-based PV inverter with enhanced operating range," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1677–1689, Mar./Apr. 2019.
[7] P. Salmen et al., "Gate-switching-stress test: Electrical parameter stability of SiC MOSFETs in switching operation," *Microelectronics Rel.*, vol. 135, 2022, Art. no. 114575.

[8] X. Zhong et al., "Bias temperature instability of silicon carbide power MOSFET under AC gate stresses," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1998–2008, Feb. 2022.
[9] M. Regardi et al., "How Infineon controls and assures the reliability of SiC based power semiconductors," Infineon, Neubiberg, Germany, 2020.
[10] V. Smet et al., "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4931–4941, Oct. 2011.
[11] B. Zhao, Q. Yu, P. Sun, Y. Cai, and Z. Zhao, "Device screening strategy for suppressing current imbalance in parallel-connected SiC MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 4, pp. 556–568, Dec. 2021.
[12] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Chips classification for suppressing transient current imbalance of parallel-connected silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3963–3972, Apr. 2020.
[13] J. P. Kozak, R. Zhang, J. Liu, K. D. T. Ngo, and Y. Zhang, "Physics of degradation in SiC MOSFETs stressed by overvoltage and overcurrent switching," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–6.
[14] L. Tang et al., "Impact of the threshold dispersity evolution on the current sharing of parallel SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6312–6326, May 2024.
[15] Moomoo, "Tesla recalls 127,785 Model 3 vehicles in China due to risk of losing power while driving," Apr. 2022. [Online]. Available: https://www.moomoo.com/hant/news/post/9628680?level=1&data_ticket=1692150030902817
[16] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.
[17] H. Li, S. Zhao, X. Wang, L. Ding, and H. A. Mantooth, "Parallel connection of silicon carbide MOSFETs—Challenges, mechanism, and solutions," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9731–9749, Aug. 2023.
[18] B. Zhang et al., "Common source inductance compensation technique for dynamic current balancing in SiC MOSFETs parallel operations," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13944–13956, Nov. 2023.
[19] H. Li et al., "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.
[20] S. Liang, Z. Zhao, P. Sun, and Y. Cai, "Study on the influence of gate parasitic inductance on the SiC MOSFET switching performance," in *Proc. IEEE 1st Int. Power Electron. Appl. Symp.*, 2021, pp. 1–5.
[21] J. Witcher. *Methodology for Switching Characterization of Power Devices and Modules*. Blacksburg, VA, USA: Virginia Polytechnic Inst. State Univ., 2002.
[22] Z. Zeng, X. Zhang, and X. Li, "Layout-dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.
[23] S. Zare and H. Farzanehfard, "Single-switch discontinuous current-source gate driver with voltage boosting capability and no current diversion," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12922–12931, Oct. 2023.
[24] H. Jiang, X. Zhong, G. Qiu, L. Tang, X. Qi, and L. Ran, "Dynamic gate stress induced threshold voltage drift of silicon carbide MOSFET," *IEEE Electron Device Lett.*, vol. 41, no. 9, pp. 1284–1287, Sep. 2020.
[25] D. Qin et al., "Oscillation issue and solution for solid-state circuit breaker using high power IGBT module," *IEEE Trans. Ind. Appl.*, vol. 60, no. 1, pp. 765–772, Jan./Feb. 2024.
[26] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.
[27] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021.

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