Hysteretic Current Mode Control of a Wide Output Voltage Three-Level Converter

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***Abstract*—Multilevel dc–dc converters can offer very high efficiency but have been generally limited to voltage mode control schemes for wide output voltage applications due to difficulties with current mode control near certain duty-cycles. For applications that require current mode control, this article proposes a hysteretic current mode control scheme which allows cycle-by-cycle control of multilevel converters over a wide duty-cycle range while also allowing operation at the critical duty-cycles found in multilevel converters. This enables high-efficiency solutions for applications that require a wide range of tightly regulated outputs, such as capacitor and battery charging, direct laser diode driving, and motor control. This is achieved using a multimode control scheme with ramped current references, a maximum interval timer, and reference offsetting for flying capacitor balancing. This control scheme is verified in Simulink modeling and implemented on a prototype three-level buck converter using a combination of a low-cost field programmable gate array and discrete analog circuitry. Alternative implementations are also described.**

***Index Terms*—Current mode control (CMC), cycle-by-cycle, hysteresis, multilevel (ML), wide output range.**

I. Introduction

ADVANCES in consumer electronics, medical devices and industrial products have demanded commerical off-the-shelf power supplies to provide increased power density, cooler operation, and better value while also being capable of powering a variety of load types [1], [2], [3]. This has led to a significant increase in research into alternative converter topologies that can deliver these demands. Multilevel (ML) converters promise improved efficiency compared to equivalent two-level (2L) topologies by utilizing flying capacitors and additional switches to divide the voltage across the components, leading to a reduction in losses, smaller passive components, and the capability to use components rated for lower voltages [4], [5], [6]. However, these advantages are achieved at the expense of increased component count and more complex control schemes [7], [8], [9]. There are many applications where cycle-by-cycle current mode control (CMC) is preferred over voltage mode control (VMC) since it better regulates the output current, minimizing issues with overshoot, inductor saturation and has inherent over current protection [10]. For example, in capacitor charging applications the current needs to be tightly regulated to prevent the inductor from saturating quickly when starting to charge a capacitor from 0 V [11]. In direct laser diode driving applications, the output current needs to be carefully regulated to avoid damaging the diodes [12], [13]. For battery charging it is desirable to switch between constant current and constant voltage charging modes as the battery voltage increases [14]. As well as requiring CMC, when directly driving diodes or battery charging it is advantageous to provide a wide output voltage (WOV) range to allow different series or parallel load configurations. In motor control applications it is important to limit the maximum output current when stalled or during times of high torque, while also regulating the output voltage to provide speed control.

Despite the advantages of increased efficiency and reduced component sizes offered by ML topologies, the challenges associated with cycle-by-cycle CMC have impeded their uptake in wide output range applications. For ML converters, cycle-by-cycle CMC differs significantly compared to the conventional 2L converter predominantly caused by the flying capacitor and the associated control considerations. For an ML converter with cycle-by-cycle CMC, the PWM generation scheme needs to change depending on the output voltage and the number of levels. This is further complicated by the need to change between PWM generation schemes during operation while keeping the flying capacitor balanced.

Currently, the majority of the proposed controls schemes for ML converters focus on fixed frequency voltage mode PWM control due to its simplicity, or a modified cycle-by-cycle CMC where the switching order of the switches is modified to increase the inductor current ripple at certain duty-cycles where it would otherwise be near zero (frequently referred to as the critical duty-cycles), which alleviates some control issues [7], [8], [15]. When it comes to WOV range applications there are even fewer options available. The solution described by Vukadinović et al. [8] uses a fixed frequency PWM generation scheme that changes when operating around the critical duty-cycle(s) (to prevent the inductor current ripple from approaching zero); effectively dithering

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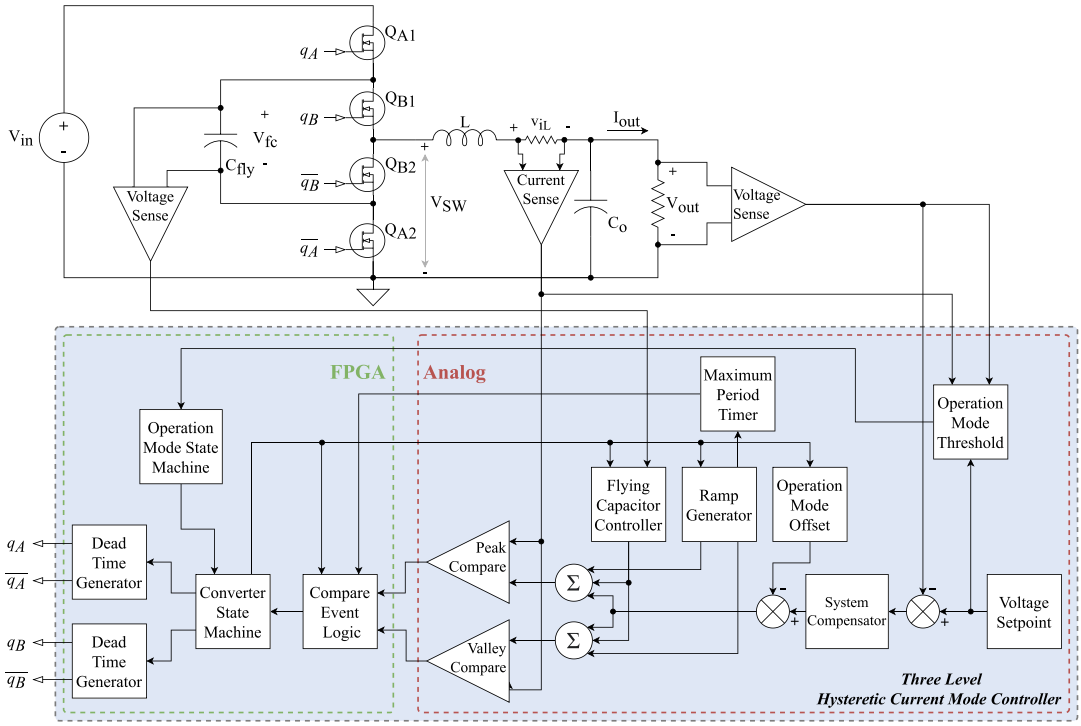


Fig. 1. Functional block diagram of the HCMC for a 3L converter.

the duty-cycles above and below the critical values, increasing power losses. Similarly, Lu et al. [7] utilized either peak current mode control (PCMC) or valley current mode control (VCMC) depending on the output voltage of the converter but avoids the zero current ripple when operating near critical duty-cycles by shaping the inductor current as a trapezoid. The implementation by Josipović et al. [15] uses a mix of CMC and PWM control but does not actively limit the peak or valley of the inductor current or demonstrate operation around 50 % duty-cycle ($D = 0.5$) for an equivalent buck topology. These implementations generally compromise on the converter efficiency when near critical duty cycles by forcing nonzero inductor current ripple or avoiding operation near the critical values.

This article presents a hysteretic current mode control (HCMC) scheme for ML converters that allows cycle-by-cycle inductor current limiting over a WOV range without diminishing the efficiency benefits offered by ML converters when operating in the zero current ripple regions at the critical duty-cycles. HCMC is preferred over PCMC as it limits both the maximum and minimum of the inductor current (and similarly for VCMC). This is beneficial as the tight control of the inductor current during voltage or current transients allows for more predictable output characteristics during these dynamic events. This WOV operation is achieved by changing the PWM generation scheme when transitioning above or below the critical duty-cycles of the converter, as well as limiting the variable frequency aspects of HCMC schemes by implementing current reference ramps and a maximum interval timer.

The proposed control scheme is demonstrated for a three-level (3L), 300 W, 36 V input, 1–30 V, 16 A output converter. Section II describes the operating principles of the proposed scheme with Simulink examples. Section III describes the design and considerations of the system compensation. Section IV describes an example implementation for the given converter specifications. Section V confirms the predicted performance of the prototype through measurements produced using a combination of a low-cost FPGA and discrete analog control circuitry. Successful control of the converter is demonstrated with load steps from 25 % → 75 %, 75 % → 25 % and voltage steps from 12 V → 24 V and 24 V → 12 V at full load which includes transitioning around the critical duty-cycle. While the control scheme is demonstrated for a 3L converter in this article, it is possible to expand this control scheme to other ML converters with more levels.

II. 3L HCMC

The proposed HCMC scheme makes use of peak and valley current references which limit the inductor current between these two values. Fig. 1 shows the different elements present in the proposed implementation for a 3L converter. It consists of a state machine that controls the switching sequence of the four switches through an HCMC scheme. There are two modes of operation, above and below the critical duty cycle, D_{crit}, which is $D = 0.5$ in the 3L converter. Each mode of operation requires a different switching sequence. The controller incorporates flying capacitor voltage balancing, and includes ramped current references and circuitry to limit the maximum switching period so as to ensure consistent operation around the critical duty cycle. Full details are described in the following sections. The analog

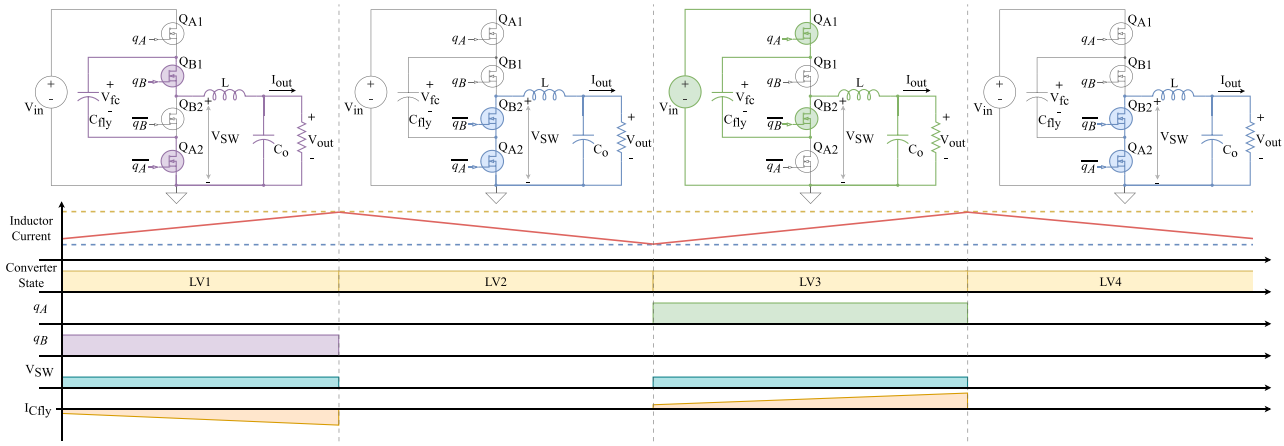


Fig. 2. 3L converter switch states for $D < 0.5$.

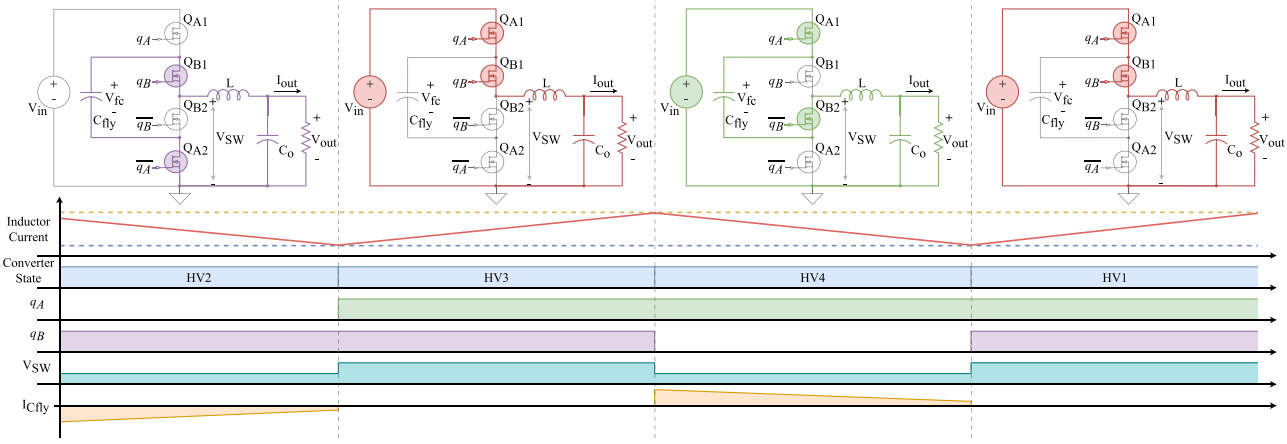


Fig. 3. 3L converter switch states for $D > 0.5$.

circuitry is used to generate the current references and compare the inductor current against the current references, while the field programmable gate array (FPGA) is used to implement the state machine required to generate the correct PWM signals and peripheral control signals, depending on operation above versus below the critical duty-cycle.

A. Duty-Cycle and Switching Order

For the 3L buck converter, there are two modes of operation depending on whether the duty-cycle, D, is less or greater than $50\,\%$, respectively. For both modes, the converter iterates through four switch states, two of which are always flying capacitor charge and discharge states. The switch node is connected to either the input voltage (V_{in}) or ground (*GND*) for the two remaining states depending on whether $D > 0.5$ or $D < 0.5$, respectively. These states are illustrated for $D = 0.25$ in Fig. 2 and for $D = 0.75$ in Fig. 3. The four switches are controlled by two complimentary PWM signals q_A and q_B, with dead time included between the switching transitions of the complimentary pairs. When operating at $D < 0.5$ the switch node voltage (V_{sw}) alternates between $0\,\mathrm{V}$ and $\frac{1}{2}V_{in}$, according to the switching sequence *LV1–LV4* seen in Fig. 3 and the output voltage (V_{out}) can be calculated as

$$V_{out} = D_{q_A}\frac{1}{2}V_{in} + D_{q_B}\frac{1}{2}V_{in} = DV_{in} \quad (0 \le D \le 0.5) \tag{1}$$

where D_{q_A} and D_{q_B} are the duty-cycle ratios of the PWM signals q_A and q_B, respectively, and normally $D_{q_A} = D_{q_B} = D$. When operating above $50\,\%$ duty-cycle ($D > 0.5$), V_{sw} alternates between V_{in} and $\frac{1}{2}V_{in}$ according to the switching sequence *HV1–HV4* which can be seen in Fig. 3. In this case V_{out} can be calculated as

$$\begin{aligned} V_{out} &= \frac{1}{2}V_{in} + \left((D_{q_A} - 0.5)\frac{1}{2}V_{in}\right) + \left((D_{q_B} - 0.5)\frac{1}{2}V_{in}\right) \\ &= DV_{in} \quad (0.5 \le D \le 1) \end{aligned} \tag{2}$$

Again assuming $D_{q_A} = D_{q_B} = D$, from (1) and (2) the converter voltage transformation ratio is directly proportional to the duty-cycle just like the conventional 2L buck converter. The PWM signals q_A and q_B are very similar to an interleaved buck

converter with the PWM signals being offset by 180 ° (see Figs. 2 and 3).

Under standard HCMC, the 3L inductor current would be bounded by the peak and valley current references, as shown in Figs. 2 and 3, which are the yellow and blue lines, respectively. The distance between the two current references is the hysteresis amplitude (Δ_{i_H}). When the inductor current reaches one of the current references, the converter changes state and causes the inductor current ripple to switch direction until it reaches the other current reference. When the converter is operating around D_{crit}, the inductor current ripple approaches zero because the voltage across the inductor for some switch states, $|V_L| = \frac{1}{2}V_{in} - DV_{in}$, approaches zero. This causes the switching frequency of the converter to approach zero as these intervals approach infinity. This is the same situation in the 2L HCMC buck converter the duty-cycle approaches 0 % or 100 %.

When operating at $D < 0.5$ but $D \to D_{crit}$, the durations of switch states *LV1* and *LV3* approach infinity, dominating the converter period making the intervals *LV2* and *LV4* negligible according to the switching scheme shown in Fig. 2. Similarly in Fig. 3 when operating at $D > 0.5$ and $D \to D_{crit}$, *HV2* and *HV4* are the predominant states in the period, while *HV1* and *HV3* are negligible. This also means that when operating at D_{crit}, the converter acts like a switched capacitor converter.

The low $|V_L|$ poses challenges for the implementation of HCMC as the low inductor voltage prevents the inductor current from reaching the peak or valley current references. This is solved through the application of ramps in the current references, as described in the next section. A ML converter with more levels will have more modes of operation, more critical duty-cycles, and more switch states within a mode of operation, which is outside the scope of this work.

B. HCMC With Current Reference Ramps

With standard HCMC, the hysteresis amplitude is generally constant, and the time duration of each of the switch states (therefore the operating frequency) varies with duty-cycle. For a 3L converter however, the duration of *LV1* (and its equivalent *LV3*) under standard HCMC would be given by

$$T_{LV1} = \frac{L\,\Delta_{i_H}}{V_{fc} - (V_{in}\,D)} = \frac{L\,\Delta_{i_H}}{\frac{1}{2}V_{in} - (V_{in}\,D)} \tag{3}$$

while the durations of *LV2* (and *LV4*) can be calculated as

$$T_{LV2} = \frac{L\,\Delta_{i_H}}{V_{in}\,D} \tag{4}$$

Clearly, as D approaches D_{crit}, the time durations of *LV1* (and *LV3*) would extend theoretically toward infinity, dominating the duration of the converter period. In order to limit these time durations, ramps are added to the peak and valley current references shown in Figs. 2 and 3. The addition of a ramp to the current reference helps limit the switch interval when $\frac{di_L}{dt}$ is very low. This also helps reduce the switching frequency range, simplifying the controller design as well as reducing the electromagnetic spectrum produced, easing electromagnetic interference compliance.

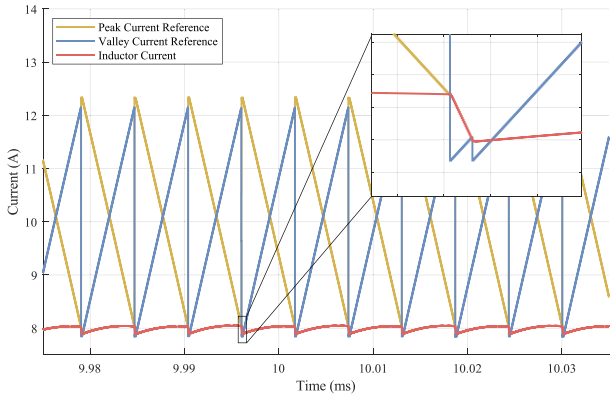


Fig. 4. Simulated 3L converter at $D = 0.48$ with the short switch interval highlighted.

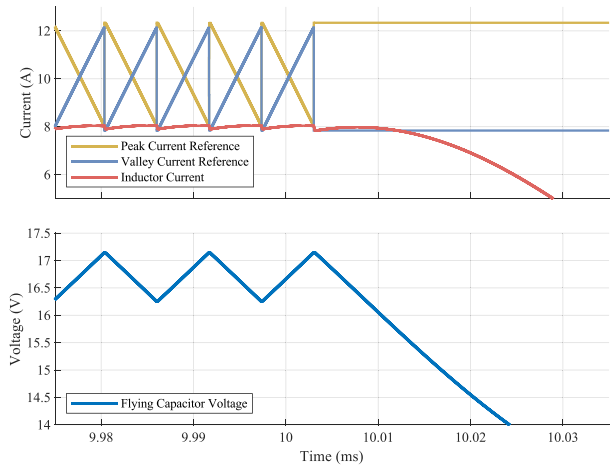


Fig. 5. Simulated 3L converter demonstrating operation at $D \approx 0.49$ with the current reference ramps at $T \lessapprox 10\,\text{ms}$ and without the current reference ramps at $T \gtrapprox 10\,\text{ms}$.

To illustrate, Fig. 4 shows the converter operating at $D = 0.48$ with the current reference ramps enabled. When operating at $D = 0.48$, the switch states *LV1* and *LV3* dominate the converter period since $|V_L| \approx 0\,\text{V}$, while the states *LV2* and *LV4* are very short to maintain the correct duty-cycle. The highlighted portion of the simulation at $T \approx 9.996\,\text{ms}$ shows a very short switch interval for the state *LV4* when the inductor current is decreasing. After the inductor current reaches the valley current reference, the converter changes to switch state *LV1*, resets the current references and waits for the inductor current to reach the peak current reference. Since $V_{fc} - V_{out} \approx 0\,\text{V}$ the inductor current rises very slowly, and the switch interval only ends once the peak current reference reaches the inductor current forcing a peak compare event to occur. The curve on the inductor current is caused by the voltage across the inductor decreasing as the limited charge of the flying capacitor depletes while supplying the load.

Fig. 5 shows the converter operating at $D \approx 0.49$ with the current reference ramps enabled initially. At $T \lessapprox 10\,\text{ms}$, the

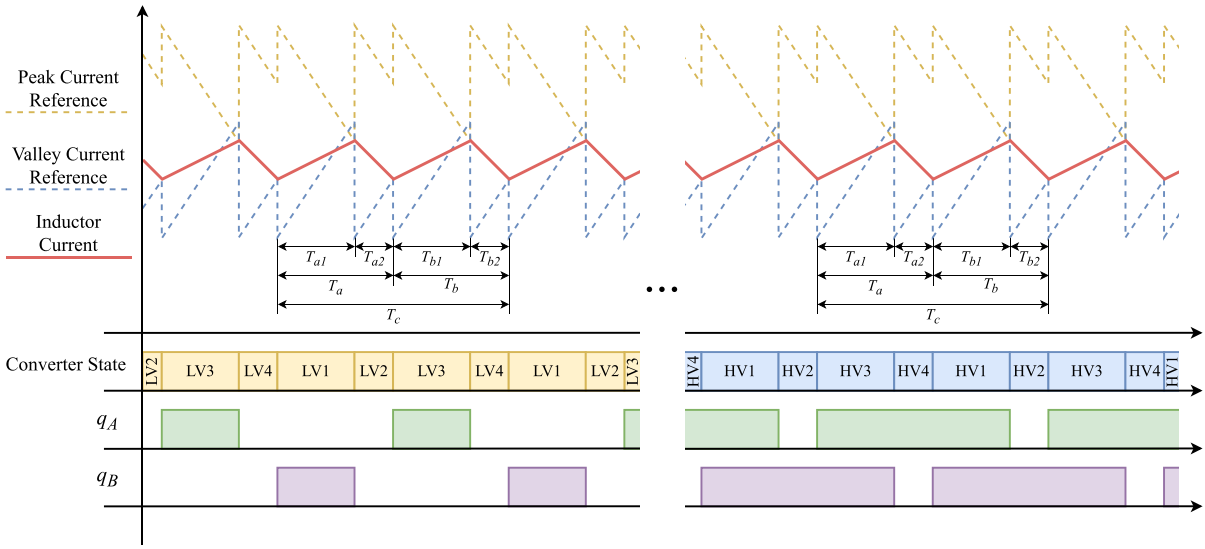


Fig. 6. 3L converter timing diagram for $D < 0.5$ and $D > 0.5$.

switch interval length is limited in steady-state operation by the peak current reference ramp approaching the inductor current. At $T \approx 10\,\text{ms}$ the ramps are disabled. In this state, the flying capacitor is connected to V_{sw} (i.e., state *LV1*), and attempts to drive the inductor current to the peak current reference. Since $V_{fc} - V_{out} = |V_L| \approx 0\,\text{V}$, the inductor current rises very slowly while the flying capacitor is discharging. As V_{fc} decreases, V_{sw} decreases. Eventually V_{fc} falls enough that the resultant V_{sw} cannot drive the inductor current to the peak reference. The converter is now stalled and cannot regulate the inductor current anymore. In this state the flying capacitor, inductor and output capacitor will oscillate.

At $D > 0.5$ with $D \to D_{crit}$ a similar situation would occur, except the switch states involved would be *HV2* and *HV4* for the long intervals and *HV1* and *HV3* for the short intervals. When the converter approaches $D \to 0$ or $D \to 1$ the same regulation scheme will occur allowing for very high and low output voltages while maintaining a limited switching frequency range.

C. HCMC Parameter Selection

With HCMC, the transitions between switch states are activated by either a peak or valley current compare event depending on the state of the converter. For example, the converter will transition for *LV1* to *LV2* on a peak current compare event shown in Fig. 2, and from *HV2* to *HV3* on a valley current compare event shown in Fig. 3.

For this control scheme, the choice of the current reference ramp ($m_r = \frac{d_{i_{ref}}}{dt}$), current reference hysteresis amplitude (Δ_{i_H}), and inductance (L) depend on the desired input voltage (V_{in}), output voltage (V_{out}), maximum inductor current ripple amplitude ($\Delta_{i_{L(max)}}$) and maximum switching frequency ($f_{sw(max)}$). For this analysis it is assumed that the flying capacitor voltage is always at half the input voltage ($V_{cfly} = \frac{1}{2}V_{in}$), but details of flying capacitor voltage control are detailed in Section III-C.

HCMC schemes do not operate at a fixed frequency, and generally the 3L buck experiences the highest switching frequencies at at $D = \{0.25, 0.75\}$, while the lowest frequency is found at $D = \{0, D_{crit}, 1\}$. It is worth noting that the switching frequency of an ML converter can refer to two different characteristics: the effective switching frequency seen by the inductor and the switching frequency of the complimentary switch pairs.

Fig. 6 shows the timing diagram of the 3L converter where T_c is the period of the full converter and the period of the pairs of switches, while T_a and T_b are usually half the converter period, which is the effective switch period seen by the inductor. Under normal operation where the flying capacitor is balanced, $T_a = T_b$. The effective switching frequency of any individual switch is $\frac{1}{T_c}$, while the equivalent switching frequency seen by the inductor is $\frac{1}{T_a}$ or $\frac{1}{T_b}$ due to the interleaving operation of the switches. For the purposes of this article, any reference to the switching frequency of the converter will refer to the effective switching frequency seen by the inductor so: $f_{sw} = \frac{1}{T_a} = \frac{1}{T_b}$. However, the converter duty-cycle is still determined by the ratio of switch on time to the converter period T_c; i.e., $D = \frac{T_{q_A}}{T_c} = \frac{T_{q_B}}{T_c}$.

For $D < 0.5$, the converter switching frequency may be calculated by considering the inductor current, I_L, shown in Fig. 6 during the states *LV1* and *LV2*. During *LV1*, I_L increases according to

$$i_L(t) = I_{L(avg)} + \left(\frac{V_{in}\,(0.5 - D)}{L}\left(t - \frac{T_{a1}}{2}\right)\right) \quad (0 < t < T_{a1}) \tag{5}$$

where $I_{L(avg)}$ is the average inductor current and $T_{a1} = DT$ is the duration of state *LV1* when the flying capacitor is connected to the switch node, assuming $V_{cfly} = \frac{1}{2}V_{in}$. Meanwhile, the reference current, I_{ref}, decreases from its maximum value at a

rate m_r

$$i_{ref}(t) = I_{ref(avg)} + \frac{\Delta_{i_H}}{2} - m_r t \quad (0 < t < T_{a1}) \tag{6}$$

where $I_{ref(avg)}$ is the average reference current, set by the voltage controller loop, and Δ_{i_H} is the hysteresis amplitude. The duration of *LV1*, T_{a1}, is found at the time where $I_L = I_{ref}$

$$\begin{aligned} &I_{L(avg)} + \frac{V_{in}\,(0.5-D)}{L}\frac{T_{a1}}{2} \\ &= I_{ref(avg)} + \frac{\Delta_{i_H}}{2} - \frac{V_{in}}{4L}T_{a1} \end{aligned} \tag{7}$$

$$\text{i.e.:}\quad T_{a1} = \frac{\frac{\Delta_{i_H}}{2} + \left(I_{ref(avg)} - I_{L(avg)}\right)}{V_{in}(1-D)/2L} \tag{8}$$

With m_r selected to be half the maximum inductor current slope following the stability guidelines described in [16] to potentially provide some passive flying capacitor balancing, although this control scheme also implements active flying capacitor balancing.

Similarly, the time duration T_{a2}, is found by analyzing the inductor current and reference current waveforms shown in Fig. 6 during *LV2* when the inductor is connected across the output, $V_{out} = DV_{in}$

$$I_{L(avg)} - \frac{DV_{in}}{L}\frac{T_{a2}}{2} = I_{ref(avg)} - \frac{\Delta_{i_H}}{2} + \frac{V_{in}}{4L}T_{a2} \tag{9}$$

$$\text{i.e.:}\quad T_{a2} = \frac{\frac{\Delta_{i_H}}{2} - \left(I_{ref(avg)} - I_{L(avg)}\right)}{V_{in}(1+2D)/4L} \tag{10}$$

The converter switching frequency is then given by

$$f_{sw} = \frac{1}{T_{a1} + T_{a2}} \tag{11}$$

For this control scheme and topology combination, the maximum switching frequency is found at $D = 0.25$, where it is true that $T_{a1} = T_{a2}$ and $I_{L(avg)} = I_{ref(avg)}$

$$\begin{aligned} T_{a1(\min)} = T_{a2(\min)} &= \frac{\Delta_{i_H}}{3V_{in}/4L} \\ \text{so:}\quad f_{sw(\max)} &= \frac{3V_{in}}{8L\Delta_{i_H}} \end{aligned} \tag{12}$$

Furthermore, the maximum inductor current ripple, $\Delta_{i_L(max)}$, is also found at $D = 0.25$, from which it is found

$$\Delta_{i_L(\max)} = \frac{V_{in}/4}{L}T_{a1(\min)} = \frac{\Delta_{i_H}}{3} \tag{13}$$

The choice of the hysteresis band may therefore be determined from a maximum specified ripple current level. Note, this relationship between the inductor and reference current ripple values depend on the chosen value of m_r. Then, for a required maximum switching frequency, the inductance may be calculated by rewriting (12) and incorporating (13) as

$$L = \frac{V_{in}}{8f_{sw(max)}\Delta_{i_L(max)}} \tag{14}$$

The minimum switching frequency is found at a duty-cycle close to D_{crit}, which is due to the very low inductor voltage and therefore a very low ripple current during *LV1* or *LV3*; i.e., $|V_L| \to 0$. As $D \to D_{crit}$, the switch interval T_{a1} is at a maximum, minimizing the duration of the interval T_{a2}. Based on (10), it is found that

$$\left(I_{ref(avg)} - I_{L(avg)}\right) = \frac{\Delta_{i_H}}{2} \tag{15}$$

and T_{a1} is found by substituting the condition of (15) into (8) to calculate the maximum value of T_{a1} as

$$T_{a1(\max)} = \frac{\Delta_{i_H}}{V_{in}/4L} \quad \text{so:} \quad f_{sw(\min)} = \frac{V_{in}}{4L\Delta_{i_H}} \tag{16}$$

Comparing (12) and (16), it is seen that $f_{sw(max)} = \frac{3}{2}f_{sw(min)}$ for the chosen value of m_r. For $D > 0.5$, the voltages at the switch node and the output would differ, but would result in the same equations for switching frequency and minimum required inductance.

Analysis of the effect of m_r, shows that for the same choice of other circuit parameters, increasing the slope of m_r will shift the switching frequency range higher and decrease the difference between the minimum and maximum switching frequency; if m_r is decreased the opposite will occur. As previously described in Section II-B, the main purpose of these ramps is to limit the minimum switching frequency of the converter to prevent the flying capacitor from over charging/discharging, so it is generally advised to keep $m_r \geq 0.5\frac{di_L}{dt}$.

In relation to the operating frequency, a high maximum switching frequency would increase losses, particularly in the switches, but due to the voltage reducing effect of the ML topology these switch losses can still be lower compared to the equivalent 2L converter [5]. Due to the frequency multiplying effect of ML topologies, the choice of inductor core material can also limit the maximum switching frequency as there are fewer choices of ferrite materials for frequencies above 1 MHz. The main limitation in this implementation is the need for high speed digital and analog components to evaluate the state of the converter quickly and accurately, which is covered in more detailed in Section IV-C.

The flying capacitor sizing depends on the minimum switching frequency, the maximum voltage deviation acceptable, and the maximum output current. The flying capacitor conducts the most when operating at D_{crit} (100 % of the converter period), so the minimum size required for the flying capacitor can be estimated by the following equation:

$$C_{fly} \approx \frac{I_{out(\max)}}{f_{sw(\min)}\,\Delta_{V_{fc}(\max)}} \tag{17}$$

The control bandwidth of the system is determined by the minimum switching frequency following the rule of thumb that the closed loop bandwidth of the system should be one tenth of the switching frequency. Since the individual switch switching frequency is less than the effective frequency seen by the inductor, the relationship between the output filter resonance and the closed loop bandwidth can begin to overlap. For a CMC scheme this will not cause many issues due to the simplified control to output frequency response, but for VMC schemes the closed loop bandwidth might be forced to a lower frequency to be prevent the *LC* resonance impacting the frequency response.

D. Flying Capacitor Balancing

Many of the control issues associated with ML converters come from managing the voltage of the flying capacitor(s), which needs to stay within a narrow range to ensure the converter can regulate effectively and ensure components are not damaged if they are only rated for a portion of the input voltage. If V_{fc} significantly deviates, the output voltage ripple increases, losses can increase, the converter can stall, or components may be damaged by exceeding their voltage rating (e.g., the switches).

While the flying capacitor can be passively balanced in some situations [16], [17] generally it needs to be actively balanced, particularly for transient events. Active balancing is usually achieved by manipulating the charge and discharge cycles of the converter, which can be performed a few different ways [9], [18], [19], [20]. For PWM-based control schemes, the duty-cycle of the switch pairs can be modified to introduce a difference in duty-cycle between them. This changes the duration of the flying capacitor's charge and discharge cycles, allowing for a net positive or negative charge into the capacitor every switching cycle. The solution proposed by Carvalho et al. [9] details an example of such a PWM-based ML converter. For cycle-by-cycle CMC control schemes, the duty-cycle is indirectly controlled and therefore cannot be directly manipulated. Instead, the duration of the flying capacitor charge and discharge cycles can be manipulated by moving the peak current reference level either toward or away from the inductor current signal, again allowing for a net negative or positive charge into the capacitors, which is described by Abdelhamid et al. [18].

For the proposed implementation, a scheme similar to the one in [18] is implemented but expanded upon to work on both the peak and valley current references. This is achieved by adjusting the peak and valley current references either toward or away from the inductor current, which adjusts the duration of the intervals, therefore manipulating the flying capacitor charge and discharge cycles. For example, if the flying capacitor is overcharged and the converter is operating in $D < 0.5$, the states *LV1* (T_{a1}) and *LV3* (T_{b1}) need to be lengthened and shortened, respectively, to net discharge the flying capacitor. When the flying capacitor is over discharged, the lengthening and shortening of the intervals is reversed to net charge the capacitor.

In the previous example, the other intervals (T_{a2} and T_{b2}) were not adjusted, as they do not affect the charging or discharging of the flying capacitor. To simplify the flying capacitor balancing circuitry in this implementation, these periods are also modified. This does not affect the operation of the converter or the output voltage regulation because the effective duration of the converter periods (T_a and T_b) is kept constant.

E. Maximum Switch Interval Timer

While the current reference ramps help keep the flying capacitor balanced during steady-state operation, during dynamic events, such as a significant step in output voltage or current, the resulting large difference between inductor current and current references increases the time taken for the inductor current to reach the references; beyond what it would be under steady-state.

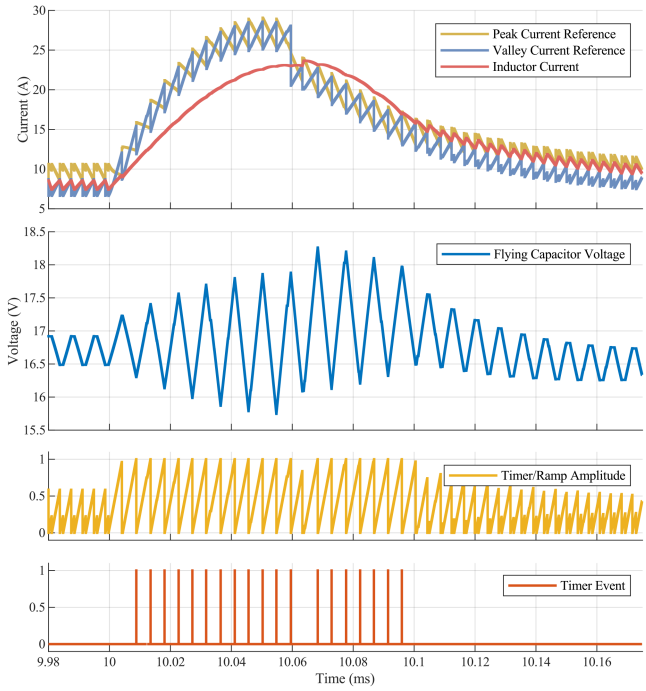


Fig. 7. Simulated 3L converter increasing the output voltage from 12 to 24 V at 8 A, with a smaller *RC* filter on the setpoint signal.

This can cause the converter to "stall" as the limited charge of the flying capacitor cannot drive the inductor current to the current reference.

To prevent this, the converter should limit the switch interval duration to prevent the flying capacitor from overcharging/discharging. This can be achieved by forcing the converter to transition to the next state if the switch interval extends for too long. When this maximum switch interval logic takes control, the converter can operate like a fixed frequency switched capacitor converter at D_{crit}, or like a regular PCMC/VCMC scheme by continuously connecting V_{in} or *GND* to the switch node.

Fig. 7 shows an example case where the maximum interval timer needs to act. In this scenario, the system compensator gain was modified to illustrate the maximum interval logic operation more clearly. The converter is commanded to change V_{out} from 12 to 24 V at $T = 10\,\text{ms}$, which requires transitioning from one mode of operation to another. The inductor current rises slower than the current references and moves outside the current references, leading to an "unregulated" state where the inductor current is not directly manipulated by the current references, but instead is controlled by the maximum interval timer.

This is similar to the situation in a 2L PCMC converter when the compensator commands a sudden increase in inductor current and the current reference go very high; well beyond the current inductor current level. The switch duty-cycle goes to the maximum while the controller waits for the inductor current to "catch up" to the current references before it starts regulating again. For the 3L converter, the duty-cycle is limited by the current mode of operation rather than the maximum duty-cycle. During this time, the converter is expecting a peak compare

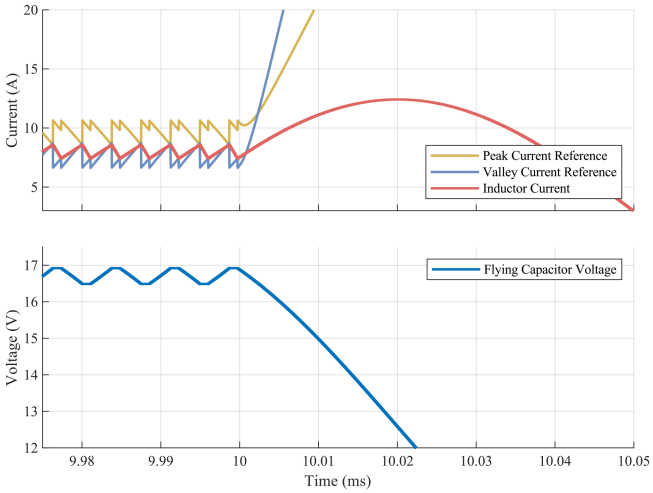


Fig. 8. Simulated 3L converter increasing the output voltage from 12 to 24 V at 8 A, without the maximum switch interval timer.

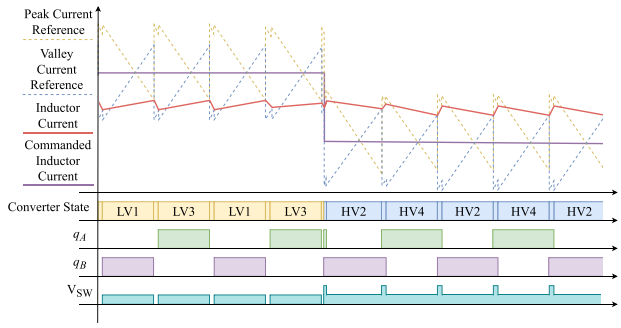


Fig. 9. 3L converter transition from $D < 0.5$ to $D > 0.5$ waveform.

event, but this will not occur in a reasonable time as the inductor current rises too slowly. While this might be allowable for a 2L converter as the input power source is assumed to be ideal, the limited charge of the flying capacitor prevents this. The maximum interval timer then activates at $T \approx 10.01\,\text{ms}$ and forces the converter to advance to the next state. In the new state, the converter expects a valley compare event, which is immediately processed since the valley current reference is above the inductor current. This cycle continues until the inductor current reaches the references, where normal regulation resumes.

At the start of the voltage step, the converter is operating with $D < 0.5$, so V_{sw} alternates between *GND* and $\frac{1}{2}V_{in}$ with a maximum duty-cycle of $50\,\%$. As V_{out} approaches $\frac{1}{2}V_{in}$, $|V_L|$ becomes smaller, and so $\frac{di_L}{dt}$ decreases causing the inductor current to level off. Once the converter changes mode of operation to $D > 0.5$ at $T \approx 10.06\,\text{ms}$, V_{sw} starts to alternate between V_{in} and $\frac{1}{2}V_{in}$. Here, the compensator wants to reduce the output current and reduces the commanded current, but when operating in $D > 0.5$, the minimum duty-cycle possible is $50\,\%$. After a few more switching cycles, the converter resumes normal regulation at $T \approx 10.1\,\text{ms}$. The current references suddenly shift down at $T \approx 10.06\,\text{ms}$ to prevent the inductor current from jumping when changing mode of operation, described in the next section, Section II-F.

While the compensator could be designed to prevent the current references moving faster than the inductor current, this would reduce the dynamic performance of the converter at all outputs. By implementing the maximum interval timer, the system bandwidth can be kept high while still allowing regulation during large voltage steps.

Fig. 8 shows the same scenario shown in Fig. 7 except the maximum interval timer is disabled during the voltage step command. Here, the current references increase significantly, leaving the inductor current behind. This means as V_{fc} decreases, V_{sw} also decreases, and eventually V_{fc} falls low enough that the resultant V_{sw} cannot drive the inductor current to the peak reference, stalling the converter; which is similar to the failure mode described in Section II-B.

The maximum interval timer simplifies the flying capacitor balancing during transients and helps narrow the electromagnetic compatibility design considerations as the converter's minimum frequency is restricted. The maximum interval timer should have a duration slightly longer than the interval calculated by (16), such that the timer only affects the operation of the converter during transients.

F. Inductor Current Reference Offset

As the duty-cycle of the converter changes, the inductor current will move within the hysteresis amplitude which can have some unexpected effects on the output of the converter when changing modes of operation. When the converter is operating near D_{crit}, the inductor current will remain higher or lower in the hysteresis band depending on the mode of operation the converter is in. This is caused by the ramps added to the current references and how they interact with the rising and falling inductor current slopes which with duty-cycle. For example, at $D \approx 0.49$ (high duty-cycle in the mode of operation $D < 0.5$), the inductor current would be located low in the hysteresis band because the inductor current rises slowly but falls quickly. At $D \approx 0.51$ the inductor current stays high in the hysteresis band, since the inductor current rises quickly but falls slowly. For ML converters with more levels, this pattern would repeat for every mode of operation.

When changing from one mode of operation to another (e.g., $D = 0.49$ to $D = 0.51$), the inductor current will want to suddenly jump from low to high in the hysteresis band. As a result, a disturbance can appear on the output as the output current is changed unexpectedly and the output compensator tries to bring the inductor current to the expected level. The compensator's output can be manipulated such that the inductor current does not need to jump when changing from one mode to another, preventing the unexpected change in output current. This can be achieved by offsetting the compensator output by the amplitude of the hysteresis; negatively when transitioning from a lower mode of operation to a higher one and vice versa. Fig. 9 shows an example of this transition when converter is changing mode of operation from $D = 0.49$ to $D = 0.51$, and so the inductor

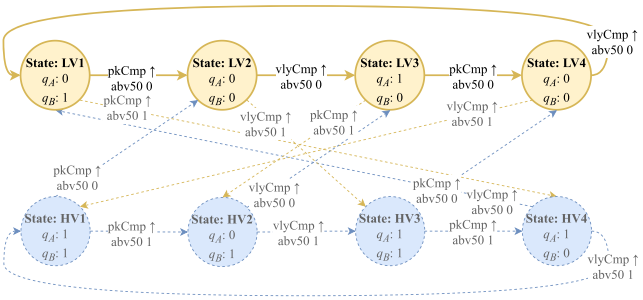


Fig. 10. HCMC state machine for a 3L converter, with $D < 0.5$ states highlighted.

current will want to move from low in the hysteresis band to high in the hysteresis band. When the converter changes mode of operation, the compensator is offset such that the inductor current level does not need to move to change, preventing the disturbance from appearing. In this implementation, the offset is always applied to the compensator output when the converter is operating $D > 0.5$.

III. Control System Modeling and Design

This section details the modeling and design of the control proposed scheme for a 36 V input, 1–30 V output, 16 A converter, taken as an example. To determine the transfer function of the system plant, the switching scheme of the control scheme needs to consider.

A. State Machine Model of HCMC

With four switches and a flying capacitor in the 3L buck, there are several switch states that need to be tracked. To ensure the correct switching order of the converter, a state machine with eight possible states is proposed: four for $D < 0.5$, and four for $D > 0.5$, where the switch states determine which switches should be ON or OFF. During steady-state operation the converter remains in one mode of operation, and so iterates through just one set of four states. The full state machine is shown in Fig. 10, with the steady-state transition order for $D < 0.5$ highlighted. When $D < 0.5$ the converter will iterate through the switch states $\ldots \rightarrow LV4 \rightarrow LV1 \rightarrow LV2 \rightarrow LV3 \rightarrow LV4 \rightarrow LV1 \rightarrow \ldots$ every time the correct compare event occurs. The other states shown describe the converter operating states at $D > 0.5$ and are labelled *HVn*. Table I shows the properties of the converter in each possible state for the 3L converter, where q_{compfc} is the control signal of the switches used to generate the inverting or noninverting flying capacitor compensator signal, and Q_{fc} is the charge of the flying capacitor.

The 3L HCMC state machine transitions from one state to another when one of three events occur: a peak compare, valley compare or maximum interval timer. For these state machines, the up-arrow symbol (↑) represents the rising edge of the signal, which is used to control when the state machine transitions between states. When the inductor current surpasses the peak current reference ($I_L > I_{pkref}$), the `pkCmp` signal goes high, and similarly when the inductor current falls below the valley current reference ($I_L < I_{vlyref}$) the `vlyCmp` signal goes high. Usually only the `pkCmp` or `vlyCmp` events cause the converter to change states but if the switch period becomes too long, the maximum interval timer will force the converter to change to the next state as if the appropriate `pkCmp` or `vlyCmp` event had occurred.

TABLE I
3L Converter State Characteristics

State	q_A	q_B	q_{compfc}	Q_{fc}	$\frac{dI_L}{dt}$	V_{SW}
LV1	0	1	1	Decr.	Incr.	$\frac{1}{2}V_{in}$
LV2	0	0	x	x	Decr.	0 V
LV3	1	0	0	Incr.	Incr.	$\frac{1}{2}V_{in}$
LV4	0	0	x	x	Decr.	0 V
HV1	1	1	x	x	Incr.	V_{in}
HV2	0	1	0	Decr.	Decr.	$\frac{1}{2}V_{in}$
HV3	1	1	x	x	Incr.	V_{in}
HV4	1	0	1	Incr.	Decr.	$\frac{1}{2}V_{in}$

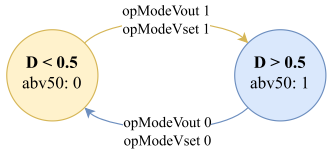


Fig. 11. Operation mode state machine.

When the state machine is about to transition to the next state, it checks if the mode of operation needs to be changed. This is controlled by the operation mode state machine shown in Fig. 11. It produces a logic signal `abv50`, which indicates if the converter should operate with a duty-cycle of $D < 0.5$ or $D > 0.5$. To minimize potential disturbances caused by an unexpected voltage across the inductor, the operation mode state machine is designed to only change when the converter is operating near D_{crit}. The operation mode state machine is controlled by two logic signals: output voltage threshold signal (`opModeVout`) and output voltage setpoint threshold signal (`opModeVset`). The `opModeVout` signal produces a logic high when $V_{out} > \frac{1}{2}V_{in}$, because for these output voltages $D > 0.5$. The signal `opModeVset` operates similarly, except it monitors the setpoint voltage (V_{set}) for $V_{set} > \frac{1}{2}V_{in}$. Using these two control signals, the operation mode state machine will only change `abv50` if both `opModeVout` and `opModeVset` are the same value, to prevent spurious mode switching.

The converter may need to change mode of operation at any time (due to a change in V_{set} or V_{in}), but this can break the relationship between the next expected compare event, the flying capacitor charge/discharge cycle and the inductor current slope direction if the state machine transitions to the wrong switch state. This is because while the flying capacitor voltage (V_{fc}) for

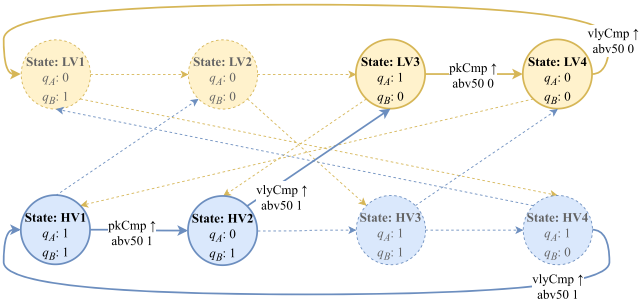


Fig. 12. HCMC state machine for a 3L converter transitioning from $D > 0.5$ to $D < 0.5$.

a 3L converter should be at $\frac{1}{2}V_{in}$, V_{out} could be anywhere between 0 V and V_{in} for WOV applications. Consequently during the capacitor charge/discharge states, the inductor current slope will be rising when operating below $D < 0.5$ but falling when operating $D > 0.5$. Since the proposed converter state machine depends on peak and valley compare events to determine when to switch, it is important that the PWM signals produce the correct inductor current slope direction during the switch states where the flying capacitor charges/discharges. This relationship is ensured by only transitioning to specific PWM states such that the next expected compare event and inductor current slope direction is preserved.

Fig. 12 shows an example transition from $D > 0.5$ to $D < 0.5$ where the converter transitions to a specific switch state to preserve the next expected `pkCmp` or `vlyCmp` event. In this example, at some point during *HV2* the `abv50` state is changed from 1 ($D > 0.5$) to 0 ($D < 0.5$) (e.g., due to V_{out} changing from 18 to 15 V). When the next valley compare event occurs, rather than moving to *HV3*, it transitions to *LV3* instead since this allows $D < 0.5$ and maintains the next expected compare event, which should be a peak compare event.

B. Converter Compensation

The input voltage used to test the prototype converter is 33.4 V, as this is the maximum output voltage of the upstream dc power source used for testing. Table II shows the components used in this prototype assuming operation at an ambient of 25 °C. By precharging the flying capacitor and utilizing active flying capacitor balancing the voltage across the switches can be kept at $\frac{1}{2}V_{in}$, allowing for lower voltage components to be used, improving the power density and efficiency. For this implementation, the components used are rated for more than the full input voltage to increase robustness and to accommodate experimentation. If the flying capacitor voltage deviates too much, the voltage across the switches will exceed $\frac{1}{2}V_{in}$, potentially causing damage.

The design of the voltage to current compensator control scheme is similar to a regular 2L buck converter under PCMC/VCMC since the inductor current is steered by the inductor current references, and so the inductor can be treated as a constant current source. The converter transfer function was estimated using the transfer function derived by Park et al. [21]

TABLE II
PROTOTYPE 3L CONVERTER COMPONENTS

Characteristic	Value
Input voltage	36 V Nom.
Output voltage	1 V to 30 V
Output current	0 A to 16 A
Inductor	10.8 µH, 2×EQ30, N97, 550 µm gap, 6 turns
Output capacitor	1×100 µF Alu-Elec + 3×10 µF MLCC
Flying capacitor	5×10 µF MLCC
MOSFETs	4×60 V, 2.8 mΩ
Hysteresis amplitude	4.5 A
Effective switching frequency	≈ 172 kHz to 258 kHz

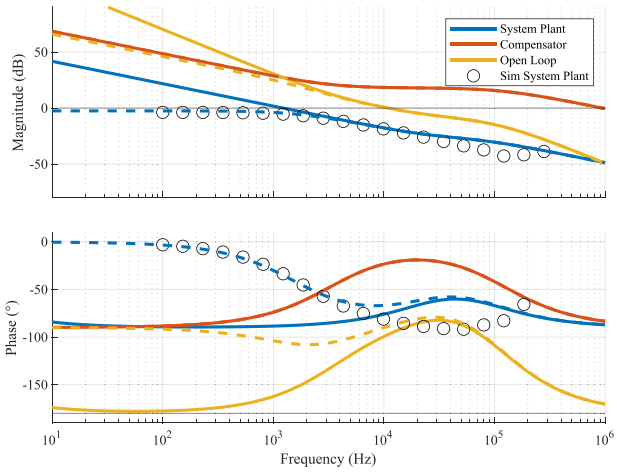


Fig. 13. Calculated frequency response of the 3L HCMC system plant, compensator, and the combined open-loop system. Light load response is shown with solid lines, while the full load response uses dashed lines.

of a 2L converter hysteretic converter. While this averaged PWM switch model does not account for the added ramps to the current references, it is a good starting point for designing the system compensator. The compensator was modeled assuming a 12 V output at both full load (16 A) and light load (10 mA).

Fig. 13 shows the frequency response of the calculated 3L HCMC converter transfer function. The converter plant, compensator, and combined open-loop system at light load and full load with solid and dashed lines, respectively. The frequency response of the system plant at full load was also extracted from simulation, with the simulation points shown with black circles. The simulation frequency response shows good agreement up to half the switching frequency, after which the phase begins to deviate. It was found that a Type-II compensator is suitable to compensate the converter and the method described in [22] was

applied in this case; although the gain of the compensator was adjusted to prevent oscillations when changing from one mode of operation to another, and to account for the WOV operation.

The transient response of CMC ML converters are generally worse compared to the 2L equivalents due to the lower voltage across the inductor, but this can be improved by modifying the switching order of the converter during transients [23]. Implementing a modified PWM scheme is outside the scope of this article but will be considered for future work.

The compensator offset scheme described in Section II-F needs to be implemented in a way transparent to the output compensator, which is achieved by adding the offset to the output of the compensator instead of the input. For an ML converter with more levels, this offset would need to be repeated every time the mode of operation changes.

When it comes to the voltage step performance of the converter, there is a tradeoff between maximizing the speed of the response and controlling the peak inductor current during the transient (in the case of a positive voltage step). As the bandwidth of the system is increased, the peak inductor current will also increase. This can have adverse effects on the performance of the converter, as the upstream power converter could become overloaded momentarily or the inductor becomes saturated. The voltage setpoint signal for the compensator in this implementation is filtered to reduce the speed of the converter during a voltage step while maintaining high performance during a load transient. In this implementation, the voltage setpoint signal is filtered by a $100\,\mathrm{nF}$ capacitor. The voltage setpoint is controlled by a $10\,\mathrm{k}\Omega$ potentiometer, so the exact *RC* time constant depends on the voltage setpoint.

C. Flying Capacitor Balancing

While the implementation of the active balanced flying capacitor is complex, the design of the flying capacitor compensator is much simpler as it can be compensated with just a proportional controller, although most designs implement a proportional and integral controller to eliminate steady-state error [9], [19], [24], [25]. Sensing the voltage across the capacitor can be difficult due to the significant changes in common mode voltage during the switching cycles. For most applications, the flying capacitor voltage signal can be filtered heavily without compromising the efficacy of the balancing circuit, removing the voltage spikes that the flying capacitor can produce from its equivalent series inductance.

The output of this compensator is applied to the current references to lengthen or shorten the flying capacitor cycles appropriately. To ensure the adjusted PWM waveforms maintain symmetry, a positive or negative offset needs to be applied to the inductor current waveform, depending on the type of correction required. This is implemented using an additional inverting opamp and high-speed analog multiplexer which is controlled by the signal q_{compfc}, connecting either the original compensator output or the inverted signal. For this implementation, there are two versions of the flying capacitor compensator output, one unmodified signal and the invert of the compensator. These two signals are then passed through a high-speed analog multiplexer,

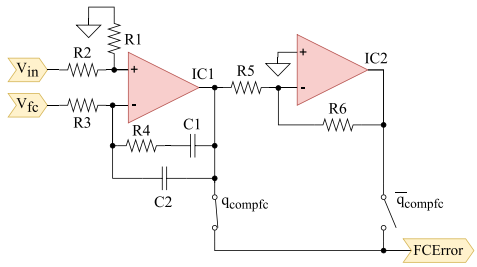


Fig. 14. Simplified diagram of the flying capacitor compensator and multiplexer.

which adds either the normal or inverted output of the flying capacitor compensator to the current reference ramps, depending on what the state machine requires.

Fig. 14 shows a simplified circuit diagram of this compensator and the analog multiplexer. The opamp *IC1* is the flying capacitor compensator, while *IC2* inverts this signal. This circuitry would be found in the "flying capacitor controller" block in Fig. 1. The switches q_{compfc} and $\overline{q}_{compfc}$ control if the inverted or noninverted control signal is added to the current references summing amplifier.

For this implementation, a PI compensator was implemented, with an additional pole to filter the switching noise produced by the converter (making the compensator equivalent to a Type II). The gain of the compensator was tuned to provide a high bandwidth without causing instability at higher loads [17], [19].

IV. Practical Implementation

The control scheme can be implemented with varying proportions of analog, digital, and discrete components. The state machine could be implemented using discrete flip-flops and analog components; low-cost FPGAs and complex programmable logic devices provide a more flexibility, speed, and density compared to their discrete counterparts.

Initially the STM32G474 microcontroller was used to manage all the mixed signal aspects using the built-in comparators, DACs, and ADCs, while the low-cost iCE40UL1K FPGA managed the PWM generation. However, the processing overhead when controlling the microcontroller peripherals prevented the converter from operating correctly around the critical duty-cycle, as the time to evaluate the compare events was longer than the minimum required switch interval. If the microcontroller had a sufficient number of FPGA, such as logic cells (akin to the dsPIC configurable logic cells), which were tightly integrated with the microcontroller peripherals, this likely would have been avoided.

To address this limitation, all the mixed signal logic managed by the microcontroller were replaced by discrete analog circuitry, while the digital logic blocks were transferred to the FPGA. Fig. 1 shows the function split of the control scheme between the digital and analog elements. The analog circuitry required a high bandwidth signal chain to properly reproduce the sawtooth ramp required for the inductor current references, particularly the sharp reset edges of the sawtooth which needs to

be as fast as possible to minimize the dead-band of the converter around D_{crit}.

The proposed solution uses the iCE40UL1K FPGA from Lattice Semiconductor to implement the digital logic of the converter startup, the state machine and PWM outputs; while the discrete analog circuitry will handle the compensation, current references, maximum interval timer and flying capacitor balancing.

A. Analog Circuitry

The main functions implemented is the analog circuitry include the converter output controller, ramp generator, current reference comparators, flying capacitor compensator and multiplexer, flying capacitor pre-charger, current reference generation, maximum interval timer, operation mode offset and comparators. This circuitry is composed of six comparators and 14 opamps, the majority of which are used for the current reference generation, since there are seven analog signals that are combined to produce the peak and valley current references. Due to the very fast reset of the current reference ramps, the opamps need to have high bandwidth and slew rates to prevent distortion of the sharp reset edge. The comparators used also need to be very fast to minimize the time to evaluate a compare event, maximizing the duty-cycle resolution of the converter. In this implementation, the comparators were level shifted to detect negative signals, but this reduced the signal drive strength and increased the time for the signals to settle, requiring the FPGA to "wait" longer after switching for the system to stabilize.

Since the control scheme relies on both the peak and valley of the inductor current, sensing the inductor current directly is required. While the inductor current peaks and valleys could be measured in different locations or inferred from other signals, the most direct method is the simplest in this case. The inductor current could be directly sensed using a hall-effect sensor, with an auxiliary sense winding on the inductor [26] but the use of a current sense resistor in series with the inductor current is the simplest and most robust solution, even if this produces slightly higher losses than the "lossless" solutions. The main consideration when sensing the inductor current directly is the high common-mode voltage at the sense resistor, the parasitic inductance of the sense resistor and the proximity to the noisy switch-node while also utilizing a high gain.

B. Digital Controls

The digital logic and state machines were implemented using the iCE40UL1k low-cost FPGA, which can operate at $84\,\mathrm{MHz}$ with a three clock-cycle ($\sim$ 36 ns) pipeline delay. The FPGA waits $\sim$ 80 ns after a compare event for the comparators and current ramps to stabilize before evaluating them again. This wait time could be reduced significantly by changing some of the components and circuitry to prioritize speed. The resource utilization of the FPGA is very low, at $\sim$ 10% of the look up tables available, although the majority of the 26 GPIO pins available are in use for controlling the converter and the analog circuitry. Four pins for the complimentary PWM signals, four for the timer/ramp reset/peak and valley compares, three for the operation mode logic, three for the flying capacitor, and four for reset/enable/precharge logic. The other pins on the FPGA are used for power, flash memory and debugging.

While a higher speed FPGA could be used instead of the iCE40UL1K device, the performance gains will be marginal for the significant increase in cost associated with higher end FPGAs; as the majority of FPGAs are segmented to provide significantly more logic cells compared to the increase in operational frequency. In this particular implementation, the settling times of the analog systems were the performance bottleneck rather than the FPGA clock frequency.

As shown in Fig. 1, the majority of the FPGA logic can be split into three logical blocks: one block handles the output of the comparators for processing and conditioning, another implements the state machines and the final block handles the PWM deadtime generation. The general operation of these digital blocks has been described in Section II.

C. Implementation Limitations

1) Duty-Cycle Range: In this control scheme the peak and valley compare events need to be evaluated quickly to maximize the output resolution of the converter, particularly when the converter is operating at the extremes of the modes of operation. At D_{crit} two compare events will occur simultaneously for one of the switch intervals assuming they can be evaluated instantaneously. In practicality, this is not possible as it takes time for the system to reset and stabilize before evaluating the next compare event. This minimum switch interval limits the duty-cycle of the converter, and since this can occur at $D = 0.5$ in the 3L converter, a duty-cycle deadband can occur around $D = 0.5$, leading to an output voltage deadband. This issue is very similar to the minimum and maximum duty-cycles of other converters

$$D_{deadband} = D_{crit} \pm \left(\left(\frac{T_{compare}}{T_{converter}} \right) \times 100\,\% \right) \tag{18}$$

The dead band can be calculated using (18) where $T_{compare}$ is the fastest time the state machine can detect two compare events back-to-back, and $T_{converter}$ is the full converter period length (T_c) when operating near D_{crit}. For the example implementation the FPGA operates at $84\,\mathrm{MHz}$ and can evaluate a compare event once per clock cycle leading to a deadband of $\pm$ 0.9% around D_{crit}. This means it cannot output a voltage between $\sim$ 16.4 and $\sim$ 17 V. The dead-band can be minimized by decreasing the time it takes to evaluate a compare event, or by reducing the switching frequency of the converter.

2) Changing Mode of Operation: The converter determines when to change mode of operation based on V_{set} and V_{out}. These thresholds are based on the idealized converter where there are no losses present which can cause issues when the converter is heavily loaded, and the losses are higher. As the output current increases, the difference between the duty-cycle calculated output voltage and the actual output voltage begins to increase. This can cause issues when attempting to change modes of operation as the output voltage of the converter might not reach the required. This can be alleviated by offsetting the

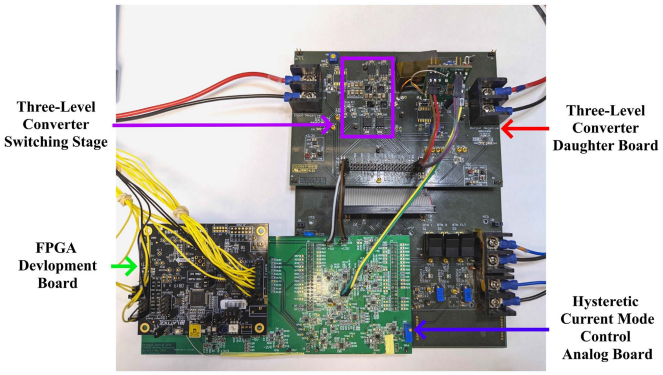


Fig. 15. Prototype converter daughtercard, controller card, and motherboard.

TABLE III
PROTOTYPE MEASURED PERFORMANCE: LOAD STEPS

Load Step	Deviation	Settling Time to 0.5%
25 % → 75 %, at 12 V	922 mV	179 µs
75 % → 25 %, at 12 V	934 mV	170 µs
25 % → 75 %, at 24 V	915 mV	635 µs
75 % → 25 %, at 24 V	1329 mV	206 µs

threshold to change mode proportional to the output current of the converter.

3) Inductor Current Sensing: Due to the offset required when changing modes of operation, the required resolution of the analog circuitry is increased

$$I_{sense_{max}} = I_{out_{max}} + (\Delta_{i_H} \times (N-2)) \quad (19)$$

$$I_{sense_{min}} = I_{out_{min}} - (\Delta_{i_H} \times (N-2)) \quad (20)$$

The minimum and maximum current sensing range required can be calculated using (19) and (20). The current sensing range required can be reduced by implementing a dynamic offset when changing mode of operation, but for this implementation only a fixed offset was implemented.

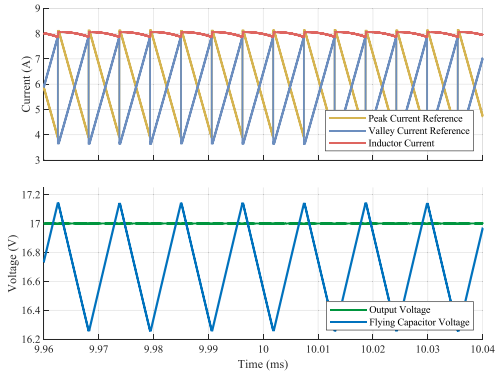
V. SIMULATED AND EXPERIMENTAL VERIFICATION

The control scheme and converter were implemented in Simulink using idealized components and a state machine. The converter design described in Section IV was then implemented in hardware with the parameters described in Table II. A prototype of the control scheme was implemented on a converter test platform, as seen in Fig. 15. The following scenarios were simulated and experimentally verified: 25 % → 75 % and 75 % → 25 % load steps at 12 and 24 V, voltage steps from 12 V → 24 V and 24 V → 12 V at 8 A. The measured results are shown in Tables III and IV, as well as Figs. 17–20.

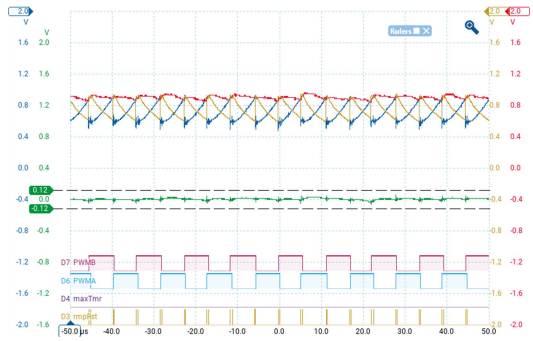
The measured and simulated results use the same color scheme: the red waveform is the inductor current signal, yellow the peak current reference signal, blue the valley current

TABLE IV
PROTOTYPE MEASURED PERFORMANCE: VOLTAGE STEPS

Voltage step	10%→90% / 90%→10% rise/fall times	10% / 90% to 0.5% settling time
12 V → 24 V	417 µs	553 µs
24 V → 12 V	129 µs	214 µs



(a)

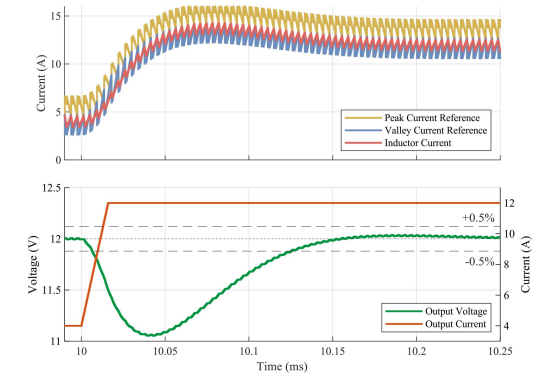


(b)

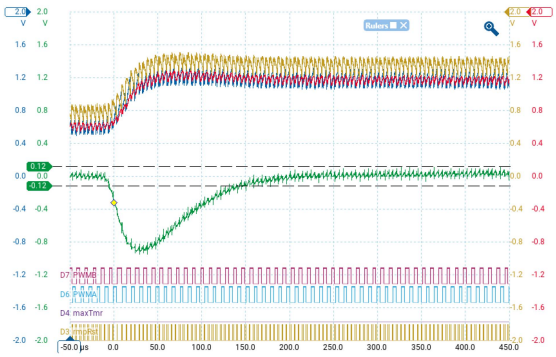
Fig. 16. Converter operating at $D \approx 0.51$. (a) Simulated. (b) Measured.

reference signal, and green the output voltage. The measured current waveforms are scaled to 73.6 mV/A (13.59 A/V) with a scale of 400 mV/div. The output voltage is ac coupled for Figs. 16–18 with a scale of 400 mV/div, while the output voltage is dc coupled and offset by −10 V for Figs. 19 and 20 with a scale of 4 V/div. All measured waveforms are filtered to 20 MHz.

Fig. 16 shows the converter operating near D_{crit}, highlighting the low output voltage ripple as the converter operates similarly to a switched capacitor converter. Fig. 16(b) shows the inductor current sometimes decreasing for three switch cycle and only rising momentarily for one switch interval, while Fig. 16(a) shows the inductor current rising and falling every switch interval. This is caused by the time it takes for the FPGA to analyze the `pkCmp` and `vlyCmp` signals before changing the PWM signals, which does not occur in the ideal simulation. This does not affect the operation of the converter except slightly increase

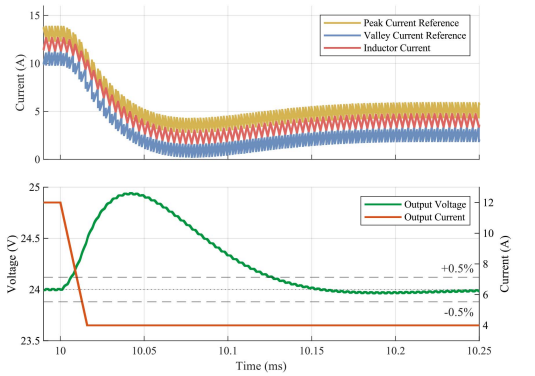


(a)

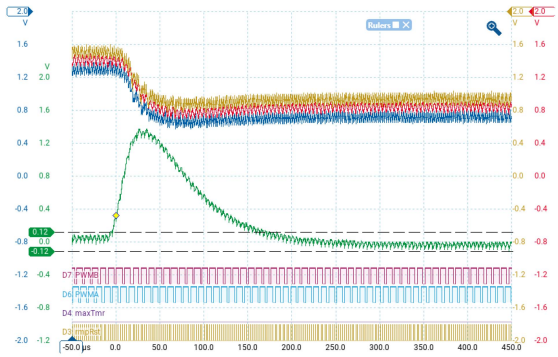


(b)

Fig. 17. 25 % → 75 % load step, 12 V output. (a) Simulated. (b) Measured.



(a)



(b)

Fig. 18. 75 % → 25 % load step, 24 V output. (a) Simulated. (b) Measured.

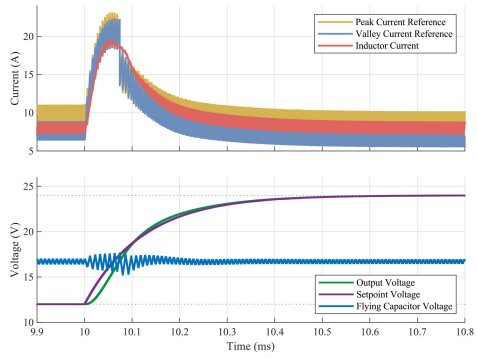
the output voltage ripple amplitude. As previously described in Section IV-C, this could be alleviated with faster digital and analog circuitry.

As can be seen in the load steps in Figs. 17 and 18, the converter has tight control over the inductor current, and so does not have issues controlling the output voltage. The ac coupled output voltage seen in Figs. 17(b) and 18(b) does not completely return to the nominal output voltage due to noise that couples to the output voltage sensing opamp, which causes an offset dependent on the load of the converter.

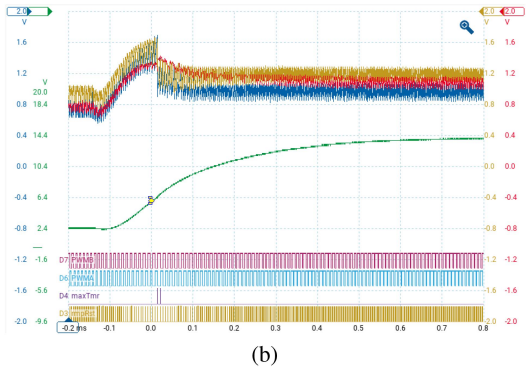
Figs. 19 and 20 shows the voltage steps, where the inductor current is tightly controlled until the converter approaches D_{crit} and changes mode of operation. At this point of the transient, the inductor cannot be driven fast enough to the current references, and so it "detaches" from the current references. The maximum interval timer takes over to ensure the flying capacitor voltage does not deviate too much. Once the inductor current reaches the current references again, returns to normal regulation. The step response of the converter is dominated by the *RC* filter on the voltage setpoint signal to prevent the converter from producing significant swings when quickly stepping from one voltage to another, which is detailed in Section III-B.

A. Comparison With Other Control Schemes

This control scheme offers some benefits over other control schemes, which is compared in Table V. The scalability of these

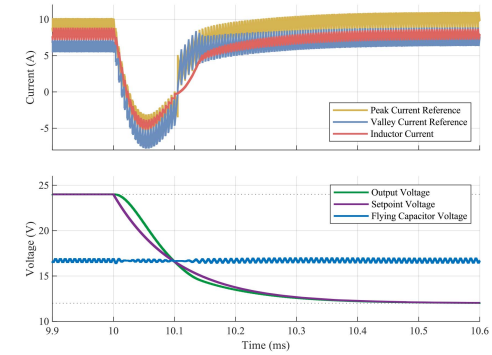


(a)

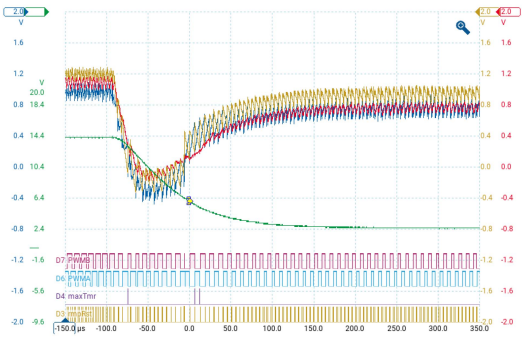


(b)

Fig. 19. 12 V → 24 V voltage step, 8 A output. (a) Simulated. (b) Measured.



(a)



(b)

Fig. 20. 24 V → 12 V voltage step, 8 A output. (a) Simulated. (b) Measured.

TABLE V
CONTROL SCHEME COMPARISON

Control scheme	PCMC	VCMC	Low ripple	WOV	V_{out} step tested
Peak / valley CMC [7]	$D <$ 0.52	$D >$ 0.48	✗	✓	✗
PWM mode control [8]	✗	✗	✗	✓	Voltage Ramp
Minimum deviation CMC [15]	Indirect	Indirect	✓	Not discussed	✗
This work	Always	Always	✓	✓	✓

control schemes would be similar, with the PWM mode control scheme again being the simplest to expand to operate with more levels. The other control schemes would not require significant additional hardware, but the software/firmware would require significant effort to correctly encode all the different modes of operation and switch states.

Generally, the control scheme described in this work offers a more comprehensive set of features that keeps many of the ML converter benefits while also providing a very robust output regulation that can be used with many different load types and in a variety of situations. The main benefits of this control scheme over the existing solutions is the ability to limit both the peak and valley of the inductor current while still allowing low ripple and high efficiency operation. These additional benefits come with added complexity in the control scheme implementation.

VI. CONCLUSION

This article presents an HCMC scheme that provides cycle-by-cycle CMC over a wide range of outputs for ML converters. This is achieved with a PWM state machine, operation mode logic, current reference ramp generator, a maximum interval timer, and a flying capacitor offset generator. This scheme has been shown to have minimal disturbances on the output or impact the control of the converter when changing operating modes. This control scheme also allows operation at certain critical duty-cycles when the converter is at its most efficient. The control scheme was simulated in Simulink then verified experimentally in a variety of scenarios using a 300 W, 36 V input, 1–30 V, 16 A output prototype. The control scheme implemented using discrete analog circuitry and a low-cost FPGA.

While this control scheme could be easily expanded upon to work with an *N*-level converter, the complexity increases greatly as the number of switches and flying capacitors would require a state machine that can track $2(N-1)^2$ switch states.

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