Digital Implementation of Discontinuous PWMs: Mitigating Parasitic Active Vectors for Improved Load Current Quality in Inverter Systems

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***Abstract*—Discontinuous PWM (DPWM) strategies are widely used in voltage-source inverters (VSIs) due to reduced switching losses and improved harmonic performance at higher modulation indexes. However, DPWMs with discontinuous zero-sequence signals (ZSS) can cause current spikes at clamping instants, which depend on the modulation index and load parameters. In the literature, this behavior is often attributed to the rapid changes in ZSS. This article demonstrates that the current spikes are primarily caused by improper modulator implementation on digital signal processors (DSPs), which introduces an unintended active vector instead of a zero vector at the end of a positive bus clamp for a given phase. The issue arises because PWM modules operate as set-reset units based on a timer and compare values, unlike analog comparators, which react instantaneously. We propose a simple solution using an auxiliary compare register, which is effective for most DSPs. The solution's effectiveness is demonstrated on a VSI-fed 12-kW induction machine controlled by a C2000 Texas Instruments DSP.**

***Index Terms*—Current spikes, digital implementation, discontinuous PWM, inverters.**

I. Introduction

In THE context of voltage-source inverters (VSIs), discontinuous PWM (DPWM) strategies are a viable alternative to continuous PWMs (CPWM), primarily represented by space vector modulation PWM (SVPWM). Due to their bus clamping features, DPWMs can reduce switching losses by approximately one-third compared to CPWMs at the same carrier frequency, and in specific situations, reductions approaching 50% can be achieved [1], [2], [3], [4]. In addition, DPWMs exhibit better harmonic performance in terms of the harmonic distortion factor (HDF) at higher modulation indexes compared to SVPWM [1], [2], [3], [5]. The most straightforward and most efficient implementation of DPWM strategies involves reference signal modification, where reference voltages are modified by a zero-sequence signal (ZSS) calculated from instantaneous voltage values and compared with a triangular carrier signal [6], [7], which is also the approach used in this article.

The most recognized DPWM types among scholars and engineers are DPWMMAX, DPWMMIN, and DPWM0–3 [3], [5]. DPWMMAX and DPWMMIN have the disadvantage of uneven thermal stress on high-side (HS) and low-side (LS) switches, but their ZSS is continuous [2], [5]. DPWM0–2, a particular case of generalized DPWM (GDPWM) proposed in [1], exhibit a 60° phase symmetrical and alternating (with respect to positive and negative dc rail) clamp. They differ by the start of the clamping instant and offer even semiconductor thermal stress [1], [2]. However, their ZSS is discontinuous, with lower modulation indexes increasing the discontinuity. DPWM3, with a 30° clamp duration, also has ZSS discontinuity but offers the best harmonic performance concerning the HDF [2]. Depenbrock's DPWM1 then exhibits the best behavior concerning dead-time distortion [3].

The discontinuity in ZSS of DPWMs presents a challenge in their digital implementation on digital signal processors (DSPs). PWM units in DSPs use an up-down counter as the carrier signal and compare registers containing samples of the reference voltage as the modulating signal. These PWM units do not react instantaneously but function as set–reset logical circuits, causing issues when the modulating signal is discontinuous. The problem arises at the end of a positive clamp of a given phase. Ideally, the control signal for the HS and LS switch should be driven low and high, respectively, immediately at the end of the clamp, i.e., at the start of the following PWM period. However, due to the logic of the PWM unit, the respective phase remains clamped for up to half of the following PWM period, depending on the next period duty cycle (i.e., modulation index), introducing an unwanted active voltage vector. This unwanted vector causes current spikes and oscillations dependent on the modulation index and load parameters. The lower the modulation index and the lower the inductances and resistances of the load, the worse the overshoots.

In the literature, it is believed that the current imperfections (visible, for instance, on the current waveforms in [7], [8], [9], and [10]) are caused by the abrupt change in ZSS charging the parasitic capacitances [11], [12], [13], [14]. Although common mode voltage in DPWMs poses a threat to power systems,

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as analyzed in [15], [16], and [17], it is not the root cause of the rapid current changes. The papers try to mitigate the parasitic currents by limiting the slew rate of the clamping signal [11], [12], [13], [14], [18], [19]. However, this solution only suppresses the problem and does not account for the fact that there is a principal error in the digital implementation of the modulator.

This article demonstrates that the above described phenomenon can be effectively mitigated by employing an additional compare register to force the respective logic level at the end of the clamp. The problem is first theoretically analyzed, and it is shown that its origin is the combination of the discontinuity in the modulating signal (the term "discontinuity" refers here to the mathematical concept, not the clamping feature) and the behavior of the PWM unit at the end of a positive clamp. The analysis also shows that only three of the six active VSI vectors appear as parasitic vectors. Furthermore, the duration of the parasitic active vector is mathematically quantified, and it is shown that it is the same for DPWM1 and DPWM3 but differs in the case of the GDPWM.

The problem mentioned above and the proposed solution, i.e., the usage of an auxiliary compare register, are experimentally validated on a VSI-fed induction machine (IM) controlled by TMDSCNCD28P65X controlCARD evaluation module from Texas Instruments (TI) programmed in C. The IM operates in open V/Hz and closed-loop field-oriented control (FOC). The reason is to demonstrate that the current waveforms differ when the load current is directly regulated. In the case of closed-loop control, the current controllers try to suppress the current spikes, which introduces overshoots into the reference d- and q-axis voltage and may lead to control loop instabilities. Also, the results demonstrate the influence of the switching frequency since the lower it is, the longer the duration of the parasitic active vector and the higher the current spike.

However, it is important to note that the electric drive is chosen as a convenient example for the problem demonstration. The adverse effect of the parasitic active vector on the current response will vary depending on the load parameters, but the phenomenon itself will persist regardless of the specific system connected to the inverter.

The main subject of interest is the behavior of DPWM1 and DPWM3 algorithms. The results also show the influence of the phase shift in the GDPWM case and the seamless behavior of DPWMMAX and SVPWM for comparison. In summary, the contributions and merits of this article are summarized as follows.

1) The article re-examines the assumption that current spikes in DPWM strategies are primarily caused by the rapid change of the ZSS. It shows that the leading cause is the implementation of DPWM on DSPs, which leads to parasitic active vectors at the end of positive clamps.
2) The article offers a detailed examination of how parasitic vectors form in DPWM operations, including a mathematical quantification of their duration. This analysis reveals the types of vectors that appear across different DPWM strategies. It is demonstrated that DPWMs with continuous modulating signals do not pose a threat.
3) A simple yet effective solution using an auxiliary compare register is presented to mitigate the formation of parasitic active vectors, improving load current quality. This approach ensures correct phase reset during clamping transitions in most DSPs.
4) The proposed solution is experimentally validated on a VSI-fed 12-kW induction machine using both open-loop V/Hz and closed-loop FOC. The results demonstrate the elimination of current (and voltage, in the case of FOC) spikes and improved current waveforms with the proposed fix.
5) The findings and solutions presented in this article apply to various industrial and traction inverter systems. The simplicity of the proposed solution makes it suitable for immediate adoption in existing systems with no HW and minimal SW changes.

This article is organized as follows. Section II provides a detailed description of the challenges associated with the digital implementation of DPWM strategies on DSPs, focusing on the issue of parasitic active vectors. Section III presents a deeper analysis of the parasitic active vectors and their duration, along with our proposed solution that leverages DSP auxiliary compare registers. Section IV presents the experimental validation, comparing the results of the proposed solution with conventional approaches using both open-loop and closed-loop control of an IM drive. Finally, the conclusion summarizes the article's key contributions, insights, and results.

II. Problem Description

This article defines the modulation index m as

$$m = \frac{\sqrt{3}v^*}{V_{\mathrm{DC}}} \tag{1}$$

where v^* denotes the reference voltage vector magnitude and V_{DC} is the dc-bus voltage. According to this definition, $m = 1$ corresponds to the maximum voltage in a linear modulation mode, i.e., to the inscribed circle of the voltage hexagon. However, it is important to note that other definitions of the modulation index are also possible.

The reference modulating signal, along with the ZSS for DPWM1, DPWM3, DPWMMAX, and SVPWM, which are the main modulations studied in this article, are depicted in Fig. 1. The low value of m was purposefully chosen to highlight the significant change in the duty cycle at both the beginning and end of each clamp for DPWM1 and DPWM3 and the discontinuous nature of their signal. This change translates into a substantial difference in the compare values between the two consecutive switching periods.

A symmetric up-down counter is assumed, as it is the most commonly used timer configuration in motor drives. Therefore, the pulses are centered around the top/bottom of the counter. Although the following analysis is done for the latter case, i.e., pulses are centered around the bottom of the counter, the conclusions drawn are valid for both cases. Concerning the compare register update, we consider the so-called regularly

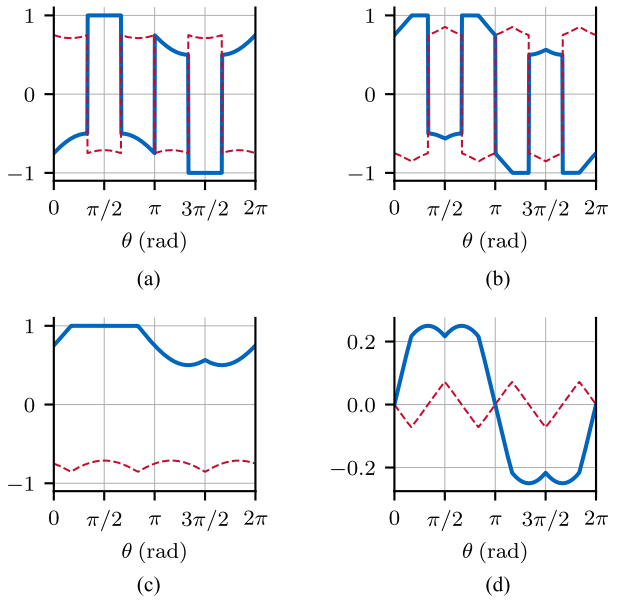

Fig. 1. Modulating signals for $m = 0.25$ – solid blue: phase "a" voltage reference, dashed red: ZSS. (a) DPWM1. (b) DWPM3. (c) DPWMMAX. (d) SVPWM.

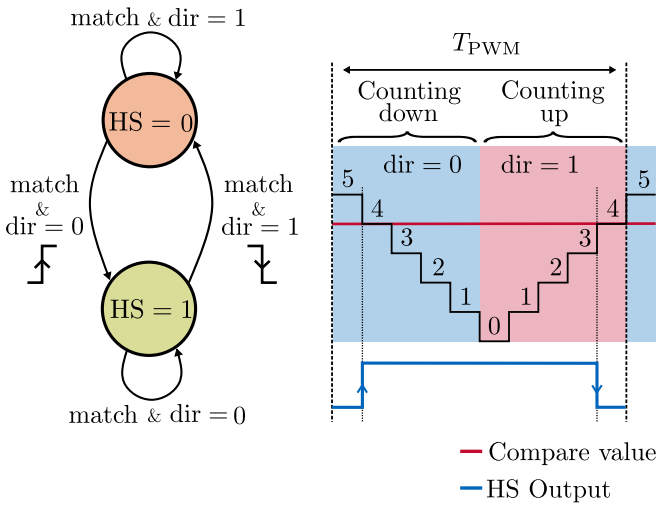

Fig. 2. Operating principle of a symmetric up-down PWM counter. Variable HS represents the state of the corresponding HS PWM output, and "match" signifies that the counter value equals the compare register value.

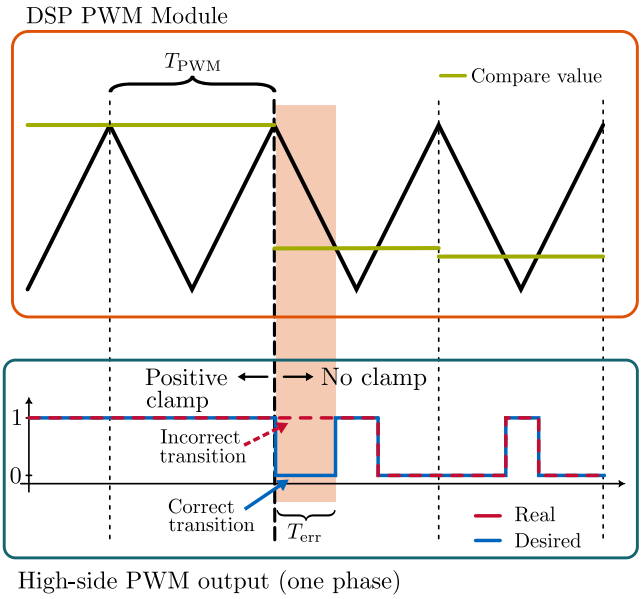

Fig. 3. Creation principle of a parasitic voltage vector at the end of a positive clamp.

sampled PWM with the compare value update at the top of the PWM counter.

In controlling two-level inverters, the HS and LS switches in each leg operate complementarily—when the HS switch is ON, the LS switch is OFF, and vice versa. Deadtime is inserted between switching events, typically by delaying the rising edge of the control signal for the respective switch. As a result, each inverter leg can be represented by a single binary switching variable: 1 for HS being ON and LS OFF and 0 for HS being OFF and LS ON.

When the pulses are centered around the counter bottom, a match between the counter and compare register during counting down means the switching variable is set, and a match during counting up means it is cleared. The PWM module then, in principle, works as a simple state machine performing set and reset of the control variable. The behavior is illustrated in Fig. 2.

Using a symmetric up-down counter imposes an implicit assumption that the output is set to "low" at the start of each sampling period to generate the desired pulse pattern properly. However, suppose the particular phase was clamped during the previous switching period due to the set–reset behavior of the PWM logic. In that case, the subsequent switching period starts with the output set to "high" instead of "low," causing a parasitic active voltage vector to appear at the inverter output as seen in Fig. 3, which shows the transition from positive clamp to modulation for one inverter leg and DPWM1 chosen as a reference for the following analysis. In addition, the bottom part of Fig. 4 (which will be described in more detail in the following section) demonstrates this phenomenon by showcasing the HS DSP PWM signals at the end of the positive clamp of phase "a."

In other words, when an action on the output pin is configured to happen when the match occurs during the upcount, it cannot take effect when the timer is at its top since, in most DSPs, the top is defined as "counting down." Similarly, when an action on the output pin is configured to happen when the match occurs during the downcount, it cannot take effect when the timer is at the bottom since the bottom is defined as "counting up." This behavior is also illustrated in Fig. 2.

Therefore, it is impossible to achieve the correct modulator behavior using a single compare register, and the creation of the parasitic active vector at the end of the positive clamp becomes inevitable. The duration of the parasitic vector is denoted as T_{err}. It will be later shown that the duration is contingent upon the modulating index and the phase shift corresponding to the end of the clamp. Also, $0 < T_{\text{err}} < T_{\text{PWM}}/2$.

On the contrary, no such issue arises when the transition from negative clamp to modulation is considered, as evident from

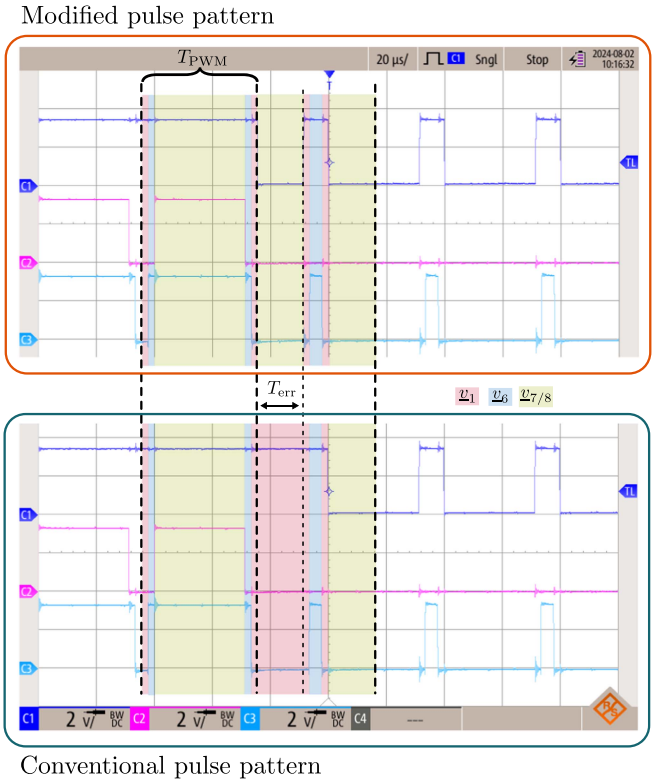

Fig. 4. Parasitic active vector formation ($m = 0.25$). DSP control signals for HS switches: phase "a" (C1), phase "b" (C2), and phase "c" (C3). Colored areas: red – voltage vector $\underline{v}_1$ ("100"); blue – voltage vector $\underline{v}_6$ ("101"); green – voltage vector $\underline{v}_{0/7}$ ("000"/"111").

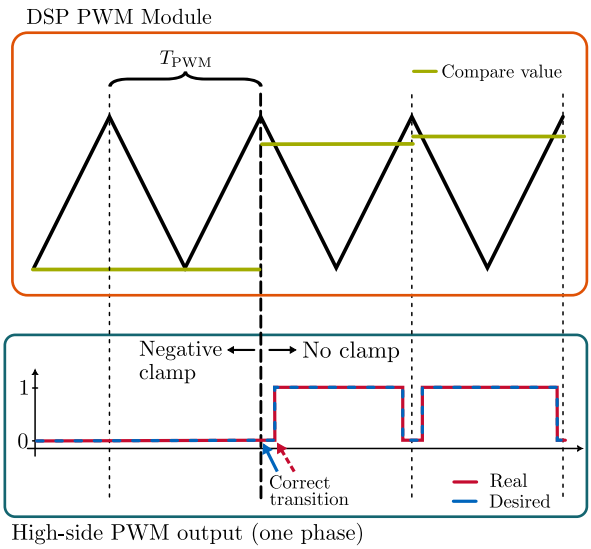

Fig. 5. Detailed transition from negative clamp to modulation.

Figs. 5 and 6. This is because at the start of the subsequent switching period, after the negative clamp, the output is already correctly set to "low"; therefore, the pulse pattern is not distorted.

Consequently, there is one critical transition per phase and fundamental cycle when the respective phase transitions from positive clamp to modulation. An incorrect active vector is applied to the load during each critical transition, causing a

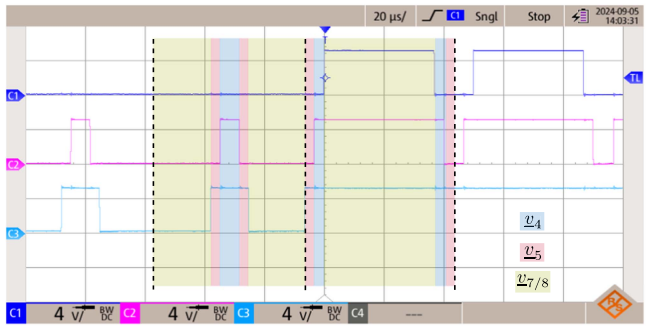

Fig. 6. End of a negative clamp ($m = 0.25$). DSP control signals for HS switches: phase "a" (C1), phase "b" (C2), and phase "c" (C3). Colored areas: blue–voltage vector $\underline{v}_4$ ("011"); red–voltage vector $\underline{v}_5$ ("001"); green–voltage vector $\underline{v}_{0/7}$ ("000"/"111").

current spike. The spike is the largest in the phase where the critical transition occurs. However, due to the mutual connection of the winding, the current transient also appears in the other two phases, albeit with half the magnitude. Due to the 120° phase shift between the phases, the current transients are distributed in such a way that might lead to the incorrect assumption that the step-like nature of the common-mode voltage exciting the parasitic capacitances of the machine is causing the current spikes.

It is important to emphasize that the observed issue originates solely from the intrinsic operation of the DSP's PWM module, as described above. While high-resolution PWM features enhance the resolution of the timer and compare registers, they do not alter the fundamental set–reset logic of the module. In addition, although this article employs a carrier-based implementation with reference signal modification, the conclusions remain equally valid for the space-vector-based approach, as both methods are equivalent. Parameters such as PWM and carrier synchronization (synchronous versus asynchronous PWM) or the carrier-to-fundamental frequency ratio also do not impact the described behavior, as the problem is inherent to the PWM module architecture.

III. Parasitic Vector Analysis

Fig. 4 shows the output DSP signals for the HS switches within DPWM1 at the end of the positive clamp of phase "a." The control signals for LS switches are complementary. The deadtime is set to 160 ns. The signals were measured at the output of our DSP control board equipped with a TMDSCNCD28P65X control card for an open-loop voltage reference with $m = 0.25$, fundamental frequency 50 Hz, and PWM frequency 20 kHz. The same control board is later used for the experimental verification. The bottom part of Fig. 4 corresponds to the conventional pulse pattern, and the top part shows a modified pulse pattern with the proposed solution, which will be described in detail later.

In the conventional DSP-implemented DPWM1 pattern, it can be seen that the positive clamp erroneously persists into the next period, introducing a parasitic active vector. In other words, instead of the desired zero vector marked in green in the

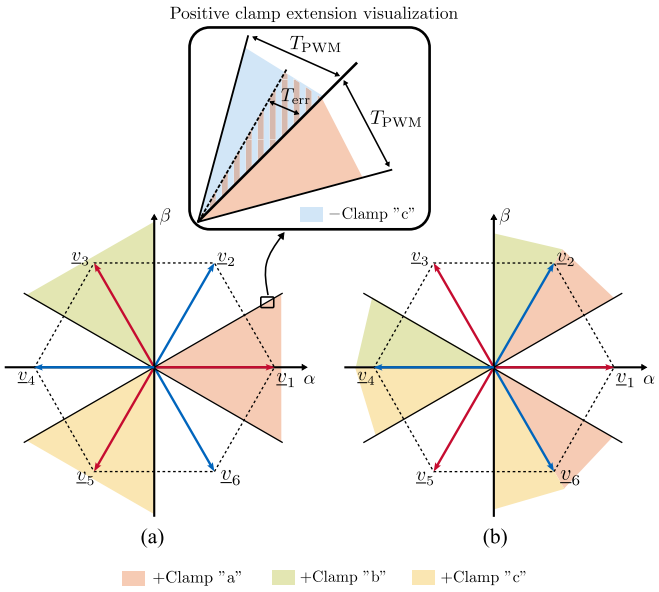

Fig. 7. Graphical depiction of the parasitic active voltage vectors, denoted in red, generated during one fundamental cycle along with the positive clamping instants of (a) DPWM1 and (b) DPWM3.

top part of the figure, an active vector $\underline{v}_1$ corresponding to the switching combination "100," marked in red in the bottom part of the figure, is introduced. The duration of this parasitic active vector is then proportional to the modulation index.

To completely fix this issue, we must modify the switching pattern following the top part of Fig. 4 by resetting the output of the PWM phase "a." Papers that reduce the slew rate of the ZSS only suppress this issue by lowering the duration of the parasitic active vector, gradually changing the duty cycle from maximum to the target value.

Fig. 6 shows the situation for the end of the negative clamp for phase "a" and the beginning of the positive clamp for phase "c." Here, the problem is not present since, initially, the timers are reset, i.e., zero vector "000" is present. Then, in the first period of the positive clamp, the control signal for phase "c" is correctly set at the beginning of the period.

By performing the parasitic vector analysis for DPWM1 and DPWM3, it can be concluded that they consist of $\underline{v}_1$ in the case of the phase "a" clamp, $\underline{v}_3$ in the case of the phase "b" clamp, and $\underline{v}_5$ in the case of the phase "c" clamp, respectively. The situation is depicted in Fig. 7. The figure also shows the positive clamping instants of DPWM1 and DPWM3. Furthermore, the top part of Fig. 7 highlights the formation of the parasitic vector at the end of the positive clamp of phase "a," assuming counterclockwise rotation of the reference voltage vector. Ideally, when the output voltage vector trajectory crosses the midpoint of the sector, the positive clamp on phase "a" is removed and followed by the negative clamp of phase "c." However, due to the phenomenon presented in Figs. 3 and 4, the positive clamp of phase "a" persists for up to $T_{\mathrm{PWM}}/2$ longer, causing it to overlap with the negative clamp of phase "c." The overlap manifests as the parasitic active vector at the output of the inverter. Concerning GDPWM, the clamp duration agrees with DPWM1 as it is its particular

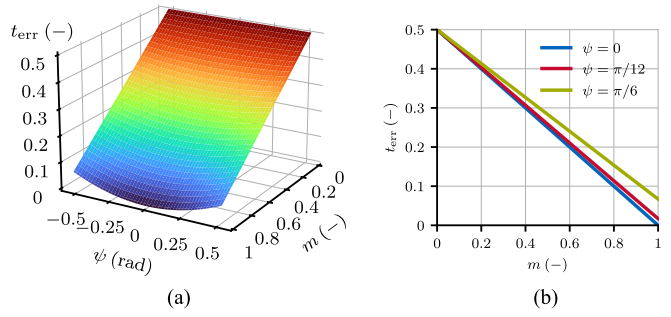

Fig. 8. Relative time of the parasitic vector. (a) Entire GDPWM range. (b) Specific cross-sections for selected phase shifts.

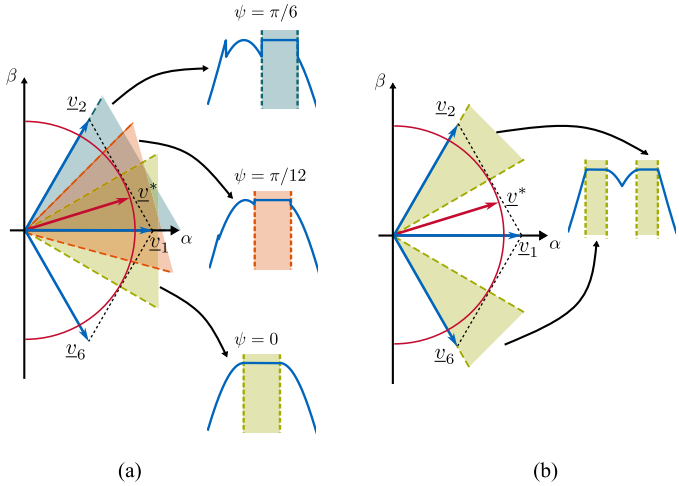

Fig. 9. Visualization of clamping instances within the positive half-cycle of phase "a" for (a) GDPWM and (b) DPWM3.

case but can be shifted up to $\pm\pi/6$ (shown later in Fig. 9). The parasitic vector types remain the same.

A. Duration of Parasitic Vector

To determine the duration of the parasitic voltage vector for discontinuous modulation strategies, the modulating signal values immediately after transitioning from the clamping state to modulation must be evaluated. This value (indicated by the green line in Fig. 3) is then compared with the up-down counter (depicted by the black line in Fig. 3) to establish the duration of the parasitic voltage vector. The mathematical expressions for the modulating signals are detailed in [2].

For simplicity, we assume that the value loaded into the DSP's compare register corresponds precisely to the modulation signal value immediately after the positive clamp. Here, sampling errors of the modulation signal and quantization effects of the counter are neglected. As a result, the counter waveform is approximated by straight lines, with direction changes determined by whether the counter is counting up or down.

To derive T_{err}, which directly equals the duration of the parasitic active vector, it is useful to rescale both the modulating signal and the counter range to span from 0 to 1. For DPWM3, the value of the modulating signal after the positive clamp is equal to m. The duration T_{err} can then be determined by solving the

following equation, which represents the intersection between the counter's downcount (right-hand side of the equation) and the modulating signal value after the positive clamp (left-hand side of the equation):

$$m = 1 - \frac{2}{T_{\text{PWM}}} T_{\text{err}} \tag{2}$$

where T_{PWM} is the period of the up-down counter. Solving (2) for T_{err} yields

$$T_{\text{err}} = \frac{T_{\text{PWM}}}{2}(1 - m). \tag{3}$$

Since DPWM1 is a specific case of GDPWM, where the clamped area is centered around the maximum of the reference voltage, it suffices to derive T_{err} for GDPWM. Like DPWM3, the modulating signal value must be evaluated after the positive clamp. This value depends on the modulation index and the phase shift ψ, which determines the position of the clamped area relative to the maximum reference voltage. The modulation signal value after the positive clamp is $m\cos(\psi)$, while the counter's mathematical expression remains the same as on the right-hand side of (2). Therefore, the equation for determining T_{err} becomes

$$m\cos(\psi) = 1 - \frac{2}{T_{\text{PWM}}} T_{\text{err}} \tag{4}$$

and the solution is

$$T_{\text{err}} = \frac{T_{\text{PWM}}}{2}(1 - m\cos(\psi)). \tag{5}$$

For $\psi = 0$, the modulating signal of GDPWM corresponds to that of DPWM1.

Therefore, the duration of the parasitic vector is directly proportional to the switching period T_{PWM}. The relative time of the parasitic vector $t_{\text{err}} = T_{\text{err}}/T_{\text{PWM}}$ for GDPWM is illustrated in Fig. 8. Fig. 8(a) graphically shows the dependence given by (5), while Fig. 8(b) shows specific cross-sections corresponding to different GDPWM phase shifts. This analysis demonstrates that the parasitic active vector duration is identical for DPWM1 and DPWM3, while for GDPWM, it depends on the phase shift, reaching its maximum at $\psi = \pm\pi/6$.

Fig. 9 illustrates the clamping instances within the positive half-cycle of phase "a" for GDPWM and DPWM3. GDPWM is shown with various phase shifts ψ, including DPWM1 when $\psi = 0$. The figure highlights the areas where positive clamping instants occur.

For DPWM1 and DPWM3, the positive clamp ends when the reference vector's trajectory touches the hexagon boundary. At this point, the zero vector duration in the subsequent PWM period is nearly zero, meaning the modulation index m directly corresponds to the duty cycle of phase "a" (or the zero vector duration, respectively) after the positive clamp. This graphically supports the mathematical basis of (3) in defining the parasitic vector duration.

In Fig. 9, the areas of the positive clamp are marked by colored triangles. GDPWM introduces a phase shift ψ in the clamping instants, altering the clamp position in the complex plane. Fig. 9 shows the clamp positions for $\psi = 0$ (DPWM1), $\psi = \pi/12$, and $\psi = \pi/6$ (maximum positive phase shift).

When $\psi > 0$, the positive clamp ends when the voltage vector trajectory is further from the hexagon boundary, i.e., in a nonzero voltage vector region. This explains the dependence of parasitic vector duration on the clamp's phase shift, as described in (5), and shows that increasing ψ toward $\pm\pi/6$ prolongs the parasitic vector duration.

Algorithm 1: Pulse Pattern Correction for GDPWM (phase "a").

Require: x_k, x_{k-1}, v_a, CMPB $\leftarrow$ TMR_MAX
1: Determine $x_k \in \{a, b, c\}$ as the phase with the highest absolute value of the phase-shifted reference voltage by ψ
2: **if** $x_{k-1} == a$ **and** $x_{k-1} \neq x_k$ **and** $v_a > 0$ **then**
3: CBD $\leftarrow 1$
4: **else**
5: CBD $\leftarrow 0$
6: **end if**
7: $x_{k-1} \leftarrow x_k$

Algorithm 2: Pulse Pattern Correction for DPWM3 (phase "a").

Require: x_k, x_{k-1}, v_a, CMPB $\leftarrow$ TMR_MAX
1: Determine $x_k \in \{a, b, c\}$ as the phase with the highest absolute value of the reference voltage
2: **if** $x_k == a$ **and** $x_{k-1} \neq x_k$ **and** $v_a > 0$ **then**
3: CBD $\leftarrow 1$
4: **else**
5: CBD $\leftarrow 0$
6: **end if**
7: $x_{k-1} \leftarrow x_k$

B. Proposed Solution

A straightforward solution can address the issue mentioned above. The end of a positive clamp must be tracked for each phase. Upon detection, the PWM channel of the affected phase is reconfigured to reset its output to "low" at the start of the next switching period. Subsequently, this reset mechanism is disabled for the rest of the fundamental cycle to prevent distortion of the pulse pattern.

This paper proposes utilizing a second compare register loaded with the PWM timer's peak value. The PWM channel is configured to set the output "low" when the timer value matches the second compare register during the downcount. The procedure for GDPWM is summarized in Algorithm 1.

Since DPWM1 is a specific case of GDPWM with a phase angle $\psi = 0$, the algorithm remains identical. For DPWM3, the algorithm slightly differs, as shown in Algorithm 2.

In these algorithms, "CMPB" denotes the auxiliary compare register. At the same time, "CBD" specifies the required action on the PWM output when the timer matches the "CMPB" register (CBD $= 1$ indicates clearing the output on a downcount

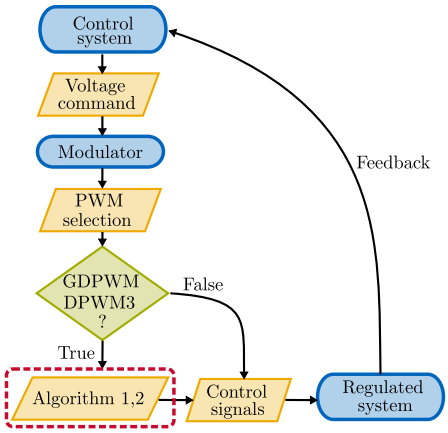

Fig. 10. High-level flowchart depicting the incorporation of the proposed pulse pattern correction into the control system.

match, while CBD $= 0$ means no action is taken). This approach assumes pulses are centered around the bottom of the timer. In addition, the incorporation of the proposed solution into the inverter control algorithm on a system level is illustrated by means of a flowchart in Fig. 10.

Although the solution described focuses on C2000 processors, the underlying principle can be adapted to other DSP platforms. Minor implementation adjustments may be required to accommodate platform-specific PWM module architectures. The merit of the mentioned solution is that the implementation involves only a few conditional statements, resulting in an execution overhead of approximately 300 ns on the DSP used in the experimental section (optimization level set to "Level 3—Interprocedural Optimization").

Concerning the comparison with the rate-limiting techniques, while they can smoothen the transitions in the DPWM signal and duty cycle, they only reduce the duration of the parasitic active vector without addressing its root cause. Also, the inherent DPWMs' clamping feature and switching loss savings are slightly disrupted. However, at higher modulation indexes, the discontinuity starts to diminish, making the impact of the rate limiter on the DPM performance negligible.

IV. Simulation Results

A simulation model was developed in PLECS to validate the presented issue of the parasitic vector in the described discontinuous modulation strategies. The model includes a squirrel-cage induction motor (IM), a voltage source inverter, and a PWM module.

The IM was parameterized based on the machine used in the experimental setup, with its parameters listed in Table I. The simulation was performed at the same operating points as the experimental results under open-loop operation. Furthermore, ideal switches were used in the voltage source inverter model, which was fed by a 565 V dc source to match the voltage used in the real measurements.

A C-script was used to program the state machine with the up-down counter to simulate the behavior of the DSP's PWM module, as demonstrated in Fig. 2. The C-script was evaluated

TABLE I
IM Parameters and Nameplate Data

Power	12 kW	**Stat. resistance**	370 mΩ
Frequency	50 Hz	**Rot. resistance**	225 mΩ
Voltage	400 V	**Stat. leak. inductance**	2.27 mH
Current	22 A	**Rot. leak. inductance**	2.27 mH
Speed	1460 rpm	**Mag. inductance**	82.5 mH
No. poles	4	**Stat. inductance**	84.77 mH
Power factor	0.8	**Rot. inductance**	84.77 mH

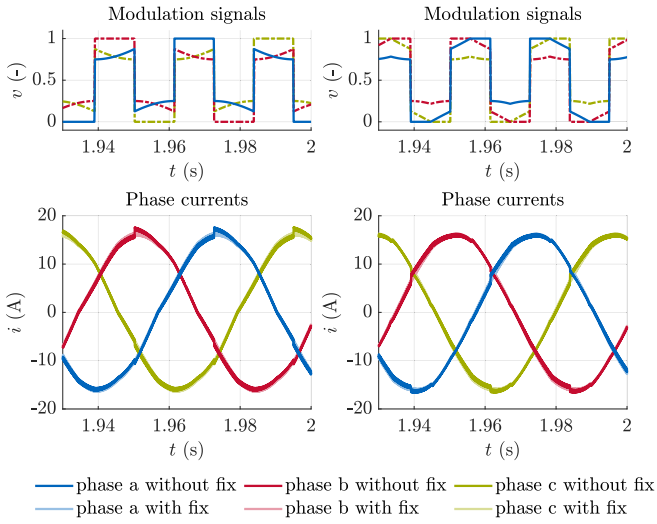

Fig. 11. Simulation results of modulation signals and phase currents, with and without the proposed fix, for DPWM1 (left column) and DPWM3 (right column) at a PWM frequency of $f_{\text{PWM}} = 20\,\text{kHz}$ and modulation index $m = 0.25$.

at the same frequency the counter updates its value in the Texas Instruments DSP, with an identical counter resolution to match that of the DSP. A C-script was also used to calculate the modulation signals from the reference voltages, which was evaluated at the switching frequency. This C-script was synchronized with the C-script representing the PWM module with the up-down counter. Consequently, the modulation signal values (compare values for the PWM module) were updated at the counter's maximum, as implemented in the actual DSP.

Fig. 11 shows the modulation signals and phase currents with and without the proposed fix at a modulation index of $m = 0.25$. The current spikes occur after the positive clamp of the modulation signals, caused by the parasitic voltage vector due to the DPWM implementation. According to (3) and (5), the duration of the parasitic voltage vector depends on the modulation index. As shown in Fig. 12, for $m = 0.5$, the duration of the parasitic voltage vector is shorter, reducing the magnitude of the current spikes.

The duration of the parasitic voltage vector, which causes the current spikes, depends not only on the modulation index but also on the switching frequency. Thus, the phase currents for a lower switching frequency of $f_{\text{PWM}} = 5\,\text{kHz}$ are shown in Fig. 13. From the figure, two kinds of ripples can be clearly observed—the one introduced by the pulsating voltage and switching frequency and the current spikes that are caused by the duration of the parasitic voltage vector—each with a different root cause.

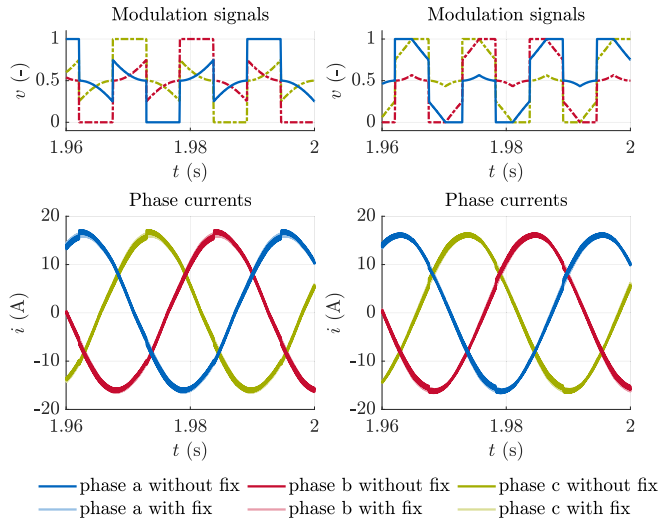

Fig. 12. Simulation results of modulation signals and phase currents, with and without the proposed fix, for DPWM1 (left column) and DPWM3 (right column) at a PWM frequency of $f_{\text{PWM}} = 20\,\text{kHz}$ and modulation index $m = 0.5$.

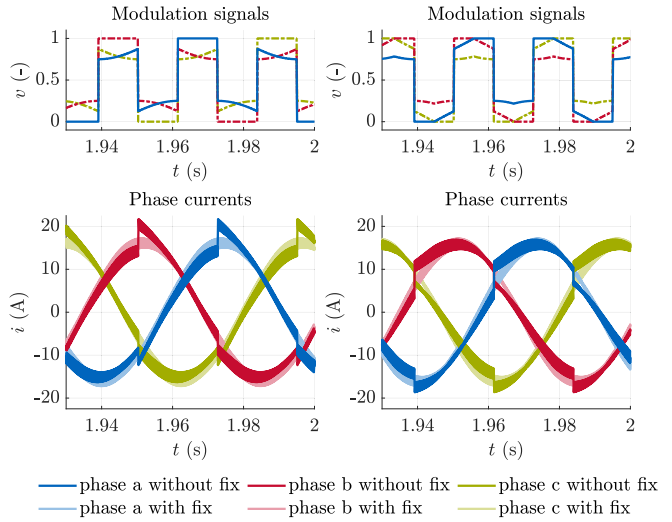

Fig. 13. Simulation results of modulation signals and phase currents, with and without the proposed fix, for DPWM1 (left column) and DPWM3 (right column) at a PWM frequency of $f_{\text{PWM}} = 5\,\text{kHz}$ and modulation index $m = 0.25$.

Finally, Fig. 14 shows the modulation signals and phase currents for GDPWM at $f_{\text{PWM}} = 5\,\text{kHz}$ under different phase angles ψ. The position of the current spikes depends on the location of the clamped area.

The important conclusion is that since the simulation model does not account for the parasitic parameters of the inverter and IM that create a path for the zero-sequence currents, it demonstrates that the current spikes are primarily not caused by the rapid change in ZSS of the modulation strategies but rather by the duration of the described parasitic voltage vector.

V. Experimental Results

To validate the analyzed problem and the proposed solution, experiments were conducted on a three-phase 12-kW, 400 V IM fed by a SiC-based VSI equipped with CAS120M12BM2 power

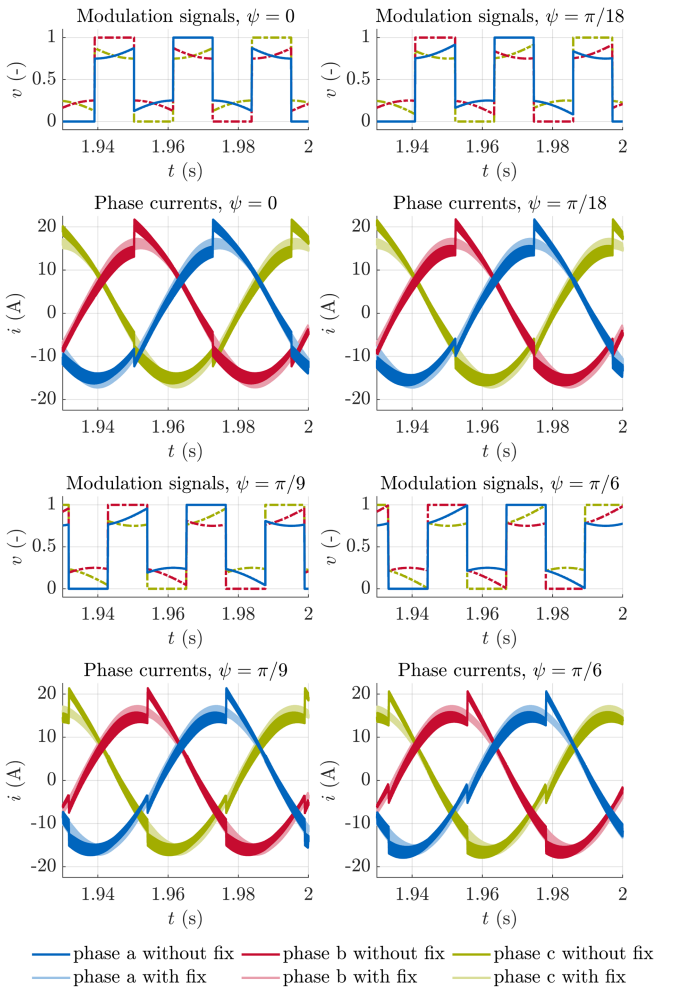

Fig. 14. Simulation results of modulation signals and phase currents, with and without the proposed fix, for GDPWM at different phase angles ψ, with a PWM frequency of $f_{\text{PWM}} = 5\,\text{kHz}$ and modulation index of $m = 0.25$.

modules from Wolfspeed/CREE. The IM is part of a Ward–Leonard machine set, accompanied by an 8.8-kW dc machine used as the load. The IM parameters are listed in Table I. The inverter is powered by a bidirectional power supply (ITECH IT6018C-800-75) with the dc-bus voltage set to 565 V. The entire system is controlled by a TMDSCNCD28P65X controlCARD from Texas Instruments. A photograph of the experimental setup is provided in Fig. 15.

Both open-loop V/Hz and closed-loop FOC schemes were used to analyze the behavior of the DPWM strategies. A block diagram of the closed-loop FOC scheme is shown in Fig. 16. It utilizes the conventional direct FOC approach with a speed controller. The PWM carrier frequency was set to 20 kHz, and the system sample time to 10 kHz. For closed-loop operation, measured data were sampled at the system sample time, buffered, and transmitted to a PC via UART.

The DC-link voltage and motor currents are measured using sigma-delta modulators with a 20 MHz clock. The DSP demodulates the signals using a Sinc3 filter with an oversampling rate of 100, yielding an effective data rate of 5 μs. To ensure synchronization with the PWM period (50 μs, i.e., 20 kHz),

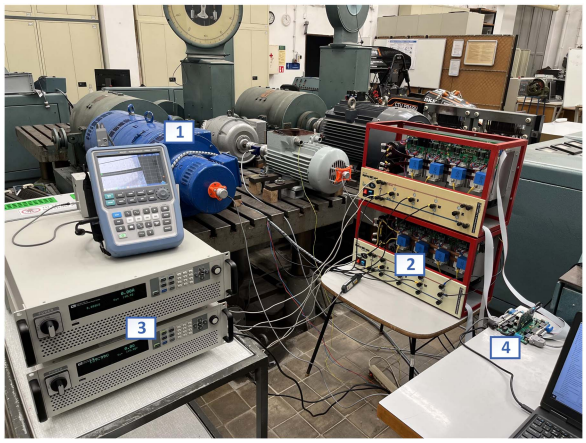

Fig. 15. Photograph of the experimental setup: 1—Ward-Leonard machine set with 12-kW induction and 8.8-kW DC machine, 2—SiC inverter, 3—bidirectional dc supplies, 4—DSP control board.

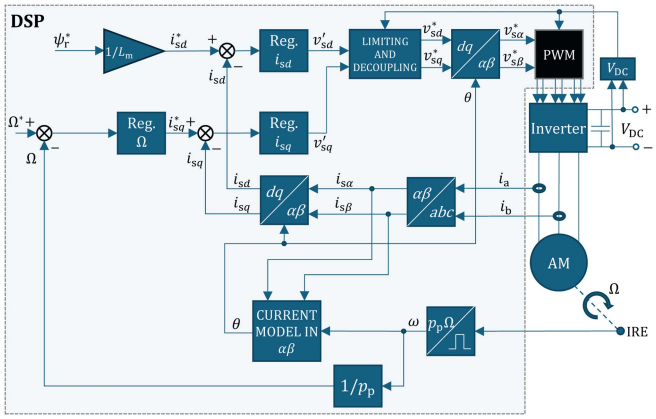

Fig. 16. Block diagram of the implemented closed-loop direct FOC. The pulse pattern modification is integrated into the "PWM block."

data acquisition starts 10 μs before the end of each PWM cycle. The first two Sinc3-filtered samples are discarded due to filter latency, while the subsequent 10 valid samples are averaged to produce filtered readings for each control period (100 μs, i.e., 10 kHz).

The shaft speed was measured using an incremental encoder with 2048 pulses per revolution. The load torque of the separately excited dc machine was controlled by connecting its armature to a second bidirectional power supply.

In the open-loop V/Hz control mode, experiments were conducted with a switching frequency of 20 kHz. To demonstrate the effect of lower switching frequencies on the duration of parasitic vectors and the resulting current spikes, additional experiments were performed at 5 kHz.

A. Closed-Loop Control

First, closed-loop tests were carried out. In the FOC, the machine flux was set to 0.9 Wb. It is also important to note that the current control loops were experimentally tuned by observing the step response of d-axis current when SVPWM was utilized, i.e., with "clean" modulated voltages. The IM was, in all

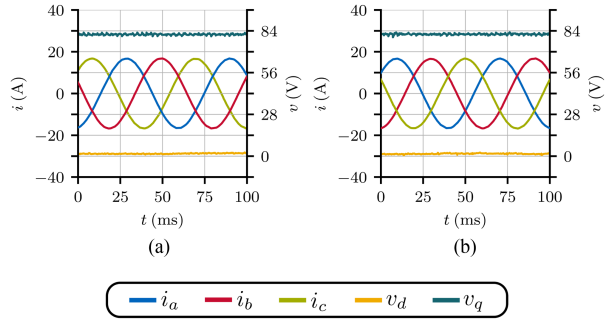

Fig. 17. Motor phase currents and reference d- and q-axis voltages from DSP for $m = 0.25$. (a) SVPWM. (b) DPWM.

cases, loaded with 30 N · m. By setting different reference rotor speeds, various modulation indexes were achieved. The ones under examination were $m = 0.25$ ($\omega_r = 45\,\text{rad} \cdot \text{s}^{-1}$), $m = 0.5$ ($\omega_r = 95\,\text{rad} \cdot \text{s}^{-1}$), and $m = 0.75$ ($\omega_r = 142\,\text{rad} \cdot \text{s}^{-1}$).

As a reference, Fig. 17 shows the behavior of SVPWM and DPWMMAX for the worst-case scenario, i.e., when $m = 0.25$. Due to the continuous nature of the modified reference voltages, no problem with the parasitic active vector is present since the modulating waveforms are smooth.

Fig. 18 shows the three-phase current measured by the DSP along with the reference d- and q-axis voltages from the current controllers for DPWM1. The left column of the figure shows the currents and reference voltages without the proposed solution, and the right column shows the currents with the proposed solution. In line with the theoretical analysis, spikes occur when the positive clamp of the respective phase ends. These spikes trigger a reaction from the current controllers, which operate in the synchronous dq-reference frame and attempt to counteract the sudden error to maintain sinusoidal currents. This response results in sharp modifications of the dq-axis voltage references, which are particularly noticeable at lower modulation indexes. In an extreme case, the attempt to suppress the spikes can lead to high-frequency oscillatory behavior in the current waveforms.

Such a behavior can be seen in Fig. 19, which shows DPWM3 with 30° clamps. Here, it can be seen that for $m = 0.25$, the current spikes are so high they trigger a very sharp response with superimposed oscillations. The intensity of this behavior depends on the controllers' bandwidth (i.e., gain settings). Therefore, the current spikes, especially at lower modulation indexes, can potentially disrupt the stability of the control loops.

B. Open-Loop

Additional tests in open-loop, where the voltage and frequency were set directly, were conducted to assess the modulators' behavior without the controllers' influence. For a qualitative comparison, the same operating points corresponding to the closed-loop tests were performed, i.e., the voltage and frequency corresponding to the operating points in Figs. 18 and 19 were utilized, and the load torque was set again to 30 N · m.

Fig. 20 shows the comparison of the currents and reference modulating signal (obtained by measuring DSP PWM output for the HS switch) for DPWM1 without (left column) and

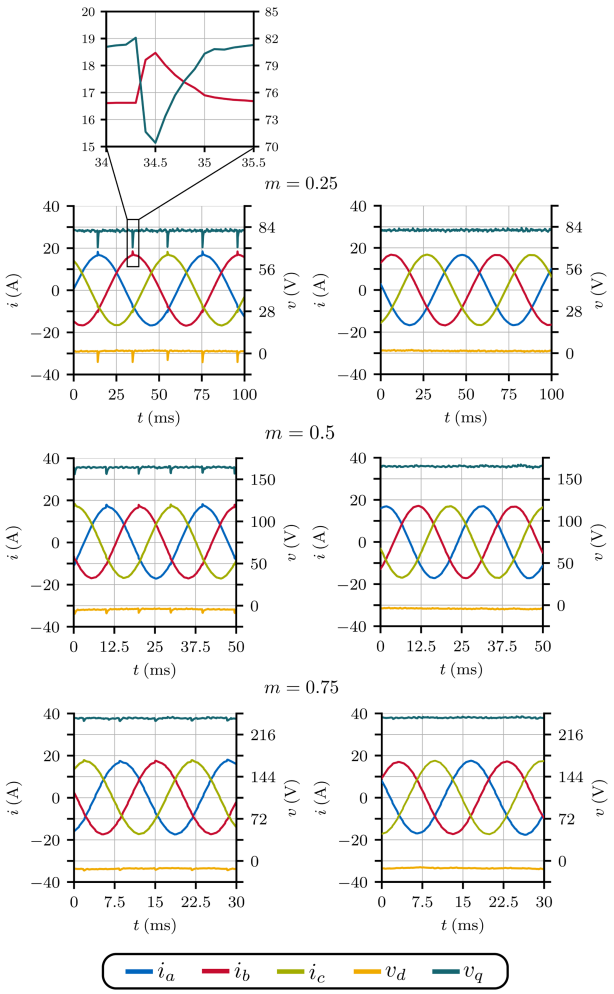

Fig. 18. Motor phase currents and reference d- and q-axis voltages from DSP for different motor speeds corresponding to different modulation indexes when DPWM1 is employed. Left column—without the proposed fix, right column—with the proposed fix.

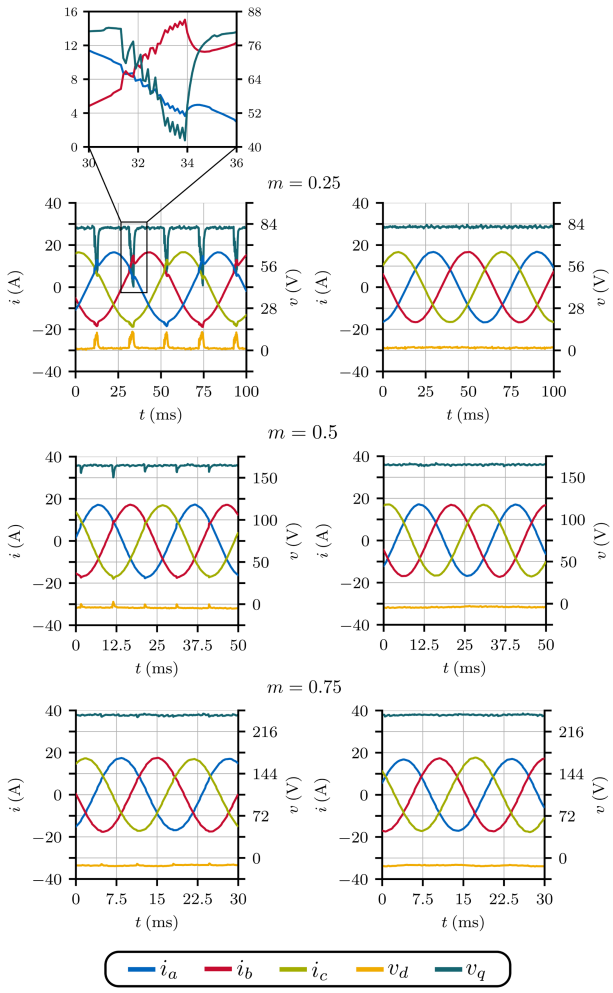

Fig. 19. Motor phase currents and reference d- and q-axis voltages from DSP for different motor speeds corresponding to different modulation indexes when DPWM3 is employed. Left column—without the proposed fix, right column—with the proposed fix.

with (right column) the proposed fix. The input bandwidth of the oscilloscope was set to 10 kHz to filter out the switching harmonics on the voltage and also current waveform. Following the theoretical analysis, the current spikes appear at the end of the positive clamp and are contingent upon the reference modulation index. For completeness, the behavior of the SVPWM and DPWMMAX at $m = 0.25$ is shown in Fig. 21. Again, no problems are visible due to the continuity of the modulating signal.

Finally, Fig. 22 shows the same situation as in Fig. 20 but for DPWM3. Although the reference voltage signal is different, at the end of a positive clamp, a current spike occurs but is now at a different position due to the shift of the clamping instant compared to DPWM1.

Table II shows the current THD for the cases shown in Figs. 20 and 22. With the proposed DPWM fix, the THD is, in all cases, below 1%. Without the DPWM fix, the worst situation occurs for $m = 0.25$, with the THD being almost 3% for both modulations. DPWM1 then exhibits slightly better THD performance than DPWM3.

TABLE II
MOTOR PHASE CURRENT THD COMPARISON FOR DPWM1 AND DPWM3, $f_{\text{PWM}} = 20$ KHZ

	m	THD without DPWM fix	THD with DPWM fix
DPWM1	0.25	2.74%	0.63%
	0.5	1.92%	0.66%
	0.75	1.10%	0.61%
DPWM3	0.25	2.94%	0.97%
	0.5	2.01%	0.83%
	0.75	1.11%	0.74%

Fig. 23 then shows the comparison of DPWM1 and DPWM3 at $m = 0.25$ for two different switching frequencies—the so-far utilized 20 and 5 kHz (oscilloscope bandwidth set to 2 kHz). As demonstrated in the theoretical analysis, the longer the PWM period (or the lower the switching frequency), the proportionally higher the current spike. In the case of 5 kHz, the spikes reach almost 10 A in magnitude for the studied case. If the load parameters (resistances and inductances) were lower, for instance, as in the case of high-power machines, the overshoots would reach even higher magnitudes.

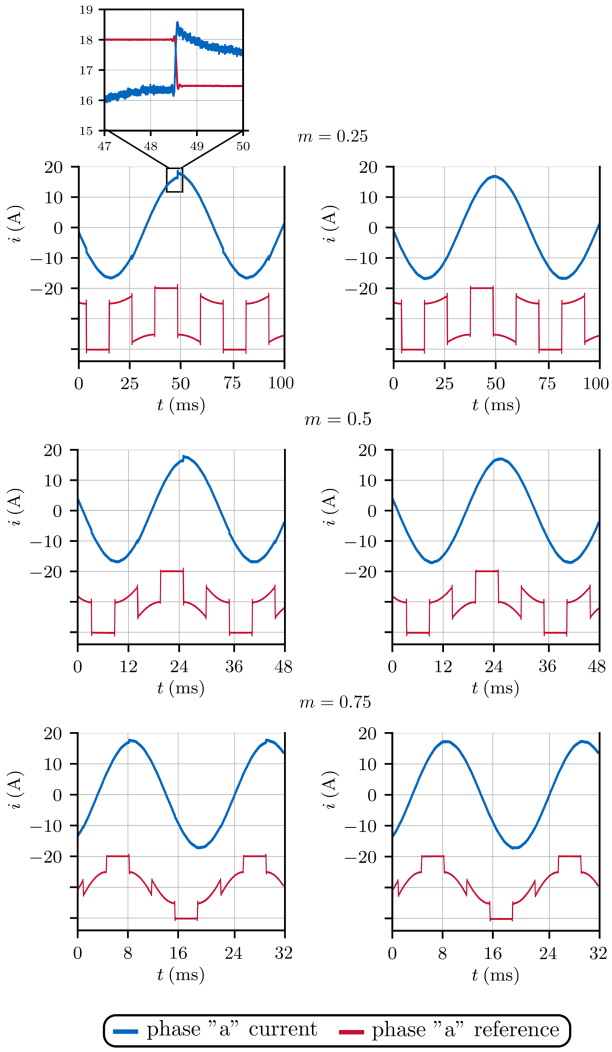

Fig. 20. Measured phase "a" reference voltage (not to scale) and current waveform in an open-loop for DPWM1. Left column: without the proposed fix, and right column: with the proposed fix.

TABLE III
MOTOR PHASE CURRENT THD COMPARISON FOR DPWM1 AND DPWM3, $f_{\text{PWM}} = 5$ kHz, $m = 0.25$

	$f_{\text{PWM}} = 5$ kHz	$f_{\text{PWM}} = 20$ kHz
DPWM1	11.49%	2.74%
DPWM3	11.64%	2.94%

Table III shows the current THD for the waveforms in Fig. 23. The influence of the switching frequency on the duration of the parasitic active vector can also be seen in the form of the THD. At 5 kHz, the THD for both DPWM1 and DPWM3 is over 11%, which is approximately four times higher than in the case of 20 kHz.

Finally, Fig. 24 shows the results for GDPWM operating at 5-kHz switching frequency with various phase shifts and $m = 0.25$. The oscillograms also show the measured magnitude of the highest current spike. The THD for the demonstrated cases (and also for the clean waveforms with the DPWM fix implemented) is shown in Table IV. It can be seen that

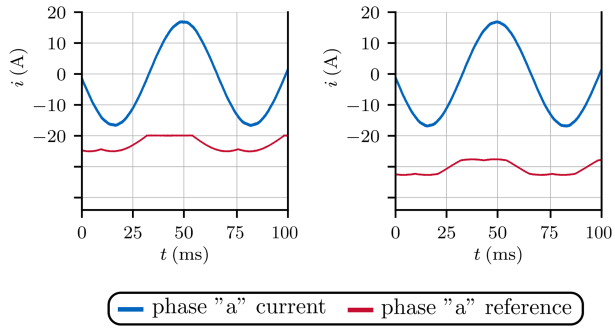

Fig. 21. Measured phase "a" reference voltage (not to scale) and current waveform in an open-loop for SVPWM (left column) and DPWMMAX (right column) at $m = 0.25$.

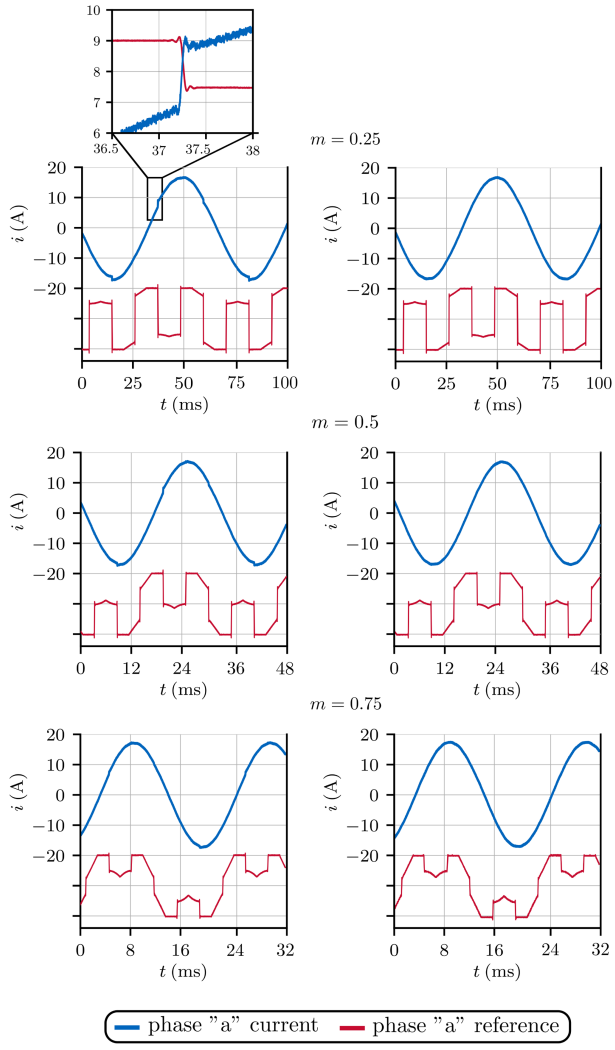

Fig. 22. Measured phase "a" reference voltage (not to scale) and current waveform in an open-loop for DPWM3. Left column: without the proposed fix, and right column: with the proposed fix.

TABLE IV
MOTOR PHASE CURRENT THD COMPARISON FOR GDPWM, $f_{\text{PWM}} = 5$ kHz, $m = 0.25$

	$\psi = 0$	$\psi = \pi/18$	$\psi = \pi/9$	$\psi = \pi/6$
GDPWM without fix	11.49%	11.61%	11.73%	11.91%
GDPWM with fix	0.64%	0.68%	0.65%	0.66%

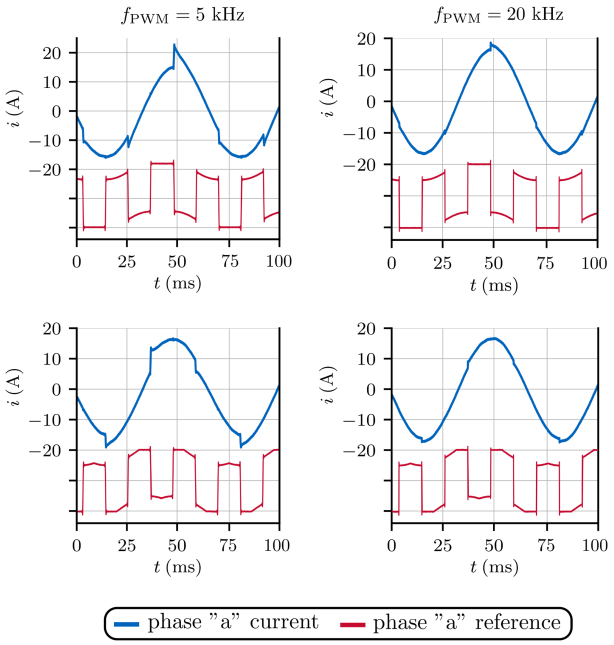

Fig. 23. Measured phase "a" reference voltage (not to scale) and current waveform in an open-loop for DPWM1 and DPWM3 and $f_{PWM} = 5$ kHz (left column), and $f_{PWM} = 20$ kHz (right column) at $m = 0.25$.

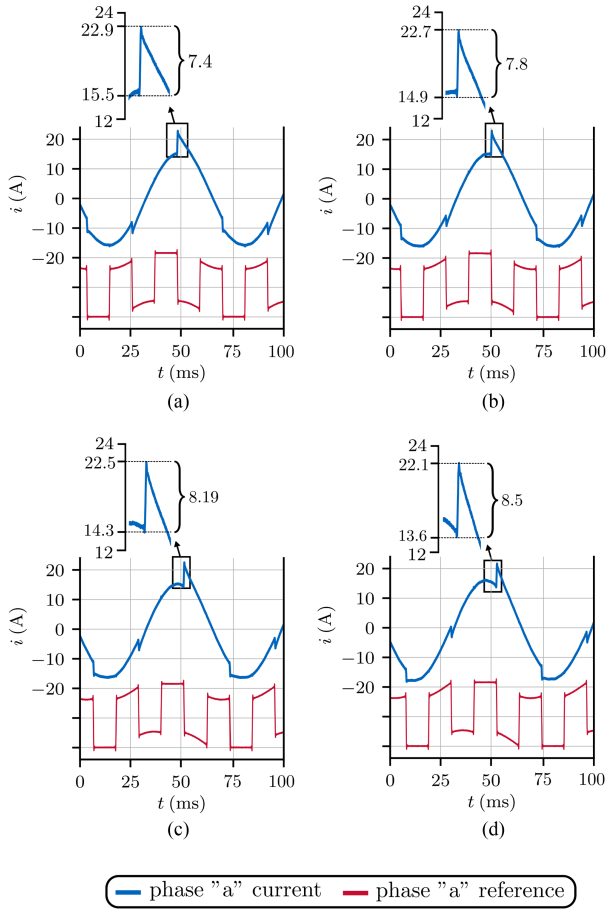

Fig. 24. Measured phase "a" reference voltage (not to scale) and current waveform in an open-loop for GDPWM at $m = 0.25$ and $f_{PWM} = 5$ kHz under different phase angle ψ. (a) $\psi = 0$. (b) $\psi = \pi/18$. (c) $\psi = \pi/9$. (d) $\psi = \pi/6$.

with the increasing phase shift, the magnitude of the spikes increases, which, on the one hand, agrees with the previous theoretical analysis. Still, on the other hand, it is essential to note that the load is a rotating electrical machine. Therefore, the current spike will also depend on the value of back-electromotive force (BEMF) at the instant of the end of the positive clamp since, according to the equivalent circuit, it is the difference between the supply voltage (i.e., parasitic active vector) and BEMF that drives the current through the machine's winding.

While the primary indicator of the PWM error in this study was the current THD, it is important to note that the error may also affect other performance metrics, such as torque ripple, acoustic noise, and electromagnetic interference. However, directly quantifying these effects analytically or experimentally is challenging, and their significance largely depends on specific operating conditions, particularly low modulation indexes and low switching frequencies.

VI. Conclusion

This article investigates the primary cause of current imperfections in VSI-based systems controlled by conventional DPWM strategies, mainly focusing on DPWM strategies with mathematically discontinuous modulating signals. Traditionally, these imperfections have been attributed to abrupt changes in common-mode voltage, with mitigation approaches centered on limiting the slew rate of the clamping signal. Our research, however, reveals that the primary cause lies within the logic of the PWM modules in DSPs, which introduces an unintended active vector at the end of each positive clamping instance. This phenomenon, specific to DSP-based DPWM implementations, creates phase-specific current spikes that are not effectively suppressed by common-mode mitigation techniques alone.

This article's innovation lies in identifying this DSP-specific implementation issue and providing a straightforward, DSP-compatible solution that preserves the intended characteristics of DPWM. By incorporating an auxiliary compare register, our method ensures accurate PWM output transitions at the end of clamping intervals, eliminating the parasitic active vector and achieving smooth load current waveforms, improving both open-loop and closed-loop performance.

The THD analysis of DPWM1 and DPWM3 in open-loop operation at a switching frequency of 20 kHz revealed that, without the proposed fix, the THD for a low modulation index ($m = 0.25$) could reach nearly 3%. In contrast, it remained below 1% when the fix was applied. At a reduced switching frequency of 5 kHz, the THD rose to 11.5% for both DPWM1 and DPWM3 without the fix due to the prolonged parasitic active vector duration.

Overall, our proposed method offers broad applicability across DPWM-driven systems, including topologies beyond VSI. Future studies may build on this foundation to explore how such improvements apply to more complex or multilevel inverter systems, further advancing the robustness and efficiency of DPWM implementations on DSPs.

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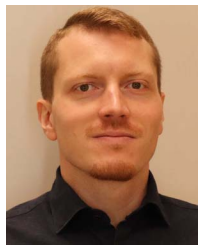

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