Letters

Adjustable Virtual Impedance via Anti-windup Method for Enhancing Transient Stability and Grid-Forming Capability Under Current Limiting Conditions

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***Abstract*—This letter presents a novel method to enhance the transient stability and grid forming (GFM) capability under current limiting conditions. The proposed method employs dual-loop vector voltage control with a back-calculation anti-windup strategy, using adjustable gain to modify the reactance-to-resistance ratio of the equivalent virtual impedance. The method ensures seamless operation during transitions between normal and abnormal grid conditions while significantly improving transient stability and GFM capability. Theoretical analysis has been validated through 2-kVA-scale experiments, demonstrating the effectiveness of the proposed method.**

***Index Terms*—Anti-windup, current limitation, grid forming (GFM), transient stability, virtual impedance.**

I. Introduction

THE grid-forming voltage-source converters (GFM-VSCs) are controlled as voltage sources behind an impedance, capable of independently establishing system voltage and frequency. Such voltage-source operation can lead to overcurrent depending on external grid conditions. Besides, GFM-VSCs are composed of semiconductor devices, requiring specific overcurrent management techniques essential for reliable operation [1]. The GFM-VSC typically achieves current limitation during abnormal grid events, such as voltage dips or phase angle jumps, by emulating the magnitude and phase angle of the virtual impedance, referred to as the virtual impedance method (VIM) [2].

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During grid faults that lead to current limitation, aligning the phase angle of the virtual impedance with that of grid impedance can maximize the GFM capability within the permissible limits [3]. In this study, GFM capability refers to the ability to provide grid services, such as inertia power during frequency changes, active phase jump power during phase angle jump faults, and reactive fault current during voltage dip faults. Also, when large disturbances, such as voltage dips and phase angle jumps, occur, emulating the virtual impedance to be more inductive enhances the transient stability of the GFM-VSC [4]. This indicates that if the phase angle of the virtual impedance is appropriately emulated, the GFM-VSC can significantly improve transient stability and GFM capability.

When achieving current limitation through the VIM, the current is indirectly limited by modifying the existing voltage reference to a new one that subtracts the voltage drop caused by the virtual impedance. However, the VIM has two main issues [5], [6]. First, the VIM achieves current limitation under the assumption that the reduced voltage reference can be tracked quickly; however, due to the relatively low bandwidth of the voltage controller, temporary overcurrent beyond the current limit occurs both immediately after the fault and right after fault clears. Second, when selecting the magnitude of the virtual impedance for current limiting, there is a tradeoff between current limiting capability and stability. In contrast, directly limiting the current reference (e.g., using a circular current limiter) not only resolves these issues but is generally considered a more intuitive and effective approach for overcurrent management.

Therefore, this letter applies dual-loop vector voltage (DLVV) control [7], which includes a cascaded configuration of a voltage controller and a current controller using proportional–integral controllers, along with a circular current limiter. This control ensures that the point of common coupling (PCC) voltage tracks the voltage reference without the steady-state error under normal conditions. However, this method can cause windup in the integrator of the outer loop, namely, the voltage controller, during current limitation, making the implementation of an anti-windup method essential. The anti-windup method can be categorized into two main strategies: one that freezes the operation of the integrator during saturation and other that feeds back the windup error to the integrator during the same state [8]. The first strategy involves maintaining the output of the integrator in the voltage

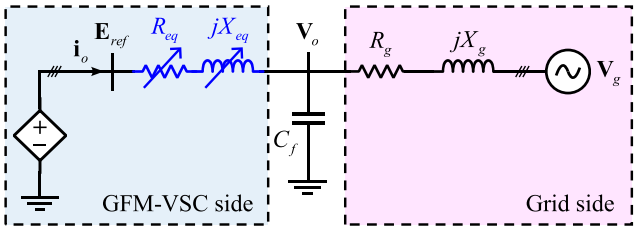

Fig. 1. Equivalent single-line circuit diagram of a grid-connected GFM-VSC.

controller at zero during current limitation. It has been revealed in the literature that when this method is employed, the DLVV control with the circular current limiter is equivalently modeled as a pure virtual resistor under current limiting conditions [9]. However, when it is equivalent to a pure virtual resistor, the transient stability and GFM capability may not be fully achieved, as previously described. To overcome these challenges, this letter employs the back-calculation anti-windup (BCAW) method in the control loop, which prevents integrator windup by using the difference between the saturated control signal and the original unsaturated signal from the voltage controller output before passing through the current limiter. This letter proposes a new approach that uses adjustable back-calculation gain as an additional control degree of freedom. This approach allows for the independent adjustment of the phase angle (or reactance-to-resistance (X/R) ratio) of the equivalently modeled virtual impedance for current limitation, thereby enhancing the transient stability and GFM capability. Note that these methods do not directly emulate the virtual impedance; rather, the voltage controller with BCAW and the circular current limiter is equivalently modeled as an adjustable virtual impedance without requiring any control mode switching.

II. Background Theory on Transient Stability and GFM Capability Considering Current Constraints

A. Equivalent Circuit Model of Current Limiting Control

Fig. 1 shows the general single-line circuit diagram of a grid-connected GFM-VSC. $\mathbf{E}_{\text{ref}}$, $\mathbf{V}_o$, $\mathbf{V}_g$, $\mathbf{i}_o$, R_g, and X_g represent the reference value of the electromotive force, the PCC voltage, the grid voltage, the converter-side current of the GFM-VSC, the grid resistance, and the grid reactance, respectively. R_{eq} and X_{eq} represent the equivalent virtual resistance and reactance, respectively, and can be introduced to describe the current limiting algorithm. The VIM can be directly expressed as R_{eq} and X_{eq} in Fig. 1, and even the circular current limiter, used independently, can also be mathematically expressed as changes in R_{eq} and X_{eq} shown in Fig. 1. In other words, since the current limiting algorithm can be mathematically modeled as an equivalent virtual impedance, the impact of the current limiting algorithm on the transient stability and GFM capability can be analyzed through the equivalent virtual impedance values of the circuit in Fig. 1 during current limitation.

B. Impact of Virtual Impedance on Transient Stability and GFM Capability

In this section, the relationship between the phase angle of the virtual impedance and both transient stability and GFM capability is discussed. The smaller the change in the PCC voltage between the prefault and during-fault states, the greater the GFM capability under fault conditions [10]. In [3], it is shown that as $\angle(R_{\text{eq}} + jX_{\text{eq}})$ approaches $\angle(R_g + jX_g)$, the variation in the PCC voltage decreases, as shown in Fig. 2. Moreover, it has been mathematically proven that when $\angle(R_{\text{eq}} + jX_{\text{eq}})$ is equal to $\angle(R_g + jX_g)$, the change in the PCC voltage is minimized, as illustrated in Fig. 2(c). In conclusion, when a voltage dip fault occurs, the reactive fault current contribution is maximized at $\angle(R_{\text{eq}} + jX_{\text{eq}}) = \angle(R_g + jX_g)$, and similarly, when a grid phase angle jump fault occurs, the active phase jump power is also maximized under the same condition.

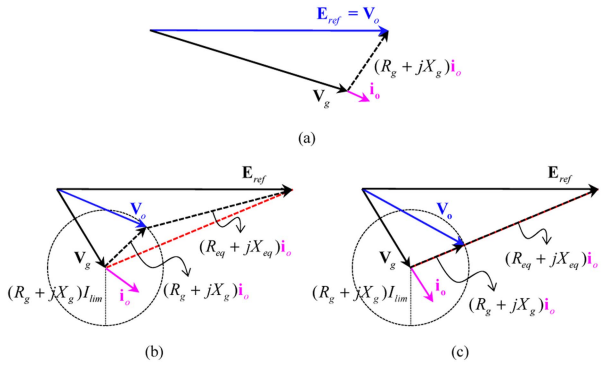

Fig. 2. Phasor diagram of a grid-connected GFM-VSC. (a) Under normal conditions. (b) Under current limiting conditions when $\angle(R_{\text{eq}} + jX_{\text{eq}}) \neq \angle(R_g + jX_g)$. (c) Under current limiting conditions when $\angle(R_{\text{eq}} + jX_{\text{eq}}) = \angle(R_g + jX_g)$.

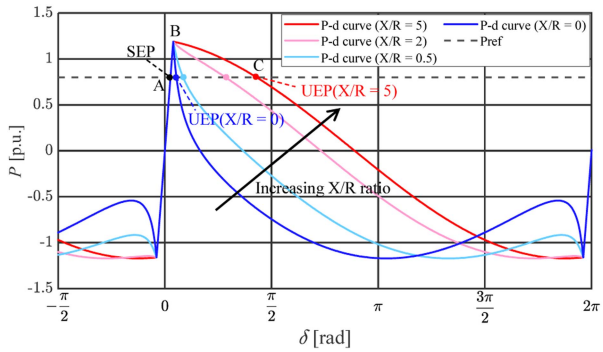

Fig. 3. Influence of the X/R ratio of the virtual impedance on P–δ curve under current limiting conditions.

Fig. 3 illustrates the influence of the X/R ratio of the virtual impedance on P-δ curve for current limitation. The grid reactance and resistance used for the plot in Fig. 3 are 0.1 and 0.02 p.u., respectively, and δ represents the power angle, which is the angle difference between $\mathbf{E}_{\text{ref}}$ and $\mathbf{V}_g$. The voltage dip withstand capability of the GFM-VSC can be qualitatively analyzed using the energy function method [11]. Using this method, the region of attraction, i.e., the stability boundary at the operating point, can be determined, as shown in Fig. 4. Fig. 4 shows the influence of the X/R ratio of the virtual impedance on the region of attraction boundary (stability boundary). For an X/R ratio of 5, the stability boundary is significantly larger than that for an X/R ratio of 1, indicating improved robustness in terms of voltage dip

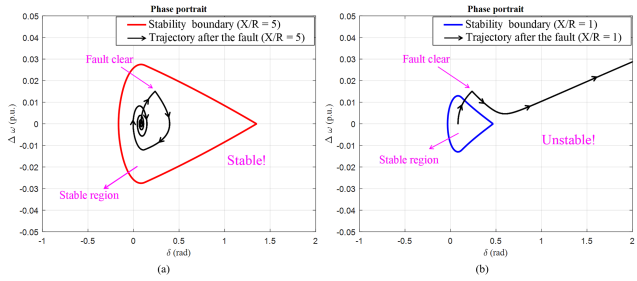

Fig. 4. Influence of the X/R ratio of the virtual impedance on the region of attraction boundary (stability boundary) under voltage dip fault. (a) X/R = 5. (b) X/R = 1.

withstand capability. This can be verified through the postfault trajectory, consisting of the power angle and angular frequency. After the fault, the trajectory deviates from the stable region. Once the fault is cleared, if the trajectory remains within the stability boundary, it converges to the original stable equilibrium point (SEP) when the X/R ratio is 5; otherwise, it diverges when the X/R ratio is 1.

In addition, the phase angle jump withstand capability of the GFM-VSC can be assessed through the distance between the SEP and the unstable equilibrium point (UEP) on the P-δ curve, as shown in Fig. 3. This distance represents the stability margin of the GFM-VSC following a phase angle jump fault. A larger distance between SEP and UEP ensures that δ remains stable without exceeding the UEP after a phase angle jump fault.

In conclusion, as shown in Figs. 3 and 4, increasing the X/R ratio of the virtual impedance enhances the voltage dip and the phase angle jump withstand capabilities of the GFM-VSC [3], [4].

These three analyses indicate that equivalent virtual impedance with a flexible phase angle (or X/R ratio) under current limiting conditions can lead to an improvement in transient stability and GFM capability.

III. Proposed DLVV Control Using the BCAW Method

In this letter, DLVV control is used in the inner loop control, and current limitation is achieved through a circular current limiter, as shown in Fig. 5. $V_{\rm DC}$, L_f, C_f, and i_g represent the dc-link voltage, the filter inductance, the filter capacitance, and the grid-side current of the GFM-VSC, respectively. $P_{\rm ref}$, P_o, J, D, $\theta_{\rm ref}$, ω_g, K_P^V, K_I^V, and $\mathbf{V}_{dq}^{\rm PWM}$ denote the active power reference, output active power, inertia constant, damping coefficient, angle reference of the GFM-VSC, grid angular frequency, proportional and integral gains of the voltage controller, and the pulsewidth modulation signal, respectively. Subscript "dq" denotes a complex variable in the synchronous dq-frame.

$$\overline{\mathbf{i}_{odq}^{\rm ref}} = c\,\mathbf{i}_{odq}^{\rm ref}, \quad c = \min\{1, I_{\rm lim}/\left|\mathbf{i}_{odq}^{\rm ref}\right|\} \tag{1}$$

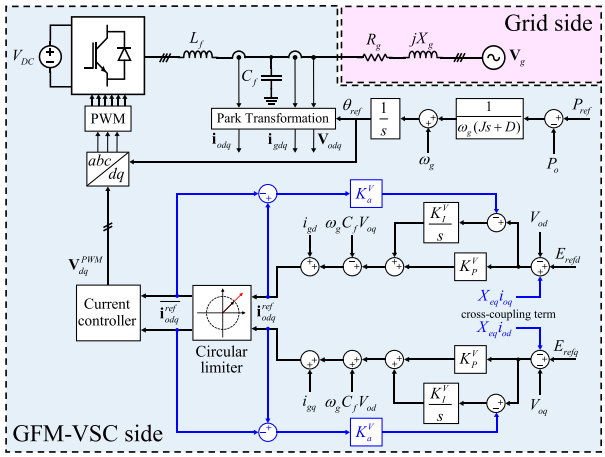

Fig. 5. Overall GFM-VSC block diagram of the proposed DLVV control using the BCAW method.

The circular current limiter, as expressed in (1), limits the magnitude of the current reference to the allowable maximum current, $I_{\rm lim}$, while maintaining the phase angle of the original current reference. $\mathbf{i}_{odq}^{\rm ref}$ and $\overline{\mathbf{i}_{odq}^{\rm ref}}$ represent the current reference before and after the current limitation in the GFM-VSC, respectively. The parameter c represents the ratio of the saturated current reference to the value before saturation. When the current limiter is not triggered, c equals 1; when triggered, c becomes a value less than 1.

This letter proves that the DLVV control with the circular current limiter is equivalent to a virtual impedance with the desired X/R ratio through the BCAW method. As shown in Fig. 5, the BCAW method prevents windup of the integrator by compensating for the difference between the presaturation and saturated values during current limitation conditions, using the back-calculation gain K_a^V. From Fig. 5 and (1), $\overline{\mathbf{i}_{odq}^{\rm ref}}$ can be derived as (2) shown at the bottom of this page.

For simplified analysis, if the dynamics of the filter capacitor are neglected, the relationship between the converter- and grid-side currents in the synchronous dq-frame can be derived as

$$\mathbf{i}_{odq} = \mathbf{i}_{gdq} + j\omega_g C_f \mathbf{V}_{odq}. \tag{3}$$

Furthermore, as the bandwidth of the current controller is sufficiently larger than that of the outer loop, the current controller can be assumed as unity gain (i.e., $\overline{\mathbf{i}_{odq}^{\rm ref}} = \mathbf{i}_{odq}$). Through $\overline{\mathbf{i}_{odq}^{\rm ref}} = \mathbf{i}_{odq}$, along with (2) and (3), the equations can be rearranged into (4), indicating that the DLVV control with the circular current limiter can be equivalently modeled as a virtual impedance, as described in (5)

$$\mathbf{E}_{{\rm ref}dq} - \mathbf{V}_{odq} = \frac{(1-c)(s + K_a^V K_I^V)}{cK_P^V s + cK_I^V}\mathbf{i}_{odq} \tag{4}$$

$$\overline{\mathbf{i}_{odq}^{\rm ref}} = c\begin{bmatrix} K_P^V(\mathbf{E}_{{\rm ref}dq} - \mathbf{V}_{odq}) + \left\{(\mathbf{E}_{{\rm ref}dq} - \mathbf{V}_{odq}) - K_a^V(\mathbf{i}_{odq}^{\rm ref} - \overline{\mathbf{i}_{odq}^{\rm ref}})\right\}\frac{K_I^V}{s} \\ +\mathbf{i}_{gdq} + jC_f\omega_g\mathbf{V}_{odq} \end{bmatrix}. \tag{2}$$

$$R_{\text{eq}} + jX_{\text{eq}} = \frac{(1-c)(j\omega + K_a^V K_I^V)}{j\omega c K_P^V + cK_I^V}. \tag{5}$$

From (5), it can be observed that when the circular current limiter is not triggered (i.e., $c = 1$), $\mathbf{E}_{\text{ref}dq} = \mathbf{V}_{odq}$ and $R_{\text{eq}} + jX_{\text{eq}} = 0$, which is mathematically consistent with the behavior when current limitation is not active. When the current limiter is active (i.e., $c < 1$), setting K_P^V to zero during the current limiting period yields the equivalent virtual impedance as follows:

$$R_{\text{eq}} + jX_{\text{eq}}|_{K_P^V=0} = \frac{(1-c)K_a^V}{c} + j\omega\frac{(1-c)}{cK_I^V} \tag{6}$$

where ω and K_I^V are known values obtained from the controller. Note that while adjusting K_P^V to values other than zero allows the virtual impedance to be capacitive as well as inductive, in this analysis, K_P^V is set to zero for simplicity of implementation and because the focus is on emulating an inductive virtual impedance. The X/R ratio σ of the equivalent impedance can be calculated as shown in (7) using X_{eq} and R_{eq} from (6). Then, by expressing K_a^V in terms of σ, the value of K_a^V needed to emulate the equivalent virtual impedance with the desired X/R ratio σ can also be derived as

$$\sigma = \frac{\omega}{K_I^V K_a^V} \rightarrow K_a^V = \frac{\omega}{K_I^V \sigma}. \tag{7}$$

This suggests that the DLVV control with the circular current limiter can be equivalently modeled as a virtual impedance with a desired X/R ratio σ, utilizing the degrees of freedom provided by K_a^V. Consequently, the proposed control can enhance both the transient stability and GFM capability, as described in Section II. Furthermore, this approach allows the controller to maintain smooth operation without reinitialization, even after fault recovery, thus avoiding undesirable transient behavior as the system returns to normal operation. Note that under normal conditions where $i_{odq}^{\text{ref}} - \overline{i_{odq}^{\text{ref}}} = 0$ and $c = 1$, the BCAW term is inactive, and the equivalent virtual impedance is zero ($R_{\text{eq}} + jX_{\text{eq}} = 0$), which means that the cross-coupling compensation term does not exist. Under abnormal conditions, rather than resetting the integrator, only the proportional gain K_P^V is set to zero, while the back-calculation gain K_a^V is adjusted. As a result, the proposed method achieves seamless transitions between normal and abnormal operating conditions. In addition, the proposed method automatically determines the magnitude of the equivalent virtual impedance through the circular current limiter, as shown in (6), to ensure that the output current does not exceed the set value of I_{lim} during the current limiting period.

IV. Experimental Results

To validate the theoretical analysis of the proposed method, 2-kVA downscaled experiments were conducted. The grid reactance and resistance are 0.2 p.u. and 0.04 p.u., respectively, yielding a grid X/R ratio of 5. In addition, I_{lim} was set to 1.2 p.u., and P_{ref} was set at 1 p.u. The detailed parameters are provided in Table I.

Figs. 6 and 7 present experimental results when the grid voltage drops from 1 to 0.2 p.u. for 300 ms, with the X/R ratios

TABLE I
Experimental Parameters

Symbol	Description	Value
V_g	Grid voltage (line to line)	220 V
f_g	Grid frequency	60 Hz
R_g, L_g	Grid impedance value	1 Ω, 12 mH
S	Rated power of the VSC	2 kVA
E_{ref}	Voltage reference	1.08 p.u.
P_{ref}	Active power reference	2 kW
L_f, C_f	LC filter values	2 mH, 10 μF
K_P^V, K_I^V	Voltage control P and I gains	0.1 p.u., 50 p.u.
K_P^I, K_I^I	Current control P and I gains	4 p.u., 50 p.u.
H	Inertia time constant	1 s
I_{lim}	Maximum allowable current	1.2 p.u.
f_{sw}	Switching frequency	15 kHz

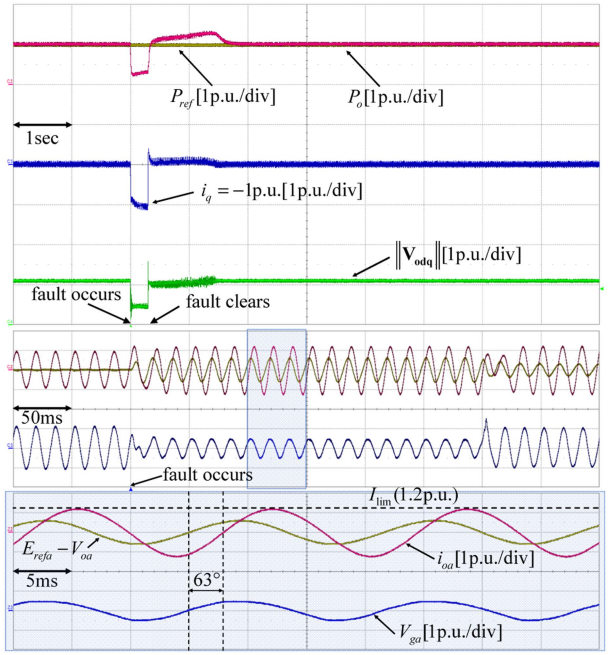

Fig. 6. Experimental results when the grid voltage drops from 1 to 0.2 p.u. for 300 ms with the X/R ratio of the equivalent impedance being 2. (Case I: $K_a^V \approx 3.77$ and $K_I^V = 50$).

of the equivalent virtual impedance being 2 (see Case I) and 0.3 (see Case II), respectively. Therefore, $\theta_z{}^{\text{I}}$ is approximately 63° in Case I, and $\theta_z{}^{\text{II}}$ is approximately 16° in Case II. Here, θ_z refers to the phase angle of the equivalent virtual impedance [i.e., $\theta_z = \tan^{-1}(\sigma)$]. The X/R ratio of the grid impedance is 5, corresponding to $\theta_z{}^{\text{g}}$ being approximately 78°. Consequently, $\theta_z{}^{\text{I}}$ is closer to $\theta_z{}^{\text{g}}$ than $\theta_z{}^{\text{II}}$, indicating that Case I maintains a voltage closer to the prefault voltage-source operation (i.e., near the maximum GFM capability) during a fault compared with Case II. During the voltage dip fault, Case I shows that the GFM-VSC outputs 1 p.u. of q-axis current, as shown in Fig. 6, whereas Case II outputs only 0.5 p.u. of q-axis current, as shown in Fig. 7. In addition, it can be observed that Case I

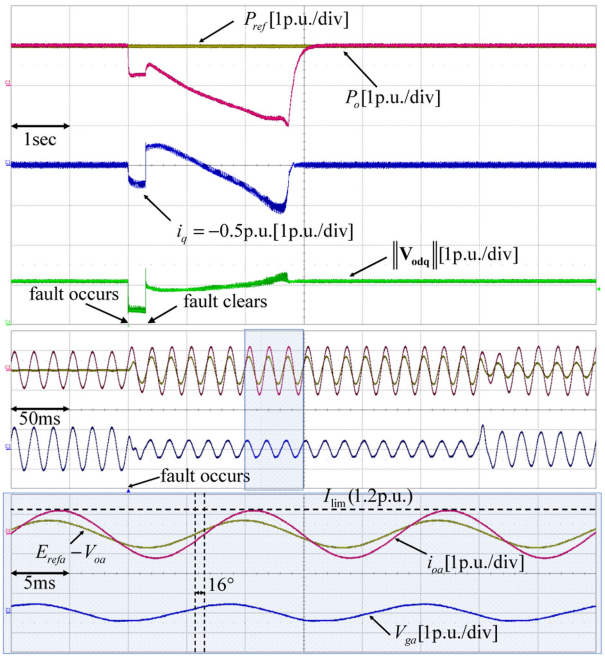

Fig. 7. Experimental results when the grid voltage drops from 1 to 0.2 p.u. for 300 ms with the X/R ratio of the equivalent impedance being 0.3. (Case II: $K_a^V \approx 25.13$ and $K_I^V = 50$).

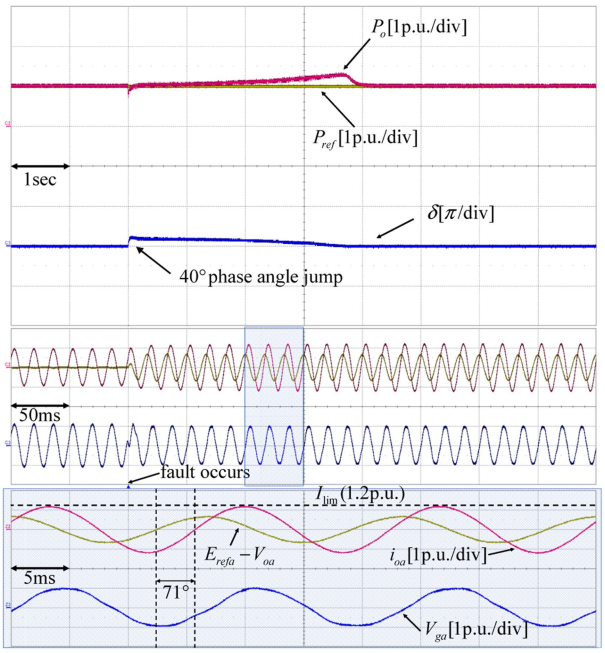

Fig. 8. Experimental results with a 40° grid phase angle jump when the X/R ratio of the equivalent impedance is 3. (Case III: $K_a^V \approx 2.51$ and $K_I^V = 50$).

demonstrates greater robustness in maintaining synchronization after the voltage dip fault compared with Case II, due to the higher X/R ratio of the equivalent virtual impedance.

Figs. 8 and 9 present experimental results when a 40° grid phase angle jump is applied, with the X/R ratios of the equivalent virtual impedance being 3 (see Case III) and 1 (see Case IV),

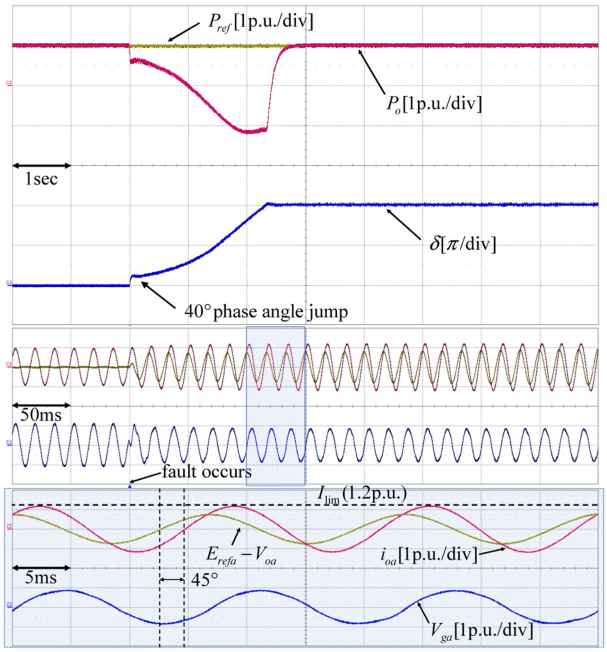

Fig. 9. Experimental results with a 40° grid phase angle jump when the X/R ratio of the equivalent impedance is 1. (Case IV: $K_a^V \approx 7.54$ and $K_I^V = 50$).

respectively. Therefore, $\theta_z{}^{\mathrm{III}}$ is approximately 71° in Case III and $\theta_z{}^{\mathrm{IV}}$ is 45° in Case IV. Consequently, $\theta_z{}^{\mathrm{III}}$ is closer to $\theta_z{}^g$ compared to $\theta_z{}^{\mathrm{IV}}$. As shown in Figs. 8 and 9, Case IV loses synchronization after the grid phase angle jump, unlike Case III, due to the lower X/R ratio of the virtual impedance.

The experimental results demonstrated that the proposed method operates correctly across four distinct equivalent impedances with varying X/R ratios while achieving a current limit of 1.2 p.u. Furthermore, in the prefault condition, there is no equivalent virtual impedance, resulting in $E_{\mathrm{ref}a} - V_{oa} = 0$. However, after the fault occurs, the phase angle difference between $E_{\mathrm{ref}a} - V_{oa}$ and i_{oa}, corresponding to each θ_z, can be observed. This observation confirms that seamless transitions between normal and abnormal conditions are achieved.

V. Conclusion

This letter proposed a method to enhance the transient stability and GFM capability under current limiting conditions. The proposed method utilizes the back-calculation gain in anti-windup as an additional degree of freedom. This allows the phase angle of the equivalent virtual impedance to adapt to fault conditions, which can significantly improve transient stability and GFM capability. Furthermore, the proposed method operates seamlessly during transitions between normal and abnormal conditions without any control mode switching. Finally, the theoretical analysis has been validated through 2-kVA-scale experiments.

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