Letters

A Zero Net Flux Modulation Scheme for 3-Leg Core Transformer Based 3-Phase AC–DC Topologies

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***Abstract*—Existing single-stage 3-phase ac–dc isolated topologies typically use three separate C-core high-frequency transformers (HFTs), which require significant space and reduce power density. A key challenge preventing the use of a more compact 3-leg core HFT is the lack of suitable modulation schemes, as current methods do not ensure a zero net flux condition considering all 3 legs. Violating this condition can lead to stray fluxes that induce common mode (CM) currents and high peak magnetizing currents, resulting in increased electromagnetic interferences and losses. This article proposes a new modulation scheme that, by strategic alignment of switching pulses for a dual inverter setup, both avoids CM winding voltage generation and preserves the shape of transformer secondary-side voltage waveforms for power transfer at twice the carrier frequency. These features allow the use of a single compact 3-leg core HFT. The scheme also offers: 1) high-quality 3/5-level ac pulse-width modulated grid voltages, 2) a 3-level high-frequency voltage for the power transmitted via transformer action, 3) higher overall average winding volt–seconds compared to dual active bridge converters at low modulation indices, and 4) reduced switching losses due to the discontinuous nature of the scheme. Adopting a 3-leg core can cut the size of 3 C-core designs by 35%–40% while achieving 4% total current harmonic distortion at full load. The presented modulation scheme is verified using both simulation and experimental results for a 250 V_{dc}, 122 V_{ac}, 750 W prototype.**

***Index Terms*—3-Leg core high-frequency transformer (HFT), ac–dc converter, pulse-width modulation (PWM) converters, standard discontinuous PWM (SDPWM), zero common mode (CM) winding voltage.**

I. Introduction

DC SYSTEMS are revolutionizing ac–dc conversion technology. Key sectors, including utility grids, electric vehicles, data centers, and industrial systems, are increasingly adopting dc infrastructure [1]. The emergence of Silicon Carbide switches, with higher pulse-to-continuous current ratios, has paved the way for innovative topologies. These new designs enhance power density in isolated ac–dc converters, improving their effectiveness in high-performance applications.

The footprint of an isolated ac–dc converter is influenced by factors such as the size of the high-frequency transformer (HFT), grid interface reactors, number of switches, modularity, and the modulation scheme. Topologies that use 6-switch, 2-level voltage-sourced converter (VSC) modules offer advantages like simplicity, lower cost, and a more compact design. In a well-designed system, using power switches with active or passive cooling can further minimize weight and space requirements compared to magnetic components [2].

Recently, single-stage 3-phase topologies have garnered significant interest due to their compact design and fewer conversion stages [3]. In a single-stage topology, the primary side handles both the grid current and the high-frequency (HF) current, simplifying the overall system. However, the vast majority of existing works utilize three separate C-core HFT designs [1], [3], [4], [5], [6], [7], [8], [9] that limits the potential savings in overall

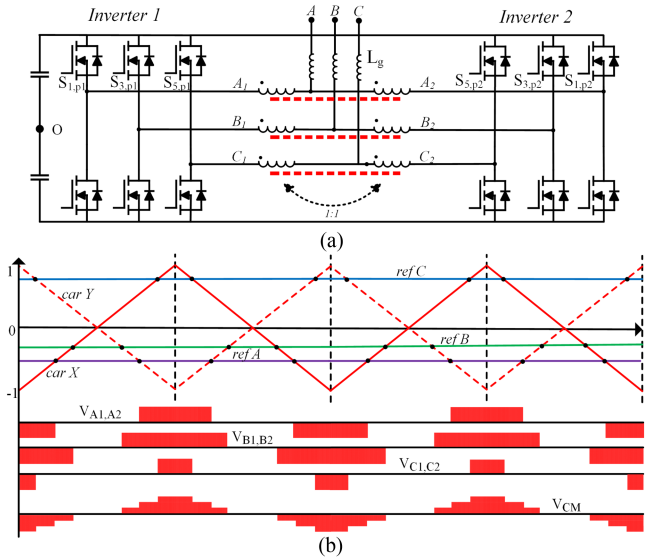

Fig. 1. Conventional 3-phase DP-VSCs arrangement (a) circuit shown with coupled inductors or grid side center-tapped transformer winding (b) differential winding voltages and CM winding voltage generated from conventional sinusoidal PWM with 180° interleaved carriers.

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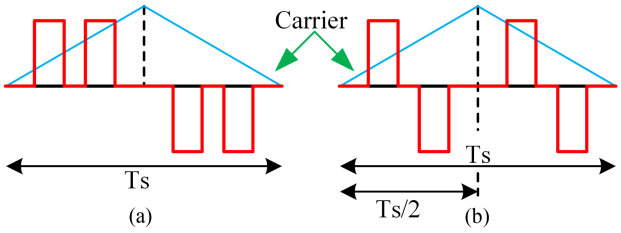


Fig. 2. HF voltage waveform shapes. (a) Unflipped version. (b) Flipped version (FDPWM1).

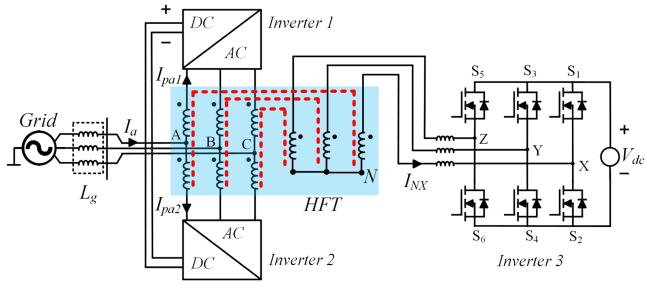


Fig. 3. Isolated ac–dc converter with DP-VSCs on primary side and wye connected secondary side windings.

footprint that can be achieved. A 3-leg core is used for the ac–dc topology in [10], however, the adopted modulation scheme results in tightly coupled dynamics between the ac and dc sides. Adopting one physical 3-leg core HFT instead of three separate C-core HFTs can significantly increase the power density and reduce core losses. But to date, the use of a 3-leg core HFT has been restrained by the existing modulation schemes that cannot provide zero net flux inside the 3-leg core structure at all times. The inability to guarantee zero net flux conditions can cause stray fluxes that induce common mode (CM) currents and high peak magnetizing currents, potentially saturating some parts of the core and leading to high electromagnetic interferences.

The grid-side power conversion circuit utilizing dual parallel VSCs (DP-VSCs), shown in Fig. 1(a), has been widely used in various applications, such as increasing drive power ratings [11], isolated ac–dc converters [1], isolated ac–ac converters [12], and bipolar dc systems [13].

Almeida et al. [1] and Chambayil and Chattopadhyay [7] implemented the DP-VSCs circuit in Fig. 1(a) for the primary side (grid side) with three separate C-core HFTs to provide isolated ac–dc conversion. For each grid phase, two inverter legs are switched with carriers 180° apart using sinusoidal modulation producing a 3/5-level pulsewidth modulation (PWM) voltage at the ac output and a 3-level HF differential voltage across the two inverter legs. The three HF differential voltages ($V_{A1,A2}$, $V_{B1,B2}$, and $V_{C1,C2}$) generate a nonzero CM voltage, see V_{CM} in Fig. 1(b). Consequently, due to the adopted sinusoidal modulation scheme in [1,7], the instantaneous sum of these three voltages is not always equal to zero, which would result in nonzero net flux in a 3-leg core, necessitating the use of three C-core HFTs to provide independent flux paths for each phase. However, with a DP-VSC arrangement for the grid side transformer windings, it is possible to achieve zero net flux conditions by strategically choosing the switching patterns of the two VSCs, enabling use of a single 3-leg HFT. Such modulation strategies have been developed in the past [11] but were limited to only non-isolated applications using coupled inductors and not for HF power transfer via transformer action. These schemes produce winding voltages that either have reduced average winding volt–seconds (a measure of voltage utilization) limiting HF power transfer capability, or operate at variable frequencies, affecting magnetic core size.

This work overcomes the aforementioned challenges by developing a modulation scheme that allows use of compact 3-leg core HFTs for the general class of isolated ac–dc systems in Fig. 1(a), where the primary side utilizes DP-VSCs. It features zero CM winding voltage generation, 3/5-level PWM voltages at the ac output, 3-level HF transformer winding voltages with constant frequency operation, an average winding volt–seconds similar to modified DPWM [11], and preserved wave-shape of HFT voltages at the secondary-side where only a single VSC is needed. Moreover, a discontinuous modulation approach is adopted that offers reduced primary side switching losses.

II. Proposed Modulation Scheme: Flipped DPWM1 (FDPWM1)

This section presents the proposed modulation scheme, termed FDPWM1 (flipped discontinuous PWM). "Flipped" refers to the action of inverting one of the pulses per polarity while maintaining the same quality ac PWM voltages. See Fig. 2(b) (flipped) and Fig. 2(a) (unflipped). This results in a single positive pulse per polarity per HF cycle, effectively doubling the HF voltage waveform frequency compared to the carrier frequency.

A. Isolated AC–DC Topology Under Study

The isolated ac–dc topology under study in this work is shown in Fig. 3, which features DP-VSCs on the grid (primary) side and one VSC on the dc (secondary) side. The secondary windings are wye connected to facilitate matching of the HF voltage waveforms created on the primary and secondary sides. The flux generated by the grid currents cancel out, due to the orientation of the center-tapped windings, resulting in only HF flux within the HFT [1]. The 3-leg HFT windings orientation and electrical connections are shown in Fig. 4. To facilitate HF power transfer via transformer action, external inductors are added in series with the secondary side inverter terminals.

B. Proposed FDPWM1 Scheme With Zero Net Flux Generation

Each primary transformer winding in Fig. 4 can be excited positively, negatively, or short circuited by the DP-VSC configuration in Fig. 3. Many PWM switching patterns can be potentially used, however their applicability for a 3-leg core HFT is decided by the (voltage driven) magnetic flux inside the core. The magnetic flux generated by a CM winding voltage could

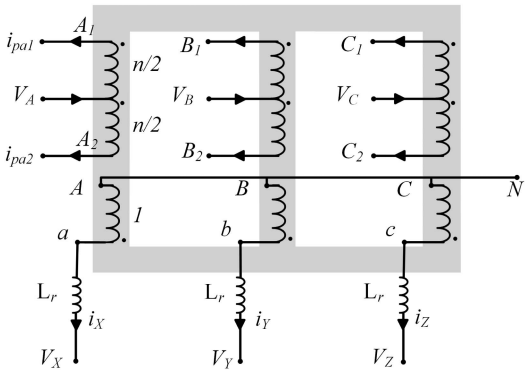


Fig. 4. 3-Leg HFT and its connections for the topology in Fig. 3.

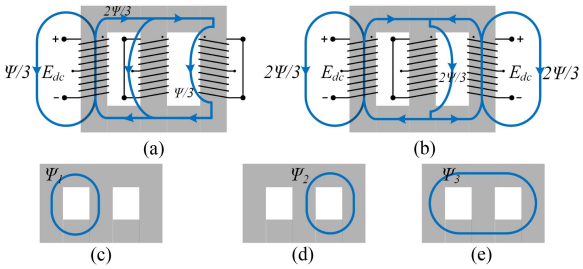


Fig. 5. Undesirable winding excitation states with stray fluxes moving out from the core through leakage paths: (a) 2 phases short circuited and other excited (b) 2 phases excited with same polarity and other short circuited. Desirable 3-leg core flux paths, i.e. zero net flux conditions: (c) path 1, (d) path 2, and (e) path 3. (Only primary side windings are illustrated.)

produce unbalanced flux ($\sum \psi \neq 0$) that is forced to leave the core, resulting in stray magnetic fields [see Fig. 5(a), (b)].

The compatibility of a specific PWM scheme with a 3-leg core can be guaranteed by keeping the sum of primary side winding voltages equal to zero, i.e., $V_{\text{CM}} = (V_{A1,A2} + V_{B1,B2} + V_{C1,C2})/3 = 0$ where V_{CM} is the winding CM voltage. The secondary side windings follow the same pattern with or without a phase shift. Fig. 5 illustrates both the undesirable winding excitations and desirable 3-leg core flux paths.

The classical standard discontinuous PWM (SDPWM) approach can be used as a starting point to derive the proposed FDPWM1 scheme that avoids the undesirable winding excitation states in Fig. 5(a) and (b). In SDPWM, one phase out of three modulating signals is held high or low for 60° and the other two produce PWM signals. Comparing these signals with inverse carriers [11] creates a 3-level PWM pattern.

First, a 60° sample period (a sector) is selected in Fig. 6(a), where one signal is clamped high/low. As the clamped signal cannot generate a PWM pattern, the other two signals impose the magnetic core excitation. Observing the nature of the other two signals in a sector, especially how one signal's mirror image is equal to the other over the cross-over line [see Fig. 6(a)], reveals that a combination of an average and a difference signal can create an altered switching pattern while maintaining the same volt–seconds over a carrier cycle. As illustrated in Fig. 6, ref *B* and ref *C* are used to create ref *M*, representing the average. Another bipolar reference signal, ref *N*, is created representing the absolute difference between ref *B* and ref *C*. For sector 1 and

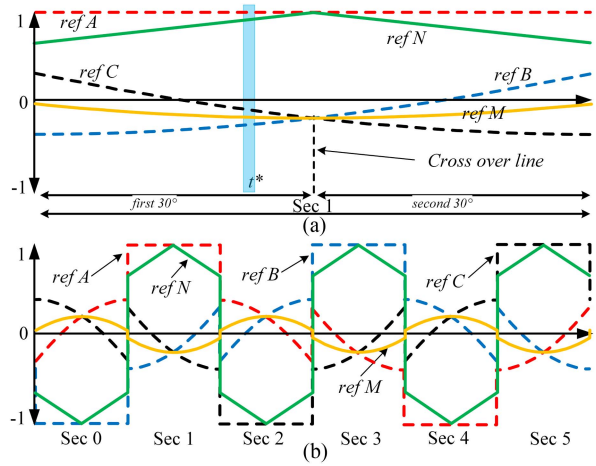


Fig. 6. Ref *A*, ref *B*, ref *C* from SDPWM; ref *M* and ref *N* for FDPWM1, (a) Spanned over the sector 1 and (b) spanned over a complete grid cycle.

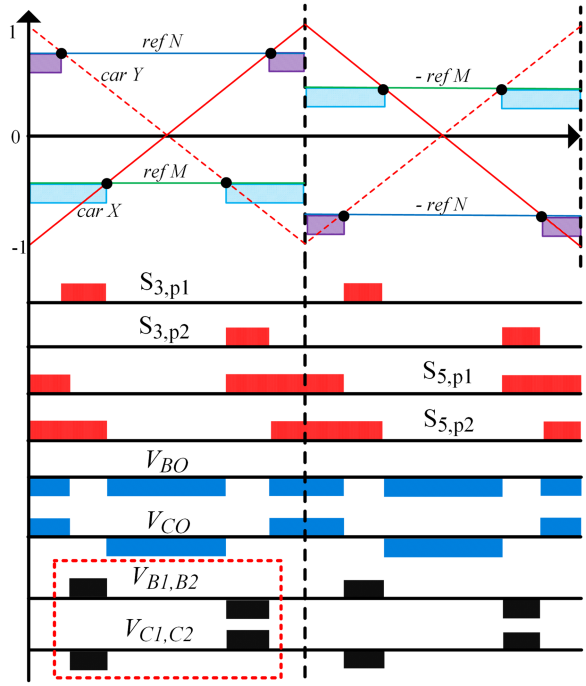


Fig. 7. FDPWM1: Final switching pattern with ref *M* and ref *N*.

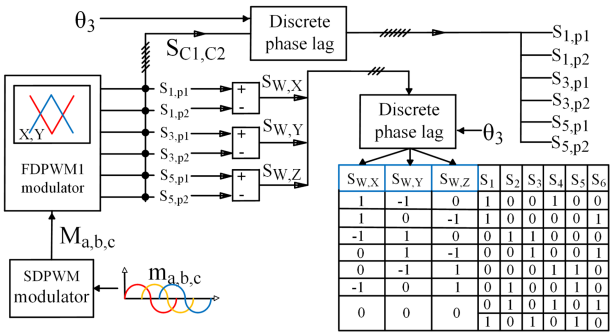
sector 4, the two new references can be represented as follows:

$$\text{ref}M_{\text{sec1,sec4}} = (\text{ref}B + \text{ref}C)/2 \tag{1}$$

$$\text{ref}N_{\text{sec1}} = 1 - |(\text{ref}B - \text{ref}C)/2| \tag{2}$$

$$\text{ref}N_{\text{sec4}} = -1 + |(\text{ref}B - \text{ref}C)/2|. \tag{3}$$

Hereinafter, without the loss of generality, PWM generation at time instant t^* in Fig. 6(a) is discussed. Ref *M* together with inverse carrier interleaved PWM is then used to generate an average switching pattern for phases *B* and *C* (see Fig. 7 light blue pulses on carriers). Inverting the ref *M* and ref *N* during the second carrier half (180°–360°) changes the waveform shape from unflipped to flipped, doubling the frequency of the winding voltage (see Fig. 7). Identical PWM output voltages are created



$S_{W,X}$	$S_{W,Y}$	$S_{W,Z}$	S_1	S_2	S_3	S_4	S_5	S_6
1	-1	0	1	0	0	1	0	0
1	0	-1	1	0	0	0	0	1
-1	1	0	0	1	1	0	0	0
0	1	-1	0	0	1	0	0	1
0	-1	1	0	0	0	1	1	0
-1	0	1	0	1	0	0	1	0
0	0	0	0	1	0	1	0	1
			1	0	1	0	1	0

Fig. 8. Secondary side gating system with the lookup table, θ_3 corresponds to the phase shift.

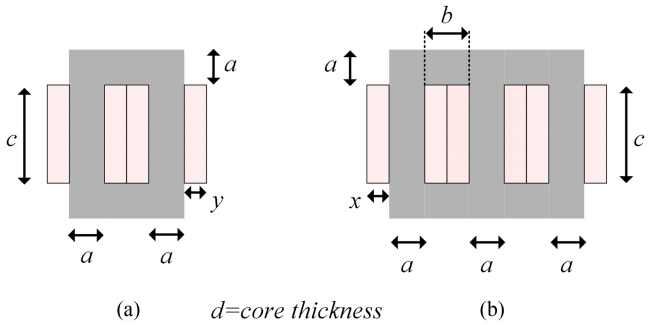


Fig. 9. Comparing the core volumes for similar power and voltage rating. (a) Equivalent C-core HFT per phase. (b) 3-Leg core HFT.

at phase outputs determined by the ref *M*. Then, ref *N* is used to create the difference between average PWM patterns relative to the average value of ref *B* and ref *C*. For that, pulses created from ref *N* (see Fig. 7 purple pulses on carriers) are subtracted from phase B gate signals ($S_{3,p1}$, $S_{3,p2}$) to minimize the switch on time and added to phase C gate signals ($S_{5,p1}$, $S_{5,p2}$) to maximize switch on time (see Fig. 7). This results in PWM output voltages that are related to magnitudes of ref *B* and ref *C*. The winding voltages ($V_{B1,B2}$, $V_{C1,C2}$) are perfectly aligned with a 180° phase shift, yielding $V_{B1,B2} + V_{C1,C2} = 0$ (see Fig. 7). The PWM logic for two references are flipped during the second 30° duration of each sector since one signal's mirror image is equal to the other signal over the cross-over line. At the same instant, the carriers are also flipped to avoid repetitive pulses on the differential winding voltages. This helps to maintain a fixed frequency operation for voltages $V_{A1,A2}, V_{B1,B2}$, and $V_{C1,C2}$ at twice the carrier frequency. The references are updated discretely every half carrier cycle either at 1 or -1. This guarantees no net average volt–sec within a winding voltage cycle, hence avoiding dc saturation of the HFT.

Fig. 8 illustrates gate signals generation for the wye-connected VSC at the secondary side. Normalized primary side voltages ($S_{W,X}$, $S_{W,Y}$, and $S_{W,Z}$) are represented by six active and two null vectors in a lookup table. Power transfer from primary to secondary through the HFT uses the base switching pattern ($S_{C1,C2}$) for the primary VSCs and a delayed version for the secondary. For reverse power flow conditions, the base pattern ($S_{C1,C2}$: see Fig. 8) controls the secondary VSC, while the delayed version controls the primary.

C. HFT Core Volume Savings

In Fig. 3, utilizing a single 3-leg HFT in place of three separate C-core HFTs offers significant volume savings. This section provides an estimate of the expected savings for the assumed structures in Fig. 9. Since the magnetic flux is driven by voltage, in the following analysis, the cross-sectional areas of the C-core and the 3-leg core are assumed to be equal.

Each C-core HFT would handle one-third of the total power, whereas a 3-leg core HFT would process the total power of all three phases. Consequently, the copper volume in one C-core HFT must be approximately equal to the copper volume in a single leg of the 3-leg HFT [14]. By equating these two copper volumes, we derive the dimensional relationship $\sqrt{2}y \simeq x$ where $b = 2x$. Given these conditions, the volume ratio between 3-leg HFT and three C-core HFTs can be quantified as follows:

$$V_{\text{ratio},p.u} = \left[\frac{6a + 3c + 8x}{12a + 6c + 6\sqrt{2}x}\right] \tag{4}$$

where *a, b, c*, and *d* are dimensions that can be taken from standard data sheets for amorphous 3-leg cores. To account for coil former volumes and clearances, the volume ratio is increased by 10%, and the volume savings are calculated as $(1 - 1.1V_{ratio,p.u})\%$. Based on the data provided in data sheets for amorphous 3-leg cores, a volume savings of 35%–40% was confirmed for a standard range of 3-leg cores. The custom 3-leg core HFT used in the experiments, constructed with amorphous material, achieved volume savings of 38.1%, with $a = 10$ mm, $b = 14$ mm, $c = 40$ mm, and $d = 25$ mm.

III. Simulation and Experimental Results

The proposed FDPWM1 scheme was simulated in PLECS and experimentally validated using a 750 W prototype, with a 250 V dc-link voltage, 0.8 modulation index, and 20 kHz carrier frequency (yielding a transformer operating frequency of 2×20 kHz$= 40$ kHz). The experimental setup including the constructed 3-leg core HFT is given in Fig. 10.

The HFT turns ratio was set to 1:1:1 (n=2) to equalize the dc-link voltages. The HFT has been carefully designed to minimize leakage inductance between the primary and secondary windings for each phase. Unequal leakage inductances between phases could result in an imbalance in HF power transfer. This issue is addressed in this work through the use of externally connected inductances L_r (see Fig. 4) and minimizing the leakage inductances of the HFT. The design ensures that both the primary and secondary windings of the same phase are placed on the same leg, with interlayered windings employed to achieve a tight coupling between the primary and secondary windings. A 3-leg amorphous core was selected for the HFT. Due to the increased core losses above 50 kHz, the operating frequency for HF power transfer was limited to 40 kHz. The winding average volt–seconds were analyzed to assess the power transfer capability. A higher average volt–seconds product enables greater power transfer. When comparing different PWM schemes, it is

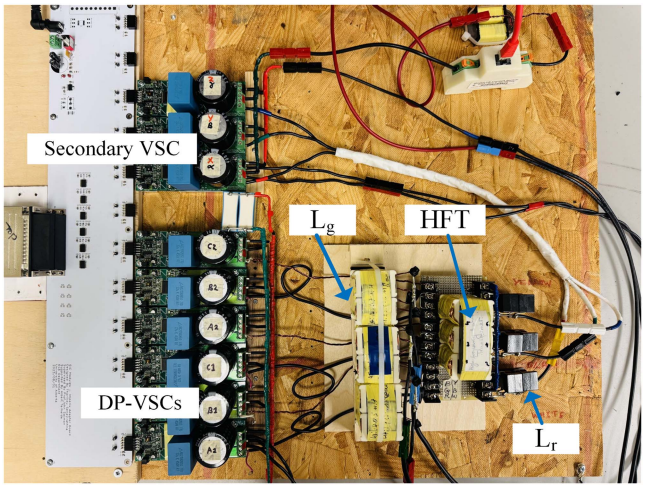


Fig. 10. Experimental setup of the isolated ac–dc converter featuring a 3-leg HFT constructed from amorphous material.

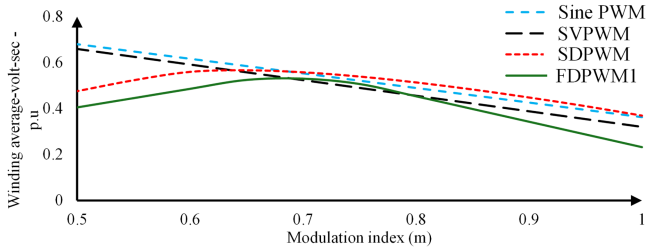


Fig. 11. Winding average volt–sec in p.u per phase (averaged over a grid cycle since pulse widths are affected by instantaneous grid angle).

crucial to analyze the winding average volt–seconds under the same voltage levels to accurately evaluate the impact of PWM strategies on power transfer capability. The isolated single-stage 3-phase ac–dc system in [1] is simulated to compare the performances of 1) sine PWM, 2) space vector PWM, 3) SDPWM, and 4) proposed FDPWM1; results are shown in Fig. 11 on a per-phase normalized basis. Observe that all schemes perform similarly between modulation indices of 0.7 and 0.8. A net winding average volt-seconds of 1.35 (0.45×3, due to 3-phase structure) is produced at $m = 0.8$ which is equal to [1] and 0.35 higher compared to the traditional solution, which is an active rectifier followed by a dual active bridge.

The experimental results presented in Fig. 12 confirm the feasibility of the proposed modulation scheme, demonstrating 3/5-level PWM output voltages, the HF voltages and currents, along with the grid current (I_a) and inverter current ($I_{p,a1}$). Fig. 13 illustrates the HF voltages on the primary with negligible CM winding voltage enabling the operation of the 3-leg core HFT, i.e., $V_{\text{CM}} = 0$ at all times. Bi-directional power transfer through the HFT is also confirmed in Fig. 14. A comparison of various modulation schemes for the DP-VSCs architecture is presented in Table I. The schemes that generate winding CM voltages (#1-3) are not suitable for use with a 3-leg core HFT. Moreover, the schemes that results in variable frequency operation (operating point dependent) for the winding differential voltages (#4-5) would require significant

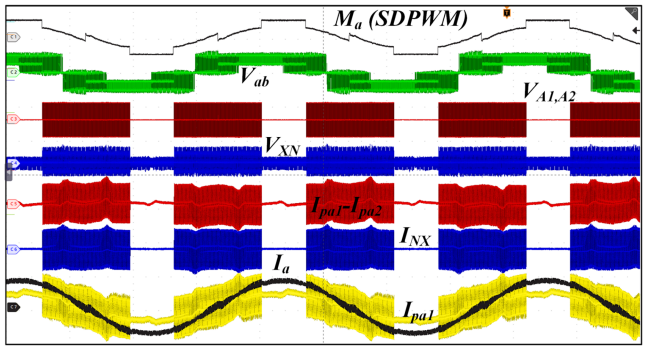


Fig. 12. Experimental waveforms from topology: SDPWM Modulation signal, PWM line voltage, primary HF voltage, secondary HF voltage, primary HF current, secondary HF current, primary inverter phase A current and phase A grid current (Ch1: 2 V/div, Ch2, Ch3, and Ch4: 500 V/div, Ch5, and Ch6:10 A/div, Ch7, and Ch8:5 A/div,and time 4 ms/div).

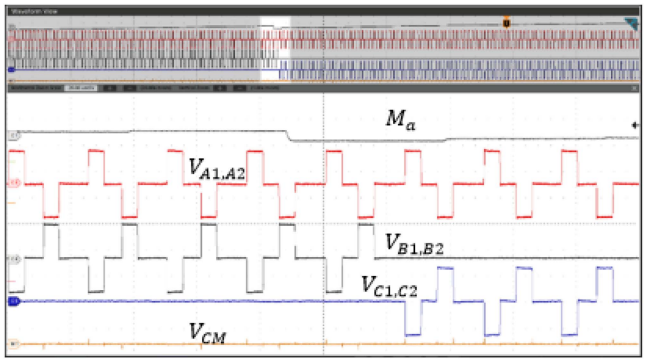


Fig. 13. Experimental waveforms of primary winding voltages. Waveforms expanded over 4 ms, horizontal zoom scale 20 μs/div (Ch1: M_a, Ch2: $V_{A1,A2}$, Ch3: $V_{B1,B2}$, Ch4: $V_{C1,C2}$, and Ch5: V_{CM} all channels in 200 V/div).

TABLE I
COMPARISON OF MODULATION SCHEMES FOR DP-VSCS OPERATING WITH 180° INTERLEAVED CARRIERS

#	Modulation Scheme	Average winding Volt-secs at $m_a = 0.8$	winding CM voltages	Frequency of winding differential voltages
1	Sinusoidal PWM [1], [7]	0.489	Yes	fixed (CF)[1]
2	Space vector PWM	0.456	Yes	fixed (CF)
3	Standard DPWM	0.513	Yes	fixed (CF)
4	Modified DPWM [11]	0.453	No	varying (CF-2CF)
5	PWM2 [11]	0.405	No	varying (CF-2CF)
6	PWM3 [11]	0.38	No	fixed (CF)
7	This work (FDPWM1)	0.453	No	fixed (2CF)

over-rating of the transformer core to avoid saturation. Among the listed modulation schemes, FDPWM1 achieves the highest average winding volt–seconds with zero CM winding voltage generation and is the only one that can produce differential winding voltages at a fixed frequency equal to twice the carrier frequency, leading to the most compact 3-leg core HFT design.

[1]CF corresponds to carrier frequency.

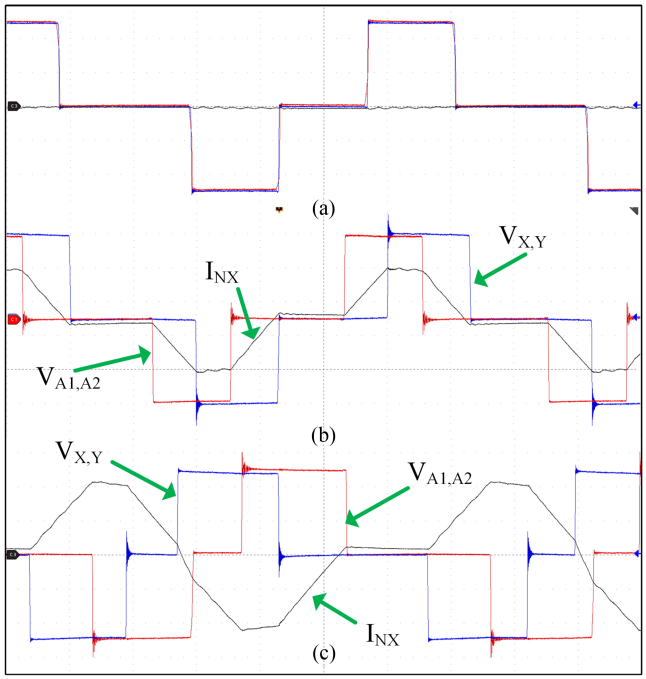


Fig. 14. Experimental HF waveforms for bi-directional power flow: (a) no power flow, (b) AC to DC power flow, and (c) DC to AC power flow (voltage scale 100 V/div, current 5 A/div, time 4 μs/div).

IV. Conclusion

A novel modulation technique for bidirectional HF isolated ac–dc converters utilizing DP-VSCs is presented that allows use of more compact 3-leg core HFT designs, by guaranteeing zero CM voltage generation at all times. The proposed technique achieves other key benefits, including generating 3/5-level ac PWM voltage at the ac output, 3-level HF voltage for HF power transfer, and increased winding volt-seconds, particularly at low modulation indexes compared to traditional dual active bridge converters. The elimination of CM winding voltages is necessary to exploit 3-leg core HFT devices that can reduce the size of conventional 3, C-core designs by 35%–40% while achieving 4% total current harmonic distortion at full load. Moreover, the synthesized differential HF winding voltages responsible for power transfer are at twice the carrier frequency, yielding a more compact design. Both simulation and experimental results verify the practical efficacy of the proposed modulation scheme for applications where a compact converter footprint is key.

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