A Novel Adaptive Model Predictive Current Control for Three-Level Simplified Neutral-Point-Clamped Inverter With Carrier-Based Modulation

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***Abstract*—This article proposes an adaptive model predictive current control for three-level simplified neutral-point-clamped inverter (3L-SNPCI), which eliminates the model dependence problem of the conventional model predictive current control (MPCC). The system parameter is estimated by a new observer with high accuracy and fast convergence. The observed parameter is then utilized by the deadbeat MPCC to attain accurate reference voltage vector calculation, achieving low computational burden and constant switching frequency. Furthermore, a novel carrier-based space vector modulation (CBSVM) is proposed to synthesize the reference VV for 3L-SNPCI. Compared to the existing space vector modulation schemes of 3L-SNPCI, the proposed CBSVM reduces the hardware implementation cost while ensuring the neutral point voltage balance. Experimental results are presented to verify the validity of the proposed method.**

***Index Terms*—Carrier-based space vector modulation (CBSVM), deadbeat, model predictive current control (MPCC), parameter observer, three-level simplified neutral point clamped inverter (3L-SNPCI).**

I. Introduction

In THE past decade, the multilevel inverters have been increasingly employed in renewable generation, energy storage systems and electrical drives owing to their advantages of effectively reducing harmonics and undertaking higher dc bus voltage [1], [2], [3], [4]. Among them, the conventional three-level neutral-point clamped inverter (3L-NPCI) and T-type 3L-NPCI are widely used in industry [5], [6]. Nevertheless, the high semiconductor counts of these two topologies indicate high hardware costs compared to the two-level inverters. One feasible solution to further remove two active switches and their driver circuits compared to the T-type 3L-NPCI is to utilize the three-level simplified neutral point clamped inverter (3L-SNPCI) [7]. Unlike the 3L-NPCI and T-type 3L-NPCI, the 3L-SNPCI does not have medium voltage vectors (VVs) in its space vector diagram. Consequently, it has alleviated neutral point voltage (NPV) fluctuations.

Despite these benefits, the control and modulation of 3L-SNPCI remain as two key challenges on its applications. On one hand, the existing control approaches for three-level dc/ac inverters suffer from some common problems, such as variable switching frequency, model dependence, and/or sluggish dynamic responses. For instance, a direct current control is proposed for the grid-connected 3L-NPCI [8], which achieves equal switching frequencies in three phases. However, its average switching frequency varies with the modulation index. To address this issue, a digital hysteresis current controller that combines a mixed-level scheme and prediction-based sampling is adopted in [9]. Unfortunately, this controller results in higher current harmonics. After measuring the average inverter output voltages, another hysteresis-based current control [10] is proposed, which maintains a nearly constant switching frequency by varying the hysteresis band according to the output voltages. However, the NPV balancing issue is not discussed in [10].

Apart from the afore-mentioned hysteresis controllers, the model predictive control (MPC) is increasingly employed to regulate the three-level inverters due to its fast dynamics and straightforward configuration [11], [12], [13]. Nonetheless, these methods result in variable switching frequencies, which require large filters or high sampling frequency to attenuate the harmonics. To improve the performance, two modulated MPCs with fixed switching frequency are proposed in [14]. This article divides the space vector diagram into 24 sectors and the duty cycles of VVs are calculated by minimizing the weighted errors of each sector. However, it produces limited performance improvement compared to [11] and [12]. Furthermore, numerous predictions and optimizations cause heavy computational burdens as all sectors need to be evaluated. The same problem is also experienced by other methods [15], [16]. To reduce the computational complexity of MPC for multilevel inverters, the fast predictive current control methods based on the

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deadbeat principle are proposed in [17] and [18]. Noticeably, the weighting factor is eliminated in these methods through the application of redundant VVs. Nevertheless, these methods are highly dependent on model parameters. Moreover, they cannot be directly applied to the 3L-SNPCI because of changes in sectors when medium VVs are missing. To mitigate the model dependence issue, Abdelrahem et al. [19] combined the finite control set MPC with an extended Kalman filter for online parameter estimation, which is robust to the parameter mismatches. Unfortunately, the computational burden of [19] is large. Therefore, Zhang et al. [20] proposed another online inductance identification technique based on the gradient correction method and verifies its efficacy in predictive power control. Furthermore, a forgetting-factor-based least squares method is proposed in [21] to estimate the filter inductance in a plug-in manner. The authors in both [20] and [21] achieved solid estimation performance, which are computationally efficient. However, the dynamic time responses of convergence in these two methods are relatively gradual.

On the other hand, most of the existing modulation schemes for the 3L-SNPCI are not carrier based [11], [22], and [23], which generally result in large current harmonics or high implementation cost. For example, an MPC algorithm is utilized to regulate the 3L-SNPCI in [11]. It applies only one VV in each switching period and hence, suffers from severe harmonic distortions. Even when six virtual medium VVs are synthesized to increase the control freedom of MPC in [22], the current harmonics are still relatively high. A space vector modulation (SVM) scheme is proposed for the 3L-SNPCI in [23], which provides low total harmonic distortions. However, an extra complex programmable logic device (CPLD) is needed to implement this scheme since it is noncarrier-based, leading to increased hardware costs. Although a carrier-based SVM applying different switching sequences to balance NPV is introduced in [24], it makes transitions jump between two large VVs, which is inappropriate in the 3L inverter.

To address the aforementioned issues encountered by the existing 3L-SNPCI control and modulation approaches, this article proposes a new adaptive model predictive current control (AMPCC). Its control block diagram is depicted in Fig. 1. The proposed AMPCC attains small THD, low computational burden and constant switching frequency while eliminating the model dependence problem of the mentioned MPCC with accurate estimation and fast convergence. Furthermore, a novel carrier-based SVM strategy is proposed to synthesize the reference VV, which utilizes a low sampling frequency in all sectors and simultaneously guarantees the NPV balance. In addition, it simplifies the implementation by effectively reducing hardware costs.

The rest of this article is organized as follows. Section II presents the topology of 3L-SNPCI and its mathematical model. Then, the proposed AMPCC is elaborated in Section III. Subsequently, a novel carrier-based SVM for 3L-SNPCI is presented in Section IV. After that, experimental results are shown in Section V to verify the effectiveness of the proposed method. Finally, Section VI concludes this article.

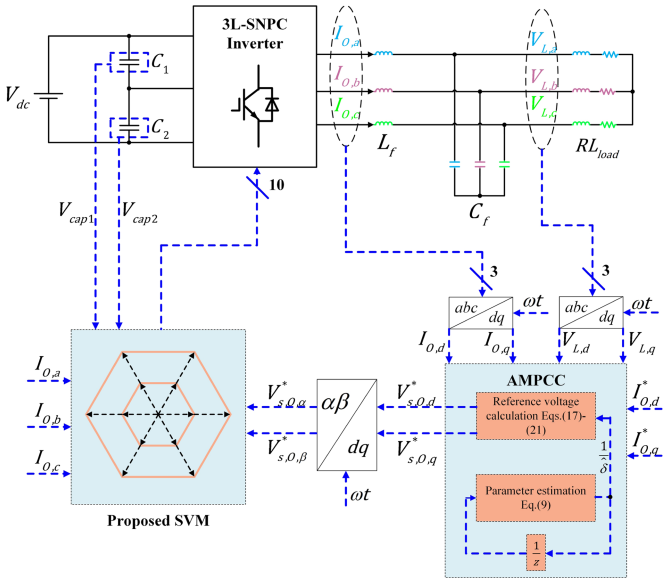

Fig. 1. Control block diagram of the proposed method.

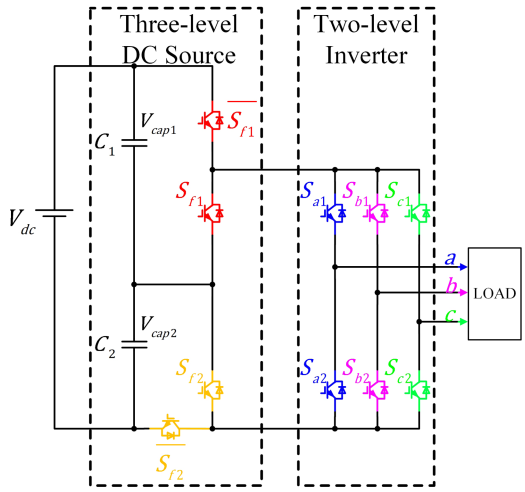

Fig. 2. Circuit diagram of 3L-SNPC inverter.

II. Topology of 3L-SNPC Inverter and Its Mathematical Model

A. Topology of 3L-SNPC Inverter

The topology of the 3L-SNPC inverter is shown in Fig. 2. The four switches S_{f1}, $\overline{S_{f1}}$, S_{f2}, and $\overline{S_{f2}}$ in the left dashed block of Fig. 2 generate three distinct voltage levels ($V_{\rm dc}/2$, 0, $-V_{\rm dc}/2$). Then, the conventional three-phase two-level inverter in the right dashed block applies these voltage levels to three-phase loads, resulting in the space vector diagram in Fig. 3. It is apparent that there are only large and small VVs shown in Fig. 3, whereas the medium VVs are absent.

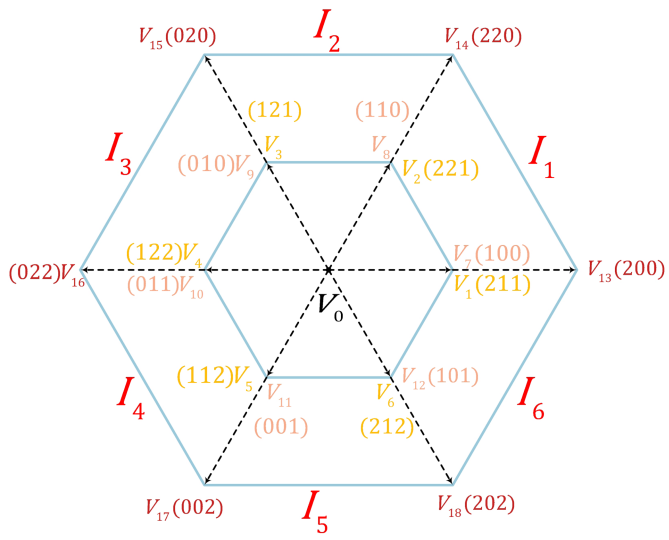

Fig. 3. Space vector diagram of 3L-SNPC inverter.

B. Mathematical Model

The mathematical model of 3L-SNPCI in the rotating d, q-reference frame can be described as

$$\begin{cases} \frac{dI_{O,d}}{dt} = \omega I_{O,q} - \frac{R_f}{L_f} I_{O,d} - \frac{1}{L_f} V_{L,d} + \frac{1}{L_f} V_{O,d} \\ \frac{dI_{O,q}}{dt} = -\omega I_{O,d} - \frac{R_f}{L_f} I_{O,q} - \frac{1}{L_f} V_{L,q} + \frac{1}{L_f} V_{O,q} \end{cases} \tag{1}$$

where L_f and R_f are the inductance and parasitic resistance of the filter inductor, respectively. $I_{O,d}$ and $I_{O,q}$ are inverter output currents in d and q axes. ω is the angular velocity. $V_{L,d}$ and $V_{L,q}$ are the load voltages in d and q axes, and $V_{O,d}$ and $V_{O,q}$ are the inverter terminal voltages.

Applying the forward Euler method [19], [25], the discretized model of 3L-SNPCI can be derived as

$$I_{O,k+1} = A_d I_{O,k} + B_d V_{O,k} + D_d V_{L,k} \tag{2}$$

where

$$I_{O,k} = \begin{bmatrix} I_{O,d,k} \\ I_{O,q,k} \end{bmatrix}, \quad I_{O,k+1} = \begin{bmatrix} I_{O,d,k+1} \\ I_{O,q,k+1} \end{bmatrix}$$

$$V_{O,k} = \begin{bmatrix} V_{O,d,k} \\ V_{O,q,k} \end{bmatrix}, \quad V_{L,k} = \begin{bmatrix} V_{L,d,k} \\ V_{L,q,k} \end{bmatrix}$$

and

$$A_d = \begin{bmatrix} 1 - \frac{R_f T_s}{L_f} & \omega T_s \\ -\omega T_s & 1 - \frac{R_f T_s}{L_f} \end{bmatrix}$$

$$B_d = \begin{bmatrix} \frac{T_s}{L_f} & 0 \\ 0 & \frac{T_s}{L_f} \end{bmatrix}, \quad D_d = \begin{bmatrix} -\frac{T_s}{L_f} & 0 \\ 0 & -\frac{T_s}{L_f} \end{bmatrix}.$$

In the above-mentioned equations, T_s denotes the sampling period. $I_{O,d,k+1}$ and $I_{O,q,k+1}$ are the predicted inverter output current at $(k+1)$th time instant.

III. Proposed AMPCC

A. Adaptive Observer

In this section, a novel adaptive observer is introduced for the estimation of the filter inductance L_f. It is emphasized that R_f shows negligible influence on the control performance of 3L-SNPCI due to its very small amplitude and therefore, does not need to be estimated. First, the inverter output current observer can be designed based on the mathematical model in (2) as

$$\begin{aligned} \widehat{I}_{O,k+1} = \widehat{I}_{O,k} + \mathrm{P}_{d,k} + \mathrm{T}_{d,k}\widehat{\delta}_{k+1} \\ + K_k e_k + (\Psi_k - K_k \Psi_k)\gamma_{k+1} \end{aligned} \tag{3}$$

where

$$\mathrm{P}_{d,k} = \begin{bmatrix} \omega I_{O,q,k} T_s \\ -\omega I_{O,d,k} T_s \end{bmatrix}$$

$$\mathrm{T}_{d,k} = \begin{bmatrix} (-R_f I_{O,d,k} - V_{L,d,k} + V_{O,d,k}) T_s \\ (-R_f I_{O,q,k} - V_{L,q,k} + V_{O,q,k}) T_s \end{bmatrix}$$

and $\widehat{\delta}_{k+1}$ is the updated estimation of filter inductance in reciprocal form. $e(k) = I_{O,k} - \widehat{I}_{O,k}$ is the estimation error of inverter output current. γ_{k+1} represents the difference between $\widehat{\delta}_{k+1}$ and $\widehat{\delta}_k$. To construct a recursive updating scheme for a supplementary variable η_k, Ψ obeys the following dynamics:

$$\Psi_{k+1} = I\left(1 - K_k\right)\Psi_k + \mathrm{T}_{d,k}, \quad \Psi_0 = 0. \tag{4}$$

The correcting factor $K_k > 0$ is introduced to construct the forgetting factor $(1 - K_k)$, which aims to alleviate the influence of estimation errors from preceding cycles. In accordance with (3) and (4), the dynamics of states prediction error can be subsequently derived

$$\begin{aligned} e_{k+1} = e_k + \mathrm{T}_{d,k}\widehat{\delta}_{k+1} - K_k e_k \\ + (K_k \Psi_k - \Psi_k)\gamma_{k+1} \end{aligned} \tag{5}$$

where $\overline{\delta}_k = \delta - \widehat{\delta}_k$ represents the error between the estimated value $\widehat{\delta}_k$ and its true value δ. Then, the complementary variable η_k is formulated to signify the estimation progress of $\widehat{I}_{O,k}$ and $\widehat{\delta}_k$

$$\eta_k = e_k - \Psi_k \overline{\delta}_k. \tag{6}$$

The dynamics of complementary variable (7) can be deduced from (4), (5), and (6)

$$\eta_{k+1} = \eta_k - K_k \eta_k, \quad \eta_0 = e_0. \tag{7}$$

To achieve rapid observer convergence, an identifying variable is introduced as follows:

$$\varphi_{k+1} = \varphi_k + \Psi_k^T \Psi_k, \quad \varphi_0 = \alpha I \tag{8}$$

where α is an extremely small positive number. Subsequently, the parameter updating mechanism is obtained from (3), (4), (7), and (8)

$$\widehat{\delta}_{k+1} = \widehat{\delta}_k + \varphi_k^{-1} \Psi_k^T H_k \left(e_k - \eta_k\right) \tag{9}$$

where

$$H_k = (I + \Psi_k \varphi_k^{-1} \Psi_k^T)^{-1}.$$

To guarantee that $\widehat{\delta}$ is always located in the initially defined set E, $\widehat{\delta}_{k+1}$ is adjusted by

$$\widetilde{\delta}_{k+1} = L\left(\widehat{\delta}_{k+1}, E\right). \tag{10}$$

$L(\widehat{\delta}_{k+1}, E)$ needs to meet the following requirement:

$$\overline{\widetilde{\delta}}_{k+1}^T \varphi_{k+1} \overline{\widetilde{\delta}}_{k+1} \le \overline{\delta}_{k+1}^T \varphi_{k+1} \overline{\delta}_{k+1} \tag{11}$$

where $\overline{\widetilde{\delta}}_{k+1}$ represents the difference between δ and $\widetilde{\delta}_{k+1}$.

Lemma: The convergence of the parameter estimation error can be guaranteed provided that the identifier variable meets the following condition:

$$\lim_{k\to\infty} \varphi_k = \infty. \tag{12}$$

Proof: Choose $V_{\overline{\delta}_k} = \overline{\delta}_k^T \varphi_k \overline{\delta}_k$ as the Lyapunov function of the estimation error. From (3), (4), (7), (8), and (9), ΔV can be expressed as

$$\begin{aligned} \Delta V &= V_{\overline{\delta}_{k+1}} - V_{\overline{\delta}_k} \\ &\le -(\Psi_k \overline{\delta}_k)^T H_k \Psi_k \overline{\delta}_k. \end{aligned} \tag{13}$$

The limit of $V_{\overline{\delta}_k}$ is then shown below when $k \to \infty$

$$\lim_{k\to\infty} V_{\overline{\delta}_k} \le V_{\overline{\delta}_0} - \sum_{k=0}^{\infty} \left[(\Psi_k \overline{\delta}_k)^T H_k \Psi_k \overline{\delta}_k \right]. \tag{14}$$

Given the bounded nature of the system, there exists a positive number λ such that it satisfies the following inequality:

$$\Gamma \le \|H(k)\| \le 1. \tag{15}$$

Then, (14) can be rewritten as

$$\lim_{k\to\infty} V_{\overline{\delta}_k} \le V_{\overline{\delta}_0} - \Gamma \sum_{k=0}^{\infty} \left[(\Psi_k \overline{\delta}_k)^T \Psi_k \overline{\delta}_k^T \right]. \tag{16}$$

If (12) is satisfied, the limit of $\overline{\delta}_k$ will converge to 0 asymptotically as the right-hand side of (16) is a finite value.

Remark: Given that the inverter d-axis current $I_{O,d}$ is never precisely 0 owing to the presence of noises and disturbances, (12) can be satisfied all the time based on (4) and (8).

B. Adaptive Model Predictive Current Control

In this article, the MPCC is implemented based on deadbeat principle with one-cycle digital delay compensation

$$\begin{cases} I^*_{O,d,k+2} = I_{O,d,k+1} - \frac{R_f T_s}{L_f} I_{O,d,k+1} + \omega T_s I_{O,q,k+1} \\ \qquad + \frac{T_s}{L_f} V^*_{O,d,k+1} - \frac{T_s}{L_f} V_{L,d,k+1} \\ I^*_{O,q,k+2} = I_{O,q,k+1} - \omega T_s I_{O,d,k+1} - \frac{R_f T_s}{L_f} I_{O,q,k+1} \\ \qquad + \frac{T_s}{L_f} V^*_{O,q,k+1} - \frac{T_s}{L_f} V_{L,q,k+1} \end{cases} \tag{17}$$

where $V_{L,k+1}$ can be assumed to be the same as $V_{L,k}$ under a short control period [14], [26]. $I^*_{O,d,k+2}$ and $I^*_{O,q,k+2}$ denote the reference d, q-axis currents at $(k+2)$th time instant, derived through linear interpolation as follows:

$$\begin{bmatrix} I^*_{O,d,k+2} \\ I^*_{O,q,k+2} \end{bmatrix} = 3 \begin{bmatrix} I^*_{O,d,k} \\ I^*_{O,q,k} \end{bmatrix} - 2 \begin{bmatrix} I^*_{O,d,k-1} \\ I^*_{O,q,k-1} \end{bmatrix}. \tag{18}$$

Since the filter inductance is uncertain, the reference voltages $V^*_{O,d,k+1}$ and $V^*_{O,q,k+1}$ can then be obtained by applying the adaptive observer proposed previously, as demonstrated in the following expression:

$$\begin{cases} V^*_{O,d,k+1} = \frac{1}{T_s \widehat{\delta}_{k+1}} \left(I^*_{O,d,k+2} - I_{O,d,k+1} \right) + R_f I_{O,d,k+1} \\ \qquad - \frac{\omega I_{O,q,k+1}}{\widehat{\delta}_{k+1}} + V_{L,d,k+1} \\ V^*_{O,q,k+1} = \frac{1}{T_s \widehat{\delta}_{k+1}} \left(I^*_{O,q,k+2} - I_{O,q,k+1} \right) + R_f I_{O,q,k+1} \\ \qquad + \frac{\omega I_{O,d,k+1}}{\widehat{\delta}_{k+1}} + V_{L,q,k+1}. \end{cases} \tag{19}$$

Given that calculations based on deadbeat principle may lead to reference voltages exceeding the space vector diagram, a constraint in (20) is applied to restrict the amplitude of reference voltages while maintaining low current harmonics

$$\left\| V^*_{O,k+1} \right\| \le \frac{V_{\text{dc}}}{\sqrt{3}}, \quad V^*_{O,k+1} = \begin{bmatrix} V^*_{O,d,k+1} \\ V^*_{O,q,k+1} \end{bmatrix} \tag{20}$$

where V_{dc} denotes the dc-link voltage.

Thus, the reference voltages $V^*_{s,O,k+1}$ satisfying the constraint are represented as follows:

$$V^*_{s,O,k+1} = \begin{cases} V^*_{O,k+1}, & \text{if } \left\| V^*_{O,k+1} \right\| \le \frac{V_{\text{dc}}}{\sqrt{3}} \\ \frac{V^*_{O,k+1} V_{\text{dc}}}{\sqrt{3} \left\| V^*_{O,k+1} \right\|}, & \text{if } \left\| V^*_{O,k+1} \right\| > \frac{V_{\text{dc}}}{\sqrt{3}}. \end{cases} \tag{21}$$

IV. Proposed New SVM

In traditional 3L-NPC inverters, the synthesis of reference voltages is generally accomplished by utilizing the nearest three VVs. In order to obey the rules that line-to-line voltage is only permitted to jump to the adjacent voltage levels at most during every VV transition, four triangular subsectors are created in each of the six large sectors in the space VV diagram. However, this method is not applicable to the 3L-SNPCI owing to the absence of the medium VVs. To address this issue, a new SVM scheme is proposed for the 3L-SNPCI, which utilizes a different subsector division, as shown in Fig. 4.

A. Sector Determination

As shown in Fig. 4, the large sector I_1 is divided into four small subsectors and the same rule can be applied to the other five large sectors. In order to determine which sector the reference VV is located, the magnitude of $V^*_{s,O}$ is decomposed into V_a and V_b according to phase angle θ as

$$\begin{cases} V_a = \left\| V^*_{s,O} \right\| \cos\theta \\ V_b = \left\| V^*_{s,O} \right\| \sin\theta. \end{cases} \tag{22}$$

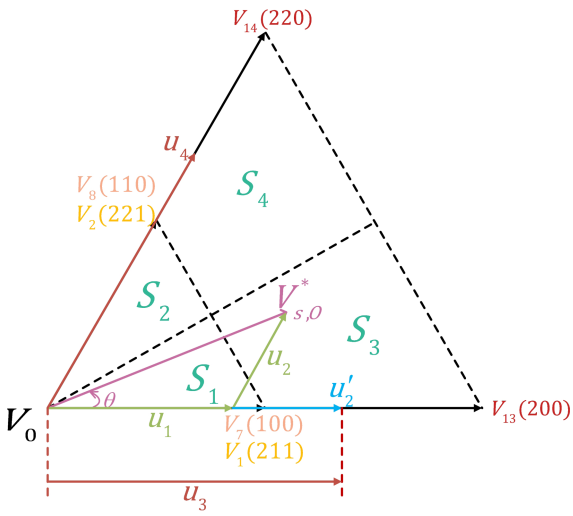

Fig. 4. Sector determination in I_1.

Then, the conditions that determine the location of reference VV are mathematically described as follows:

$$S_1 : V_b \le -\sqrt{3}V_a + \frac{\sqrt{3}V_{\rm dc}}{3}, \quad 0^\circ \le \theta < 30^\circ \tag{23}$$

$$S_2 : V_b \le -\sqrt{3}V_a + \frac{\sqrt{3}V_{\rm dc}}{3}, \quad 30^\circ \le \theta < 60^\circ \tag{24}$$

$$S_3 : -\sqrt{3}V_a + \frac{\sqrt{3}V_{\rm dc}}{3} \le V_b \le -\sqrt{3}V_a + \frac{2\sqrt{3}V_{\rm dc}}{3}, \quad 0^\circ \le \theta < 30^\circ \tag{25}$$

$$S_4 : -\sqrt{3}V_a + \frac{\sqrt{3}V_{\rm dc}}{3} \le V_b \le -\sqrt{3}V_a + \frac{2\sqrt{3}V_{\rm dc}}{3}, \quad 30^\circ \le \theta < 60^\circ. \tag{26}$$

B. Dwelling Time Calculation

For simplicity, T_0 refers to the dwelling time of zero VV V_0. T_1 and T_2 represent the dwelling time of redundant small VV pairs V_1/V_7 and V_2/V_8, respectively. T_3 and T_4 are the dwelling time of large VVs V_{13} and V_{14}, respectively.

When $V^*_{s,O}$ is located in subsectors S_1 and S_2, the dwelling time (28)–(30) are simply obtained based on voltage–second (27)

$$\begin{cases} V_{1/7}T_1 + V_{2/8}T_2 + V_0T_0 = V^*_{s,O}T_s \\ T_0 + T_1 + T_2 = T_s \end{cases} \tag{27}$$

$$T_1 = 2mT_s \sin\left(\frac{\pi}{3} - \theta\right) \tag{28}$$

$$T_2 = 2mT_s \sin(\theta) \tag{29}$$

$$T_0 = T_s - T_1 - T_2 \tag{30}$$

where m represents the modulation index $\frac{\sqrt{3}|V^*_{s,O}|}{V_{\rm dc}}$.

Regarding subsectors S_3 and S_4, the reference VV $V^*_{s,O}$ is built up by

$$\begin{aligned} \left|V^*_{s,O}\right| \angle\theta &= d_1\frac{V_{\rm dc}}{3}\angle 0^\circ + d_3\frac{2V_{\rm dc}}{3}\angle 0^\circ + d_2\frac{V_{\rm dc}}{3}\angle 60^\circ \\ &\quad + d_4\frac{2V_{\rm dc}}{3}\angle 60^\circ \\ &= u_1 + u_2 \end{aligned} \tag{31}$$

where d_n denotes T_n/T_s for $n \in \{1,2,3,4\}$. u_1 represents $(d_1\frac{V_{\rm dc}}{3}\angle 0^\circ + d_3\frac{2V_{\rm dc}}{3}\angle 0^\circ)$ and u_2 is $(d_2\frac{V_{\rm dc}}{3}\angle 60^\circ + d_4\frac{2V_{\rm dc}}{3}\angle 60^\circ)$, which are illustrated in Fig. 4. Then, a new vector u_3 can be defined by

$$u_3 = u_1 + |u_2|\angle 0^\circ = u_1 + u'_2. \tag{32}$$

A similar vector u_4 is subsequently introduced with the same magnitude as u_3, but phase shifted by 60°. Thus

$$V^*_{s,O} = D_1u_3 + D_2u_4 \tag{33}$$

where D_1 equals to $\frac{|u_1|}{|u_3|}$ and D_2 is $\frac{|u_2|}{|u_4|}$.

According to Fig. 4, the values of u_1, u_2, and u_3 are shown as (34)–(36)

$$u_1 = \left(|u_3| - \frac{2\sqrt{3}\left|V^*_{s,O}\right|\sin\theta}{3}\right)\angle 0^\circ \tag{34}$$

$$u_2 = \frac{2\sqrt{3}\left|V^*_{s,O}\right|\sin\theta}{3}\angle 60^\circ \tag{35}$$

$$u_3 = \left|V^*_{s,O}\right|\left(\cos\theta + \frac{\sqrt{3}\sin\theta}{3}\right)\angle 0^\circ. \tag{36}$$

Particularly, when

$$\begin{cases} d'_1 + d'_3 = 1 \\ d'_1\frac{V_{\rm dc}}{3} + d'_3\frac{2V_{\rm dc}}{3} = |u_3|. \end{cases} \tag{37}$$

Pseudo d_1 and d_3 are illustrated as

$$d'_1 = 2 - \frac{3|u_3|}{V_{\rm dc}}, \quad d'_3 = \frac{3|u_3|}{V_{\rm dc}} - 1. \tag{38}$$

Consequently, the dwelling time is depicted as

$$\begin{cases} T_1 = d'_1D_1T_s \\ T_2 = d'_1D_2T_s \\ T_3 = d'_3D_1T_s \\ T_4 = d'_3D_2T_s. \end{cases} \tag{39}$$

C. Switching Sequence

With the aim of minimizing the line-to-line voltage jumps during VV transition, it is crucial that VVs are only allowed to move to their adjacent VVs in the SVM. Consequently, the switching sequences with a fixed number of switching events are presented as follows:

$$s_1 : V_0 \to V_8 \to V_7 \to V_1 \to V_7 \to V_8 \to V_0$$

$$s_2 : V_0 \to V_1 \to V_2 \to V_8 \to V_2 \to V_1 \to V_0$$

$$s_{3,1} : V_{13} \to V_1 \to V_2 \to V_{14} \to V_2 \to V_1 \to V_{13}$$

$$s_{3,2}: V_{13} \rightarrow V_7 \rightarrow V_8 \rightarrow V_{14} \rightarrow V_8 \rightarrow V_7 \rightarrow V_{13}$$
$$s_{4,1}: V_{14} \rightarrow V_2 \rightarrow V_1 \rightarrow V_{13} \rightarrow V_1 \rightarrow V_2 \rightarrow V_{14}$$
$$s_{4,2}: V_{14} \rightarrow V_8 \rightarrow V_7 \rightarrow V_{13} \rightarrow V_7 \rightarrow V_8 \rightarrow V_{14}.$$

According to the above-mentioned switching sequences and Fig. 4, it is obvious that NPV can be efficiently balanced in sectors S_1 and S_2 by applying the redundant small VV pairs V_1/V_7 and V_2/V_8. As an illustration, assume that reference VV $V^*_{s,O}$ is located in S_1 with $V_{\text{cap1}} < V_{\text{cap2}}$. Given that the total duty ratio of V_1/V_7 is fixed in one sampling period as V_1 and V_7 have the same effect on reference VV synthesis, the NPV level will decline by increasing the duty ratio of V_7 or decreasing the duty ratio of V_1.

So as to balance the NPV while satisfying the voltage transition rules mentioned earlier when the reference VV resides in subsectors S_3 or S_4, two switching sequences will need to be used in each subsector. Specifically, sequence $s_{3,1}$ will be chosen if $V^*_{s,O}$ is located in S_3 with $V_{\text{cap1}} > V_{\text{cap2}}$, whereas $s_{3,2}$ will be selected when $V_{\text{cap1}} < V_{\text{cap2}}$.

Once the dwelling time and switching sequences are determined, the next step is to generate appropriate gate signals. As shown in Fig. 2, the 3L-SNPCI contains five pairs of complementary switches. Thus, an equal amount of control signals are required, represented by $C_{a1}, C_{b1}, C_{c1}, C_{f1}$, and C_{f2}. Due to the fact that polarity of gate signals varies with the sector rotation in each switch, only comparing control signals with carrier signals cannot satisfy all scenarios. Therefore, five supplementary signals are introduced to handle this issue, denoted as ${C_{a1}}^*, {C_{b1}}^*, {C_{c1}}^*, {C_{f1}}^*$, and ${C_{f2}}^*$. Then the gate signals are generated from the exclusively-OR (XOR) logic operation, where the results of respectively comparing control signal and supplementary signal with carrier signal are the inputs of XOR.

In small subsectors S_1 and S_2, only zero VV and small VVs are selected to synthesize the reference VV, which are shown in Fig. 5. d_{Vx} is the duty ratio of each VV, calculated as

$$d_{Vx} = T_{Vx}/T_s \tag{40}$$

where

$$d_{V0} + d_{V1} + d_{V7} + d_{V8} = d_{V0} + d_{V1} + d_{V2} + d_{V8} = 1.$$

Then, the gate signals corresponding to their switching sequences are illustrated on the right-hand side of Fig. 5 after XOR operations.

In subsmall sector S_3, zero VV is replaced by two large VVs, V_{13} and V_{14}. The corresponding gate signals are displayed in Fig. 6. The difference between two switching sequences is the selection of the small VVs. Specifically, P-O type small VVs are applied in $s_{3,1}$, whereas O-N type small VVs are selected in $s_{3,2}$. Thus, the gate signals for two-level inverter side keep consistent. However, the gate signals of S_{f1} and S_{f2} in these two switching sequences are alternated due to the varied output voltage level in the three-level dc source side. Similarly, the gate signals in subsector S_4 are depicted in Fig. 7. Then the step-by-step procedure to implement the proposed scheme is given in the form of a flowchart, as shown in Fig. 8.

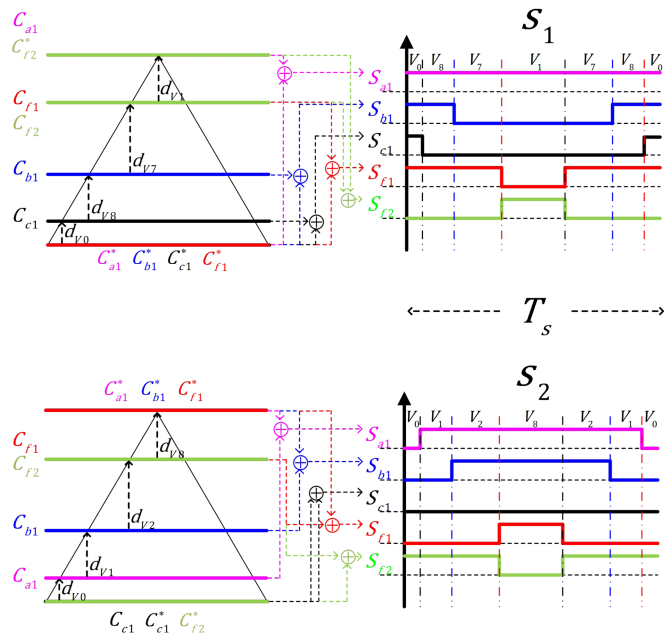

Fig. 5. Gate signals generation in subsectors S_1 and S_2.

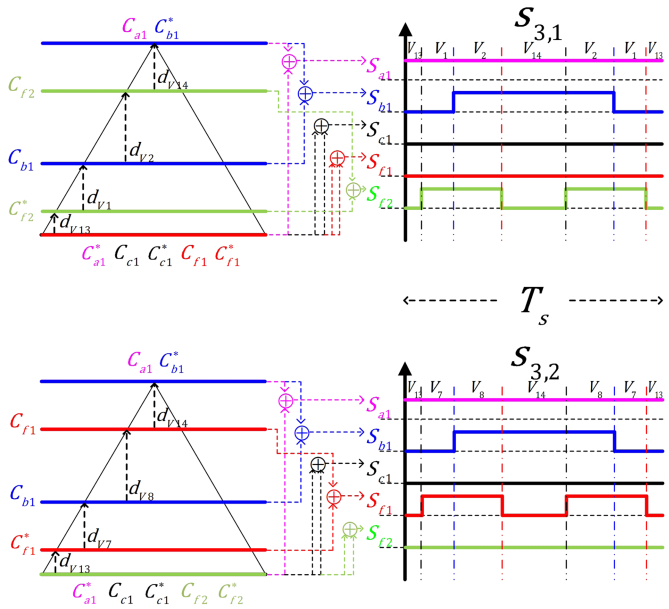

Fig. 6. Gate signals generation in subsector S_3.

V. Experimental Results

To validate the efficacy of the proposed method, hardware experiments are implemented on a 3L-SNPC inverter, as illustrated in Fig. 9. A control board equipped with digital signal processor Texas Instrument F28346 is utilized to implement the proposed algorithm. Three-phase *LC* filter followed by a resistive-inductive load is connected to the output port of the 3L-SNPC inverter. It is noteworthy that the sampling and switching frequencies are both chosen as 10 kHz. Detailed parameters of the experimental setup are tabulated in Table I.

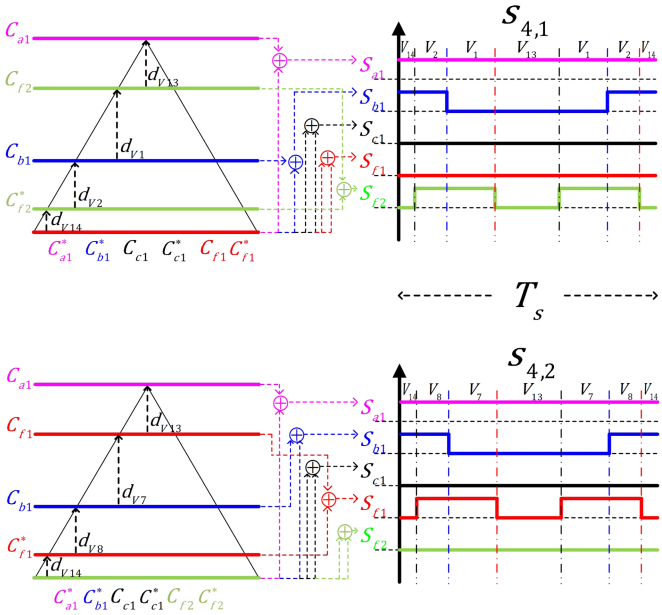

Fig. 7. Gate signals generation in subsector S_4.

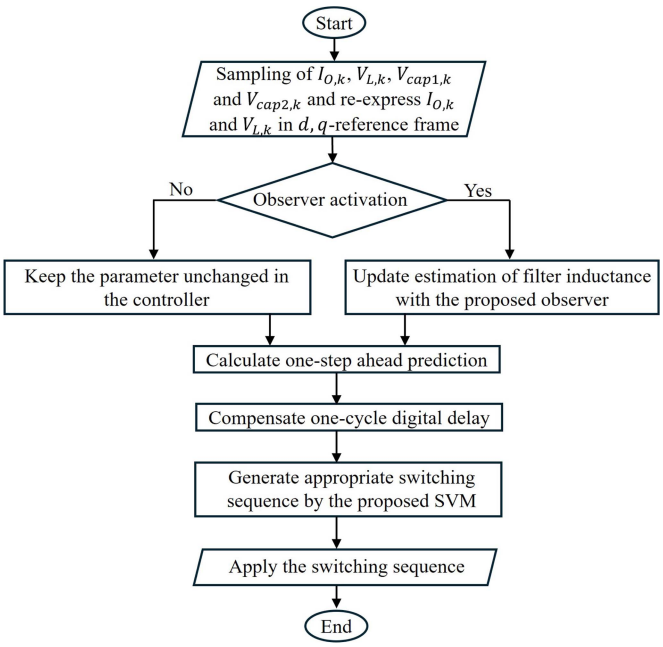

Fig. 8. Implementation flowchart of the proposed method.

TABLE I
PARAMETERS OF EXPERIMENTAL SETUP

Parameters	Values
Input dc voltage	$V_{\rm dc} = 220$ V
Dc-link capacitance	$C_{\rm dc} = 680$ μF
Switching frequency	$f_{\rm sw} = 10$ kHz
Filter inductance	$L_f = 5$ mH
Parasitic resistance	$R_f = 0.1$ Ω
Filter capacitance	$C_f = 5$ μF
Output three-phase frequency	$f = 50$ Hz
Load resistance	$R = 10$ Ω
Load inductance	$L = 50$ μH
Sampling frequency	$f_s = 10$ kHz

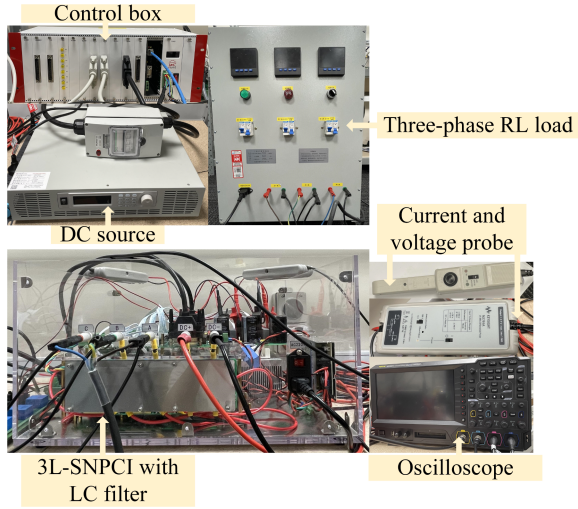

Fig. 9. Experiment setup.

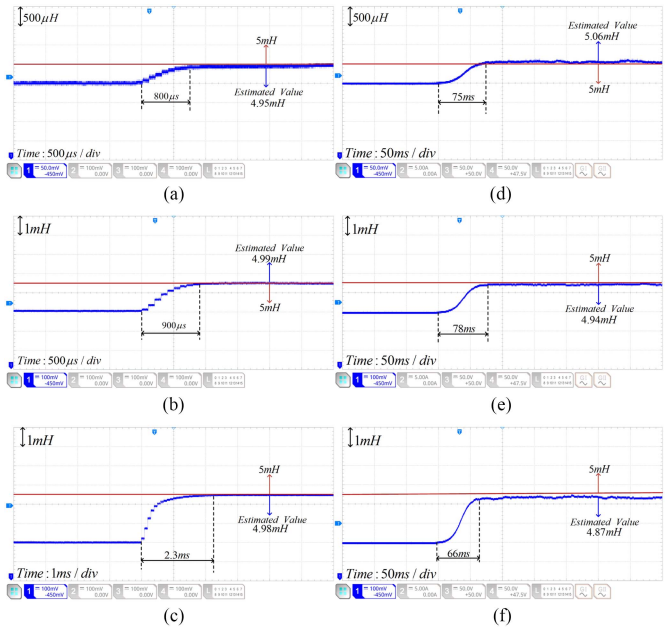

Fig. 10. Estimated results under -10%, -30%, and -50% erroneous filter inductance. (a)–(c) Proposed method. (d)–(f) Method [21].

A. Parameter Estimation Performance

Initially, the performance of the proposed observer is verified with model parameter variation. With the real inductance value of 5 mH, six groups of comparative tests are carried out with each of them starting at a purposely detuned inductance value. The percentage of inductance detuning is up to $\pm 50\%$ of the real value. The results with the proposed method and [21] are clearly illustrated in Figs. 10(a)–(f) and 11(a)–(f). Two crucial performance indices, i.e., estimated value and converging time, are depicted in each subfigure.

To be particular, the estimated inductance with the proposed method approaches 4.95 mH from its initial value of 4.5 mH within 800 μs in Fig. 10(a), resulting in an estimation error

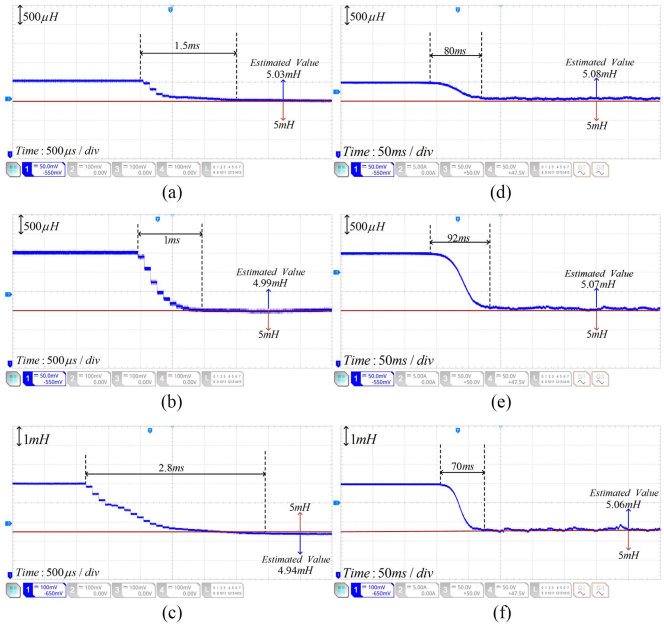

Fig. 11. Estimated results under +10%, +30%, and +50% erroneous filter inductance. (a)–(c) Proposed method. (d)–(f) Method [21].

of only about 1%. More accurate inductance estimations are achieved with the inductance variations of −30% and −50%, as shown in Fig. 10(b) and (c), which obtain the estimated values of 4.99 and 4.98 mH. The estimation errors are 0.2% and 0.4%, respectively, where the corresponding convergences are measured as 900 μs and 2.3 ms. Compared to Fig. 10(a)–(c) and (d)–(f) illustrates the estimation results with method [21] under the same initial inductances detuned conditions. The converging times of [21] in Fig. 10(d)–(f) are about 75, 78, and 66 ms. After entering steady states, their estimated inductances are 5.06, 4.94, and 4.87 mH, respectively, where the estimation errors are 1.2%, 1.2%, and 2.6%. Thus, after comparing (a)–(c) with (d)–(f) in Fig. 10, the filter inductance estimation accuracies are improved by 0.2%, 1%, and 2.2%. It is also noteworthy that the average converging time with the proposed method is 1.3 ms, which is 71.7 ms faster than the method [21].

To investigate the effectiveness of the proposed observer under positively detuned inductance, +10%, +30%, and +50% erroneous filter inductance is applied in Fig. 11. From Fig. 11(d)–(f), the converging times of method [21] are 80, 92, and 70 ms, respectively. Their estimated values are 5.08, 5.07, and 5.06 mH, leading to estimation errors of 1.6%, 1.4%, and 1.2%. Compared to that, Fig. 11(a)–(c) shows the parameter estimation results with the proposed method. It is noted that the observed converging times are 1.5, 1, and 2.8 ms. The estimated results are 5.03, 4.99, and 4.94 mH, respectively, where the estimation errors are calculated as 0.6%, 0.2%, and 1.2%. From the above-mentioned comparisons, the proposed method achieves higher estimation accuracy and faster convergence, therefore, verifying the superior performance.

B. Steady-State Performance

The steady-state performance of the proposed AMPCC and SVM is first analyzed under different reference currents of $I_{O,d}$.

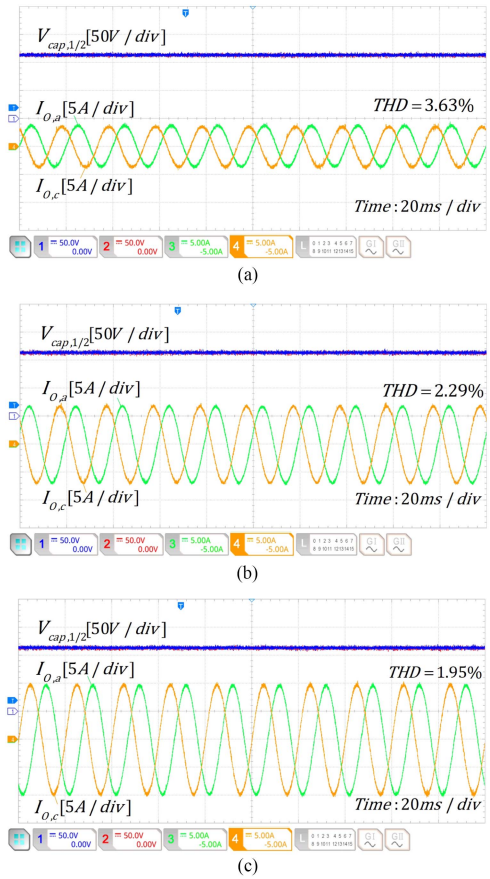

Fig. 12. Steady-state performance under different reference $I_{O,d}$ current while $I_{O,q} = 0$A. (a) $I_{O,d} = 4$A. (b) $I_{O,d} = 7$A. (c) $I_{O,d} = 10$A.

It is noteworthy that initial filter inductances in these tests are all purposely detuned by +25%. Then, the steady-state results with estimated inductances are shown in Fig. 12(a)–(c). From Fig. 12, it is clear that the inverter output currents are effectively regulated by the proposed method. To be more specific, the proposed method achieves a THD of 3.63% under light load condition when $I_{O,d} = 4$A, as depicted in Fig. 12(a). Likewise, the current THDs of 2.29% and 1.95% under medium load and heavy load conditions are illustrated in Fig. 12(b) and (c), respectively. In addition, effective NPV balancing is realized under all operating conditions, as shown by the equal capacitor voltages $V_{\text{cap},1}$ and $V_{\text{cap},2}$ on the top of Fig. 12(a)–(c).

To further illustrate the effectiveness of the proposed AMPCC and SVM, its steady-state performance is compared with that of conventional MPCC [11] that is subject to the same initial inductance detuning. The results are demonstrated in Figs. 13 and 14. By comparing Figs. 13 and 14, it is noted that the proposed method estimates the inductance to be 5.05 mH, achieving a low THD of 2.57% that is 60.1% lower than that produced by the conventional MPCC. Such control performance improvement mainly benefits from the following two aspects. Even though the method [11] enhances the control performance by eliminating the weighting factor, it cannot handle the parameter variations, thereby leading to prediction errors. Compared to that, the proposed AMPCC is robust to the parameter mismatch due to the adaptive observer, resulting in precise current predictions.

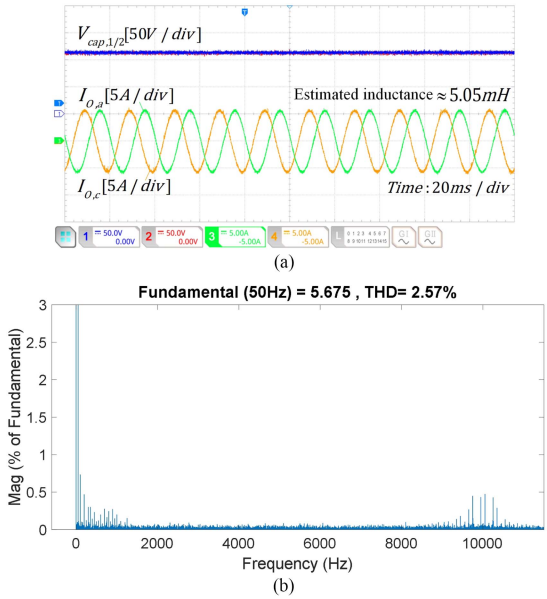

Fig. 13. Inverter output current and its harmonics spectra with estimated inductance 5.05 mH when initial erroneous inductance 6.25 mH is used in the proposed method.

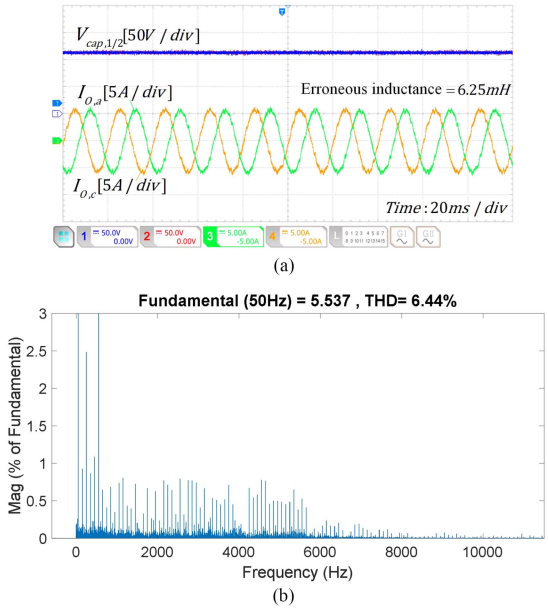

Fig. 14. Inverter output current and its harmonics spectra when erroneous inductance 6.25 mH is used in the conventional MPCC [11].

Moreover, despite all VVs being applied to evaluate the cost function in [11], the control performance is still affected as only one VV is utilized in the whole sampling period. In contrast, the method in this article accurately synthesizes the reference VV according to the proposed SVM, therefore leading to superb control performance.

The NPV recovery process of the proposed method under different tracking references is demonstrated in Fig. 15 while an initial 20 V voltage difference is made between two capacitors. With the proposed method, the NPV returns from the unbalanced state to the balanced state within a short time, verifying the NPV balancing capability. It is noted that Fig. 15(b) achieves the fastest balancing performance compared to Fig. 15(a) and (c). The reason is that when $I_{O,d}$ equals 7 A, the dwelling time of the active small VV is longer than that under the other two conditions, leading to a better balancing capability. Furthermore, the NPV remains well-regulated under different conditions after returning to the balanced state, devoid of dc offset.

C. Reference Transient Performance

The transient performances of the proposed AMPCC and SVM under reference current changes are examined with a $+25\%$ initial inductance detuning. The simulation results with estimated inductance are first performed in Fig. 16. Then, the experimental results are displayed in Fig. 17(a) to validate the modeling accuracy. To be specific, it is visible that fast dynamic current tracking responses are achieved in Fig. 17(a). Furthermore, the NPV is well balanced during the transients. For a better illustration, the dynamic current changes are plotted in the dq-reference frame in Fig. 18. From the zoom-in figure on the right-hand side of Fig. 18(a), it is visible that the settling time is 2.5 ms for the current step up. The overshoot is also insignificant in this scenario. Compared to the proposed method, the transient responses of the conventional MPCC [11] are illustrated in Figs. 17(b) and 18(b). From Fig. 17(b), Wang et al. [11] obtained abrupt transients under the current step up where smooth results are attained by the proposed method. Moreover, the settling time of the conventional MPCC is 0.5 ms longer, which is shown on the right-hand side of Fig. 18(b). In summary, the proposed method offers superior dynamic current regulation performance.

D. Computational Burden Evaluation

The experimental comparison of the execution time between the proposed method and method [11] is conducted. To be specific, a digital output (DO) port is employed to measure the execution time for these two methods. The step-up voltage on the DO port indicates the start of the program, whereas the algorithm is completed when the voltage level becomes low. The interrupt frequency is the same as the sampling frequency, which is 10 kHz. Fig. 19(a) shows that the execution time of the proposed method is about 33.6 μs. Likewise, it takes 43.39 μs to finish the implementation of method [11], which is depicted in Fig. 19(b). It is noted that the execution time of the proposed method is about 77.4% of the method [11], reducing the computational burden.

E. Switching Loss Analysis

In this section, the model of a 3L-SNPCI is established in PLECS to measure the switching losses dissipated by the inverter [27], [28]. The parameters of the IGBT modules are from FF100R12KS4 produced by Infineon. The dc-link voltage is set to 220 V, and the fundamental and switching frequencies also remain consistent with the experimental configurations of 50 Hz and 10 kHz, respectively. The switching losses of the

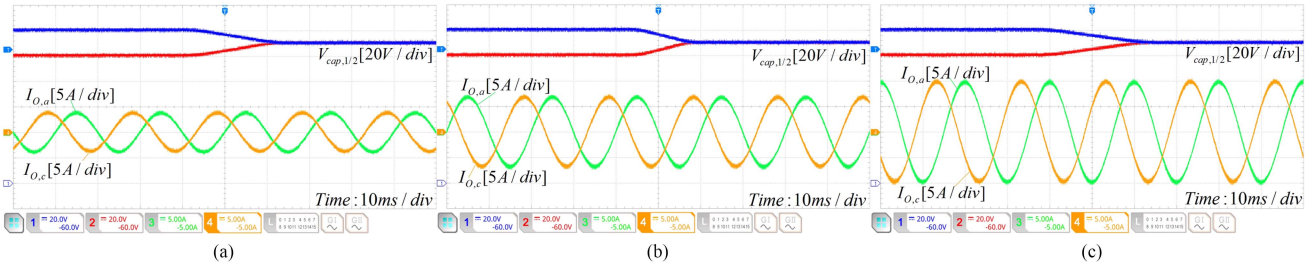

Fig. 15. NPV recovery process with the proposed method under different tracking references. (a) $I_{O,d} = 4$ A. (b) $I_{O,d} = 7$ A. (c) $I_{O,d} = 10$ A.

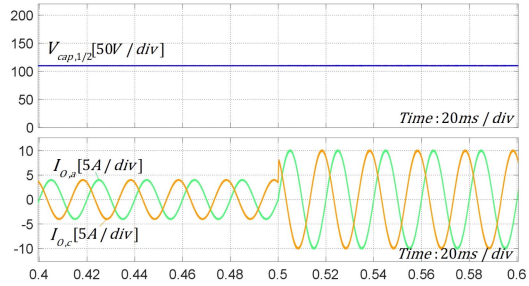

Fig. 16. Simulation results with the proposed method when reference current steps up from 4 to 10 A.

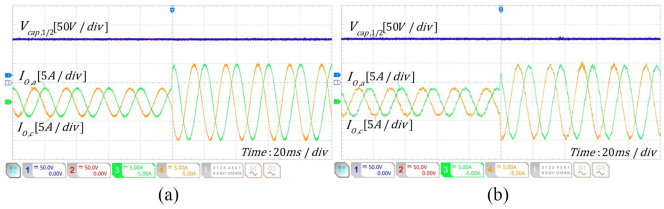

Fig. 17. Experimental results when reference current steps up from 4 to 10 A. (a) Proposed method. (b) Conventional MPCC [11].

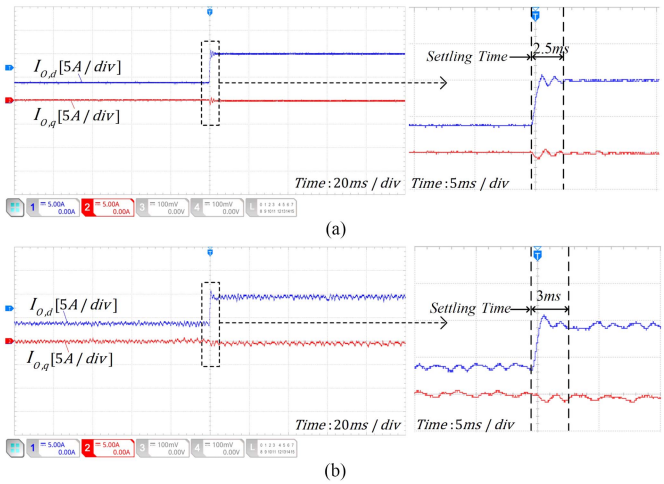

Fig. 18. Experimental results when reference current steps up from 4 to 10 A under dq-frame. (a) Proposed method. (b) Method [11].

entire inverter with the proposed SVM, modulation 1 [23] and modulation 2 [24] are compared in Fig. 20 under different conditions. In case (a), the reference VV is located in sector S_1 or S_2 of the proposed SVM, corresponding to region 1 in modulation 1. Due to the application of complementary small

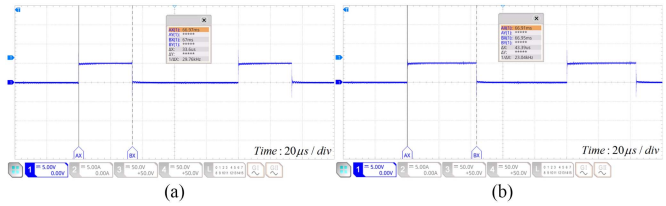

Fig. 19. Execution time comparisons. (a) Proposed method. (b) Method [11].

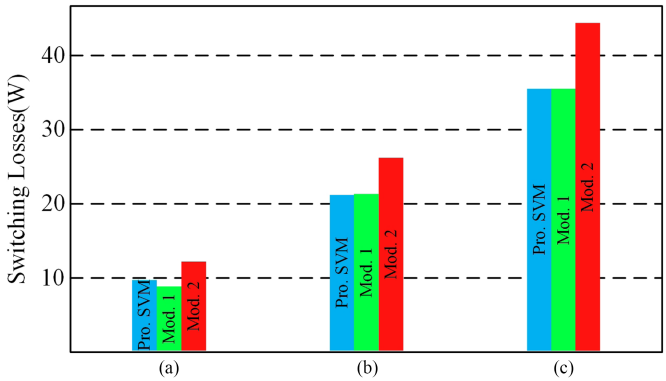

Fig. 20. Switching losses with the proposed method, [23], and [24]. (a) $I_{O,d} = 4$ A. (b) $I_{O,d} = 7$ A. (c) $I_{O,d} = 10$ A.

VVs in the switching sequence, the proposed SVM produces one more toggle on the switch, thereby faintly increasing the switching loss. In case (b) and case (c), the proposed SVM applies the switching sequence in sector S_3 or S_4, which reduces a toggle compared to case (a), leading to similar switching losses dissipated by modulation 1. Regarding modulation 2 [24], all switching sequences are passed through in reverse order in the second half of the modulation cycle, which greatly increases the toggles. Moreover, the switching loss is further enlarged in area 2 as communication in the two-level circuit with full dc-link voltage is contained. Therefore, modulation 2 obtains the largest switching losses under all conditions.

In addition, the implementation of the method [23] first requires the DSP to select the VVs and generate respective digital signals in every sampling period. Then a CPLD scans a lookup table at high frequency to identify the values corresponding to the DSP output signals. Subsequently, the gate signals are transmitted to the switches based on the high and low voltage signals stored in the table to complete the modulation. Likewise, the method [24] utilizes 11-segment switching sequences for all areas, toggling the switching function up to

three times in one modulation cycle, which requires both DSP and field-programmable gate array. Compared to the previous two methods, the proposed method generates PWM signals by directly executing logical operations to the DSP output signals through XOR, which only requires DSP and simple logic gates, therefore simplifying the real-time implementation.

VI. Conclusion

This article proposes a new AMPCC approach with excellent control performance together with a novel carrier-based SVM for the three-level simplified neutral point clamped inverter. The proposed adaptive observer attains rapid and accurate convergence to eliminate model dependence while achieving low computational burden. In addition, the proposed SVM scheme ensures the NPV balancing and requires lower sampling frequency in all sectors. Its carrier-based nature also simplifies the real-time implementation.

References

[1] T. P. Chen, "Common-mode ripple current estimator for parallel three-phase inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1330–1339, May 2009.

[2] A. Kersten et al., "Fault detection and localization for limp home functionality of three-level NPC inverters with connected neutral point for electric vehicles," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 2, pp. 416–432, Jun. 2019.

[3] S. Kumar and B. Singh, "A multipurpose PV system integrated to a threephase distribution system using an LWDF-based approach," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 739–748, Jan. 2018.

[4] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016.

[5] C. Li et al., "A modified neutral point balancing space vector modulation for three-level neutral point clamped converters in high-speed drives," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 910–921, Feb. 2019.

[6] X. Li, X. Xing, C. Zhang, A. Chen, C. Qin, and G. Zhang, "Simultaneous common-mode resonance circulating current and leakage current suppression for transformerless three-level t-type PV inverter system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4457–4467, Jun. 2019.

[7] R. Rojas, T. Ohnishi, and T. Suzuki, "Simple structure and control method for a neutral-point-clamped PWM inverter," in *Proc. Conf. Rec. Power Convers. Conf.*, Yokohama, Japan, 1993, pp. 26–31.

[8] M. Schaefer, W. Goetze, M. Hofmann, F. Bayer, D. Montesinos-Miracle, and A. Ackva, "Direct current control for grid-connected diode-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 3067–3074, Apr. 2017.

[9] H. Yi, F. Zhuo, F. Wang, and Z. Wang, "A digital hysteresis current controller for three-level neural-point-clamped inverter with mixed-levels and prediction-based sampling," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3945–3957, May 2016.

[10] R. Davoodnezhad, D. G. Holmes, and B. P. McGrath, "A novel three-level hysteresis current regulation strategy for three-phase three-level inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6100–6109, Nov. 2014.

[11] F. Wang, Z. Li, and Z. Liu, "Model predictive control methods for three-level sparse neutral point clamped inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4355–4366, Dec. 2020.

[12] S. R. Mohapatra and V. Agarwal, "Model predictive controller with reduced complexity for grid-tied multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8851–8855, Nov. 2019.

[13] E.-S. Jun, M. H. Nguyen, and S.-S. Kwak, "Model predictive control method with NP voltage balance by offset voltage injection for three-phase three-level NPC inverter," *IEEE Access*, vol. 8, pp. 172175–172195, 2020.

[14] F. Donoso, A. Mora, R. Cárdenas, A. Angulo, D. Sáez, and M. Rivera, "Finite-set model-predictive control strategies for a 3L-NPC inverter operating with fixed switching frequency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3954–3965, May 2018.

[15] W. Alhosaini, Y. Wu, and Y. Zhao, "An enhanced model predictive control using virtual space vectors for grid-connected three-level neutral-point clamped inverters," *IEEE Trans. Energy Convers.*, vol. 34, no. 4, pp. 1963–1972, Dec. 2019.

[16] Y. Yang et al., "Low complexity finite-control-set MPC based on discrete space vector modulation for t-type three-phase three-level converters," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 392–403, Jan. 2022.

[17] Y. Yang, H. Wen, M. Fan, M. Xie, and R. Chen, "Fast finite-switching-state model predictive control method without weighting factors for T-type three-level three-phase inverters," *IEEE Trans. Ind. Inform.*, vol. 15, no. 3, pp. 1298–1310, Mar. 2019.

[18] N. Bekhoucha, M. Kermadi, N. Mesbahi, and S. Mekhilef, "Performance investigation of deadbeat predictive controllers for three-level neutral point clamped inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 1165–1177, Feb. 2022.

[19] M. Abdelrahem, C. M. Hackl, and R. Kennel, "Finite set model predictive control with on-line parameter estimation for active frond-end converters," *Elect. Eng.*, vol. 100, no. 3, pp. 1497–1507, 2018.

[20] Y. Zhang, J. Jiao, and J. Liu, "Direct power control of PWM rectifiers with online inductance identification under unbalanced and distorted network conditions," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12524–12537, Dec. 2019.

[21] Y. Zhang, B. Li, and J. Liu, "Online inductance identification of a PWM rectifier under unbalanced and distorted grid voltages," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 3879–3888, Jul./Aug. 2020.

[22] T. Ngo, G. Foo, and C. Baguley, "A predictive torque control strategy for interior permanent magnet synchronous motors driven by a three-level simplified neutral point clamped inverter," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Florence, 2016, pp. 2648–2653.

[23] G. H. B. Foo, T. Ngo, X. Zhang, and M. F. Rahman, "SVM direct torque and flux control of three-level simplified neutral point clamped inverter fed interior PM synchronous motor drives," *IEEE/Amer. Soc. Mech. Engineers Trans. Mechatron.*, vol. 24, no. 3, pp. 1376–1385, Jun. 2019.

[24] A. Lange and B. Piepenbreier, "Space vector modulation for three-level simplified neutral point clamped (3L-SNPC) inverter," in *Proc. IEEE 18th Workshop Control Model. Power Electron*., 2017, pp. 1–8.

[25] A. Calle-Prado, S. Alepuz, J. Bordonau, J. Nicolas-Apruzzese, P. Cortés, and J. Rodriguez, "Model predictive current control of grid-connected neutral-point-clamped converters to meet low-voltage ride-through requirements," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1503–1514, Mar. 2015.

[26] L. Guo, Z. Xu, Y. Li, Y. Chen, N. Jin, and F. Lu, "An inductance online identification-based model predictive control method for grid-connected inverters with an improved phase-locked loop," *IEEE Trans. Transp. Electrif.*, vol. 8, no. 2, pp. 2695–2709, Jun. 2022.

[27] Q. Sun, S. M. Sharkh, Z. Wang, Z. Wang, and G. Shi, "Space vector modulation with common-mode voltage elimination and switching frequency minimization for multilevel converters," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 7952–7967, Jul. 2024.

[28] I. Chaib, E. M. Berkouk, J.-P. Gaubert, M. Kermadi, N. Sabeur, and S. Mekhilef, "An improved discontinuous space vector modulation for Z-source inverter with reduced power losses," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3479–3488, Jun. 2021.

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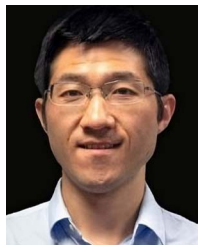

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