Universal Active Gate Driver IC With Closed-Loop Timing Control and Gate-Sensing Technique for Silicon Carbide Power Devices

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***Abstract*—Silicon carbide (SiC) power MOSFETs provide superior device characteristics, increasing their demand in high-power systems. However, the advantages of SiC also cause switching challenges, including overshoot, oscillation, and electromagnetic interference (EMI). This article introduces a universal active gate driver (AGD) IC to mitigate these issues and achieve a better tradeoff between overshoot and switching losses (E_{LOSS}). The AGD IC integrates a gate-sensing technique, eliminating the need for external sensing components, and dynamically adjusts driving strength during switching operations, effectively suppressing overshoot, oscillation, and EMI. Moreover, the proposed driver can automatically drive different SiC power devices, enhancing its utility flexibility. Validation using the 0.18-μm BCD process demonstrates the functionality of the proposed AGD, achieving notable reductions of 48.7% and 18.8% in turn-ON and turn-OFF switching losses, respectively, compared to conventional gate drivers under similar current and voltage overshoot. These findings confirm the advancements of the proposed AGD in improving the efficiency and reliability of SiC-based power management systems.**

***Index Terms*—Active gate driver (AGD), electromagnetic interference (EMI), gate-sensing, IC, oscillation, overshoot, silicon carbide (SiC).**

I. Introduction

With electric vehicle technology advancing and data centers requiring more computational power, power management systems face the challenges while achieving higher power density [1], [2], [3], [4], [5], [6], [7], [8]. At the same time, effective thermal dissipation remains a crucial consideration. Silicon carbide (SiC), a third-generation wide bandgap semiconductor, offers superior material properties compared to conventional silicon (Si) devices. Its higher breakdown electric field and dielectric critical field allow SiC to withstand higher voltages than Si under the same drift layer thickness [8], [9], [10], [11], [12], [13]. Therefore, SiC exhibits smaller on-resistance, area, and parasitic effects for the same voltage rating, achieving higher system efficiency and faster switching speed. SiC also boasts higher thermal conductivity, making it suitable for high-temperature environments [3], [4], [7], [8], [9], [13], [14], [15], [16], [17], [18]. Despite these advantages, SiC's fast switching speed causes rapid changes in drain-source voltage (dv/dt) and drain current (di/dt). The high slew rate induces energy across parasitic inductance and capacitance along the power path or device package, leading to the overshoot of voltage and current. This not only increases additional power losses but also overstresses power devices. Moreover, it gives rise to subsequent oscillations, which are responsible for electromagnetic interference (EMI) [2], [4], [5], [6], [7], [8], [10], [14], [16], [17], [18]. Robust driver solutions are essential to optimize SiC device performance. Numerous studies have proposed methods to address these challenges. The following provides detailed introductions.

A. RC Snubber Circuit

Adding additional resistors and capacitors in parallel with the power device absorbs energy and slows down the rate of current change during switching [3], [4], [14]. However, it increases power losses from the resistors, and the damping effect is degraded due to inevitable parasitic inductance [3], [5].

B. Conventional Gate Driver (CGD)

The conventional and widely used method is to increase the gate resistor (R_G) [2], [10], [15]. This approach slows the switching speed to mitigate overshoot, oscillation, and EMI issues. However, it simultaneously prolongs the switching time and results in notable switching losses. Besides, large R_G increases the risk of false triggering [2].

C. Active Gate Driver (AGD)

Different from CGD, the concept of AGD aims to partition the switching interval into several segments and reduce the driving strength during specific intervals, called weak driving intervals in this article, to address switching issues and loss [2], [7], [8], [16], [17], [18], [20], [21], [22], [23]. As shown in Fig. 1(c), the

Received 11 July 2024; revised 6 November 2024; accepted 14 December 2024. Date of publication 24 December 2024; date of current version 28 January 2025. This work was supported in part by the National Science and Technology Council, Taiwan, under Grant NSTC 113-2218-E-A49-018, Grant 113-2221-E-A49-080-MY2, and Grant 112-2221-E-A49-146-MY3, and in part by the Higher Education Sprout Project of the National Yang Ming Chiao Tung University and Ministry of Education, Taiwan. Recommended for publication by Associate Editor D. Dong. *(Corresponding author: Po-Hung Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3522068.

Digital Object Identifier 10.1109/TPEL.2024.3522068

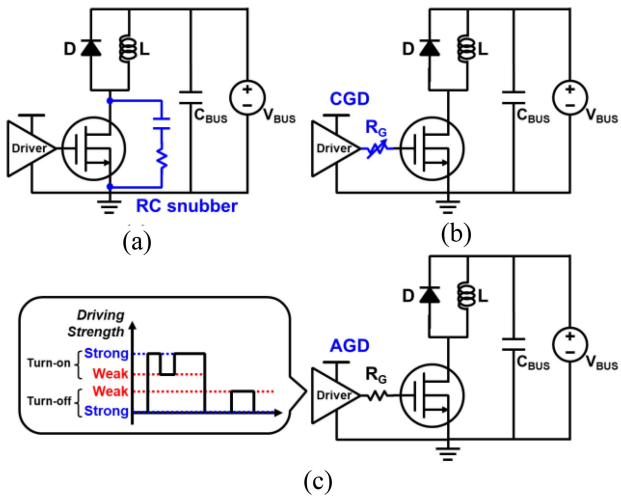

Fig. 1. Prior arts. (a) RC snubber circuit. (b) Conventional gate driver. (c) Active gate driver.

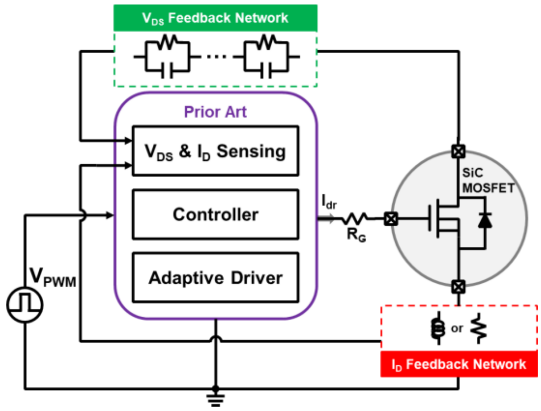

Fig. 2. Conventional I_D and V_{DS} sensing methods.

driving strength under standard operation is referred to as "strong driving strength." During weak driving intervals, the driving strength is lowered, which is termed "weak driving strength." The AGD generally comprises a sensing circuit, a controller, and a driving stage.

1) Sensing Circuit: The sensing circuit monitors the behavior of current (I_D) and drain voltage (V_{DS}). Recent research has focused on I_D and V_{DS} sensing, as shown in Fig. 2. The I_D sensing method typically uses a 4-pin package with a Kelvin source or additional external resisters to detect current behavior [7], [8], [16], [17], [18], [22], [23]. However, these approaches limit the device package flexibility or increase area. Alternatively, V_{DS} sensing has also been explored [7], [8], [17], [20], [22]. Given that V_{DS} in SiC can exceed 400 V and sometimes reach thousands of volts, typical chips cannot withstand such voltages directly. Therefore, V_{DS} sensing requires discrete resistors or capacitors to scale down V_{DS} first, restricting the V_{DS} variation range and increasing the area. This article proposes a gate-sensing technique, as shown in Fig. 3 and described subsequently, to address the aforementioned problems.

2) Controller: The controller receives signals from the sensing circuit to adjust driving strength accordingly.

3) Driving Stage: The driving stage adjusts the driving strength based on the result of the controller to drive the SiC.

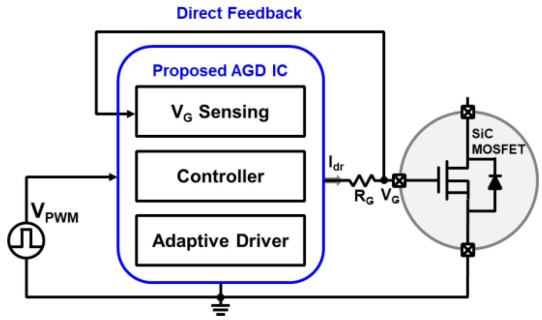

Fig. 3. Proposed gate-sensing method.

Nowadays, a wide range of SiC power devices are available. Currently, only one research focuses on a universal AGD for various SiC devices [24]. However, the turn-OFF process described in [24] requires memorizing the threshold voltage (V_{TH}) and Miller plateau voltage (V_{Miller}) during turn-ON by two analog-to-digital converters, which consumes additional area and power. Besides, due to source inductance, there is a voltage drop in V_G during turn-OFF, leading to a false trigger at the end of the weak driving interval.

This article proposes a robust universal AGD, with a primary focus on the innovation of the sensing method. To solve the problems of the I_D and V_{DS} sensing method, the gate-sensing technique eliminates the requirement for external sensing components, overcomes device packaging constraints, and extends the operable range of V_{DS} and I_{LOAD}. To solve the problems in [24], this study discards the memory-based method and applies the gate-sensing concept during the turn-OFF process to make real-time decisions of weak driving intervals, solving the false trigger problem and improving the power consumption of the driver. Furthermore, the adaptive reference generator' concept is extended to the turn-OFF process, enabling the universal gate driver. As a result, this innovation prevents redesigning drivers for various SiC devices, saving time and resources.

The subsequent sections of this article are structured as follows. Section II describes the concept of the proposed gate-sensing technique. The operation and implementation details of the proposed AGD are mentioned in Section III. Section IV presents the results and analysis of the measurements. Finally, Section V concludes this article.

II. Concept of Proposed Gate-Sensing Technique

This section shows the concept of gate-sensing technique based on the double-pulse test circuit [2], [3], [4], [5], [6], [7], [8], [14], [15], [16], [17], [18], [19], [20], [21], [22] with a constant driving current (I_{dr}), as shown in Fig. 4.

A. Effect of Source Inductance in Turn-ON Process

Fig. 5 shows the switching waveform of SiC. From t_0 to t_4, it shows the typical turn-ON process.

In stage 1 (S_1, t_0–t_1), the driver charges the gate–source capacitance (C_{GS}) of SiC, and the gate voltage (V_G), detected by the driver, starts to rise. During this period, since the gate–source voltage (V_{GS}) is below V_{TH}, I_D and V_{DS} remain constant. The rising speed of V_G is given by the following formula:

$$\frac{dV_G}{dt} = \frac{I_{dr}}{C_{GS}} \tag{1}$$

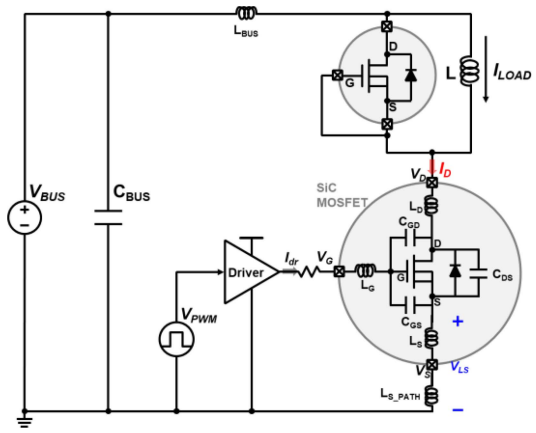

Fig. 4. Double pulse test setup.

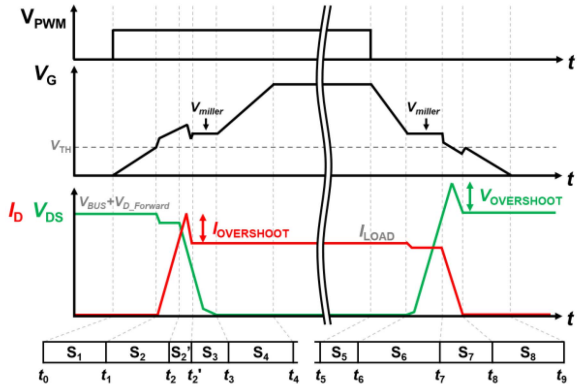

Fig. 5. Switching waveform of SiC.

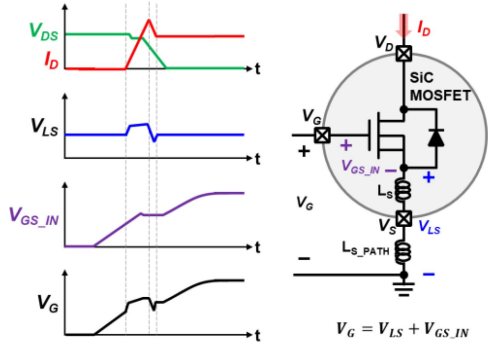

Fig. 6. Influence of inductance during turn-ON.

In stage 2 (S_2, t_1–t_2), when V_{GS} exceeds V_{TH}, I_D starts to increase with V_{GS}. The increasing speed of I_D (di/dt) induces a voltage (V_{LS}) across package source inductance (L_S) and source path inductance (L_{S_PATH}). This induced inductor voltage is expressed as follows:

$$V_{LS} = (L_S + L_{\mathrm{PATH}}) \cdot \frac{dI_D}{dt}. \tag{2}$$

Fig. 6 shows this phenomenon. Under constant I_D, V_G equals the internal gate voltage (V_{GS_IN}). However, when V_{LS} is induced, it will cause a slight rise in V_G expressed as follows:

$$V_G = V_{GS\_\mathrm{IN}} + V_{LS}. \tag{3}$$

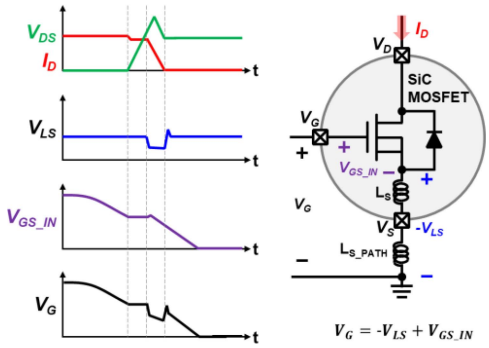

Fig. 7. Influence of inductance during turn-off.

In stage 2' (S_2', t_2–t_2') stage, due to the reverse recovery of the high-side diode, I_D overshoot ($I_{D.\mathrm{OV}}$) appears. According to [7] and [18], the magnitude of $I_{D.\mathrm{OV}}$ depends on the di/dt rate. The proposed driver controls the di/dt rate to suppress $I_{D.\mathrm{OV}}$.

In stage 3 (S_3, t_2'–t_3), after I_D reaches I_{LOAD}, V_{DS} starts to decrease. Due to V_{DS} decreasing, a current is induced from the gate to the drain of SiC through the gate–drain capacitance (C_{GD}), suppressing the rise of V_G. This results in V_G approaching a constant value called the Miller plateau.

In stage 4 (S_4, t_3–t_4), V_{DS} decreases to near zero, and V_G continues to rise until the turn-ON driver voltage.

B. Effect of Source Inductance in Turn-OFF Process

The period of t_5 to t_9 in Fig. 5 shows the turn-OFF process.

During stage 5 (S_5, t_5–t_6), the driver discharges C_{GS}, causing a slight increase in V_{DS} without inducing the Miller effect, so I_D and V_{DS} remain constant. The decline speed of V_G follows formula (1).

In stage 6 (S_6, t_6–t_7), V_G keeps decreasing until V_{DS} rises enough to induce current flow from the drain to the gate through C_{GD}, slowing V_G's decline and creating the Miller plateau.

In stage 7 (S_7, t_7–t_8), after V_{DS} increases until the high-side diode conducts, I_D begins to decrease. The negative di/dt induces a negative voltage ($-V_{LS}$) across L_S and L_{S_PATH}, as shown in Fig. 7, similar to the turn-ON process, where V_G equals V_{GS_IN} but minus V_{LS}, as expressed in the following formula:

$$V_G = V_{GS\_\mathrm{IN}} - V_{LS}. \tag{4}$$

This voltage drop on V_G helps detect current behavior, discussed in the next section. Additionally, the di/dt induces V_{LS} and causes V_{DS} overshoot ($V_{DS.\mathrm{OV}}$) via power path inductance (L_{BUS}) [2], [6], [8], [16], [17], [18]. Therefore, the driver controls di/dt rate to reduce $V_{DS.\mathrm{OV}}$.

In stage 8 (S_8, t_8–t_9), as I_D decreases to near zero, the induced V_{LS} diminishes, and V_G returns to its original value. The driver then discharges C_{GS} until V_G equals the turn-OFF driver voltage.

C. Advantages of Gate-Sensing Technique

1) Eliminating Sensing Components: Since the driver only provides V_G feedback, the system does not require external resistors for voltage scaling or external inductors to monitor I_D behavior. This advantage not only reduces the area of the driver but also decreases overall system costs.

2) Mitigating Package Limitations: Fig. 8 shows the schematic of the proposed AGD applied to both 3-pin and 4-pin

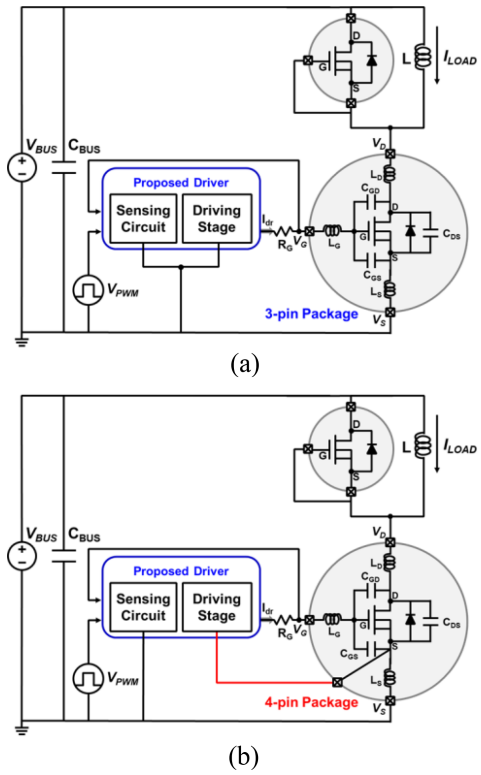

Fig. 8. Schematic of the proposed AGD applied to different packages. (a) 3-pin. (b) 4-pin.

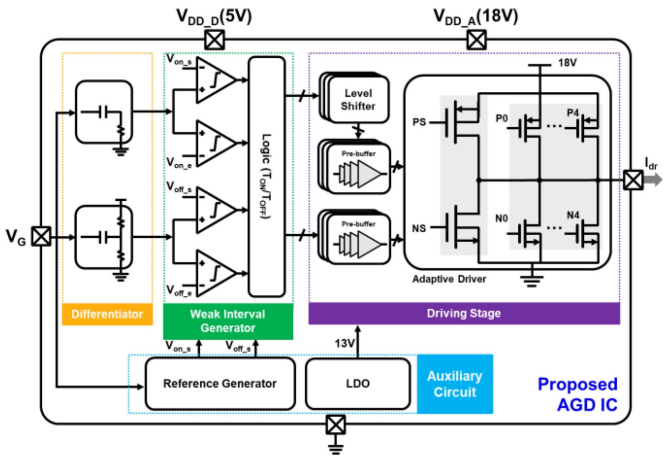

Fig. 9. Whole chip block diagram.

TABLE I
RELATIONSHIP BETWEEN V_G AND TIME POINTS

Time point	Relationship with V_G
t_1	Time of slope change (depend on C_{iss})
t_2'	Slope change from negative to positive
t_6	Time of slope change (depend on C_{iss})
t_8	Slope change from positive to negative

packages. In the 3-pin package, the ground of the sensing circuit shares a common ground with the driving stage. In contrast, for the 4-pin package, the proposed driver chip separates the grounds of the sensing circuit and the driving stage. To detect the effects of L_S, the sensing circuit ground is connected to the source pin, whereas the driver stage ground is connected to the Kelvin source for optimal driving of the SiC device. This gate-sensing technique effectively mitigates limitations imposed by the package configuration.

3) Extending I_{LOAD} *and* V_{DS} *Range:* Since the proposed AGD only feeds back V_G, it does not require sensing V_{DS}, which can potentially reach thousands of volts, or I_D, which requires a transformer to detect. The critical aspect of the gate-sensing mechanism is the magnitude of V_{LS}, which depends on I_{dr}, *di/dt*, L_S, and L_{S_PATH}; if this magnitude is too small, the mechanism may fail to operate. Therefore, we examine whether variations in I_{LOAD} and V_{DS} affect the magnitude of V_{LS}.

The magnitude of V_{DS} at stage 1 mainly influences gate–drain capacitance (C_{GD}), resulting in a low impact on the magnitude of V_{LS}. Furthermore, the magnitude of I_{LOAD} does not affect V_{LS}. Consequently, variations in I_{LOAD} and V_{DS} have minimal impact on the proposed gate-sensing mechanism, allowing an extended range for I_{LOAD} and V_{DS}.

III. IMPLEMENTATION OF PROPOSED ACTIVE GATE DRIVER

This section introduces the operation and circuit implementation of the proposed AGD. As shown in Fig. 9, the system comprises four main components: differentiator, weak driving interval generator, driving stage, and auxiliary circuit. The proposed AGD can automatically identify different SiC devices and find the target weak driving intervals for turn-ON and turn-OFF. Subsequently, it adjusts the driving strength to mitigate the switching issues mentioned in the preceding section.

A. Gate-Sensing Technique

The gate-sensing technique only detects the gate voltage (V_G) of SiC to find the target's switching intervals. Since the driver's driving voltage is provided directly by the chip which can feed back V_G without any voltage scale-down. In the traditional V_{DS} feedback approach, V_{DS} is affected by the input voltage (V_{BUS}), up to hundreds or thousands of volts, requiring external voltage division components to meet the chip's voltage range, impacting the overall area and the driver's operation.

The target's weak driving intervals are the *di/dt* interval until $I_{D.OV}$ (t_1–t_2', S_2–S_2') during turn-ON and the *dv/dt* and *di/dt* intervals (t_6–t_8, S_6–S_7) during turn-OFF. Based on the previous analysis of the device's switching behavior, Table I shows the relationships between the four detected time points and V_G.

During the turn-ON process, at t_1, V_G changes slope by *di/dt* while transitioning from S_1 to S_2. After the *di/dt* interval ends, V_{LS} disappears, causing V_G to descend to its initial state and enter the Miller plateau. In this process, V_G first decreases and then rises, indicating a slope change at t_2'. During the turn-OFF process, t_6 marks the transition from S_5 to S_6, where V_G slope changes from discharging with a constant slope to the Miller plateau with an approaching zero slope, similar to the turn-ON from S_1 to S_2. At t_8, the *di/dt* interval ends, V_G rises back to its original state, and the V_G slope transitions from negative to positive. This summarizes the relationship between the four time points and the slope of V_G.

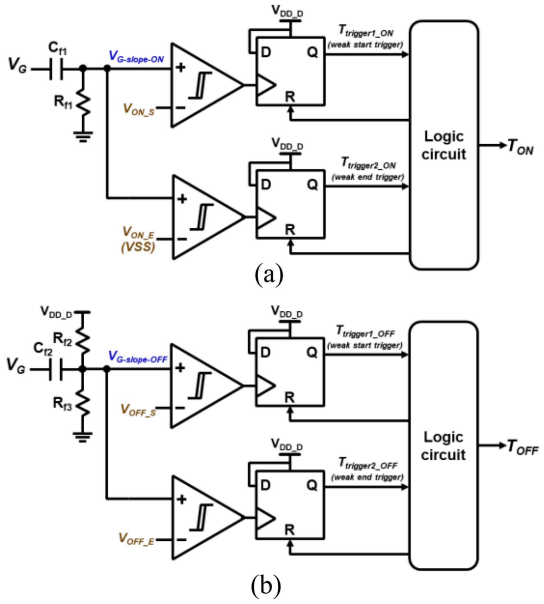

Fig. 10. Schematic of differentiator and weak driving interval generator. (a) Turn-ON. (b) Turn-off.

B. Operation Principle of Proposed AGD

According to [25], hard switching behavior generates both conducted common-mode (CM) and differential-mode (DM) EMI. CM noise occurs due to the charging and discharging of parasitic capacitances between the SiC drain and the ground. Studies have shown that the capacitance with high potential variations (*dv/dt*) offers reliable accuracy in assessing conducted EMI [26], [27]. Moreover, the high *di/dt* associated with switching actions leads to elevated emissions. Thus, the DM noise source can be represented by the loop current flowing through the power switch [27]. To eliminate conducted EMI, decreasing the speed of *di/dt* and *dv/dt* is the crucial solution in driver implementation.

Based on previous analysis, it has been found that the best way to suppress overshoot, oscillation, and EMI issues during turn-ON is to reduce driving strength during the *di/dt* interval until the current overshoot. As for turn-OFF, the target's weak driving intervals are the *dv/dt* and *di/dt* intervals (t_6–t_8). The primary reason is the occurrence of $V_{DS.OV}$ coincided with the start of I_D decline. The propagation delay in the circuit and parasitic effects may result in imprecise timing. Hence, driving strength is reduced during the *dv/dt* and *di/dt* intervals for turn-OFF, ensuring the driver's effective performance.

C. Differentiator and Weak Driving Interval Generator Circuit

Fig. 10 shows the circuit implementation for the differentiator and weak driving interval generator. In Fig. 10(a), designed for turn-ON, V_G passes through a high-pass filter composed of a series capacitor and resistor, generating the V_G slope waveform ($V_{G\text{-slope-ON}}$), which can be expressed as follows:

$$V_{G-\text{slope-ON}} = R_{f1} \cdot C_{f1} \cdot \frac{dV_G}{dt}. \tag{5}$$

Then, a comparator is used to evaluate the slope magnitude. When $V_{G\text{-slope-ON}}$ exceeds the weak start reference voltage

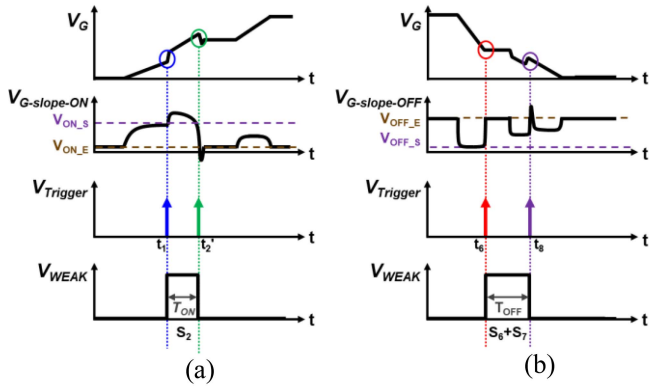

Fig. 11. Operating waveform of differentiator and weak interval generator. (a) Turn-ON. (b) Turn-OFF.

($V_{\text{ON\_}S}$), it indicates the start of I_D conduction. The endpoint of weak driving is determined by the transition of the V_G slope from negative to positive. Hence, the weak driving reference voltage ($V_{\text{ON\_}E}$) is set to VSS. Fig. 11(a) shows the waveform of this process. The weak driving interval signal (T_{ON}) is generated during the switching process and is sent to the subsequent control circuit to control driving strength.

Fig. 10(b) shows the circuit implementation for turn-OFF. Unlike turn-ON, the V_G slope during turn-OFF is negative. The high-pass filter increases the dc level using R_{f2} and R_{f3} to avoid comparison with the negative reference voltage. The output of this high-pass filter is also related to the V_G slope (dV_G/dt). The signal $V_{G\text{-slope-OFF}}$ can be expressed as follows:

$$V_{G-\text{slope-OFF}} = V_{DD\_D} * \left(\frac{R_{f3}}{R_{f2}+R_{f3}}\right) + (R_{f2}||R_{f3}) \cdot C_{f2} \cdot \frac{dV_G}{dt}. \tag{6}$$

The subsequent circuits are similar to the turn-ON part. The weak start reference voltage ($V_{\text{OFF\_}S}$) denotes the slope transition of V_G from S_5 to S_6 and is associated with C_{GS} and the high-pass filter design, which will be derived later. The weak end reference voltage ($V_{\text{OFF\_}E}$) marks the endpoint of *di/dt*, where the V_G's slope changes from negative to positive. This makes $V_{G\text{-slope-OFF}}$ cross the dc voltage division level, so $V_{\text{OFF\_}E}$ equals the voltage division result of R_{f2} and R_{f3}.

$V_{\text{ON\_}S}$ and $V_{\text{OFF\_}S}$ have similar meanings. In the previous stage, the driver charges or discharges C_{GS} of SiC, whereas there is a slope change in the next stage. To detect this transition, these reference voltages relate to the driver's charging and discharging speed of C_{GS}. Therefore, their values can be expressed as follows:

$$V_{\text{ON\_}S} = R_{f1} \cdot C_{f1} \cdot \frac{I_{dr}}{C_{\text{ISS}}} \tag{7}$$

$$V_{\text{OFF\_}S} = V_{DD\_D} * \left(\frac{R_{f3}}{R_{f2}+R_{f3}}\right) - (R_{f2}||R_{f3}) \cdot C_{f2} \cdot \frac{I_{dr}}{C_{GS}}. \tag{8}$$

D. Adaptive Driver Circuit

Fig. 12 shows the schematic of the adaptive driver without overvoltage issues. It comprises parallel-connected p-type

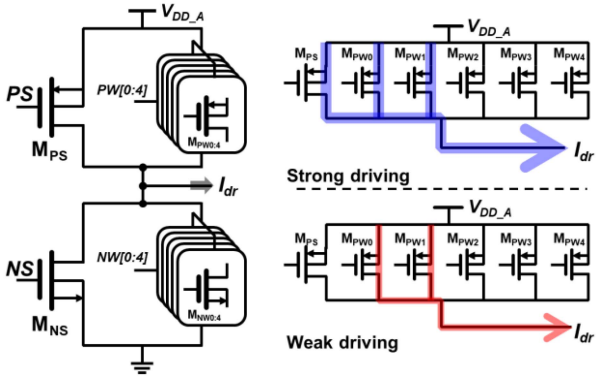

Fig. 12. Schematic of adaptive driver.

metal-oxide-semiconductor (PMOS) and n-type metal-oxide-semiconductor (NMOS) transistors of varying sizes. To achieve stronger driving strength, additional transistors are activated, whereas weaker driving strength is achieved by selectively deactivating certain transistors. External signals determine which small MOSFETs are engaged to decide the magnitude of weak driving strength. The circuit activates the largest and other smaller power MOSFETs for strong driving strength. For weak driving strength, the largest MOSFET is deactivated. This modulation of driving strength manages the *di/dt* rate during turn-ON and the *di/dt* and *dv/dt* rates during turn-OFF. This logic-based architecture is straightforward and easily implementable.

Since a larger C_{GS} results in a lower slope for V_G at the same driving strength, it also reduces the *di/dt* rate, ultimately inducing a lower V_{LS}. This, in turn, leads to a smaller detectable slope change, increasing the impact of noise. Therefore, in the design of the adaptive driver, the device with the largest C_{GS} is considered the worst case. The minimum strong driving strength is set based on this scenario to minimize noise interference. Additionally, to achieve the targeted switching frequency, the peak instantaneous current is set at 310 mA.

E. Adaptive Reference Generator Circuit

To create a universal gate driver, the driver needs to determine the weak driving intervals specific to each SiC device. Since different SiC devices have different C_{GS}, the proposed AGD requires different weak start reference voltages ($V_{\mathrm{ON\_}S}$ and $V_{\mathrm{OFF\_}S}$). Thus, the proposed adaptive reference generator's role is to detect each device's C_{GS} and generate corresponding reference voltages to achieve universal functionality.

Fig. 13 shows the turn-ON waveforms of two different SiC devices, highlighting the concept of this circuit. Device 2 has double the C_{GS} of Device 1. In interval S_1, with the same driving current, Device 1's V_G slope is twice that of Device 2. Hence, $V_{\mathrm{ON\_}S1}$ should be twice $V_{\mathrm{ON\_}S2}$. By detecting C_{GS}, the circuit can generate a corresponding reference voltage. The C_{GS} detection involves sampling V_G at the same time point (T_{Sense}) during S_1, converting the sampling voltage ($V_{G.\mathrm{Sense}}$) into current to charge the capacitor and generate the reference voltage, incorporating the high-pass filter's parameters. Since $V_{\mathrm{OFF\_}S}$ has the same properties as $V_{\mathrm{ON\_}S}$, it can also be created using this concept.

Fig. 14 shows the schematic of the adaptive reference generator circuit. This circuit only needs one cycle to create reference

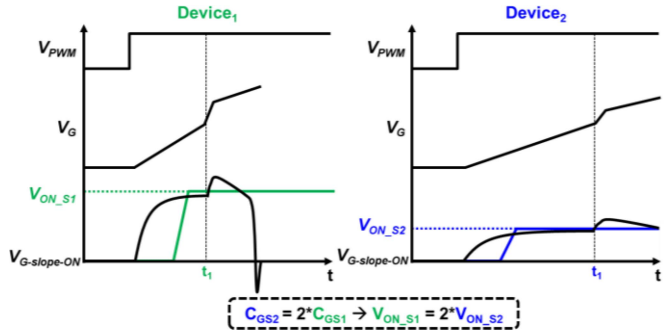

Fig. 13. Turn-ON waveforms of different SiC devices.

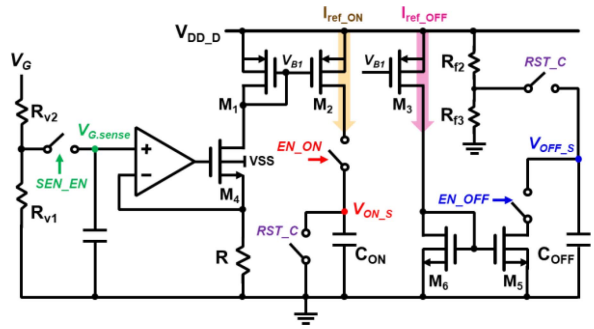

Fig. 14. Schematic of the adaptive reference generator.

voltages. The SEN_EN signal samples V_G, and the operational amplifier ensures the voltage across the resistor (R) equals $V_{G.\mathrm{Sense}}$. Therefore, a current related to $V_{G.\mathrm{Sense}}$ is generated. Then, $I_{\mathrm{ref\_ON}}$ is created by the current mirror to charge C_{ON} and produce $V_{\mathrm{ON\_}S}$. As for $V_{\mathrm{OFF\_}S}$, since it represents the negative slope, its value should be lower than the voltage divider of R_{f2} and R_{f3}. Therefore, $I_{\mathrm{ref\_OFF}}$ discharges C_{OFF} to generate $V_{\mathrm{OFF\_}S}$. $V_{\mathrm{ON\_}S}$ and $V_{\mathrm{OFF\_}S}$ can be expressed as follows:

$$V_{\mathrm{ON\_}S} = \frac{V_{G.\mathrm{Sense}}}{R} \cdot K_1 \cdot \frac{1}{C_{\mathrm{ON}}} \cdot \Delta t \tag{9}$$

$$V_{\mathrm{OFF\_}S} = V_{DD\_D} * \left(\frac{R_{f3}}{R_{f2}+R_{f3}}\right) - \frac{V_{G.\mathrm{Sense}}}{R} \cdot K_2 \cdot \frac{1}{C_{\mathrm{OFF}}} \cdot \Delta t \tag{10}$$

where K_1 represents the current mirror ratio between M_1 and M_2, whereas K_2 denotes the ratio between M_1 and M_3.

To determine the values for K_1 and C_{ON}, (7) and (9) are compared. Similarly, comparing (8) and (10) aids in designing the values for K_2 and C_{OFF}.

Fig. 15 shows the operating waveform of the adaptive reference generator. The RST_C signal initializes C_{ON} and C_{OFF} voltages. SEN_EN is the sampling signal, whereas EN_ON and EN_OFF control the charging and discharging time ($\triangle t$) for C_{ON} and C_{OFF}.

IV. Measurement Result

In the measurement, three different SiC power devices were utilized: Infineon IMW65R048M1H [28], IMW65R107M1H [29], and IMW65R027M1H [30]. Since the driving voltage for those SiC devices is 18 V, the TSMC 0.18-μm BCD process was

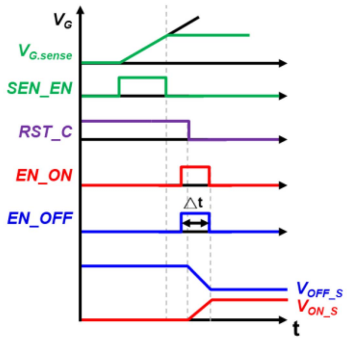

Fig. 15. Operating waveform of adaptive reference generator.

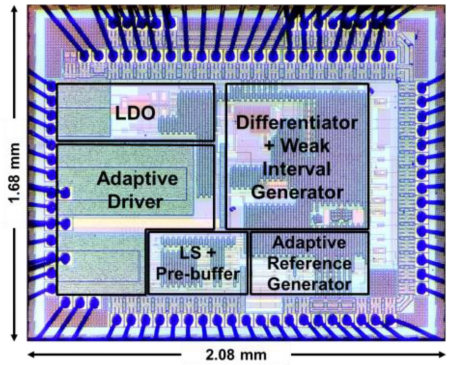

Fig. 16. Chip micrograph.

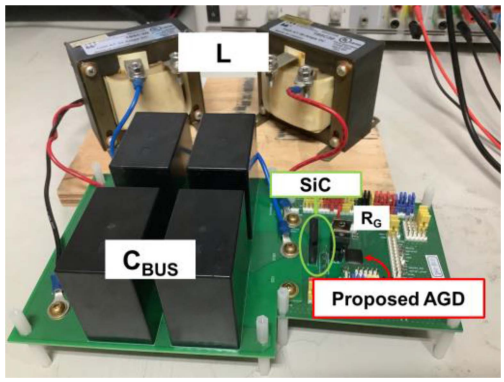

Fig. 17. Measurement setup for proposed AGD.

employed for fabrication. Fig. 16 shows the micrograph of the chip. The total chip area is 1.68×2.08 mm^2.

Fig. 17 shows the double pulse test setup, and Fig. 18 shows its schematic. C_{BUS} consists of four parallel thin film capacitors to stabilize the high-voltage input source and minimize their parasitic inductance. The load inductor (L) comprises two series inductors to reduce parasitic capacitance. The measurements utilize the same SiC devices for both high-side and low-side components.

The three SiC power devices vary in on-state resistance ($R_{\mathrm{DS.ON}}$) and C_{GS}. Validating the universality of the proposed AGD involves measuring these different kinds of SiCs. Additionally, to assess the AGD's effectiveness, the chip can be externally controlled to turn off the weak driving function, converting it into a CGD.

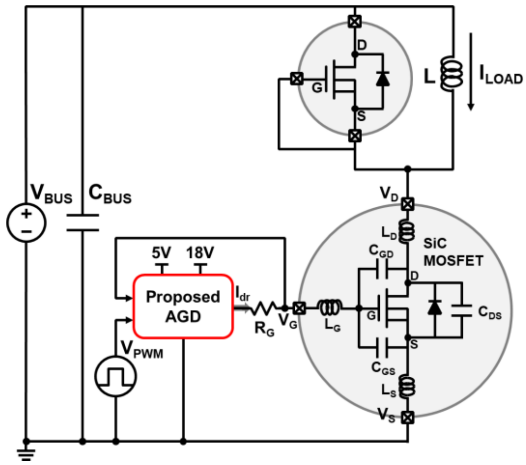

Fig. 18. Schematic of the measurement setup.

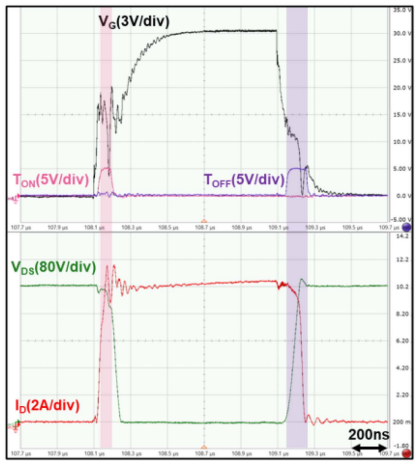

Fig. 19. AGD waveform of IMW65R048M1H @ $V_{\mathrm{BUS}}/I_{\mathrm{LOAD}} =$ 400 V/10 A.

In the measurement, the driving strength of CGD is adjustable by varying the external gate resistor (R_G). In AGD measurement, the R_G is 50 Ω for turn-ON and 30 Ω for turn-OFF. The switching frequency is configured at 0.5 MHz and the driver power consumption is about 100 mW.

A. Proposed AGD Waveform

Fig. 19 shows the measurement results of the IMW65R048M1H device using the proposed AGD. The measurement condition is set at $V_{\mathrm{BUS}}/I_{\mathrm{LOAD}} = 400$ V/10 A. The T_{ON} and T_{OFF} signals denote the weak driving intervals captured by the driver during turn-ON and turn-OFF, respectively. In the measurement result, T_{ON} includes the *di/dt* to $I_{D.\mathrm{OV}}$ interval, whereas T_{OFF} includes the *di/dt* + *dv/dt* interval. This verifies that the chip operates as expected by capturing the target's weak driving intervals.

Fig. 20 presents the I_D and V_{DS} waveforms of the IMW65R048M1H under different V_{BUS} and I_{LOAD} conditions. The comparison between the CGD (dashed line) and AGD (solid lines) shows that despite changes in V_{BUS} and I_{LOAD}, the proposed AGD consistently captures the target's weak driving intervals and reduces the driving strength to suppress I_D and

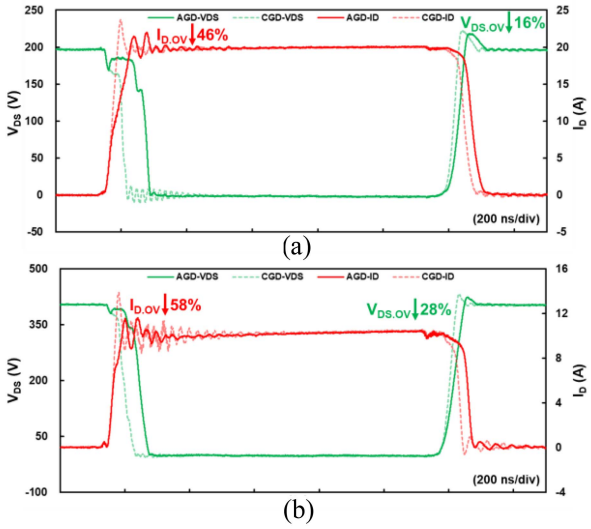

Fig. 20. AGD and CGD waveform of IMW65R048M1H. (a) $V_{\rm BUS}/I_{\rm LOAD}$ = 200 V/20 A. (b) $V_{\rm BUS}/I_{\rm LOAD}$ = 400 V/10 A.

V_{DS} overshoot and oscillation. Specifically, at $V_{\rm BUS}/I_{\rm LOAD}$ = 200 V/20 A, the AGD reduces I_D overshoot ($I_{D.\rm OV}$) by 46% and V_{DS} overshoot ($V_{DS.\rm OV}$) by 16%. At $V_{\rm BUS}/I_{\rm LOAD}$ = 400 V/10 A, $I_{D.\rm OV}$ is reduced by 58% and $V_{DS.\rm OV}$ by 28%. These results demonstrate that the proposed AGD effectively mitigates $I_{D.\rm OV}$ and $V_{DS.\rm OV}$ compared to CGD.

B. Different SiC Devices Waveform

Fig. 21 shows the waveform results of two other SiC devices, IMW65R027M1H and IMW65R107M1H. Despite the different devices, the proposed AGD successfully identifies weak driving intervals and improves switching performance issues. Fig. 22 compares the waveform results of these two devices between AGD and CGD under $V_{\rm BUS}/I_{\rm LOAD}$ = 400 V/10 A. For IMW65R027M1H, AGD reduces $I_{D.\rm OV}$ by 43% and $V_{DS.\rm OV}$ by 30%. For IMW65R107M1H, AGD achieves a remarkable reduction of 73% in $I_{D.\rm OV}$ and 27% in $V_{DS.\rm OV}$. Both $I_{D.\rm OV}$ and $V_{DS.\rm OV}$ are effectively suppressed, and the oscillation amplitude is significantly reduced.

C. Tradeoff Curve

Fig. 23 shows the tradeoff curves for IMW65R048M1H. The figure shows the improvement in switching time and losses of AGD compared to CGD under the same $I_{D.\rm OV}$ and $V_{DS.\rm OV}$ conditions. In Fig. 23(a), the relationship between $I_{D.\rm OV}$ and rise time are shown. AGD achieves a 62.9% reduction in rise time compared to CGD under the same $I_{D.\rm OV}$. Fig. 23(b) displays the relationship between $I_{D.\rm OV}$ and turn-ON switching loss ($E_{\rm LOSS}$), where AGD demonstrates a 48.7% reduction in turn-ON $E_{\rm LOSS}$ compared to CGD under the same $I_{D.\rm OV}$. Fig. 23(c) shows the relationship between $V_{DS.\rm OV}$ and fall time, indicating a 30.1% reduction in fall time with AGD compared to CGD under the same $V_{DS.\rm OV}$. In Fig. 23(d), the relationship between $V_{DS.\rm OV}$ and turn-OFF switching loss ($E_{\rm LOSS}$) are shown. Under the same $V_{DS.\rm OV}$, AGD displays an 18.8% reduction in turn-OFF $E_{\rm LOSS}$ compared to CGD. The tradeoff curves demonstrate the

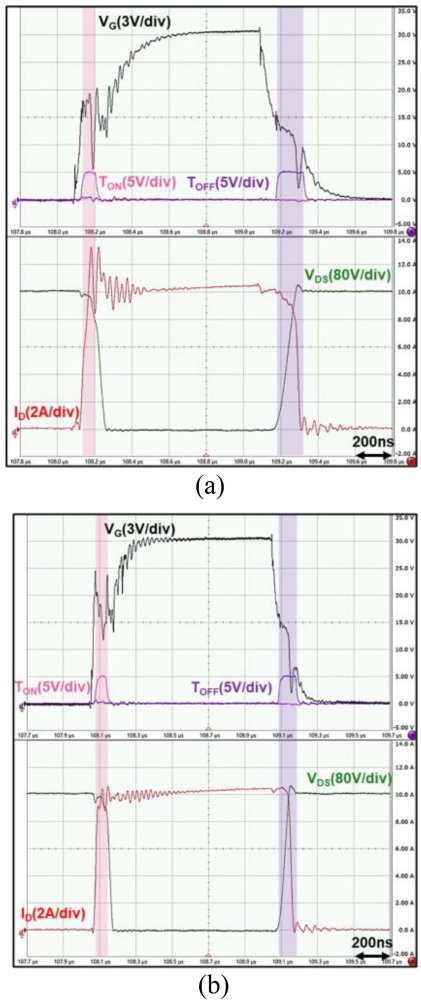

Fig. 21. AGD waveform of different SiC. (a) IMW65R027M1H. (b) IMW65R107M1H.

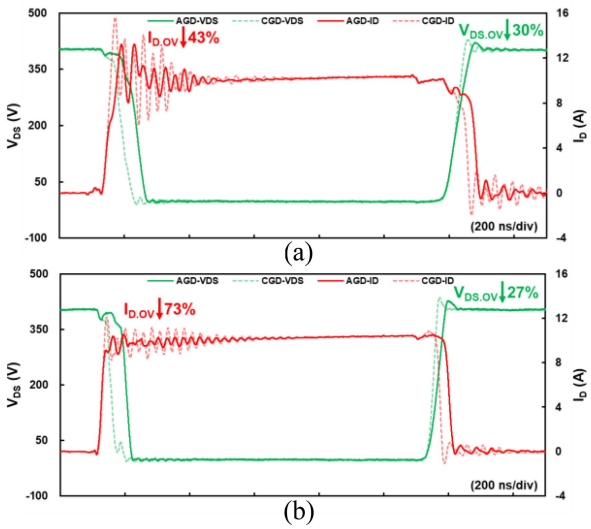

Fig. 22. AGD and CGD waveform of different SiC. (a) IMW65R027M1H. (b) IMW65R107M1H.

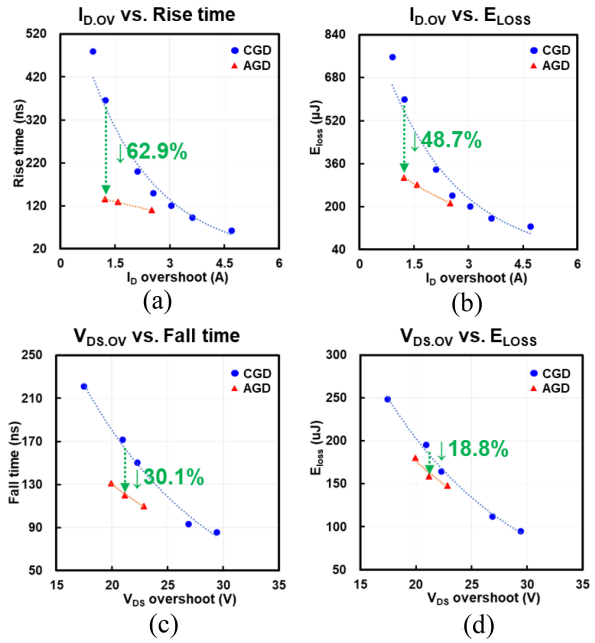

Fig. 23. Tradeoff curves for IMW65R048M1H. (a) $I_{D.\mathrm{OV}}$ versus Rise time. (b) $I_{D.\mathrm{OV}}$ versus turn-ON E_{LOSS}. (c) $V_{DS.\mathrm{OV}}$ versus fall time. (d) $V_{DS.\mathrm{OV}}$ versus turn-OFF E_{LOSS}.

advantages of AGD over CGD, breaking the tradeoff curves of CGD and delivering improved performance.

The results of this tradeoff curve show that under the same overshoot conditions for AGD and CGD, a smaller overshoot yields greater improvement with AGD. This is because, to achieve the same overshoot, the weak driving strength of AGD theoretically matches the driving strength of CGD. Larger overshoot indicates a stronger weak driving strength, resulting in AGD's strong and weak driving strengths becoming more similar and thus approaching the performance of CGD. This correlation accounts for the observed statistical results.

V. Conclusion

The proposed integrated universal AGD only detects the gate voltage of SiC and reduces driving strength during the target's intervals, saving discrete sensing components, mitigating package limation, extending I_{LOAD} and V_{DS} range, and effectively suppressing the SiC switching issues. Additionally, an adaptive reference voltage generator is proposed to allow the driver to generate corresponding reference voltage for different SiCs automatically. This feature increases the flexibility of applications. The chip is fabricated using the TSMC 0.18-μm BCD process for verification. The measurement results demonstrate that the proposed AGD can capture the target's weak driving intervals, reduce driving strength, and effectively suppress $I_{D.\mathrm{OV}}$, $V_{DS.\mathrm{OV}}$, and oscillations. Furthermore, the results under different V_{BUS} and I_{LOAD} conditions demonstrate the flexibility of the gate-sensing technique in diverse environments. Lastly, the outcomes obtained from different SiC devices show the applicability of the proposed AGD, which is suitable for various SiC devices. According to the measurement results of the IMW65R048M1H device under the same $I_{D.\mathrm{OV}}$, the turn-ON E_{LOSS} is reduced by 48.7% compared to CGD. Similarly, under the same $V_{DS.\mathrm{OV}}$, the turn-OFF E_{LOSS} is reduced by 18.8% compared to CGD. These measurement results prove the advantages and functionality of the proposed universal AGD and highlight its ability to improve SiC-based power management systems.

Acknowledgment

The authors would like to thank the Taiwan Semiconductor Research Institute for chip fabrication and the Semiconductor Research Center of Hon Hai Research Institute for technology exchange.

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