Distributed Self-Interleaving PWM Signals With Fault-Tolerant Capability for High-Performance Microprocessor Power Supply in Aerospace

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***Abstract*—In this article, we introduce a novel distributed self-interleaving management solution with enhanced noise immunity for multiphase converters applications. This solution, in conjunction with a distributed local decision self-monitoring circuit, has the potential to increase the functional safety and availability of microprocessor power supplies in aerospace. In the literature, most recent distributed control technique for interleaving the pulsewidth modulation gating signals of the converter rely on analog carrier-based signals, making it susceptible to external disturbances and noise, especially as the number of phases increases. In response, this article proposes an original distributed self-interleaving method based on a double-input phase-locked loop (2I-PLL) circuit. This approach synchronizes and interleaves oscillators using two logic-level signals where the level transition carries the phase delay information, mitigating analog signal limitations. Studies using modal analysis address challenges such as system stability and dynamic/convergence response. The 2I-PLL method is validated through simulations and experiments, covering scenarios from 4 to 10 phases and switching frequency from 50 kHz to 3 MHz.**

***Index Terms*—Aerospace, distributed control, interleaved control signals, multiphase converter, pulsewidth modulation (PWM), voltage regulator module.**

NOMENCLATURE

PWM	Pulsewidth modulation.
2I-PLL	Double-input phase-locked loop.
SPOF	Single point of failure.
VRM	Voltage regulation module.
SPS	Smart power stage.
MPCG	Multiphase clock generation.
N	Number of phases.
k	Subscript associated with the kth module where $k \in \{1, 2, 3, \ldots, N\}$.
θ_k	Phase-shift of kth local signal.
$\theta_{\Delta t}$	Phase-shift delta in interleaved steady-state.
v_{t_k}	Analog carrier signals.
v_{clk_k}	Analog PWM clock signals.
PD	Phase detector.
LF	Loop filter.
VCO	Voltage-controlled oscillator.
PAC	Periodic average circuit.
f_0	Frequency range.
λ_0	Eigenvalue of common-mode response.
$\lambda_1, \ldots, \lambda_{N-1}$	Eigenvalues of differential-mode response.
$v_{\varepsilon\theta_k}, \lvert v^{\Lambda}_{\varepsilon\theta_k} \rvert$	Local, and modal errors.

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I. INTRODUCTION

IN THE ever-advancing landscape of power electronics, the demand for high-performance microprocessor (μP) supplies, whether in terrestrial [1] or in aerospace applications [2], [3], [4], presents both exciting opportunities and challenges. Modern μPs are critical to the functionality of spacecraft and aircraft, which require efficient and reliable power supplies. To meet these demands, the multiphase-interleaved dc–dc converters introduced in [5] and [6], particularly as VRMs with centralized control, have become indispensable compared to single-phase VRM, as observed in Fig. 1. These converters not only ensure the delivery of stable and clean power but also play a pivotal role in maintaining the integrity and safety of onboard electronics.

The exponential growth in processor current consumption has led to an increased reliance on multiphase-interleaved converters, shown in Fig. 2, due to spread power, better transient response, and reduced filtering volume due to interleaved PWM signals. Most of them are based on a centralized control architecture with an unique digital controller implementing the MPCG. The modern centralized controllers are associated with SPSs. The SPSs integrate the driver IC, power MOSFETs, current sensing, and protection features, as in [8], providing a high-power density, and way to cope with thermal and EMI issues.

A second approach are the scalable–stackable control architectures where multiple controllers (also called modules), such as [9] and [10], can be associated together in a primary–secondary configuration. In this approach, despite all the building blocks being identical, some redundant elements are active only on the primary, while disabled on all secondary. During

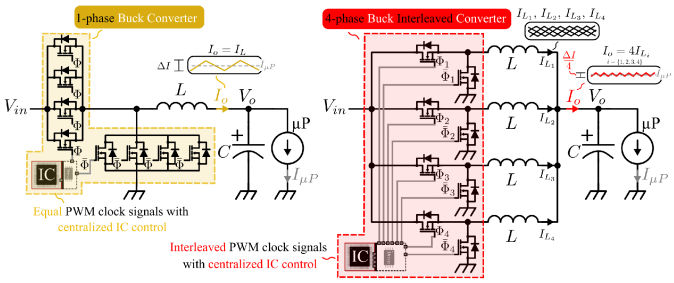

Fig. 1. Overview of VRMs used for a first generation microprocessor (μP) supply from a Intel's consortium (adapted from [7]). (On the left) 1-phase VRM. (On the right) 4-phase VRM. Note that both use centralized/nondistributed ICs.

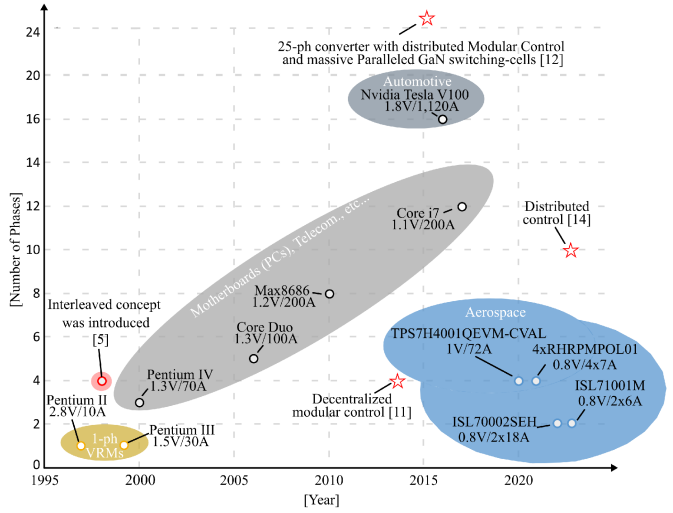

Fig. 2. Timeline of multiphase-interleaved DC–DC converter solutions. Evolution under different applications with their commercial references and ratings of V_o/I_o. The red circle shows the initial contribution of interleaved concept wih centralized control. The red stars highlight contributions proposing distributed IC control with distributed PWM signals.

operation, these converters are normally less flexible and less performing than a centralized solution. It should be noted that the scalable–stackable controller can be integrated with the SPS without significant impact to the package size.

A different kind of scalable–stackable based on distributed control architecture was presented in [11] and [12] to introduce capability of reconfiguration based on the local self-monitoring decision offering the performance of a centralized control and the modularity of the scalable–stackable approach, in addition to unique advantages, such as fault tolerance and self-reconfiguration capabilities, which are paramount in the harsh environment of aerospace. Each module is composed of local controllers for interleaving, current balance, and voltage regulation, active in all modules simultaneously.

Recently, with the arrival of self driving cars, the fault tolerance capability caught attention of automotive applications [13] with the objective to increase the availability of redundant systems and avoid triplication. As a result, some variations were proposed to improve the voltage regulation [14], interleaving [15], and phase shedding [16]. Indeed, this can be seen as

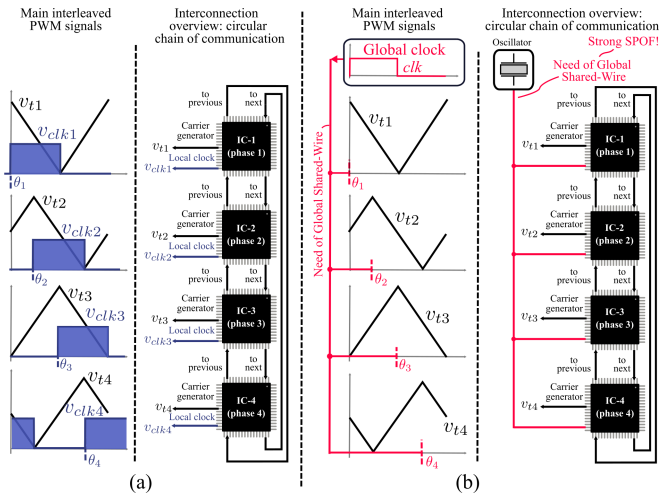

Fig. 3. Examples of self-interleaving methods. (a) Original self-interleaving solution [19]. (b) Digitalized solution with a shared wire [20].

a trend for aerospace sector too, since uninterrupted μP power supplies are critical in order to guarantee operational safety of modern/upcoming satellites.

The several control architectures in the literature for multiphase and multilevel interleaved converters present different amounts of SPOF weaknesses [17]. The microsatellite electrolysis propulsion in [17] has no dynamic phase regulation because the main concern is availability. The architecture chosen is compact, prioritized redundancy, and is assumed to be too complex to implement dynamic reconfiguration on it, therefore, the input/output current ripple is degraded in case of a phase loss. The high performance μP cannot tolerate high voltage ripple caused by improper interleaving in case of phase loss.

The proposed distributed modular self-interleaving approach, in conjunction with the bypass-circuity, the local self-monitoring circuit, and thanks to the full modularity, can ensure reconfiguration capability and drastic reduction of SPOF on the control scheme, including phase interleaving. During a fault-event, the local self-monitoring circuit detects, disables and bypass the faulty module. Then, the active modules self-reconfigure to a new steady-state interleaving arrangement with fewer active phases, ensuring safe operation, proper interleaving, and slightly degraded transient response. When a non-SPOF event happens in the power stage, the self-monitor also disables the faulty module to transition to a less degraded operation mode with proper interleaving arrangement.

It is worth to highlight that the novelty of this article is not the distributed topology and operation itself, but one of its components, the distributed self-interleaving, that was changed to be less prone to mismatches and have a higher noisy-immunity. A state-of-the-art of scalable–stackable interleaving techniques is shown in [18]. To improve availability, the SPOF shared lines must be avoided, so the circular chain of communication combined with the bypass circuits is preferred.

The self-interleaving solution in [11], [12], and [19], Fig. 3(a), with its stability study in [18], relies on exchanging analog triangular signals in a circular chain of communication to achieve

the self-interleaving mechanism. However, such a solution is vulnerable to mismatches and noise dependency (i.e., external disturbances), especially in a scenario with a high number of phases. Such vulnerability can be reduced by considering the digitalization of the self-interleaving solution introduced in [20], Fig. 3(b), with stability studied in [21]. It consists of a digital iterative solution implemented and validated into an FPGA. A clock at the converter switching frequency is sent to all carrier generators to provide a phase-shift reference. Each carrier generator receives the neighbor's phase-shift in a parallel bus by the circular chain of communication, and does its calculations to place the local phase-shift in the center of its neighbors to achieve proper interleaving. Then, each carrier generator position its PWM signal with a shift (the locally computed phase-shift) to the shared clock (reference, at the switching frequency). Despite mitigating noise and mismatches, this digital solution requires multiple connections and has strong SPOF through the global clock shared-wire.

This article introduces a more robust distributed modular self-interleaving method based on a 2I-PLL circuit. The proposed 2I-PLL is suitable/attractive to reduce the SPOFs as well as improve the performance of commercial ASICs designed to operate as multiphase dc–dc converter with peak-current mode control which require interleaved clock signals, such as [22] and [23]. This method is based on the exchange of independent local clocks (specific to each module) capable of modifying their own frequency, instantaneously, to adjust their relative phase-shift [15]. By using digital signals (clock signals), where only transitions (i.e., the rising and falling edges) convey phase-shift and frequency information, it is possible to overcome the drawbacks of analog approaches, and provide a more robust system.

The rest of this article is organized as follows. Section II, gives an overview and describes self-interleaving concept with the distributed approach. Section III presents the details of the 2I-PLL that interleaves locally the generated clock signals. Section IV presents a modal analysis of the system in order to determine its dynamic response and stability criteria. Sections V and VI present simulation and experimental results to validate the proposed self-interleaved distributed method for clock signals. Finally, Section VII concludes this article.

II. Self-Interleaving Signal Concept

A. Principle and System Overview

The basic principle to guarantee a proper interleaving of different signals placed in a circular ring is to ensure that, locally, the phase-shift θ_k of the kth signal is equally phase-shifted from its adjacent signals phase-shift θ_{k-1} and θ_{k+1}. In steady-state, the phase-shift between neighbors must be equal to $\theta_{\Delta t}$, as follows:

$$\underbrace{\theta_{k+1}}_{\text{next}} - \theta_k = \theta_k - \underbrace{\theta_{k-1}}_{\text{previous}} = \theta_{\Delta t} = \frac{2\pi}{N}, \tag{1}$$

where N is the number of phases or modules, and $k = \{1, 2, 3, \ldots, N\}$ is associated with the kth module. Variables

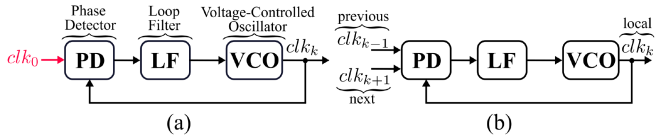

Fig. 4. PLL diagram blocks. (a) Conventional PLL. (b) Proposed 2I-PLL.

θ_{k-1}, θ_k, and θ_{k+1} represent the phase position of previous, local and next signals, respectively.

Fig. 3(a) gives an overview of the original system with triangular carrier-based self-interleaved PWM signals applied in a four-phase scenario. In the original solution, a triangular signal is produced by each carrier generator and shared with its neighbors. In this new solution, the carrier generator produces and shares a digital signal, so a different circuitry is required to achieve self-interleaving.

III. Double-Input PLL Description

The implementation of this new interleaving method can be derived from a conventional PLL block diagram Fig. 4(a), but with two inputs, named 2I-PLL, shown in Fig. 4(b).

As for conventional PLL, a VCO is required, as well as a feedback loop to make sure that the local signal clk_k is between the previous clk_{k-1} and the next clk_{k+1} signals. Hence, to provide the self-interleaving method with this new approach, a particular PD has to be designed, to track the local clock frequency and also to interleave the local VCO clock signal clk_k with the clock signals from previous (clk_{k-1}) and next (clk_{k+1}) modules, respectively. The LF contributes to improve the dynamic performance of the VCO. Note that the proposed 2I-PLL do not require any synchronizing clock (or global shared-wire signal) neither high speed clock, and the VCO frequency is the converter phase switching frequency.

A. Operation Principle

Fig. 5 shows an example of main waveforms associated with the 2I-PLL operating during transient as well as during the steady-state. Note that in this case, the self-alignment of clock signals is implemented to commute the digital signals (UP and DN) signals when a falling edge border event takes place. The duration difference between UP and DN is proportional to the self-alignment error.

B. Main Blocks of Proposed Distributed 2I-PLLs

A more detailed description of the proposed 2I-PLL will be described here.

1) Phase Detector: The first block of 2I-PLL is a nonconventional PD (shift error), depicted in Fig. 6(a), to convert a phase-shift error in a voltage.

The logical expressions of UP and DN signals can be expressed as

$$\begin{aligned} UP &= \text{clk}_{k-1} \oplus \text{clk}_k = \overline{\text{clk}}_{k-1}.\text{clk}_k + \text{clk}_{k-1}.\overline{\text{clk}}_k, \\ DN &= \text{clk}_k \oplus \text{clk}_{k+1} = \overline{\text{clk}}_k.\text{clk}_{k+1} + \text{clk}_k.\overline{\text{clk}}_{k+1}, \end{aligned} \tag{2}$$

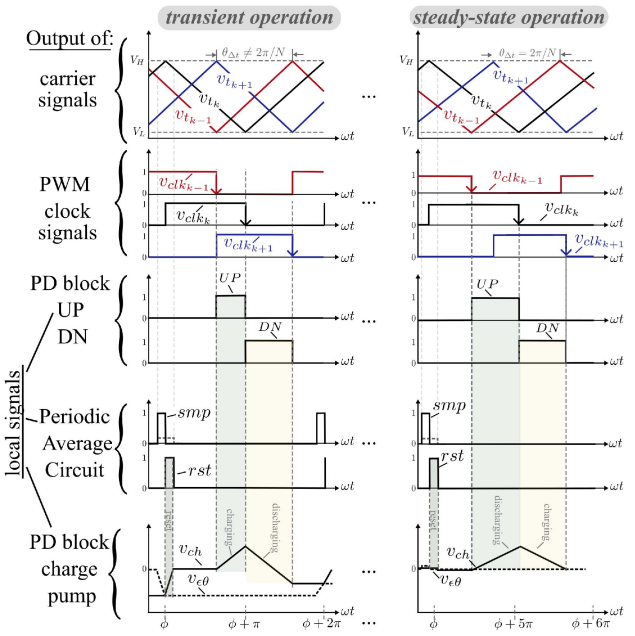

Fig. 5. Main waveforms describing the principle of proposed 2I-PLL. (on the left) during the transient or start-up. (on the right) during the steady-state.

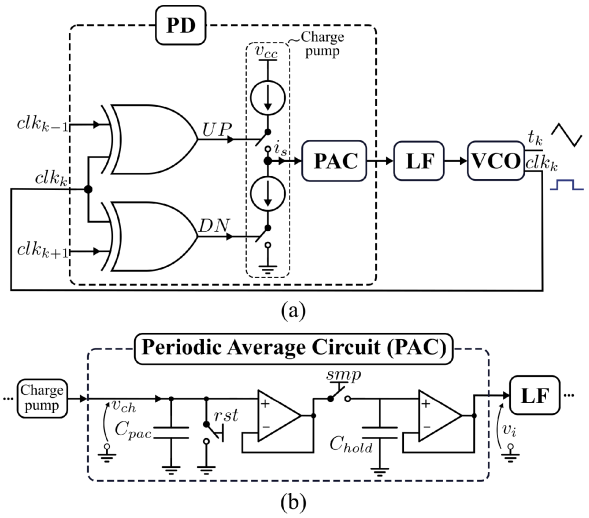

Fig. 6. 2I-PLL overview for local kth module example. (a) PD block. (b) PAC block.

where the basic operation is composed of XOR gates, which computes the sum of the error between the rising and falling edges of the clk signals. Note that the two-input XOR gate can be written as two two-input AND gates.

The first AND gate term in (2) computes the error between the falling edges and the second AND gate term computes the error between the rising edges. When only one edge must be aligned, one of the AND terms in (2) can be removed. The logical expression of UP and DN signals in (3) compute the error between falling edges of the clk signals

$$\begin{aligned} UP &= \overline{\text{clk}}_{k-1}.\text{clk}_k, \\ DN &= \overline{\text{clk}}_k.\text{clk}_{k+1}. \end{aligned} \tag{3}$$

Now, the phase-shift error of positioning of the local clock signal with its two neighbors is determined considering difference in the durations at state 1 of the *UP* and *DN* signals. Indeed, if these durations are identical, the clock signal is correctly positioned; otherwise, there is a phase-shift error, it is either in phase delay or in phase advance. The second part of the PD integrates the UP and DN signals in a VCO time period to generate a voltage representative of the phase-shift error. It is implemented by a charge pump circuit pushing and pulling current across the C_{PAC} capacitor of the PAC. The main goal of the PAC is to provide a smooth signal at the input of the LF filter and avoid integration. A current is injected into the capacitor C_{PAC} when $UP = 1$, and hence the voltage v_{ch} increases. A current is drawn out of the capacitor C_{PAC} when $DN = 1$, thereby the voltage v_{ch} decreases. The average current across C_{PAC} is proportional to the phase-shift error (self-alignment error). By the end of the VCO period, the voltage v_{ch} is sampled at C_{Hold} capacitor by smp signal, and v_{ch} is reset by rst signal to avoid integration, as shown in Fig. 5. Its simplified electrical diagram is shown in Fig. 6(b).

2) Loop Filter: The next block is the LF. It controls the bandwidth and the steady-state error of the closed-loop system. Some possible alternatives to LF are found in the literature [24], [25], [26]. In this article, a variant with active gain was chosen and will be described in details in Section IV.

3) Voltage-Controlled Oscillator: The VCO generates a clock signal with frequency and phase that can be adjusted to achieve interleaving. In this article, to have a practical demonstrator/solution of this block, a low-cost triangular oscillator with operational amplifiers is used to generate the clock signal too. The final implementation of this structure was slightly reconfigured to operate as a VCO.

A stability study using diagonalization is introduced in the next section for modal analysis.

IV. System Control Modeling

An analytical study in matrix form for modal analysis is presented. The goal is to present a robust distributed control model capable to provide a global view of system dynamics as well as keeping the regulation of the overall system stable. First a single-loop model or local modeling is developed. Next, it is aggregated in the global modeling which introduces the foundations to decouple the system and provide support to the modal analysis.

A. Local System Modeling (Single-Loop)

To improve the readability, the control modeling starts considering the control block diagram of one local module, shown in Fig. 7. Note that it is presented in Laplace-domain.

The local phase-shift reference signal $\tilde{\Theta}(s)$ is the average of the phase-shifts from next and previous modules, and it is defined as

$$\tilde{\Theta}(s) = \frac{1}{2}\underbrace{\Theta_{k+1}(s)}_{\text{next}} + \frac{1}{2}\underbrace{\Theta_{k-1}(s)}_{\text{previous}}. \tag{4}$$

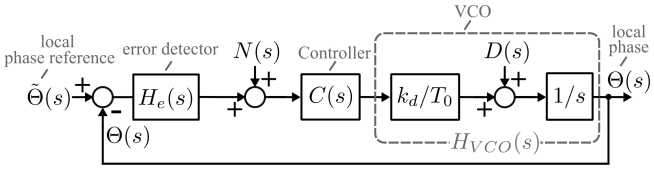

Fig. 7. Control block diagram of a single-loop representing one *LC* elements. The elements are observed locally.

The transfer function of phase-shift error detector $H_e(s)$, combines subsystems associated with delay, zero-order hold (or PAC), and the charge pump circuit, such as

$$H_e(s) = \underbrace{e^{-s.(T_0/2)}}_{H_{\text{delay}}(s)} \cdot \underbrace{\frac{1-e^{-s.(T_0)\cdot}}{s.(T_0)}}_{H_{ZOH}(s)} \cdot \underbrace{\frac{2.I_p.T_0}{C_{\text{rst}}}}_{\text{charge pump}}, \tag{5}$$

where $T_0 = 1/f_0$ is the VCO time peroid, and f_0 is the VCO frequency of local module.

The transfer function of the controller $C(s)$ is similar to the LF block presented previously. Its expression is provided by (7).

The VCO transfer function $H_{\text{VCO}}(s)$ linearized around an operation point is defined as

$$H_{\text{VCO}}(s) = \frac{1}{s} \cdot \frac{k_d}{T_0}, \tag{6}$$

where k_d $[V^{-1}]$ is the VCO gain factor.

The transfer functions of $N(s)$, and $D(s)$ are associated with noise and disturbance signals, respectively. Such signals do not affect the stability analyses and can be omitted.

Finally the output signal of this single-loop modeling represents $\Theta(s)$ which is associated with the normalized phase-shift measurement of the local clock signal clk_k to a virtual reference clock signal at the frequency f_0.

The single-loop control model (study and local analysis of distributed self-interleaving system) presented here is useful to take some insights and preliminary analyses. It can be seen as a first support to investigate more complex system (when all the modules are considered together). However the single-loop model keeps the system equations coupled and it is not capable to reveal the stability criterion and dynamic behaviors of the global system. In this way, a more in-depth study through a comprehensive modeling approach that considers the global system will be presented and discussed next.

B. Loop-Filter C(s) Design

In this work, the LF (compensator) is identical in all modules. The model shows that the transfer function is a first order with a delay. If the bandwidth is limited to a range where the phase delay is not too big, a phase-lag compensator can be used to impose the bandwidth and provide a high static gain to guarantee a low static error. The compensator should be designed to provide the largest bandwidth with minimum phase margin (PM) of 55° combined with a phase-lag to increase the static gain. In this way, the structure of active LF topology shown in Fig. 8(a) is considered. Its respective bode diagram is shown in Fig. 8(b).

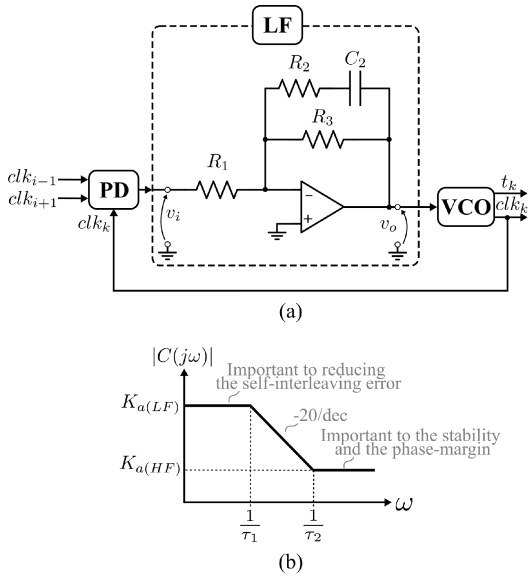

Fig. 8. 2I-PLL highlighted with LF block. (a) Diagram schematic. (b) Equivalent bode diagram.

As a result, the transfer function of the LF (phase-lag compensator) has a zero-pole pair, which can be defined in Laplace-domain as

$$C(s) = \frac{V_o(s)}{V_i(s)} = K_a \cdot \frac{\tau_1}{\tau_2} \frac{1+s.\tau_2}{1+s.\tau_1}, \tag{7}$$

where K_a is the plateau gain $K_{a(HF)}$, $\tau_1 = (R_2 + R_3).C_2$, $\tau_2 = R_2.C_2$. Once $K_{a(HF)}$ is designed to set the bandwidth, the phase-lag compensator pole-zero pair contributes to reduce self-interleaving steady-state error by increasing the static gain to a limited value $K_{a(\text{LF})}$ (no integration).

It should be noted that, for practical reasons, the self-interleaving circuit presented in the article is realized using analog blocks of the op-amp and comparator type as shown in Figs. 6 and 8. This allows high frequencies to be addressed for control signals, without requiring large digital resources (FPGA or microprocessor) using high clock frequencies. It can also be noted that the only sampling frequency that appears in the circuit is that of the smp signal, used to collect the value of the positioning error v_{ch} during each switching period.

C. Overall System Modeling (Multiloop in Matrix Form)

The modal analysis approach permits to decouple the system into N independent unidimensional subsystems, by using matrix representation by means of a suitable change of base. Such a mathematical approach enables the identification of various modes based on the diagonalization of the system in matrix form. However, for a better readability, the matrix form of the system must be presented in Fig. 9.

The previous ($\boldsymbol{\Theta}_{k-1}$) and next phase vectors ($\boldsymbol{\Theta}_{k+1}$) in matrix form are now computed using a circular shift operators $\boldsymbol{S}$, and $\boldsymbol{S}^*$, which is basically a circular convolution operation,

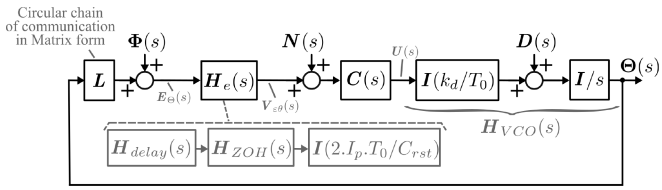

Fig. 9. Control block diagram of a multiloop represented in matrix form. Now the elements are observed globally.

such as

$$\boldsymbol{\Theta}_{k-1} = \boldsymbol{S}.\boldsymbol{\Theta} = \begin{bmatrix} 0 & & & 1 \\ 1 & & & \\ & \ddots & \ddots & \\ & & 1 & 0 \end{bmatrix} . \begin{bmatrix} \theta_1 \\ \theta_2 \\ \vdots \\ \theta_N \end{bmatrix} = \begin{bmatrix} \theta_N \\ \theta_1 \\ \vdots \\ \theta_{N-1} \end{bmatrix},$$

$$\boldsymbol{\Theta}_{k+1} = \boldsymbol{S}^*.\boldsymbol{\Theta} = \begin{bmatrix} 0 & 1 & & \\ & \ddots & \ddots & \\ & & & 1 \\ 1 & & & 0 \end{bmatrix} . \begin{bmatrix} \theta_1 \\ \theta_2 \\ \vdots \\ \theta_N \end{bmatrix} = \begin{bmatrix} \theta_2 \\ \vdots \\ \theta_N \\ \theta_1 \end{bmatrix}, \quad (8)$$

where $\boldsymbol{S}^* = \boldsymbol{S}^T$.

From these matrices, the reference phase matrix becomes

$$\tilde{\boldsymbol{\Theta}}(s) = \frac{1}{2}\boldsymbol{\Theta}_{k-1}(s) + \frac{1}{2}\boldsymbol{\Theta}_{k+1}(s). \quad (9)$$

The local phase errors are computed using the matrix $\boldsymbol{L}$, that represents the circular chain of communications (i.e., the connections between the local modules), such as

$$\boldsymbol{L} = \frac{1}{2}.(\boldsymbol{S} + \boldsymbol{S}^*) - \boldsymbol{I}$$

$$\boldsymbol{L} = \begin{bmatrix} -1 & 0.5 & 0 & \cdots & & 0.5 \\ 0.5 & -1 & 0.5 & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \ddots & & \vdots \\ \vdots & \ddots & \ddots & \ddots & \ddots & 0 \\ \vdots & & \ddots & \ddots & \ddots & 0.5 \\ 0.5 & 0 & \cdots & 0 & 0.5 & -1 \end{bmatrix}. \quad (10)$$

Note that $\boldsymbol{L}$ is a circulant matrix. As a consequence, it can be diagonalized.

This allows to define the PD error as

$$\boldsymbol{E}_\Theta(s) = \tilde{\boldsymbol{\Theta}}(s) - \boldsymbol{\Theta}(s) + \boldsymbol{\Phi}(s) = \boldsymbol{L}.\boldsymbol{\Theta}(s) + \boldsymbol{\Phi}(s). \quad (11)$$

The phase error detector circuit will include this error information and and provide at its output an error in terms of voltage signal such that

$$\boldsymbol{V}_{\varepsilon\theta}(s) = \boldsymbol{H}_e(s).\boldsymbol{E}_\Theta(s), \quad (12)$$

where $\boldsymbol{H}_e(s) = H_e(s).\boldsymbol{I}$, and $\boldsymbol{I}$ is the identity matrix.

The controller and VCO transfer functions are identical for each module. In matrix form, both of them are inherently diagonal matrices represented as

$$\boldsymbol{C}(s) = C(s).\boldsymbol{I}; \qquad \boldsymbol{H}_{\text{VCO}}(s) = H_{\text{VCO}}(s).\boldsymbol{I}. \quad (13)$$

The control modeling of the overall system can be characterized as a multiple inputs and multiple outputs (MIMO) system. Based on the this modeling and mathematical approaches, the plant transfer function (without controllers) of the overall system (in matrix form) can be defined as

$$\boldsymbol{P}(s) = -\boldsymbol{H}_e(s).\boldsymbol{H}_{\text{VCO}}(s).\boldsymbol{L}. \quad (14)$$

Considering that all modules, including the controllers, are identical, and $\boldsymbol{H}_e(s)$, $\boldsymbol{C}(s)$, and $\boldsymbol{H}_{\text{VCO}}(s)$ are diagonal, the MIMO open-loop transfer function of the system is

$$\boldsymbol{G}_o(s) = H_e(s).C(s).H_{\text{VCO}}(s).\boldsymbol{L}. \quad (15)$$

From now on, the evaluation of the dynamic response and stability study of the overall system written in this matrix form is hard since the system is coupled (i.e., $\boldsymbol{L}$ is not diagonal). However, $\boldsymbol{L}$ is diagonalizable. Hence, it is possible to decouple the system by diagonalizing $\boldsymbol{L}$, as discussed next.

D. Diagonalization for Modal Analysis

The matrix equations must be rewriting in a diagonal form. All matrix transfer functions considered in this modeling are diagonal and circulant, except to $\boldsymbol{L}$, that is only circulant. To obtain the modal open-loop transfer function, $\boldsymbol{L}$ has to be diagonalized. Since it is a circulant matrix, it can be diagonalized by using a discrete Fourier transform (DFT) matrix [21], [27], as a change of basis matrix.

In this way, the diagonal open-loop transfer function of the overall system can be expressed as

$$\boldsymbol{G}_{o\Lambda}(s) = H_e(s).C(s).H_{\text{VCO}}(s).\boldsymbol{\Lambda}, \quad (16)$$

where $\boldsymbol{\Lambda} = \boldsymbol{W}.\boldsymbol{L}.\boldsymbol{W}^*$, and $\boldsymbol{W}$ is a nonsingular and unitary DFT matrix chosen as change-of-basis matrix.

The eigenvectors of $\boldsymbol{L}$ presented in $\boldsymbol{W}$ decouple the system, while the eigenvalues of $\boldsymbol{L}$ reveal the stability. Such eigenvalues will be presented in the diagonal elements of $\boldsymbol{\Lambda}$, such as

$$\begin{aligned} &\{\boldsymbol{\Lambda}\}_{i,i} = \lambda_k, \quad i = k+1, \\ &\boldsymbol{\Lambda} = \text{diag}(\lambda_0, \lambda_1, \ldots, \lambda_{N-1}) \end{aligned} \quad (17)$$

where the subscript k stands as $k = \{0, 1, 2, \ldots, N-1\}$.

Once the system is diagonalized, the diagonal open-loop transfer functions can be expressed as

$$\begin{aligned} \{\boldsymbol{G}_{o\Lambda}(s)\}_{i,i} &= G_{ok}(s), \quad k = i-1, \\ G_{ok}(s) &= H_e(s).C(s).H_{\text{VCO}}(s).\lambda_k. \end{aligned} \quad (18)$$

The eigenvalues of $\boldsymbol{L}$ (λ_k) can be computed by taking into account the Gerschgorin's theorem [21], [28], [29], [30], as follows:

$$\lambda_k = \cos\left(\frac{2\pi k}{N}\right) - 1. \quad (19)$$

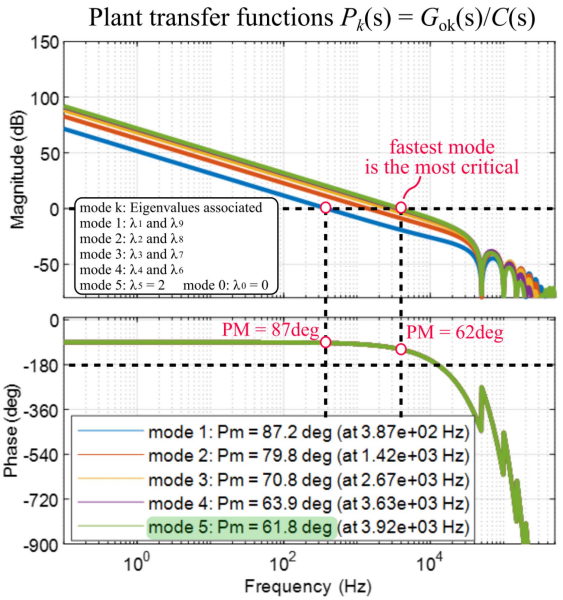

Fig. 10. Modal analysis. Bode plots of modal transfer functions of the system without controller $\boldsymbol{C}(s)$.

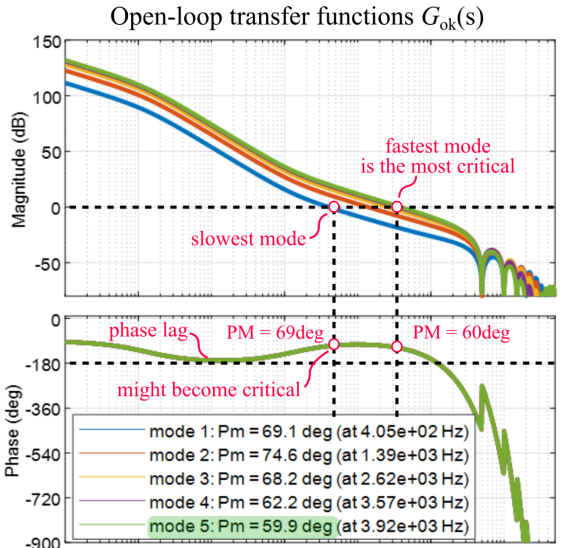

Fig. 11. Modal analysis. Bode plots of modal transfer functions of the system with controller $\boldsymbol{C}(s)$.

TABLE I
MAIN PARAMETERS FOR AN AEROSPACE APPLICATION

Parameters	Value	Description
f_0	50 – 3000 kHz	Frequency range
N	4 – 10	Number of Phases (modules)
PM	60 deg	Phase-margin reference
k_d/T_0	5 kV/Hz	VCO sensitivity
I_p	62.5 μA	Charge-Pump current
$2.I_p.T_0/C_{PAC}$	2.5 V/rad	Charge-Pump gain
$K_{a(LF)}$	100	LF gain of Loop-filter
$K_{a(HF)}$	0.5	HF gain of Loop-filter
$p = 1/\tau_1$	1.3 Hz	Pole frequency of Loop-Filter
$z = 1/\tau_2$	132 Hz	Zero frequency of Loop-Filter

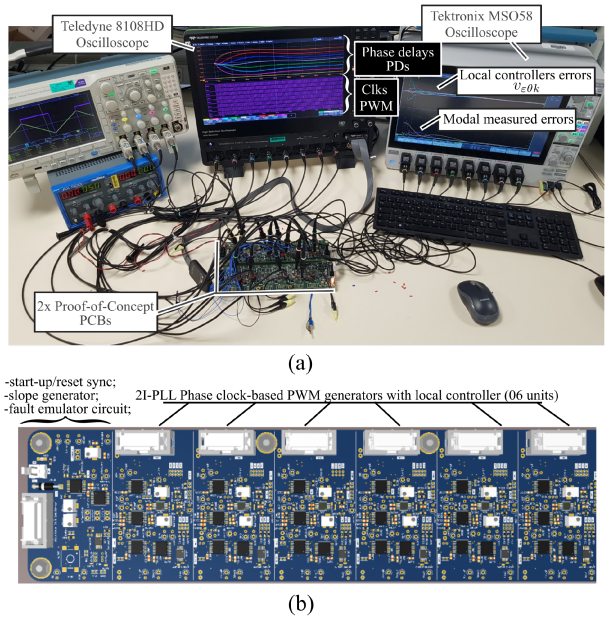

Fig. 12. Experimental setup. (a) Overview. (b) Layout view of one (1x) PoC board with six local controller boards and shared functions.

As a result, the eigenvalues are real numbers and located between -2 and 0, that affect only the transfer function $G_{0k}(s)$ magnitude, not its phase.

The first eigenvalue ($\lambda_0 = 0$) is associated with the common mode response and can be interpreted as the steady-state value corresponding to the average value of all phase-shifts. Note that this mode is not controllable. However, the most important stability information will be found in the others eigenvalues (i.e., $\lambda_1, \ldots \lambda_{N-1}$). They are associated with differential modes, that are in fact regulated. Most of differential mode will appears as double modes ($i, N-i$), and $\lambda_i = \lambda_{N-i}$. If N is even, the last mode ($N/2$) is a single mode.

Communication delays can significantly impact system performance as the number of phases N and the switching frequency f_{sw} increase. For instance, the steady-state phase-shift delta $\theta_{\Delta t}$ is given by $1/(N \cdot f_{sw})$, which results in 100 ns for 10 phases operating at 1 MHz. A delay of just 1 ns introduces a 1% phase-shift error. The communication delays are a common-mode disturbance that cause a systematic frequency error.

In the self-interleaving solution exchanging analog triangular signals, the static gain could not be set independently from the bandwidth. In this new solution, the static gain of the corrector $C(s)$ can be set high to mitigate the differential-mode static errors, but must be limited to manage the common-mode related disturbances causing frequency shift.

As a conclusion, this system is not designed to impose any fixed phase-shift value because the common mode is not controllable. Only the relative values between the near modules (local, previous, and next) are controlled (i.e., differential modes). In this context, the stability study of the system can be performed in an easier manner taking into account its eigenvalues and frequency response simulations. Further details about this approach modeling can be found in [18].

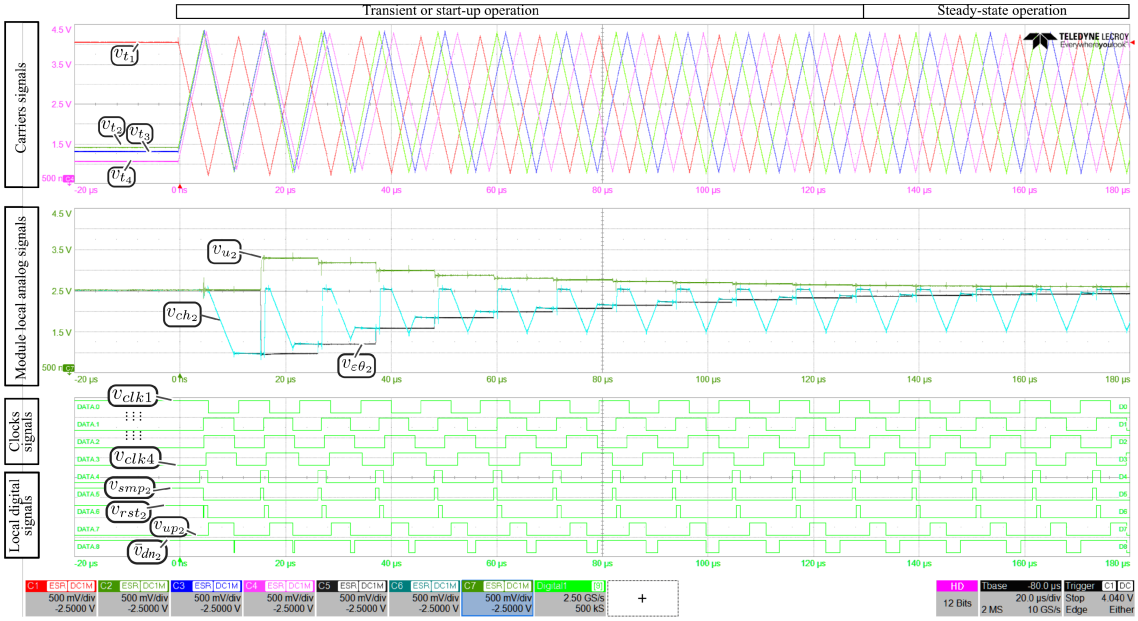

Fig. 13. Experimental result. 2I-PLL operating with four phases. (top) Carriers signals ($v_{t1} - v_{t4}$). (middle) the local controllers signals of phase 2 (v_{u_2}, $v_{\varepsilon\theta_2}$, v_{c_2}). (bottom) the clock signals ($v_{clk_1} - v_{clk_4}$) and internal signals of phase 2 (v_{smp_2}, v_{rst_2}, v_{up_2}, v_{dn_2}).

V. Simulation Results

A. Stability Study Based on Modal Analysis

This sections presents stability study based on modal analysis for an aerospace application scenario. The results were obtained from simulation at MATLAB. The impact of designed compensator (LF) in the 2I-PLL is presented. Table I lists the main parameters for this application. The transfer function of the controller (LF) is based on a phase-lag type. It is considered to increase the static gain, reduce the steady-state error and guarantee the stability.

In this work, a use case (design scenario) is considered. Such a use case highlights to the end-user a scenario in which a very large time constant may be imposed in the 2I-PLL LF if f_0 is set to 50 kHz and the highest number of modes must be considered for stability reasons (i.e., by setting N to 10). In practice, 50 kHz would require high value capacitors in the LF that should be connected externally to the ASIC. In addition, $N = 10$ sets the higher number of differential modes (i.e., 5 modes) which requires to correctly evaluate the system operation in terms of convergence and stability.

The methodology to this modal analysis is such a way to cover and keep the stability for all other cases. Fig. 10 shows a result where the modal transfer function of the overall system is considered without the controller, and Fig. 11 shows a result with the controller. It can be seen that the controller for the 2I-PLL was designed such a way that it can preserves the PM close to 60°.

VI. Experimental Results

The proposed 2I-PLL model has been validate through experimental tests in an proof-of-concept (PoC) printed-circuit board developed at LAPLACE/NXP laboratory [18]. Note that 2I-PLL as well as its PoC board is designed entirely in an analog-manner, where only a few set digital signals are considered as logic/combinatory circuit operations. All the functions were implemented in the board with discrete surface mount devices. Fig. 12(a) shows an overview of the experimental setup in which two (2x) PoC prototype boards have been considered. Fig. 12(b) shows the layout of one (1x) developed board composed of six (6x) identical self-interleaving modules that generate the clock signals (with triangular carriers available too). In addition, shared functions board is placed aside. Only the start-up synchronization circuit (reset) is used in our case. It should be noted that these auto-interleaving circuits handle the control part of a real power converter. In practice, these circuits are placed away from the power switching cells of the converter to ensure good immunity to EMI interference, particularly for communication signals between circuits, and to cancel out any thermal stress. Moreover, appropriate management of the grounds makes it possible to guarantee that the chopped power currents do not disturb the control part and small common mode filters can be placed in series with the control power supplies, as made in [12]. The EMI precautions to be taken are the same as those considered for the control circuit of power converters, due to the interfacing of digital signals, as described in [31].

A. Four-Phase Experimental Tests ($N = 4$)

Initially, the internal signals and the dynamic response of the self-interleaving module has been validated. Fig. 13 shows a set of results and internal signals of a four-phase application response where one phase delay is on phase opposition (3+1) during start-up. The system converges properly.

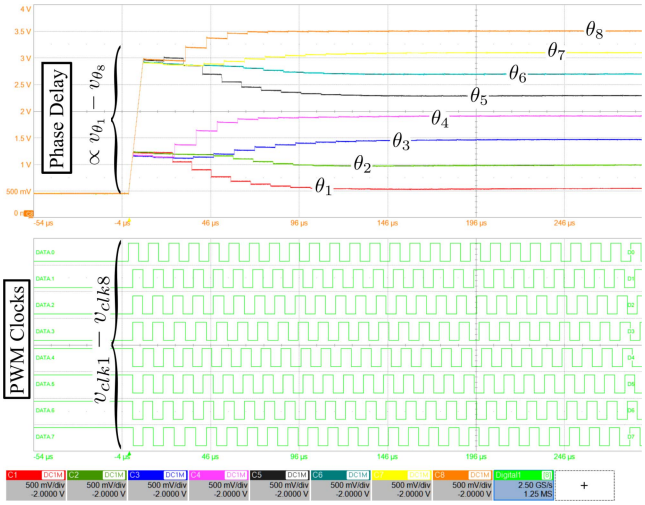

Fig. 14. Experimental result. 2I-PLL operating with eight phase (i.e., $N = 8$). Start-up of the system showing (on top) the equivalent phase-shift $v_{\theta k}$ and clock signals v_{clk-k}.

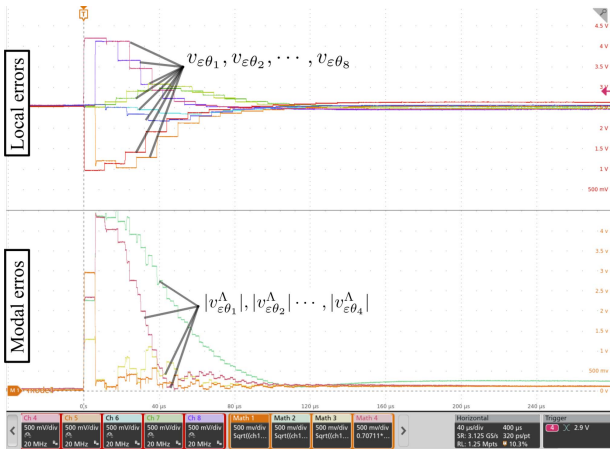

Fig. 15. Experimental result. 2I-PLL operating with eight phase (i.e., $N = 8$). Start-up showing (on top) the errors signals at the input of each local controller and (on the bottom) the absolute value of modal errors.

B. Eight-Phase Experimental Tests ($N = 8$)

Figs. 14 and 15 presents experimental responses of a system with 8 modules during a start-up by groups (4+4) where four consecutive phase delays are in phase opposition at start-up. In Fig. 14, on the top are the representation of signals proportional to the phase-shift, and on the bottom the digital signals are the interleaved clocks. Fig. 15 shows the local phase delay errors signals associated with start-up the test. The modal errors have been calculated using expression (20). The absolute values of modal errors are proportional to a voltage signal (i.e., $|v^{\Lambda}_{\varepsilon\theta_k}| \propto |\epsilon_{\theta\Lambda}|$)

$$\epsilon_{\theta\Lambda} = \boldsymbol{W}^{*}.\epsilon_{\theta}. \tag{20}$$

The start-up transient results reproduce the behavior predicted by the stability analysis. In addition, the start-up by groups has an interesting property that can provide faster convergence performance because only fast modes are disturbed during start-up. It is worth noting this set of tests allows one quantify how stable the modal responses can be, by looking to $|v^{\Lambda}_{\varepsilon\theta_k}|$ (i.e., more accurate insights in the early-stage design).

A jitter measurement was performed in the interleaved system in steady-state with $N = 8$ to observe the noise immunity aspect of this PoC, available in [18]. The frequency deviation is limited to $\pm$ 15 Hz, corresponding to $\pm$ 0.017% of the central frequency 88.6 kHz.

VII. Conclusion

This article has introduced a distributed self-interleaving method using 2I-PLL circuit. The study focused on proposing a robust solution to provide self-interleaved clock signals without a global clock. The proposed 2I-PLL is suitable for application which needs interleaved clock signal (e.g., dc–dc multiphase converters with peak current-mode control). An analytical study based on modal analysis was presented in matrix form decoupling the control block diagram in a MIMO system, in which more accurate information about the dynamic and stability study would be obtained performed. The methodology presented in this work permits to decouple the system since it diagonalizes the transfer functions in matrix form to analyze the stability of each mode. Simulation and experimental results were presented to validate theoretical approaches. Study case focusing on aerospace applications was covered.

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