Direct Drive D-Mode GaN HEMT Switching Characteristics and Turn-Off Loss Reductions

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***Abstract*—This article aims to evaluate the depletion-mode gallium nitride high electron mobility transistor (d-mode GaN HEMT) using direct-drive gating and double pulse test to assess switching energy. The gate driving circuit features a modified cascode structure for "normally OFF" operation and a charge-pump circuit to supply a negative gate voltage for turn-OFF operation. This article described these features theoretically and validated with experimental results. Similar to enhancement-mode power MOSFETs or HEMTs, adjusting the gate drive resistance can affect the switching speed and associated losses, but the d-mode GaN HEMTs present an additional feature with turn-OFF loss reduction through gate voltage control. Thus, the main contribution of this article is to propose and demonstrate significant turn-OFF loss reduction using the direct-drive approach for d-mode GaN HEMTs.**

***Index Terms*—Direct drive, d-mode gallium nitride high electron mobility transistor (d-mode GaN HEMT), double-pulse-test (DPT), gate driving, modified cascode, normally OFF, normally ON.**

I. Introduction

WHILE the depletion-mode (d-mode) gallium nitride (GaN) high electron mobility transistor (HEMT) typically exhibits "normally ON" characteristic, it can be connected in series with a low-voltage silicon (Si) MOSFET to achieve "normally OFF," which is regarded as a "cascode" device. Conventionally, the cascode device ties the gate pin of the GaN HEMT to the source pin of the MOSFET to form a negative voltage between GaN HEMT gate and source [1], [2]. This conventional cascode approach is susceptible to electrical overstress and additional energy loss mechanisms [3]. In addition, the input capacitance of the MOSFET can cause the switching delay. However, this cascode approach is relatively straightforward and cost-effective as long as the MOSFET is well-selected.

Alternatively, it is possible to make normally-OFF devices using gate-injection transistor or by adopting a p-type GaN gate to lift the potential of the heterojunction [3], [4]. The resulting device is considered an enhancement mode (e-mode) GaN HEMT, which requires a positive gate voltage to turn it ON. The major concern with the e-mode GaN is its low threshold voltage and narrow range that requires a meticulous circuit design to prevent it from false triggering.

Another approach to render the d-mode GaN "normally OFF" is a modified cascode design, which employs a charge-pump circuit to provide a negative voltage during turn OFF and zero or slightly above zero during turn ON [5]. In [6], [7], [8], [9], and [10], the charge-pump circuit is simplified by adding a capacitor in series with the gating path that stores the charge when the gate drive output is positive and discharges when the gate drive output is low, thus providing a negative voltage to turn OFF the GaN HEMT. In addition, a diode is connected between the gate of GaN HEMT and the source of Si MOSFET to clamp the gating voltage to zero during turn ON and to prevent false turn-ON during the initial power-up. With only a set of small RC components, this modified cascode structure using charge-pump circuit is also cost effective.

Instead of using charge-pump approach, there exists an integrated circuit that integrates a gate driver, a built-in buck–boost converter to provide negative gate voltage, and a d-mode GaN HEMT [11], [12]. Such a direct-drive approach has presented several advantages, such as mitigating noise induced by parasitic components, overcoming limitation of Si MOSFET dv/dt, and reducing its induced switching delay [13], [14], [15]. The major drawback of the integrated approach is lack of gate-drive voltage adjustment flexibility to adapt to different converter circuits or different operating modes for possible loss reduction.

The main aspect of adopting direct-drive approach in this study is to take the advantage of the fast switching nature of the d-mode GaN HEMT while avoiding the noisy switching caused by the Si MOSFET in a conventional cascode device. An in-house developed GaN HEMT is utilized and tested under double pulse test (DPT) condition to characterize its switching performance. A commercially available silicon carbide Schottky diode is adopted as the freewheeling device to avoid the reverse recovery effect under the GaN device turn-ON transient

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condition. A printed circuit board (PCB) with low parasitic inductance is designed to minimize the switching delays and associated losses. The device voltage is monitored with high bandwidth probes, and the device current is measured using a high-precision inductance-less current viewing resistor [16]. Despite using a high-bandwidth monitoring setup, the test results still need to undergo a de-skew process [17]. The device current magnitude needs to be calibrated with inductor current to ensure accuracy. Switching energy is obtained by integrating the product of device voltage and current.

Extensive testing has revealed that the d-mode GaN HEMT switching behavior closely resembles that of MOSFET device with a notable difference showing its ability to increase the gate driving voltage magnitude to accelerate the switching speed, which is indeed a desirable feature in applications where turn-OFF loss predominates the switching loss, such as a dc–dc converter operating under discontinuous conduction mode or critical conduction mode (CRM) [18], [19], and soft switching converters operating under quasi-resonant mode with zero-voltage switching (ZVS) or near ZVS conditions [20], [21].

It should be noticed that the increase of gate driving voltage magnitude will increase the reverse conduction voltage drop before synchronous rectification engages [10], [11], [12]. Therefore, adopting the direct drive approach should pay attention to the tradeoff between turn-OFF loss reduction and the increase of the reverse conduction voltage drop. For nonbridge type converter circuits like quasi-resonant flyback and CRM buck and boost converters, the direct-drive approach is always advantageous because their switches do not enter the reverse conducting mode.

The rest of this article is organized as follows. Section II presents an overview of the d-mode GaN HEMT utilized in the characterization study. The direct gate drive circuit and its basic operation follow in Section III. The DPT test circuit and experimental setup are given in Section IV. Section V presents the initial power-up test results. Section VI analyzes the switching loss by varying gate drive resistance and gating voltage. Sections VII delves into the measurement issues associated with GaN HEMTs. Finally, Section VIII concludes this article. Key contribution is to propose turn-OFF loss reduction method by controlling the gate drive voltage for direct-driven d-mode GaN HEMTs.

II. D-Mode GaN HEMT Structure and Internal Layout

The device evaluated in this study is an in-house developed GaN metal-insulator-semiconductor (MIS) HEMT. The MIS-HEMT adopts a low-cost silicon substrate and places a GaN/AlGaN buffer layer atop. A GaN layer is deposited on top of the buffer layer, followed by an AlN space layer, a thick AlGaN barrier layer, and finally a GaN capping layer. Its source and drain ohmic contact are created by evaporating the Ti/Al/Ni/Au multilayer metal-stack, and the metal gate electrode is insulated by a low-pressure chemical vapor deposition (LPCVD) silicon nitride (SiN) layer [22], [23], [24]. The density of the SiN insulator deposited by LPCVD is much higher due to the higher deposition temperature (800–900 °C) compared to conventional plasma-enhanced chemical vapor deposition (< 400 °C), resulting in better quality of the SiN gate insulator and GaN/SiN interface [25], [26], [27].

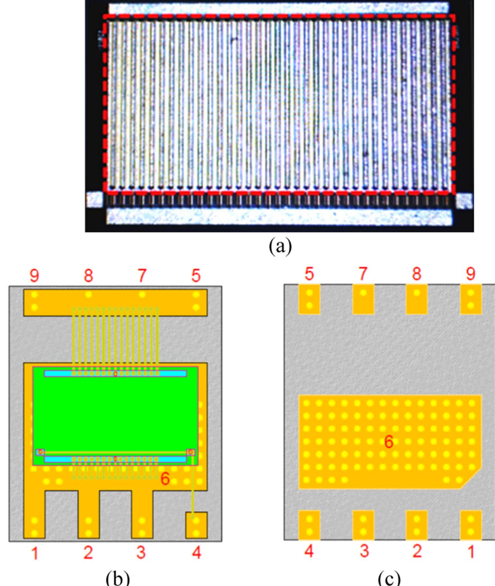

Fig. 1. In-house developed GaN packaged in 5 × 6 DFN footprint. (a) Active chip area in red frame. (b) Top view of bonding drawing. (c) Bottom view.

TABLE I
KEY PARAMETERS OF THE HEMT DEVICE USED IN THIS STUDY

Parameter	Value
Breakdown voltage V_{BV}	650 V
On-drop resistance $R_{ds\text{-}on}$	150 mΩ
Nominal $V_{th\text{-}H}$	–10 V
C_{iss} at v_{gs} = –15 V, v_{ds} = 200 V	165 pF
C_{oss} at v_{gs} = –15 V, v_{ds} = 200 V	60 pF
C_{oss} at v_{gs} = –15 V, v_{ds} = 200 V	28 pF

The experimental device has a gate width of 120 mm and is packaged in a standard 5 × 6-mm dual-flat no-leads (DFN) footprint. Fig. 1 illustrates (a) active chip area of the bare die in a red frame, (b) top view of wire bonding drawing, and (c) bottom view of the package. The dimension of the bare die is 3897 × 2316-µm. The wire bonds consist of 15 bond wires each for both drain and source and one wire for the gate. The pinout follows the industry standard with pins 1, 2, and 3 as the source, pin 4 as the gate, and pins 5, 7, 8, and 9 as the drain. Pad 6 is tied to the source for heat dissipation.

Key parameters of the HEMT device used in the experiment are listed in Table I.

III. Direct Drive Gating Circuit Operations

Fig. 2 depicts the direct-drive gating circuit using a charge pump to provide a negative voltage for the device to turn OFF. A diode D_p is connected in between the gate pin of HEMT (G_H) and the source of MOSFET (or ground) such that the voltage at G_H is clamped to ground when D_p is conducting under gate-ON condition. This clamping diode D_p not only serves as the clamping purpose, but also provides the initial power-up

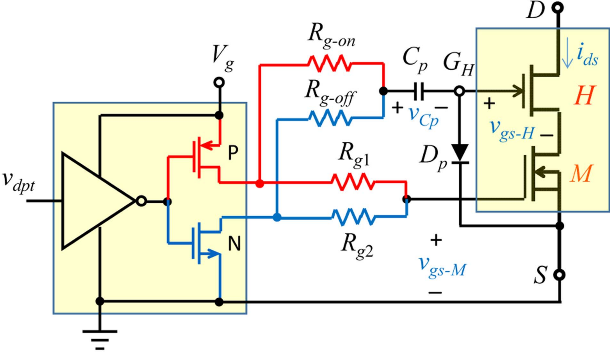

Fig. 2. Direct drive using charge pump for a modified cascode device.

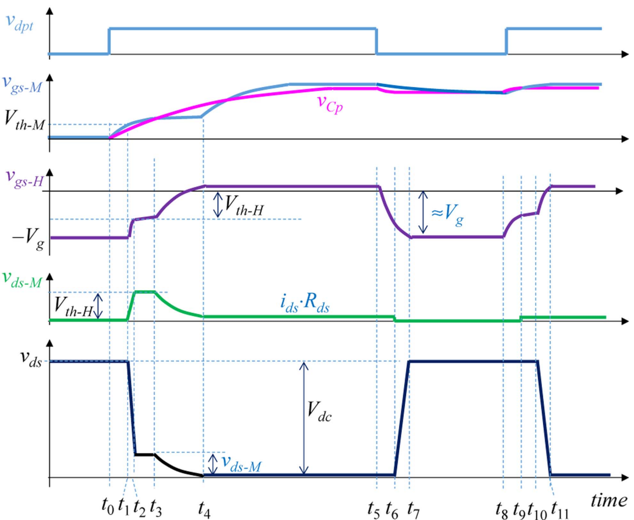

Fig. 3. Device voltage waveforms under repetitive double-pulse operation.

protection to prevent the normally-ON HEMT from conducting before the pulsewidth-modulation (PWM) operation.

The driving circuit for Si-MOSFET only works under the initial startup condition. R_{g1} is selected to have sufficient time constant on the MOSFET gating circuit to slow down the MOSFET turn-ON under the initial startup and to allow charge pump capacitor voltage established before the regular PWM switching starts. For R_{g2}, it needs to be large enough to never turn OFF the MOSFET under PWM switching after initial startup. The actual PWM switching only turns ON and OFF GaN-HEMT while MOSFET remains on all the time, which is the essence of the direct drive.

A. First Pulse Turn-On

With the normally-ON d-mode GaN, it is important that adding a low-voltage MOSFET can block the current flow. During the initial power-up with a negative gate voltage applied to the HEMT. Fig. 3 depicts the conceptual voltage waveforms under a repetitive double pulse train that repeats the operation from t_0 to t_{10} for a long period, which resembles to the burst-mode operation of a converter circuit under light load conditions. For each pulse train, the initial $v_{gs\text{-}H}$ is negative and $v_{gs\text{-}M}$ is zero, so both devices are initially turned OFF. The voltage from drain of HEMT and the source of MOSFET (v_{ds}) is shared by the drain-source voltages of HEMT ($v_{ds\text{-}H}$) and MOSFET ($v_{ds\text{-}M}$), or

$$v_{ds} = v_{ds-H} + v_{ds-M}. \tag{1}$$

<u>From t_0 to t_1:</u>

When the first pulse is applied at t_0, $v_{gs\text{-}M}$, and v_{Cp} get charged. From t_0 to t_1, the MOSFET gate-source voltage $v_{gs\text{-}M}$ reaches the threshold voltage $V_{th\text{-}M}$, and the MOSFET current builds up at t_1. The turn-ON process during period t_0-t_1 is similar to that of the traditional power MOSFET. Equation (2) expresses the gate-source voltage as a function of time [28]

$$v_{gs-M}(t) = V_g\left(1 - e^{-t/\tau_M}\right) \tag{2}$$

where $\tau_M = R_{g1} \cdot C_{iss\text{-}M}$ and $C_{iss\text{-}M} = C_{gs\text{-}M} + C_{gd\text{-}M}$. At t_1, $v_{gs\text{-}M}$ reaches the threshold voltage $V_{th\text{-}M}$, and the MOSFET conducts. For a given $V_{th\text{-}M}$, the period from t_0 to t_1 (or t_{01}) can be calculated in

$$t_{01} = \tau_M \ln\left(1 - \left|\frac{V_{th-M}}{V_g}\right|\right). \tag{3}$$

<u>From t_1 to t_2:</u>

The operation in this period is quite different from that of the conventional power MOSFET or e-mode HEMT because the GaN HEMT starts conducting, which affects the bottom MOSFET operation. Instead of charging $C_{iss\text{-}M}$ during the time period t_{01}, the time period from t_1 to t_2 (or t_{12}) relates to the charge of the HEMT input capacitance $C_{iss\text{-}H}$. The above equations can be applied but with the change of parameters from the bottom MOSFET to the top HEMT. The entire t_{12} is the period that moves the HEMT gate-source voltage from $-V_g$ to $-V_{th\text{-}H}$. At t_2, we have

$$v_{ds-M}(t_2) = -V_{th-H} \tag{4}$$

$$v_{gs-H}(t_2) = -v_{ds-M}(t_2) = V_{th-H}. \tag{5}$$

With the gate-source voltage of HEMT reaching the threshold, the current shuts OFF, and $v_{ds\text{-}H}$ remains at zero. The total drain-source voltage becomes

$$v_{ds}(t_2) = v_{ds-H} + v_{ds-M} = -V_{th-H}. \tag{6}$$

The period is typically very short and is dependent on gate drive resistances and the HEMT threshold voltage.

<u>From t_2 to t_3:</u>

At t_2, the HEMT starts conducting, and its gate current starts charging the gate-drain capacitance (C_{gd}). The t_{23} period is the well-known plateau period, during which, the HEMT device current builds up.

<u>From t_3 to t_4:</u>

At t_3, the gate-source of HEMT $v_{gs\text{-}H}$ continues rising by the gate charge. At t_4, $v_{gs\text{-}H}$ is fully charged with a voltage equal to the clamping diode (D_p) voltage drop. During t_{34}, with device current conducting, $v_{ds\text{-}M}$ and, thus, v_{ds} drop from $-V_{th\text{-}H}$ down to the conducting voltage drop $i_{ds} \cdot R_{ds}$.

Regarding the charging path on the charge pump capacitor (C_p) loop, the positive gate supply voltage V_g charges C_p through

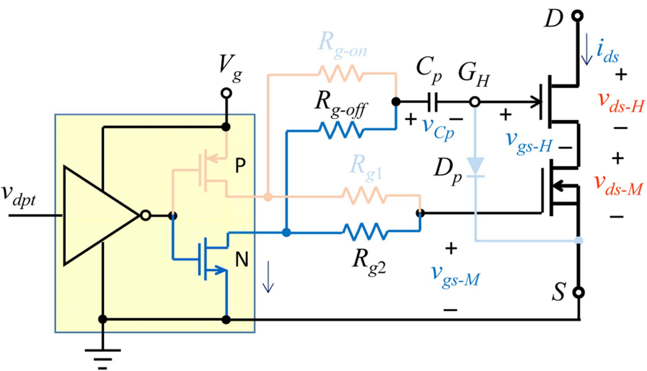

Fig. 4. Gating-OFF current path showing charge-pump capacitor discharging through gate driver.

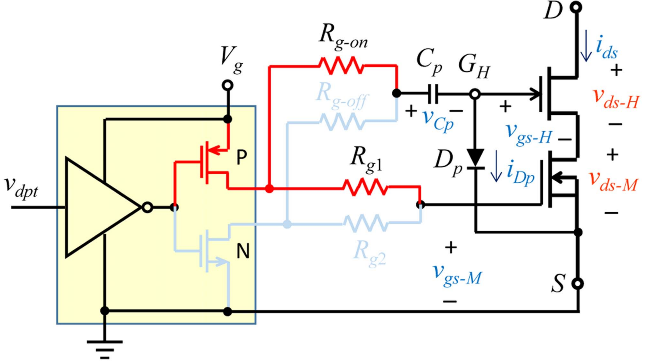

Fig. 5. Gating-ON current path showing charge-pump capacitor C_p gets charged through clamping diode D_p.

the turn-ON resistor $R_{g\text{-ON}}$ and clamping diode D_p. Similar to (2), the voltage across C_p can be expressed in

$$v_{cp}(t) = V_g(1 - e^{-t/\tau_p}) \tag{7}$$

where $\tau_p = R_{g\text{-ON}} \cdot C_p$. The charging rate can be adjusted by selecting $R_{g\text{-ON}}$ and C_p values. Under the steady-state condition, $v_{Cp} = V_g - V_{f\text{-}Dp}$, where $V_{f\text{-}Dp}$ is the forward voltage drop of diode D_p. The charge pump capacitor C_p needs to be large enough to maintain sufficiently high voltage for HEMT turn-OFF but low enough to allow fully charged during turn-ON period. For $R_{g\text{-ON}}$, the gate driver internal resistance needs to be factored in for charging time estimate. The example gate driver used in our setup has an internal turn-ON resistance of 5 Ω.

B. First Pulse Turn-Off

Similar to the turn-ON gating paths, the gating-OFF current path can be illustrated in Fig. 4. Under the gate-OFF condition, the MOSFET is intended to stay on by selecting a large R_{g2} to hold the MOSFET gate-source voltage sufficiently high. The switching action only applies to the HEMT.

From t_5 to t_6:

The bottom N-type device of the gate driver output stage is turned ON at t_5 when v_{dpt} signal becomes zero. The charge pump capacitor C_p is, thus, discharged through $R_{g\text{-OFF}}$. At t_6, $v_{gs\text{-}H}$ drops to the threshold voltage of HEMT, or

$$v_{gs-H}(t_6) = V_{th-H}. \tag{8}$$

From t_6 to t_7:

The drain-source voltage of HEMT ($v_{ds\text{-}H}$) starts rising at t_6. At t_7, $v_{ds\text{-}H}$ reaches the dc bus voltage V_{dc}, and the device current starts dropping to zero. The voltage slew rate can be controlled by the gate discharge current, which is a function of V_g magnitude and/or $R_{g\text{-OFF}}$. A large V_g magnitude or a small $R_{g\text{-OFF}}$ will result in a large gate discharge current, which will increase the voltage slew rate and reduce the turn-OFF loss. This is a unique feature of the d-mode GaN HEMT.

After t_7, the device current is zero ($i_{ds} = 0$), and the MOSFET voltage drop also drops to zero ($v_{ds\text{-}M} = 0$). With a negative voltage at the gate of HEMT, G_H, diode D_p is blocked. Here, we assume that the gate driver is a rail-to-rail type that has the gate drive output equals V_g under gate-ON condition and zero under gate-OFF condition ($v_{gs\text{-}H} \cong -V_g$). The actual gate drive output voltage or internal resistance depends on the individually selected driver chip.

C. Second Pulse Turn-On

From t_8 to t_9:

The second pulse turn-ON starts at t_8. Its gating path is the same as that of the first turn-ON path shown in Fig. 5, but the initial MOSFET drain-source voltage is different. The HEMT input capacitance charging process in this time period operation is similar to that of t_{12} except that the initial $v_{ds\text{-}M} = 0$ is zero in this case.

From t_9 to t_{10}:

At t_9, $v_{gs\text{-}H}$ reaches $V_{th\text{-}H}$, the HEMT starts conducting, and its gate current starts charging the gate-drain capacitance (C_{gd}).

From t_{10} to t_{11}:

At t_{10}, the HEMT current build up, and the drain-source voltage starts discharging. Unlike the t_{34} period, the drain-source voltage v_{ds} was pulled down to $-V_{th\text{-}H}$, the period from t_{10} to t_{11} period brings v_{ds} directly down to the conducting voltage drop, $i_{ds} \cdot R_{ds}$.

IV. Experimental Setup

Fig. 6 depicts the circuit diagram of the device under double-pulse test condition. The double pulse tester is an in-house developed DPT controller using TI DSP 320F28079D. The first pulse width T_1 is adjusted to build up the inductor current. The second time interval T_2 is set to form a window for waveform monitoring that consists of a turn-OFF falling edge and a turn-ON rising edge. The third time interval T_3 can also be set to observe rising and falling edges. Because GaN switching typically settles in 10's nanoseconds, T_2 and T_3 can be set to a few hundreds of nanoseconds to ensure all voltages and currents reach steady states. The entire period of T_1 through T_3 is repeated every two seconds to allow inductor current reset to zero while repeating the switching pattern for waveform monitoring.

Fig. 7 shows the photograph of the DPT test setup for the direct drive HEMT. The dc bus capacitor C_{dc} consists of two 550-V,

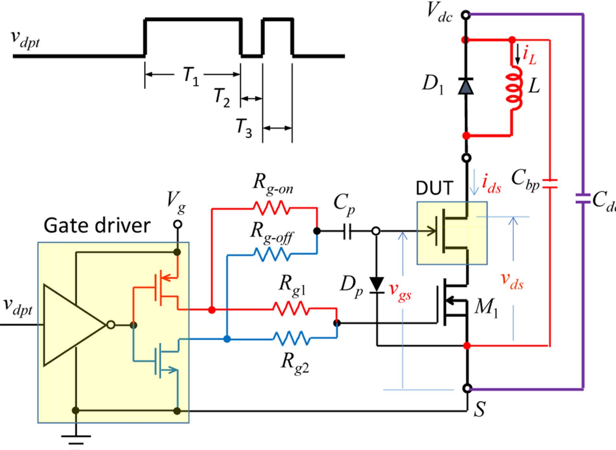

Fig. 6. Power circuit for the double-pulse test.

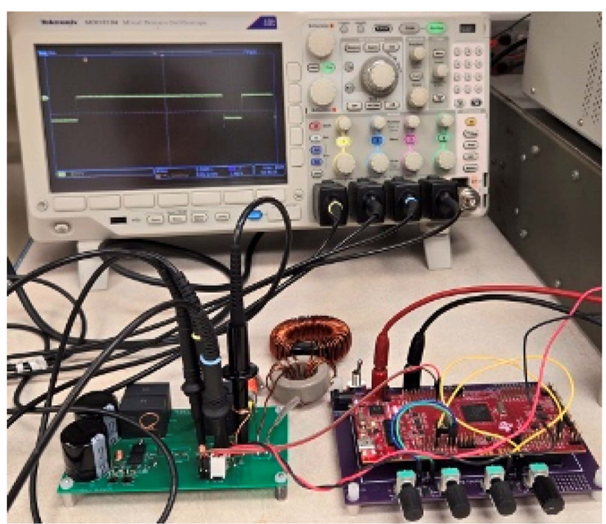

Fig. 7. Photograph of the DPT power circuits.

47-μF local bulk capacitors and two 560-V, 2.2-μF film capacitors for a maximum test voltage of 550 V. A bypass capacitor (C_{bp}) of 650-V, 47-nF across V_{dc} and ground node S is added to eliminate the switching noise across v_{gs}. A small inductor is connected in series with the main inductor to reduce the parasitic capacitance. The total inductance L is 470 μH.

Table II lists the circuit components and their key specifications used in this experiment.

The gate driver, UCC 27511A, is rated 4-A sourcing current with 5-Ω pull-up resistance and 8-A sinking current with 0.375-Ω pull-down resistance.

The device current i_{ds} is monitored with a noninductive current viewing resistor (CVR) with 0.0981-Ω resistance and 1.2-GHz bandwidth. The inductor current i_L is monitored with a scope current probe to calibrate the device current under turn-ON condition. The drain-source voltage v_{ds} is monitored with Tektronix TPP0850 rated 800-MHz bandwidth and 1-kV range. The gate-source voltages $v_{gs\text{-}H}$ and $v_{gs\text{-}M}$ and MOSFET drain-source voltage $v_{ds\text{-}M}$ are monitored with TPP1000 rated

TABLE II
CIRCUIT COMPONENTS AND THEIR KEY SPECIFICATIONS

Component	Part number	Key specifications
Diode D_1	IDL04G65C5XUMA2	650V, 4A
MOSFET M_1	AON7522E	30V, 4mΩ
Gate driver	UCC27511A	20V, 4/8A
Diode D_p	1N4148	75V, 0.5A
Bus capacitor C_{dc}	2 sets of (47µF, 550V + 2.2µF, 560V)	
Bypass C_{bp}	47nF, 630V	
Inductor L	470µH, 25A	
Capacitor C_p	0.22µF, 25V	
MOSFET R_{g1}	1kΩ, 0.1W	
MOSFET R_{g2}	10kΩ, 0.1W	
HEMT $R_{g\text{-on}}$	10Ω, 0.1W	
HEMT $R_{g\text{-off}}$	0-10Ω, 0.1W	

1-GHz bandwidth and 300-V range. The oscilloscope model is MDO3104 with 2.5-GHz sampling rate and 1-GHz bandwidth.

V. Initial Power-Up Test Results

Under startup or standby condition, the leakage current of device under test is charging the MOSFET output capacitance, which can cause MOSFET voltage higher than the absolute value of the GaN threshold voltage and even resulting in avalanche. Zojer [7] and Koyama et al. [8] suggested adding a Zener diode across the MOSFET to avoid avalanche for the direct drive circuit. In the conventional cascode configuration, it was suggested in [29] that adding a high mega-ohm resistor or antiparalleling a Zener or Schottky diode to bypass the leakage current can avoid the avalanche.

Our approach is to choose a higher C_{oss} MOSFET to lower the voltage across the MOSFET ($v_{ds\text{-}M}$). The higher the C_{oss}, the lower the $v_{ds\text{-}M}$, which also tends to be a lower conduction voltage drop. The Si MOSFET shown in Table II has been successfully tested under startup and regular DPT conditions. It was also successfully tested in an in-house designed converter circuit that runs into burst mode under no-load condition. In some occasions, if the startup or standby time is very long, then an external path should be added to bypass the leakage current to avoid MOSFET running into avalanche condition.

Fig. 8 shows the experimental voltage waveforms including MOSFET gate-source voltage $v_{gs\text{-}M}$, HEMT gate-source voltage $v_{gs\text{-}H}$, MOSFET drain-source voltage $v_{ds\text{-}M}$, and the drain-source voltage v_{ds} measured from the drain of HEMT and the source of MOSFET under a repetitive DPT operation. The measurement verifies the conceptual voltage waveforms depicted in Fig. 3 under $V_{\mathrm{dc}} = 100$ V and $V_g = 16$ V condition.

Initially $v_{gs\text{-}M} = 0$, and $v_{gs\text{-}H} = -16$ V. Using the time periods described in Fig. 3, the voltage level during the first turn-ON period can be summarized as follows.

From t_0 to t_1: $v_{gs\text{-}M}\,(t_0) = 0$, $v_{gs\text{-}M}\,(t_1) = 2$ V.

From t_1 to t_2:

$$v_{ds-M}\,(t_1) = 0, v_{ds-M}\,(t_2) = 10V$$
$$v_{gs-H}\,(t_1) == -16V, v_{gs-H}\,(t_2) = -10V\ (= V_{th-H})$$
$$v_{ds}\,(t_1) = 100V, v_{ds}\,(t_2) = 10V.$$

From t_2 to t_3: Plateau period as the current building up.

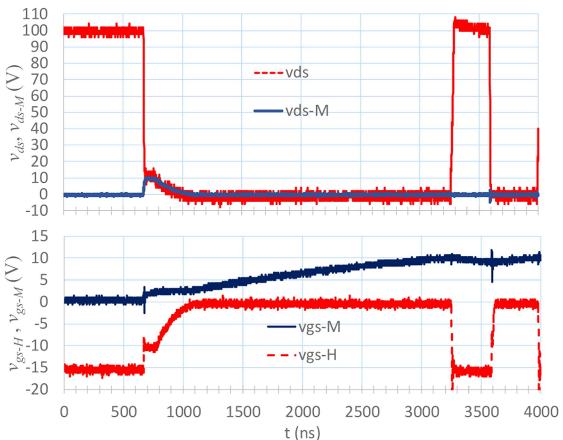

Fig. 8. Experimental drain- and gate-source voltages under a repetitive DPT condition.

From t_3 to t_4:

$$v_{gs-H}(t_3) == -10V, v_{gs-H}(t_4) = 0$$
$$v_{ds-M}(t_3) = 10V, v_{ds-M}(t_4) = 0V$$
$$v_{ds}(t_3) = 10V, v_{ds}(t_4) = 0.$$

The experimental voltage waveforms of this first pulse turn-ON period clearly verify that modified cascode structure provides the initial blocking and prevents the HEMT from turning on. For the time periods from t_5 to t_7 and t_8 to t_{11}, only HEMT is involved in switching, and the detailed voltage and current waveforms can be seen in the following section.

VI. Switching Loss Evaluation

A. Experimental Voltage and Current Waveforms and Switching Energy

Fig. 9 depicts the voltage and current waveforms during the time period T_3 of DPT shown in Fig. 6 under $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 0$, $V_g = 12$ V, and $I_L = 10$ A condition. The first switching transition turns ON the HEMT with v_{gs} rising from –10.4 to +0.6 V and v_{ds} falling from V_{dc} to its ON-drop voltage. Fig. 9(a) and (b) are under $V_{\text{dc}} = 400$ and 500 V test conditions. With the same gate drive circuit condition, their voltage and current slew rates are nearly identical. The switching energy clearly increases as the dc bus voltage increases.

Although the CVR has a faster bandwidth than that of the voltage probe, a small CVR inserted lead somehow slows down the current measurement bandwidth. In the end, the v_{ds} and i_{ds} waveforms match well in time scale coincidently. However, the gate-source voltage v_{gs} is leading by four sampling points, which needs to be deskewed.

To tune gate-source voltage (V_{gs}) and drain-source current (I_{ds}), we can perform deskew during turn-ON where the device current I_{ds} starts rising after V_{gs} passes the threshold voltage ($V_{th\text{-HEMT}}$). To tune V_{gs} and the device voltage V_{ds}, we can perform de-skew during turn-OFF where V_{ds} starts rising after V_{gs} falls below $V_{th\text{-HEMT}}$. If aligned well, we should see V_{ds} falls right after I_{ds} rises to the load current during turn-ON and I_{ds} falls right after V_{ds} rises to the dc bus voltage during turn-OFF.

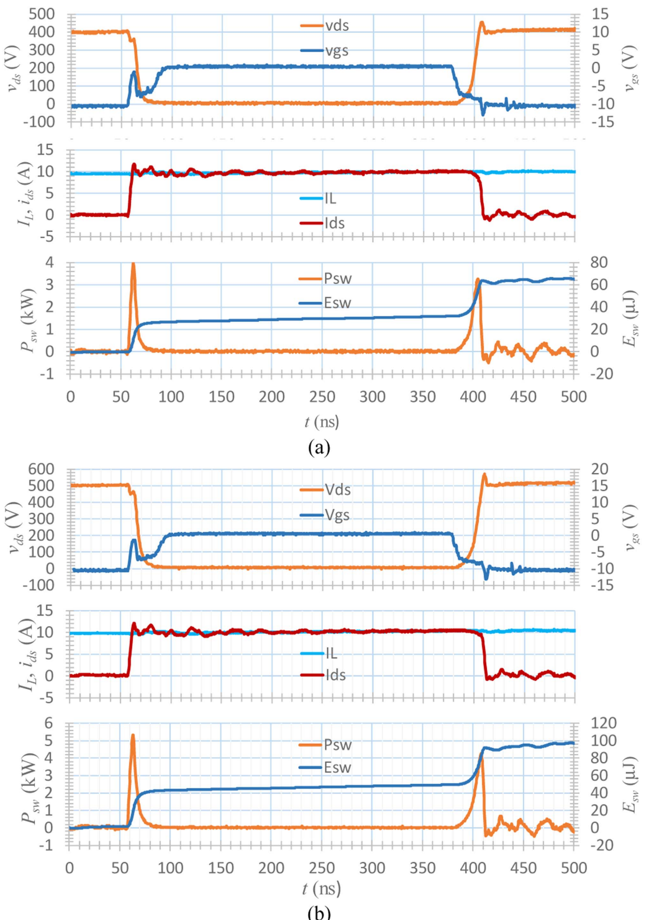

Fig. 9. Voltage and current waveforms with $I_L = 10$ A, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 0$, and $V_g = 12$ V under (a) 400-V and (b) $V_{\text{dc}} = 500$-V V_{dc} conditions.

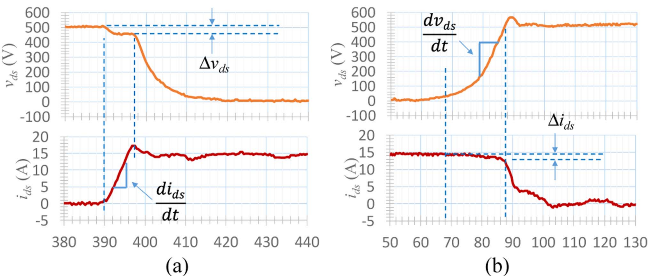

Fig. 10. Voltage and current waveforms with $V_{\text{dc}} = 500$-V, $I_L = 10$ A, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 5\ \Omega$, and $V_g = 12$ V under (a) turn-ON and (b) turn-OFF conditions.

A detailed deskew result under the test condition of 500 V, 15 A is shown in Fig. 10. Fig. 10(a) shows deskewed voltage and current waveforms under turn-ON condition. A voltage drop of Δv_{ds} can be clearly seen during current rise period where di_{ds}/dt multiplying with the loop inductance results in a voltage drop. Fig. 10(b) shows deskewed voltage and current waveforms under turn-OFF condition. A voltage drop of Δi_{ds} can be clearly seen during voltage rise period where dv_{ds}/dt multiplying with the device output capacitances results in a current drop. Notice that during turn-ON, the major portion of Δv_{ds} is constant because di_{ds}/dt is a constant. However, during turn-OFF, the voltage

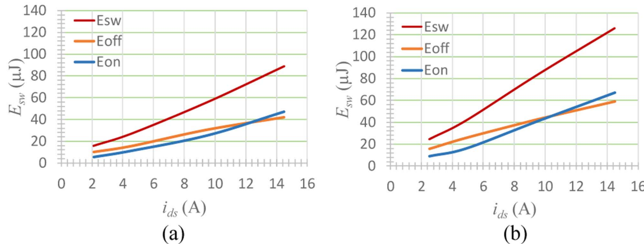

Fig. 11. Switching energy as a function of device current with $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 0$, and $V_g = 12$ V under (a) 400-V and (b) 500-V V_{dc} conditions.

rise rate is nonlinear due to highly nonlinear device output capacitances, and thus Δi_{ds} shows a slope throughout the entire voltage rise period.

With the same measurement condition, the current is increased from 2.2 to 15 A, and the switching energy including E_{ON}, E_{OFF}, and $E_{sw} = E_{\text{ON}} + E_{\text{OFF}}$ as a function of device current i_{ds} are plotted in Fig. 11 under (a) 400-V and (b) 500-V conditions. Since the device switching involves charging and discharging of the freewheeling diode junction capacitance (C_j) and the device output capacitance (C_{oss}), the increase of switching energy is not directly proportional to the dc bus voltage. Under this specific test condition, E_{ON} and E_{OFF} increase by approximately 40% when V_{dc} is increased from 400 to 500 V. In terms of switching energy as a function of current, the measurement results indicate that E_{ON} is directly proportional to i_{ds}, but E_{OFF} as a function of i_{ds} shows a slower increasing rate.

B. Gate Drive Voltage Effect on Switching Energy

In bridge-type circuits, there is a short freewheeling period that the both upper and lower devices must remain inactive. During which, the gate-source voltages of both devices are negative. In contrast, for e-mode MOSFETs or HEMTs, their gate-source voltages need to be zero or negative. On the other hand, the d-mode HEMT offers flexibility of varying gate-source voltage magnitude under direct driven condition. The question is what would be the appropriate gate drive voltage. As mentioned in [10], an excessive negative gate-source voltage tends to result in a high voltage drop under reverse conducting or freewheeling condition, which is disadvantageous in high switching frequency operations.

However, this article revealed that a high magnitude of v_{gs} could significantly reduce the turn-OFF loss. This is indeed a considerable advantage for nonbridge type converters, as they do not require a dead-time period and the associated reverse conducting voltage drop.

To examine the gate drive voltage effect, the study here is to fix all the gate drive resistances and test the circuit under various gate drive voltage conditions. Fig. 12 illustrates the example voltage and current waveforms with $V_{\text{dc}} = 500$ V, $I_L = 10$ A, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 5\ \Omega$ for (a) $V_g = 13$ V and (b) $V_g = 16$ V conditions. To assesses the turn-OFF energy (E_{OFF}), this set of waveforms starts with turn OFF as the first transition, or the T_2 period depicted in Fig. 6.

Comparing the switching energy, the case with $V_g = 16$ V versus $V_g = 13$ V indicates a significant loss reduction. The total

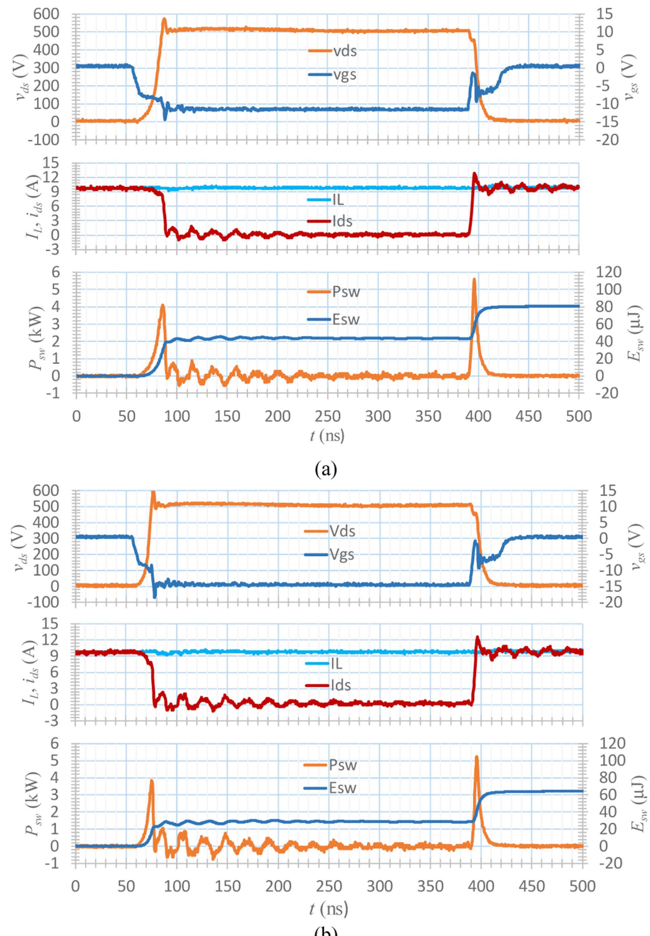

Fig. 12. Voltage and current waveforms with $V_{\text{dc}} = 500$-V, $I_L = 10$ A, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 5\ \Omega$ under (a) $V_g = 13$ V and (b) $V_g = 16$ V conditions.

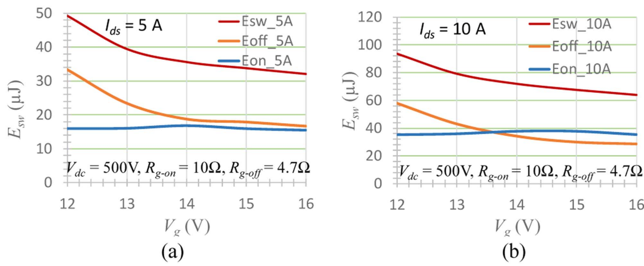

Fig. 13. Switching energy as a function of gate drive voltage showing (a) 5-A and (b) 10-A conditions.

switching energy drops from 80 to 64 μJ, or 20% reduction. By examining the details, such a loss reduction only comes from device turn-OFF, which clearly indicates a much faster turn-OFF voltage slew rate, and thus lowering the switching loss. By comparing the turn-OFF loss along, E_{OFF} is reduced from 43.1 to 28.6 μJ, or 33% reduction. Further comparison with $V_g = 12$ V shown in Fig. 9(b), both E_{ON} and E_{sw} are much higher than those under $V_g = 13$ and 16 V conditions.

Fig. 13 compares switching energy as a function of gate drive voltage V_g from 12 to 16 V for (a) $I_L = 5$ A and (b) $I_L = 10$ A under $V_{\text{dc}} = 500$ V, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 5\ \Omega$ condition.

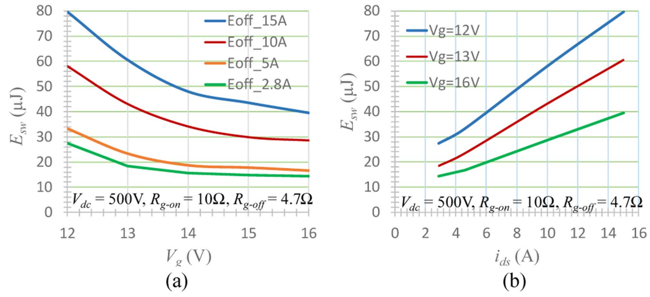

Fig. 14. (a) Turn-OFF energy as a function of gate drive voltage. (b) Turn-OFF energy as a function of load current.

Both plots in Fig. 13 indicate that turn-ON energy is constant disregard the magnitude of the gate drive voltage. The turn-OFF energy, however, reduces asymptotically, and the highest loss reduction segment occurs when V_g varies from 12 to 13 V. From 15 to 16 V, the gain on turn-OFF loss reduction becomes less noticeable.

With the same $V_{\rm dc} = 500$ V, $R_{g\text{-ON}} = 10\ \Omega$, $R_{g\text{-OFF}} = 4.7\ \Omega$ condition, Fig. 14(a) further plots $E_{\rm OFF}$ as a function of V_g under different device current conditions. The higher the device current, the clearer the $E_{\rm OFF}$ reduction with increased V_g magnitude. This can be seen in Fig. 14(b), which plots $E_{\rm OFF}$ as a function of i_{ds} under different V_g conditions with 12, 13, and 16 V for clear separations. Under all current conditions, the turn-OFF reduction reaches 50% by increasing V_g from 12 to 16 V.

It should be noticed that the experimental HEMT has a threshold voltage of –10 V. With direct drive, there is a voltage drop at the clamping diode D_p. Adding a small voltage drop at the gate driver, the actual v_{gs} is very close to $V_{th\text{-}H}$ when $V_g = 12$ V. In other words, the injected negative current to turn off the device is small when the magnitude of V_g is not high enough.

Fig. 15 further examines the waveforms in detail showing exploded view of HEMT v_{gs}, v_{ds}, and $E_{\rm OFF}$ waveforms at the turn-OFF transition under $i_{ds} = 5$ A, $V_g = 12$, 13, and 16 V conditions. Under the initial turn-on condition, v_{gs} is the voltage drop across D_p and is +0.6 V, With $V_g = 12$ V, v_{gs} is –10.4 V under turn-OFF condition. Similarly, with $V_g = 13$ and 16 V, v_{gs} is –11.4 V, and –14.4 V, respectively, under turn-OFF condition. When v_{gs} transitions from turn-ON to -OFF, during the plateau period, v_{ds} rises to $V_{\rm dc}$ with a small overshoot caused by the loop parasitic inductance. The higher the gate voltage, the faster the v_{ds} slew rate and voltage overshoot, while the lower turn-OFF energy.

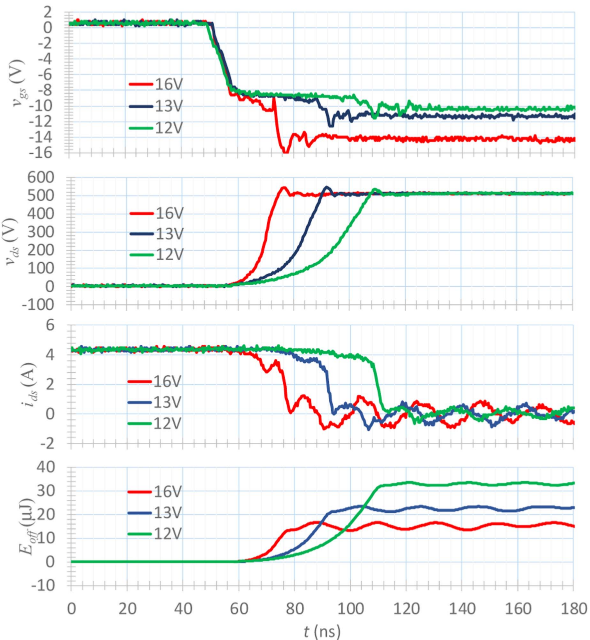

Fig. 15. Exploded view of HEMT $v_{\rm gs}$, v_{ds}, and $E_{\rm OFF}$ waveforms under $i_{ds} = 5$ A, $V_{\rm dc} = 500$ V, $V_g = 12$, 13, and 16 V conditions.

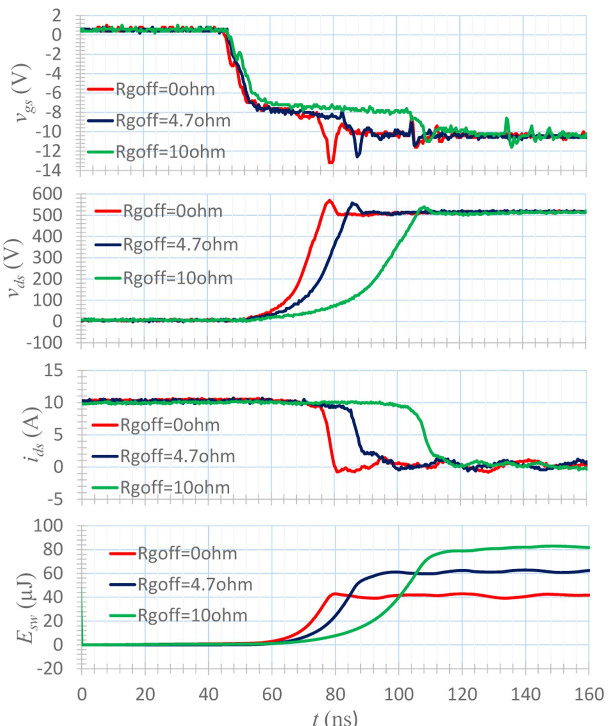

Fig. 16. Exploded view of HEMT $v_{\rm gs}$, v_{ds}, and $E_{\rm OFF}$ waveforms under $i_{ds} = 10$ A, $R_{g\text{-OFF}} = 0$, 4.7, and 10 Ω conditions.

C. Gate Resistance Effect on Turn-Off Energy

Fig. 15 suggests that the alternative turn-OFF loss reduction method is to shorten the plateau period by reducing $R_{g\text{-OFF}}$ because of the reduction of Miller capacitance (C_{rss}) discharging time. To verify $R_{g\text{-OFF}}$ effect, Fig. 16 compares detailed voltage and current waveforms for $R_{g\text{-OFF}} = 0$, 4.7, and 10 Ω under $V_{\rm dc} = 500$ V, $V_g = 12$ V, and $i_{ds} = 10$ A condition. With $R_{g\text{-OFF}} = 0$, the turn-OFF speed is fastest due to the smallest C_{rss} discharging time constant.

Comparing $R_{g\text{-OFF}} = 0$ and 10 Ω, the plateau period is reduced by 50%, or from 44 ns to 22 ns. This plateau period reduction also translates to 50% turn-OFF loss reduction (from 82 to 41

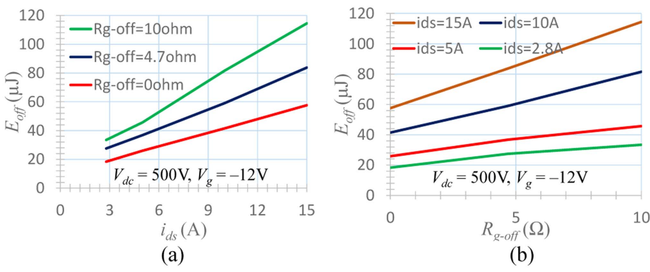

Fig. 17. (a) $E_{\rm OFF}$ as a function of i_{ds} under different $R_{g\text{-OFF}}$ conditions and (b) $E_{\rm OFF}$ as a function of $R_{g\text{-OFF}}$ under different i_{ds} conditions.

μJ) because during which the current maintains constant while the voltage is rising. At the end of the plateau period, i_{ds} drops from 10 A to zero within 4 ns with $R_{g\text{-OFF}} = 0$ and 8 ns with $R_{g\text{-OFF}} = 10\ \Omega$. The waveforms indicate that while a low $R_{g\text{-OFF}}$ can lower $E_{\rm OFF}$, the penalty is high voltage slew rate on v_{ds} and its potentially associated electromagnetic interference (EMI).

Fig. 17(a) plots the turn-OFF energy $E_{\rm OFF}$ as a function of the device current i_{ds} under different $R_{g\text{-OFF}}$ conditions. Again, by reducing $R_{g\text{-OFF}}$ from 10 Ω to 0, $E_{\rm OFF}$ is reduced approximately 50% under all different current conditions. It should be noticed that $E_{\rm OFF}$ contains both channel turn-OFF energy and output capacitance (C_{oss}) related charge energy E_{oss}, which is associated with the square of drain-source voltage [30]. As $E_{\rm OFF}$ is approximately linearly increased with i_{ds}, it is possible to extend the curve down to $i_{ds} = 0$ to obtain E_{oss} under different $R_{g\text{-OFF}}$ condition. Fig. 17(b) plots the turn-OFF energy $E_{\rm OFF}$ as a function of $R_{g\text{-OFF}}$ under different i_{ds} conditions. Similar to the above argument on E_{oss}, even if $i_{ds} = 0$, E_{oss} still exists, and $E_{\rm OFF}$ will not reduce to zero under different $R_{g\text{-OFF}}$ condition.

VII. Discussion on Measurement Issues

Despite being developed in-house, the GaN HEMT still needs wire-bonding and packaging for circuit testing. Thus, the parasitic components are unavoidable in the PCB layout. The noise and oscillation after switching transient are quite severe under fast switching transients. With a finite wire length from the power supply to the circuit board under test, sufficient bulk and bypass capacitors are necessary on PCB to ensure a stable dc bus voltage.

Three significant measurement challenges were found in the GaN HEMT device characterization.

1) Matching of the bandwidths of the voltage probes and current measurement. Before the use of matched high-voltage, high-bandwidth voltage probes, we found significant differentials and inconsistencies in their response time and overshoot during transients, and it was very difficult to de-skew.
2) Sampling rate of the oscilloscope. The one used in this characterization is 2.5 GHz, which means the highest sampling resolution is 400 ps. With the GaN current fall time <4 ns under $V_g = 12$ V and $R_{g\text{-OFF}} = 0$ turn-OFF condition, each transient can only sample less than 10 points, which is insufficient to precisely measure the switching performance.
3) Similar to the above issue, the oscilloscope should have sufficient number of bits for the vertical resolution.

VIII. Conclusion

As the commercial devices were unavailable, we employed the in-house developed device to characterize the d-mode GaN HEMTs and revealed several distinctive switching features under direct-drive gating condition. The basic switching features were first described theoretically and then validated through extensive testing with an in-house developed DPT tester.

Major findings and contributions include the following.

1) Initial power-up can be protected with a modified cascode architecture by using a diode to replace the wire from the HEMT gate to the MOSFET source.
2) Turn-OFF energy can be significantly reduced by increasing the gate drive voltage. A large magnitude of the HEMT gate-source voltage can induce a high gating current to accelerate the device turn-OFF process. This specific feature does not exist in e-mode HEMTs or conventional power MOSFETs.
3) Turn-OFF energy can also be decreased by reducing the gate drive resistance. This is a feature also found in e-mode HEMTs and conventional power MOSFETs, and the effect is quite similar to that of increasing the gate drive voltage as it shortens the plateau period.
4) Turn-ON energy is not affected by the negative gate drive voltage magnitude.

Even though the turn-ON energy is also important in many applications, its loss reduction feature is not addressed in this article because the turn-ON energy involves the opposite-side device and its reverse recovering characteristic. Furthermore, in most soft-switching converters, turn-ON energy is negligible, making it less of a concern. To further explore turn-ON losses, the converter circuit and its specific operating mode need to be well defined.

Future work can be directed to a comprehensive evaluation and comparison between the conventional cascode and direct-driven HEMT devices.

References

[1] U. K. Mishra, P. Parikh, and Y.-F. Wu, “AlGaN/GaN HEMTs - An overview of device operation and applications,” *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.
[2] K. J. Chen et al., “GaN-on-Si power technology: Devices and applications,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017.
[3] S. Bahl and M. D. Seeman, “New electrical overstress and energy loss mechanisms in GaN cascodes,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 1262–1265.
[4] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, “GaN on Si technologies for power switching devices,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013.
[5] M. Dong, J. Elmes, M. Peper, I. Batarseh, and Z. J. Shen, “Investigation on inherently safe gate drive techniques for normally-On wide bandgap power semiconductor switching devices,” in *Proc. 2009 IEEE Energy Convers. Congr. Expo.*, San Jose, CA, USA, 2009, pp. 120–125.
[6] T. Yoshida, H. Umegami, F. Hattori, M. Yamamoto, and A. Yamaguchi, “Gate drive circuit for normally On type GaN FET,” in *Proc. 2013 IEEE Int. Conf. Electric Power Equip. - Switching Technol.*, Matsue, Japan, Oct. 2013, pp. 1–4.

[7] B. Zojer, "A new driving concept for normally-on GaN switches in cascode configuration," in *Proc. 2016 IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 996–1001.
[8] M. Koyama, K. Ikeda, and K. Takao, "Novel cascode GaN module integrated a single gate driver IC with high switching speed controllability," in *Proc. 20th Eur. Conf. Power Electron. Appl.*, Riga, Lativa, Sep. 2018, pp. P.1–P.8.
[9] T. Sugiyama et al., "Stable cascode GaN HEMT operation by direct gate drive," in *Proc. 2020 Int. Symp. Power Semicond. Devices ICs*, Vienna, Austria, Sep. 2020, pp. 23–26.
[10] V. Heumesser et al., "D-mode GaN HEMT with direct drive," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, Hsinchu, Taiwan, Aug. 2023. pp. 1–6.
[11] S.-Y. Yu, "Performance evaluation of direct drive high voltage gallium-nitride devices in LLC series resonant," in *Proc. IEEE Workshop Wide Bandgap Power Device Appl.*, Fayetteville, AR, USA, Nov. 2016, pp. 64–69.
[12] (n.d.). [Online]. Available: https://www.ti.com/power-management/gallium-nitride/products.html
[13] V. Heumesser et al., "Cascode CaN HEMT gate driving analysis," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, Hsinchu, Taiwan, Aug. 2023, pp. 1–6.
[14] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.
[15] Z. Chen and J. R. Guitart, "Dv/dt immunization limit of LV MOSFET in cascode GaN FET and dv/dt safe chart for MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, Mar. 2017, pp. 1946–1949.
[16] T & M Research Products, Inc., Series SDN CVR Products. (n.d.). [Online]. Available: https://www.tandmresearch.com/
[17] V. Shivaram, S. N. H., N. Hegde, S. B, Y. Pai, and V. M, "A method to deskew probes and estimate power loop inductance of WBG-DPT circuits," in *Proc. 2023 IEEE Appl. Power Electron. Conf. Expo.*, Orlando, FL, USA, Mar. 2023, pp. 2469–2473.
[18] K. Yao, H. Tang, C. Ma, and C. Wu, "Constant switching frequency control for CRM buck PFC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4223–4234, Dec. 2020.
[19] J.-C. Crebier, B. Revol, and J.-P. Ferrieus, "Boost-chopper-derived PFC rectifiers: Interest and reality," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 36–45, Feb. 2005.
[20] C. Wang, S. Xu, S. Lu, and W. Sun, "A single-switched high-switching-frequency quasi-resonant flyback converter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8775–8786, Sep. 2019.
[21] L. Xue, X. Tian, and H. Cui, "Implementation of time division multiplexing with commercial flyback controller for multi-outputs USB power delivery charger," *IEEE Open J. Power Electron.*, vol. 3, pp. 665–678, 2022.
[22] S.-C. Liu, B.-Y. Chen, Y.-C. Lin, T.-E. Hsieh, H.-C. Wang, and E. Y. Chang, "GaN MIS-HEMTs with nitrogen passivation for power device applications," *IEEE Electron Device Lett.*, vol. 35, no. 10, pp. 1001–1003, Oct. 2014.
[23] S. C. Liu, G. M. Dai, and E. Y. Chang, "Improved reliability of GaN HEMTs using N_2 plasma surface treatment," in *Proc. 2015 IEEE Int. Symp. Phys. Failure Anal. Integr. Circuit*, Hsinchu, Taiwan, Jun. 2015, pp. 378–380.
[24] C.-Y. Yang, T.-L. Wu, T.-E. Hsieh, and E. Y. Chang, "Investigation of degradation phenomena in GaN-on-Si power MIS-HEMTs under source current and drain bias stresses," in *Proc. 2018 IEEE Int. Rel. Phys. Symp.*, Burlingame, CA, USA, Mar. 2018, pp. P-WB.5-1–P-WB.5-4.
[25] X. Wang et al., "Robust SiNx /AlGaN interface in GaN HEMTs passivated by thick LPCVD-grown SiNx layer," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 666–668, Jul. 2015, doi: 10.1109/LED.2015.2432039.
[26] S. A. Jauss, K. Hallaceli, S. Mansfeld, S. Schwaiger, W. Daves, and O. Ambacher, "Reliability analysis of LPCVD SiN gate dielectric for AlGaN/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2298–2305, May 2017, doi: 10.1109/TED.2017.2682931.
[27] Y. Qi et al., "Evaluation of LPCVD SiNx gate dielectric reliability by TDDB measurement in si-substrate-based AlGaN/GaN MIS-HEMT," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1759–1764, May 2018, doi: 10.1109/TED.2018.2813985.
[28] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.
[29] R. K. Lal et al., "Method of forming electronic components with increased reliability," U.S. Patent, US9,171,836 B2, Oct. 27, 2015.
[30] H. Wen, D. Jiao, C.-S. Yeh, and J.-S. Lai, "Channel turn-Off energy model for zero-voltage switching wide bandgap devices," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 9, no. 4, pp. 4016–4025, Aug. 2021.

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