Design and Optimization of the MMC-Based Power Electronic Transformer Considering Ripple Power Transfer

Zhixiang Li, *Graduate Student Member, IEEE*, Yunqing Pei, *Member, IEEE*, Jiahao Liu,
Laili Wang, *Senior Member, IEEE*, and Zesong Leng

***Abstract*—The modular multilevel converter (MMC)-based power electronic transformer (PET) offers the advantage of enabling ripple power transfer (RPT) through inherent dual active bridges (DABs), thereby reducing the required submodule capacitance and enhancing power density. However, the implementation of RPT leads to increased loss and volume of DABs, posing challenges to the operation mode selection and parameter design. In this article, the design and optimization of the MMC-based PET when it operates in the RPT mode are comprehensively investigated for the first time through multiobjective optimization (MOO). First, suitable models are established to estimate component losses and volumes of the MMC-based PET. Utilizing these models, an MOO program considering both efficiency and power density is developed to explore the design principles of the PET. Notably, this article also proposes a design technique based on partial RPT and verifies its benefits in the PET design. The research done in this article seeks to provide guidance for the optimal operation mode selection and parameter design of the MMC-based PET. A design example of a full-scale 30 kW/1 kV PET submodule, together with a scaled-down but complete PET prototype, validates the effectiveness of the proposed analysis and design methods.**

***Index Terms*—Dual active bridge (DAB), modular multilevel converter (MMC), multiobjective optimization (MOO), power electronic transformer (PET), ripple power transfer (RPT).**

I. INTRODUCTION

THE integration of distributed energy sources, energy storage systems, and electric vehicles has become increasingly prevalent in the pursuit of more efficient, flexible, and resilient power distribution systems. This evolution has led to the emergence of medium-voltage hybrid ac/dc distribution grids, which combine ac and dc components to accommodate diverse sources and loads [1]. However, the integration of these disparate technologies presents challenges related to voltage conversion, power flow control, and system stability. To address these, power electronic transformers (PETs), also known as solid-state transformers or electric energy routers, have garnered significant attention. Unlike conventional line-frequency transformers designed for ac systems, PETs offer the capability to interface multiple ac and dc sources and loads simultaneously, enabling bidirectional power flow and enhanced control flexibility, thus playing a crucial role in the medium-voltage hybrid ac/dc distribution grids [2].

As of now, the PET topologies acknowledged for distribution grid applications primarily feature two prevalent multilevel topologies in the input stage [3]: the cascade H-bridge (CHB) converter and the modular multilevel converter (MMC). Additionally, the dual active bridge (DAB) converter serves as the primary approach for the high-frequency isolation within the PETs [4]. The CHB-based PET lacks a medium-voltage dc (MVDC) port, which limits its applicability in applications that require an MVDC bus, such as the integration of energy storage devices [5] or distributed energy resources [6], [7], and the power systems in vessels [8]. In contrast, the MMC-based PETs, equipped with both medium-voltage ac (MVAC) and MVDC buses, stand out as more advantageous for use in the medium-voltage hybrid ac/dc distribution grids compared to the CHB-based ones. The MMC-based PET topologies applicable to distribution grids can be broadly categorized into two types according to the access modes of DABs. The first type involves a cascade connection of the MMC's dc bus with input-series-output-parallel centralized DABs, as detailed in [9]. The second type utilizes a cascade connection of MMC half-bridges (HBs) with distributed DABs that are arranged in an input-independent-output-parallel configuration [10], as illustrated in Fig. 1. In this arrangement, each HB of the MMC is linked to a DAB converter. The secondary sides of all DABs are paralleled to form a low-voltage dc (LVDC) bus, which can then be converted to a low-voltage ac bus through inverters. Comparatively, the topology in Fig. 1 offers quite a few advantages over the one in [9], including fewer capacitors, enhanced modularity, simplified balancing control, and reduced current stress on power devices, making it more apt for use in medium-voltage hybrid ac/dc distribution grids [10].

Moreover, another remarkable advantage of the PET topology depicted in Fig. 1 lies in its ability to enable ripple power transfer (RPT) through inherent DABs, thereby reducing the

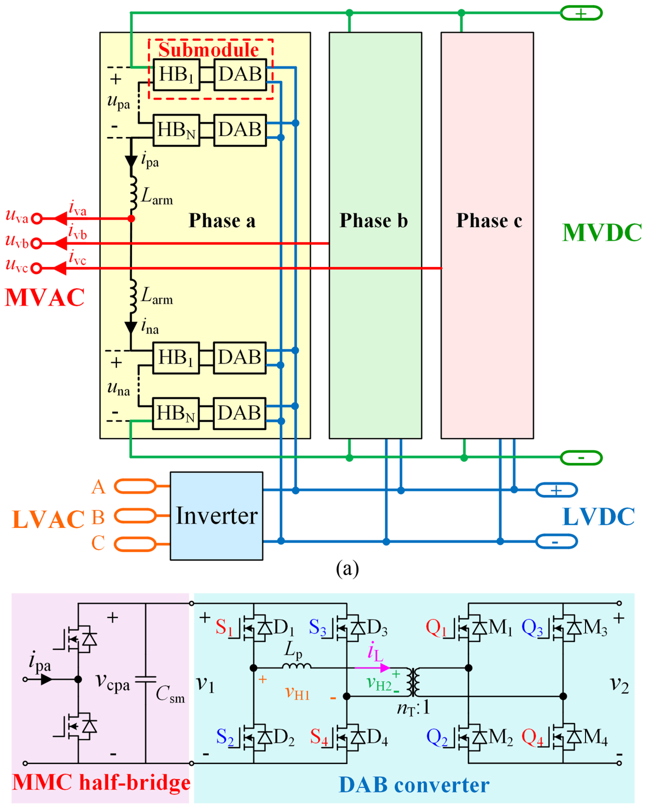
---

Received 12 July 2024; revised 5 November 2024; accepted 7 December 2024. Date of publication 11 December 2024; date of current version 28 January 2025. This work was supported by the Shaanxi Science and Technology Innovation Team Program under Grant 2022TD-64. Recommended for publication by Associate Editor M. Liserre. *(Corresponding authors: Yunqing Pei; Laili Wang.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: lizhixiang951206@stu.xjtu.edu.cn; peiyq@mail.xjtu.edu.cn; natural@stu.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; lengzs@stu.xjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3515472.

Digital Object Identifier 10.1109/TPEL.2024.3515472



(a)

(b)

Fig. 1. Topology structure of the MMC-based PET. (a) Structure of the overall PET. (b) Configuration of the submodule.

required submodule capacitance and enhancing power density [11]. In most MMC-based topologies, large submodule capacitors are needed to suppress low-frequency voltage ripple, which essentially arises from the ripple power generated by the MMC. However, as shown in Fig. 1, in the MMC-based PET, inherent DABs can serve as power channels to transfer this ripple power from the MMC arms to the low-voltage side. Due to symmetry, the ripple powers from different arms will cancel each other on the LVDC side. As a result, the required submodule capacitance can be substantially reduced, facilitating the power density enhancement of the PET.

However, when the MMC-based PET operates in the RPT mode, the transmission power of DABs increases considerably, as these DABs are required to transfer both ripple and dc power simultaneously. This can lead to larger heatsinks and magnetic components (including transformers and inductors), ultimately diminishing the intended enhancement of power density. Consequently, although RPT technology can reduce the capacitor volume, its actual contribution to the overall power density is questionable. Moreover, for PETs, efficiency is as critical as power density in performance evaluation. However, the implementation of RPT exacerbates the losses in power semiconductor devices and magnetic components, adversely affecting the PET efficiency. Hence, a tradeoff seems to exist between power density and efficiency in the design of the MMC-based PET operating in the RPT mode.

Regrettably, there is currently a gap in research on designing the MMC-based PET in the RPT mode. The above discussion illustrates that in this mode, the designs of the MMC submodule capacitance and the DAB parameters are interconnected. However, existing studies have only covered the separate design of the MMC and DAB, without considering the impact of RPT [12], [13], [14], [15], [16], [17]. Thus far, it remains uncertain whether the DAB should transfer ripple power, and, if so, what proportion of ripple power should be transferred from the perspective of overall power density and efficiency. Moreover, it is also unclear how to design the circuit parameters of the MMC-based PET operating in the RPT mode.

The above-discussed design and optimization of the MMC-based PET operating in the RPT mode is a highly complex issue, presenting more challenges compared to that of normal converters. On one hand, RPT affects not only the selection of the MMC submodule capacitance but also the design of the DAB, meaning that the parameters of the MMC and DAB are interconnected and should be optimized together. On the other hand, this process involves multiple optimization variables (e.g., the RPT proportion, the submodule capacitance, and the DAB parameters like switching frequency and inductance) and conflicting optimization objectives (including power density and efficiency), and the interdependence between these optimization objectives and variables is intricate.

Given this complexity, the multiobjective optimization (MOO) technique [18], [19], [20], [21] offers a viable approach for analysis. Specifically, analytical models for component loss and volume can establish relationships between optimization variables and objectives. Afterward, by establishing an MOO program that considers both efficiency and power density and examining the resulting Pareto-optimal solutions, it is possible to identify which operation mode and what parameters can achieve the optimal overall performance of the PET. Using this approach, this article comprehensively investigates the design and optimization of the MMC-based PET operating in the RPT mode for the first time. The main contributions of this article lie in the following three aspects.

1) The establishment of models suitable for estimating component losses and volumes of the MMC-based PET operating in the RPT mode, and the development of an MOO program considering both efficiency and power density, serving as valuable tools for the analysis and design of this topology.
2) The exploration of parameter design principles for the MMC-based PET through MOO technique, providing profound and novel insights into the design and optimization of this topology and offering guidance for the selection of its optimal operation mode.
3) The proposal of the design technique based on partial ripple power transfer (PRPT) and the demonstration of its benefits in the design and optimization of the MMC-based PET, providing a better design strategy for this topology.

The main work of this article is outlined as follows. Section II provides an overview of the RPT technique within the MMC-based PET. Section III focuses on establishing models for estimating component losses and volumes of the MMC-based

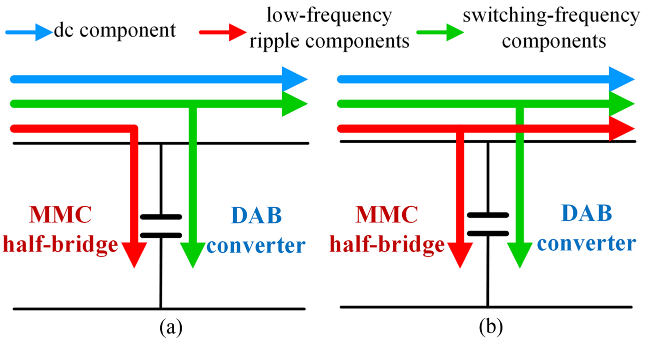


Fig. 2. Illustration of the power flow paths in the PET submodule. (a) Without RPT. (b) With RPT.

PET, accompanied by simulation verifications. Building on these models, an MOO program considering both efficiency and power density is developed in Section IV. Following this, Section V analyzes the obtained Pareto-optimal solutions and reveals the design principles. Then, Section VI presents experimental verifications through both a scaled-down but complete PET prototype and a full-scale PET submodule prototype. Finally, Section VII summarizes the conclusions drawn from this study.

II. OVERVIEW OF RIPPLE POWER TRANSFER IN THE MMC-BASED PET

This section will overview the principle, benefits, and control implementation of the RPT within the MMC-based PET, to enhance readers' comprehension of this concept and the overall work of this article.

Taking the upper arm of phase a (denoted as arm pa) as an example, the total power within an arm is determined by

$$p_{\mathrm{pa}} = u_{\mathrm{pa}} \cdot i_{\mathrm{pa}} \tag{1}$$

where i_{pa} and u_{pa} represent the arm's current and voltage, respectively, as illustrated in Fig. 1(a).

In the steady state, i_{pa} and u_{pa} are given by

$$\begin{cases} i_{\mathrm{pa}}(\omega t) = \frac{1}{3}I_{\mathrm{dc}} + \frac{1}{2}I_{\mathrm{vm}}\cos(\omega t - \varphi_i) \\ u_{\mathrm{pa}}(\omega t) = U_0 - U_{\mathrm{m}}\cos(\omega t - \varphi_u). \end{cases} \tag{2}$$

Here, I_{dc} is the MMC's dc-side current, I_{vm} and φ_i are the amplitude and initial angle of the MMC's ac-side current, respectively, U_0 is the dc component of the arm voltage, and U_{m} and φ_u represent the amplitude and initial angle of the fundamental-frequency component of the arm voltage.

Substituting (2) into (1) yields

$$\begin{aligned} p_{\mathrm{pa}}(\omega t) = {} & U_0 I_{\mathrm{dc}}/3 - U_{\mathrm{m}} I_{\mathrm{vm}}\cos(\varphi_u - \varphi_i)/4 \\ & + U_0 I_{\mathrm{vm}}\cos(\omega t - \varphi_i)/2 - U_{\mathrm{m}} I_{\mathrm{dc}}\cos(\omega t - \varphi_u)/3 \\ & - U_{\mathrm{m}} I_{\mathrm{vm}}\cos(2\omega t - \varphi_u - \varphi_i)/4. \end{aligned} \tag{3}$$

As demonstrated in (3), the arm power contains not only a dc component, but significant fundamental-frequency and second-harmonic components, commonly referred to as ripple power.

Fig. 2 depicts the power flow paths in the PET submodule. If the DAB does not transfer the ripple power (no ripple power transfer, NRPT), its power command is generated by the LVDC voltage control loop and thus contains only a dc component. As a result, the DABs transfer only the dc power required by the LVDC-side load. In this case, as indicated in Fig. 2(a), submodule capacitors absorb all the ripple power from MMC arms, necessitating large capacitance to attenuate voltage ripple. Traditionally, common-mode voltages and circulating currents are injected into the MMC arms to mitigate this ripple power [22]. While this can reduce voltage ripple, it also escalates the current stress on power semiconductor devices and limits the output voltage range of the ac port [23].

Instead, in the MMC-based PET, inherent DABs can serve as power channels to transfer the ripple power to the low-voltage side, as illustrated in Fig. 2(b). Due to the three-phase symmetry of this topology, ripple powers from different phases neutralize each other at the LVDC port. To enable this, the DAB power command should incorporate both the aforementioned dc component and the ripple components shown in (3) [11], [24], [25]. In this case, the ripple power flowing through submodule capacitors will be diminished, and the submodule capacitance required to maintain the voltage ripple within acceptable limits can also be reduced. Provided that the ripple power is completely transferred by DABs (complete ripple power transfer, CRPT), the power flowing through submodule capacitors will consist solely of switching harmonics, thereby allowing a substantial reduction in capacitance.

On the other hand, it may not be necessary for the DAB to transfer 100% of the ripple power; instead, transferring only part of it (partial ripple power transfer, PRPT) could keep the voltage ripple within an acceptable range while also reducing the DAB's transmission power. This article introduces a concept of RPT proportion (λ_{r}) to quantifies the proportion of the ripple power transferred by DABs relative to that generated by the MMC. Accordingly, the complete power command of the DABs connected to arm pa can be constructed as follows:

$$\begin{aligned} p^*_{\mathrm{T,pa}}(\omega t) = {} & k_{\mathrm{p}} \cdot (v^*_{\mathrm{LVDC}} - v_{\mathrm{LVDC}}) \\ & + k_{\mathrm{i}} \cdot \int (v^*_{\mathrm{LVDC}} - v_{\mathrm{LVDC}})dt \\ & + \lambda_{\mathrm{r}} \cdot \{U_0 I_{\mathrm{vm}}\cos(\omega t - \varphi_i)/2 \\ & - U_{\mathrm{m}} I_{\mathrm{dc}}\cos(\omega t - \varphi_u)/3 \\ & - U_{\mathrm{m}} I_{\mathrm{vm}}\cos(2\omega t - \varphi_u - \varphi_i)/4\} \end{aligned} \tag{4}$$

where the first line represents the dc component of the power command, which is generated by the LVDC voltage loop and equal to the dc component in (3) in the steady state.

Specifically, $\lambda_{\mathrm{r}} = 0$ corresponds to the NRPT mode, while $\lambda_{\mathrm{r}} = 1$ corresponds to the CRPT mode. As for the PRPT mode, λ_{r} ranges from 0 to 1 and can be generated by

$$\lambda_{\mathrm{r}} = k_{\mathrm{p}} \cdot (\delta^*_{\mathrm{v}} - \delta_{\mathrm{v}}) + k_{\mathrm{i}} \cdot \int (\delta^*_{\mathrm{v}} - \delta_{\mathrm{v}})dt \tag{5}$$

in real-time control, where δ_{v} denotes the voltage ripple factor.

With the obtained power command in (4), the phase-shift ratio of the individual DAB can be further calculated by [26]

$$D = \begin{cases} \frac{1}{2} - \frac{1}{2}\sqrt{1 - \frac{8 f_{\mathrm{sw}} L_{\mathrm{p}}}{n_{\mathrm{T}} v_1 v_2} \cdot \frac{p^*_{\mathrm{T,pa}}}{N}}, & p^*_{\mathrm{T,pa}} \geq 0 \\ -\frac{1}{2} + \frac{1}{2}\sqrt{1 + \frac{8 f_{\mathrm{sw}} L_{\mathrm{p}}}{n_{\mathrm{T}} v_1 v_2} \cdot \frac{p^*_{\mathrm{T,pa}}}{N}}, & p^*_{\mathrm{T,pa}} < 0 \end{cases} \tag{6}$$

where f_{sw} is the DAB frequency, and the other variables have been shown in Fig. 1.

Equations (4)–(6) constitute the complete control implementation of the RPT in the MMC-based PET.

III. ESTABLISHMENT OF MODELS FOR ESTIMATING COMPONENT LOSSES AND VOLUMES OF THE MMC-BASED PET

This section establishes models suitable for estimating component losses and volumes in the MMC-based PET. First, steady-state models of the MMC-based PET operating in the RPT mode are developed to solve for the steady-state electrical quantities needed for later sections. Then, detail models for estimating the conduction loss and switching loss of MOSFETs, the volume of heatsinks, and the core loss and winding loss of magnetic components are presented due to their complexity. All models are verified through simulations. The remaining estimations of component volumes and losses will be briefly covered in Section IV.

A. Steady-State Models of the MMC-Based PET Operating in the RPT Mode

First, (7) can be obtained according to the energy conservation, where $e_{c,\mathrm{pa}}$ represents the total energy stored in the N submodule capacitors of arm pa

$$\frac{de_{\mathrm{c,pa}}}{dt} = p_{\mathrm{pa}} - p_{\mathrm{T,pa}}. \tag{7}$$

Substituting (3) and (4) into (7) yields

$$\begin{aligned} e_{\mathrm{c,pa}}(\omega t) = E_{\mathrm{c},0} + (1-\lambda_{\mathrm{r}})/\omega \cdot \{&U_0 I_{\mathrm{vm}} \sin(\omega t - \varphi_i)/2 \\ &- U_{\mathrm{m}} I_{\mathrm{dc}} \sin(\omega t - \varphi_u)/3 \\ &- U_{\mathrm{m}} I_{\mathrm{vm}} \sin(2\omega t - \varphi_u - \varphi_i)/4\} \end{aligned} \tag{8}$$

where the dc component $E_{\mathrm{c},0}$ can be calculated using the dc-components of the dc-link voltage as $E_{\mathrm{c},0} = 0.5N{\cdot}C_{\mathrm{sm}}{\cdot}V_{c,0}^2$.

Then, the dc-link voltage in arm pa can be expressed by

$$v_{\mathrm{c,pa}}(\omega t) = \sqrt{\frac{2e_{\mathrm{c,pa}}(\omega t)}{N \cdot C_{\mathrm{sm}}}}. \tag{9}$$

Furthermore, the voltage ripple factor is defined as follows:

$$\begin{cases} V_{\mathrm{c,max}} = \max\left[v_{\mathrm{c,pa}}(\omega t)\right], & \omega \in [0, 2\pi) \\ V_{\mathrm{c,min}} = \min\left[v_{\mathrm{c,pa}}(\omega t)\right], & \omega \in [0, 2\pi) \\ \delta_{\mathrm{v}} = \frac{V_{\mathrm{c,max}} - V_{\mathrm{c,min}}}{2} / V_{\mathrm{c},0}. \end{cases} \tag{10}$$

Combining (8)–(10), Fig. 3 illustrates the variation of δ_{v} with λ_{r} under different capacitances. As indicated, δ_{v} decreases with the increase of λ_{r}. Once C_{sm} is fixed, the value of λ_{r} required to meet the predetermined δ_{v} can be uniquely identified.

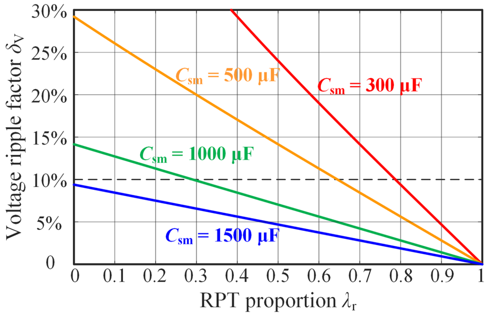
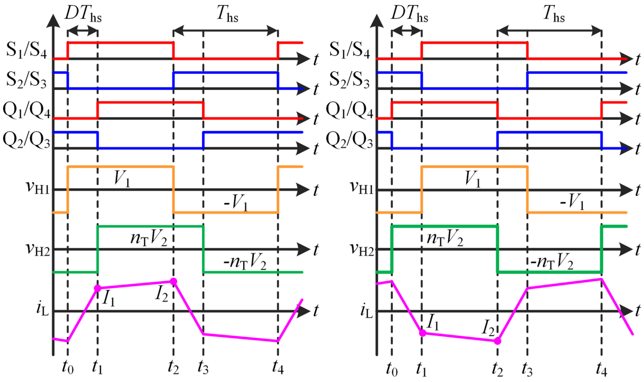


Fig. 3. Variation of the voltage ripple factor with the RPT proportion.



(a) (b)

Fig. 4. Steady-state waveforms of the DAB. (a) $P_{\mathrm{T}} > 0$. (b) $P_{\mathrm{T}} < 0$.

Afterward, the steady-state expressions for the primary-side voltage and transmission power of the DAB can be obtained by substituting λ_{r} into (4), (8), and (9).

Regarding the calculation of the internal electrical quantities of the DAB, the steady-state waveforms of the DAB for both positive ($P_{\mathrm{T}} > 0$) and negative ($P_{\mathrm{T}} < 0$) transmission power are illustrated in Fig. 4, where T_{hs} represents half of the switching period. Additionally, I_1 and I_2 denote the inductor current at time t_1 and t_2 and can be expressed by the following [26]:

$$\begin{cases} I_2 = \frac{(V_1 + n_{\mathrm{T}} V_2) D}{4 f_{\mathrm{sw}} L_{\mathrm{p}}} + \frac{(V_1 - n_{\mathrm{T}} V_2)(1 - |D|)}{4 f_{\mathrm{sw}} L_{\mathrm{p}}} \\ I_1 = -I_2 + \frac{(V_1 + n_{\mathrm{T}} V_2) D}{2 f_{\mathrm{sw}} L_{\mathrm{p}}}. \end{cases} \tag{11}$$

Then, according to Fig. 4, the steady-state expression of i_{L} within a switching period can be expressed as follows:

$$i_{\mathrm{L}} = \begin{cases} -I_2 + \frac{V_1 + nV_2}{L_{\mathrm{p}}} t, & 0 < t \leq DT_{\mathrm{hs}} \\ I_1 + \frac{V_1 - nV_2}{L_{\mathrm{p}}}(t - DT_{\mathrm{hs}}), & DT_{\mathrm{hs}} < t \leq T_{\mathrm{hs}} \\ I_2 + \frac{-V_1 - nV_2}{L_{\mathrm{p}}}(t - T_{\mathrm{hs}}), & T_{\mathrm{hs}} < t \leq (1+D)T_{\mathrm{hs}} \\ -I_1 + \frac{-V_1 + nV_2}{L_{\mathrm{p}}}(t - (1+D)T_{\mathrm{hs}}), & (1+D)T_{\mathrm{hs}} < t \leq 2T_{\mathrm{hs}}. \end{cases} \tag{12}$$

Additionally, the MOSFET current (taking S_1 as an example) can be expressed as follows:

$$i_{\mathrm{S}_1} = \begin{cases} i_{\mathrm{L}}, & 0 < t \leq T_{\mathrm{hs}} \\ 0, & T_{\mathrm{hs}} < t \leq 2T_{\mathrm{hs}} \end{cases}. \tag{13}$$

TABLE I
SWITCHING LOSSES OF THE PRIMARY-SIDE MOSFETS

Transmission power	Switching current	Turn-on loss	Turn-off loss	Reverse recovery loss
$P_T > 0$	$I_2 > 0$	0	$E_{off}(V_1, I_2)$	0
	$I_2 < 0$	$E_{on}(V_1, -I_2)$	0	$E_{rr}(V_1, -I_2)$
$P_T < 0$	$I_1 > 0$	$E_{on}(V_1, I_1)$	0	$E_{rr}(V_1, I_1)$
	$I_1 < 0$	0	$E_{off}(V_1, -I_1)$	0

B. Estimation of Losses in MOSFETs

To ensure the junction temperature of MOSFETs (T_j) below their maximum allowable temperature with an adequate safety margin, this study sets the upper limit for T_j at 125 °C. All MOSFET losses are estimated at this temperature to consider the worst case.

When the drive voltage adheres to the datasheet recommendations and T_j is set at 125 °C, the conduction loss depends solely on the conduction current. From the MOSFET manufacturer's datasheet or PLECS (a software developed for system-level simulations of power electronics) model, the voltage drops (V_{con}) for each conduction currents (I_{con}) can be derived. The conduction loss is then estimated by (14), with I_{con} determined by (12) and (13)

$$P_{con}(I_{con}) = I_{con} \cdot V_{con}(I_{con}). \tag{14}$$

Notably, the diode conduction loss is negligible since only during a small part of dead time will i_L flows through the body diodes [14].

Regarding the estimation of switching losses, numerous studies have developed analytical models [27], [28], where the waveforms of MOSFET voltage and current during the switching process are derived in segments. However, these models are time-consuming and often fail to ensure accuracy, making them less favored by the MOO. Inspired by the loss simulation in PLECS, this article proposes a lookup-table method to estimate the switching losses in the DAB.

When the drive voltage and resistance adhere to the datasheet recommendations and T_j is set at 125 °C, the switching losses are determined solely by the turn-ON current (I_{on}) and turn-OFF voltage (V_{off}). From the manufacturer's PLECS model, the turn-ON energy (E_{on}), turn-OFF energy (E_{off}), and reverse recovery energy (E_{rr}) for each combination of I_{on} and V_{off} can be obtained. By performing two-dimensional interpolation on these data, three-dimensional tables correlating I_{on}, V_{off}, and switching energies can be created. To calculate the switching energies for a specific switching period of the DAB, it is simply necessary to look up these tables based on the turn-ON current and turn-OFF voltage of that period. Table I summarizes the switching losses of the MOSFETs in the DAB during one switching period, using S_1 as an example. Here, V_1 is calculated by (8) and (9), while I_1 and I_2 are determined by (6) and (11).

From the above calculations, it is evident that with the knowledge of the primary-side voltage V_1, secondary-side voltage V_2, and transmission power P_T, all MOSFET losses within a single switching period of the DAB can be calculated. In the MMC-based PET, the waveforms of V_1 and P_T include fundamental-frequency and second-harmonic components in addition to dc components, leading to fluctuations in MOSFET losses. From the perspective of efficiency optimization, it is essential to consider the time-average loss, $P_{MOS,\ avg}$. To accomplish this, the fundamental-frequency period can be subdivided into multiple equal segments corresponding to the switching period, enabling the calculation of MOSFET losses in each period to determine the time-average value.

TABLE II
SIMULATION AND ESTIMATED RESULTS OF MOSFET LOSSES

	Simulation (W)	Estimation (W)	Error (%)
Conduction loss	17.1663	17.1316	0.20
Turn-on loss	1.0088	0.9990	0.97
Turn-off loss	5.8816	5.8770	0.08
Reverse recovery loss	0.4947	0.4842	2.12
Total loss	24.5514	24.4918	0.23

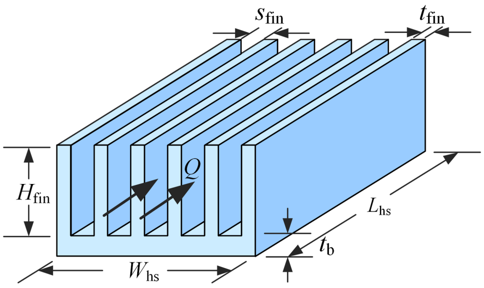


Fig. 5. Schematic of the plate-fin heatsink.

To validate the accuracy of the established models for MOSFET losses in the DAB, loss simulations are conducted in PLECS. The circuit parameters of the PET used in the simulations can be found in Sections IV-A and VI-B. An SiC MOSFET (NTH028N170M1, 1.7 kV, Onsemi) is adopted for the simulations. Table II presents the simulation and estimated losses of MOSFET S_1, demonstrating their good consistency.

C. Estimation of the Heatsink Volume

The plate-fin heatsink, featuring a parallel, uniform array of thin conductive plates mounted on a rectangular baseplate, is the predominant solution for enhancing the cooling of power electronic devices. Fig. 5 depicts the geometrical shape of the plate-fin heatsink, detailing its width (W_{hs}) and length (L_{hs}), the thickness (t_b) of the baseplate, the height (H_{fin}) and thickness (t_{fin}) of the fins, and the spacing (s_{fin}) between fins.

The required volume of the heatsinks for MOSFETs is positively correlated with their thermal resistance. According to thermal Ohm's law, the temperature rise from ambient to the MOSFET junction is given by the following:

$$T_j - T_a = P_{MOS,avg} \cdot (R_{th,jc} + R_{th,TIM} + R_{th,hs}) \tag{15}$$

where $R_{th,jc}$ is the junction-to-case thermal resistance from the datasheet, and $R_{th,TIM}$ denotes the thermal resistance of the thermal interface material. The required thermal resistance of the heatsink is then determined by

$$R_{th,hs} <= \frac{T_{j,max} - T_{a,max}}{P_{MOS,avg}} - R_{th,jc} - R_{th,TIM}. \tag{16}$$

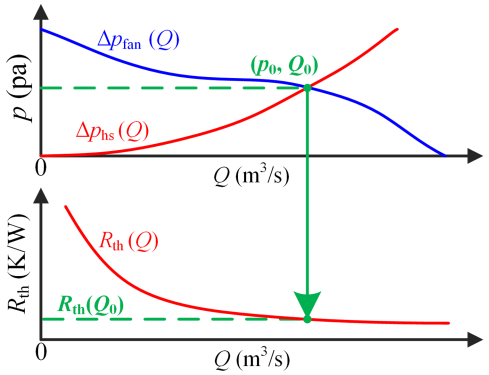


Fig. 6. Illustration of the procedure for determining the thermal resistance of a heatsink.

Both the volume and thermal resistance of a heatsink are determined by its dimensions. Given this, the optimal heatsink dimensions that achieve the minimum volume under each thermal resistance constraint can be identified. This establishes a one-to-one correspondence between the thermal resistance and the volume of the heatsink. In the MOO program, therefore, the heatsink volume can be derived by looking up tables according to the required thermal resistance from (16). Clearly, estimating the volume of the heatsink hinges on developing a model that relates its thermal resistance to dimensions.

Fig. 6 illustrates the procedure for determining the thermal resistance of a heatsink. In this figure, $\Delta p_{\mathrm{fan}}(Q)$ is the fan performance curve, indicating the relationship between the airflow rate through the fan and the resultant pressure rise; $\Delta p_{\mathrm{hs}}(Q)$ depicts the resistance curve of the heatsink, reflecting the pressure drop through the heatsink as a function of the airflow rate. With fixed dimensions, the heatsink's thermal resistance, R_{th}, directly correlates with Q, as shown in the lower subplot of Fig. 6. The intersection of $\Delta p_{\mathrm{fan}}(Q)$ and $\Delta p_{\mathrm{hs}}(Q)$ identifies the operating point of the fan (p_0, Q_0), thus determining the airflow rate through the heatsink and the specific thermal resistance $R_{\mathrm{th}}(Q_0)$.

In the aforementioned curves, $\Delta p_{\mathrm{fan}}(Q)$ can be obtained from the fan's datasheet, whereas the other two curves are both functions of heatsink dimensions. Thus, determining the heatsink's thermal resistance by its dimensions requires modeling the pressure drop and thermal resistance related to the airflow rate. These models are detailed in the Appendix.

To validate the accuracy of these models, finite element simulations are conducted in Ansys Icepak, a software for thermal simulations of electronic systems. The simulations use a Sanyo Denki fan (part number: 109P0412K3023) and heatsink dimensions specified as $W_{\mathrm{hs}} = 40$ mm, $H_{\mathrm{fin}} = 40$ mm, $L_{\mathrm{hs}} = 100$ mm, $t_{\mathrm{b}} = 3$ mm, $t_{\mathrm{fin}} = 1$mm, and $N_{\mathrm{f}} = 11$.

First, to confirm the accuracy of the convection resistance estimation, the heat source area is matched to the baseplate, resulting in zero spreading resistance. As evident in Fig. 7(a), the estimated results agree well with the simulated results, demonstrating high accuracy. Furthermore, the heat source area was reduced to 20 mm × 10 mm. Fig. 7(b) confirms that the spreading resistance estimation is also highly accurate.

Additionally, Fig. 7(c) displays the results for heatsink pressure drop. At lower flow rates, the estimated results closely match the simulations, whereas they are slightly above the simulations at higher flow rates. As indicated by Fig. 6, this deviation will lead to a conservative estimate of thermal resistance, thereby increasing the safety margin for the MOSFETs.

D. Estimation of Core Losses in Magnetic Components

Regarding the core geometry, EE cores are widely used in high-frequency transformers due to their modularity and availability in a wide range of sizes. Therefore, this core geometry is considered in this study. As illustrated in Fig. 8, such cores are characterized by six dimensions: core width W_{core}, core height H_{core}, core thickness t_{core}, window width W_{win}, window height H_{win}, and center leg width W_{leg}. Additionally, A_{c} and A_{w} represent the cross-sectional areas of the core and window, respectively.

The widely recognized method for estimating core losses is the Steinmetz equation (SE), in which the core loss density is calculated by

$$P_{\mathrm{V}} = k_{\mathrm{SE}} \cdot f^{\alpha} \cdot B_{\mathrm{m}}^{\beta}. \tag{17}$$

Here, f is the excitation frequency, B_{m} is the flux density amplitude, and k_{SE}, α, and β are material-dependent parameters. Given that (17) is only valid for sinusoidal excitations, several models have been developed to estimate core losses under arbitrary excitations. These models include the modified SE (MSE) [29], the generalized SE (GSE) [30], the improved GSE (iGSE) [31], and the further improved GSE (i^{2}GSE) [32], each enhancing the accuracy of its previous one. Among these, the iGSE offers a satisfactory tradeoff between simplicity and accuracy and is therefore adopted in this study.

The formula of the iGSE is given by the following [31]:

$$P_{\mathrm{V}} = \frac{k_{\mathrm{iGSE}}|\Delta B|^{\beta-\alpha}}{T} \int_{T} \left| \frac{dB(t)}{dt} \right|^{\alpha} dt \tag{18}$$

$$k_{\mathrm{iGSE}} = \frac{k_{\mathrm{SE}}}{(2\pi)^{\alpha-1} \int_{0}^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{19}$$

where T is the period of the excitation, $B(t)$ is the instantaneous flux density, and ΔB is the peak-to-peak value of $B(t)$.

For the DAB transformer, as shown in Fig. 4, the excitation voltage is rectangular, and $B(t)$ can be expressed as follows:

$$B_{\mathrm{T}}(t) = \frac{2B_{\mathrm{m,T}}}{T_{\mathrm{hs}}} t, \quad 0 \le t \le T_{\mathrm{hs}} \tag{20}$$

$$B_{\mathrm{m,T}} = \frac{V_2}{4N_{\mathrm{w,T}} f_{\mathrm{sw}} A_{\mathrm{c,T}}} \tag{21}$$

where $N_{\mathrm{w,T}}$ is the turn number of the transformer winding. Substituting (20) and (21) into (18) yields

$$P_{\mathrm{V,T}} = 2^{\alpha+\beta} k_{\mathrm{iGSE}} f_{\mathrm{sw}}^{\alpha} B_{\mathrm{m,T}}^{\beta}. \tag{22}$$

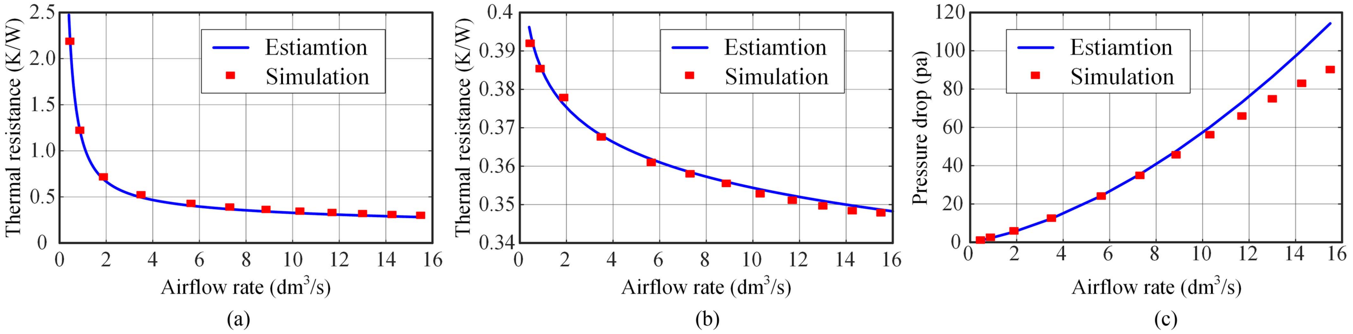


Fig. 7. Comparisons of estimated and simulations results for heat sink thermal resistance and pressure drop. (a) Thermal resistance versus airflow rate when spreading resistance is not considered. (b) Spreading resistance versus airflow rate. (c) Pressure drop versus airflow rate.

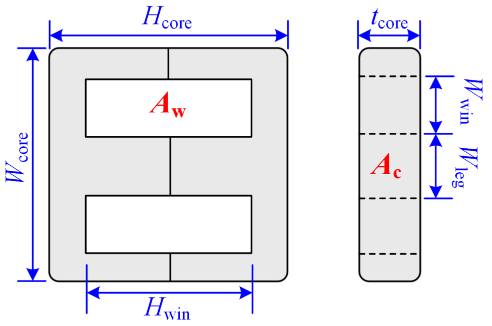


Fig. 8. Geometry and dimensions of EE cores.

As for the DAB inductor, the waveform of its flux density is the same as its excitation current i_L, accordingly

$$\frac{dB_L(t)}{dt} = \begin{cases} \frac{(B_1+B_2)}{DT_{hs}}, & 0 \le t < DT_{hs} \\ \frac{(B_2-B_1)}{(1-D)T_{hs}}, & DT_{hs} \le t < T_{hs} \end{cases} \tag{23}$$

$$B_1 = \frac{L_p \cdot I_1}{N_{w,L}A_{c,L}}, B_2 = \frac{L_p \cdot I_2}{N_{w,L}A_{c,L}} \tag{24}$$

where $N_{w,L}$ is the turn number of the inductor winding. Substituting (23) into (18) yields

$$P_{V,L} = 2^{\beta} k_{iGSE} f_{sw}^{\alpha} B_{m,L}^{\beta-\alpha} \Big[|B_1 + B_2|^{\alpha} D^{1-\alpha} + |B_1 - B_2|^{\alpha} (1-D)^{1-\alpha} \Big]. \tag{25}$$

Notably, if the core loss of the transformer or inductor is estimated by simply multiplying the core loss density obtained in (22) and (25) by the core volume, considerable error will arise due to the nonuniform flux density distribution in EE cores. Accordingly, this article proposes a correction method based on region division to compensate for this error. As illustrated in Fig. 9, the EE cores are divided into a center leg, two outer legs, four return legs, and several low-flux regions, according to the flux density distribution. Core losses for different legs are then estimated separately using the flux density calculated from their respective cross-sectional areas. Additionally, the flux density in each low-flux region is approximated as half of that in its adjacent region.

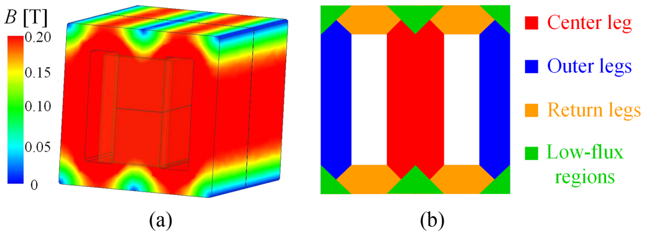


Fig. 9. Illustration of the region division for the EE cores according to flux density distribution. (a) Distribution of the flux density in the EE cores. (b) Different regions divided according to the flux density distribution.

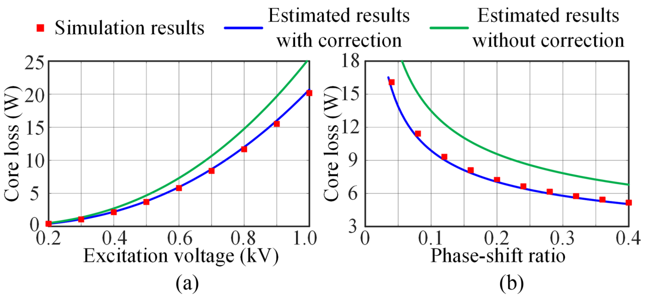


Fig. 10. Comparisons of simulated and estimated core losses. (a) Transformer core loss versus the excitation voltage amplitude. (b) Inductor core loss versus the phase-shift ratio.

To verify the accuracy of these core loss models, finite element simulations are conducted in Ansys Maxwell, a software for electromagnetic field simulations. The core dimensions, switching frequency, and winding turns used in the simulations can be found in Section VI-B. In addition, the amplitude of the transformer's rectangular excitation voltage ranges from 200 to 1000 V, I_1 and I_2 are both set to 50 A, and D varies from 0.04 to 0.4. The simulated and estimated core losses for the transformer and inductor are illustrated in Fig. 10(a) and (b), respectively. Evidently, the corrected estimated results exhibit good consistency with the simulations, whereas those without correction present considerable error.

E. Estimation of Winding Losses in Magnetic Components

Litz wires, composed of multiple enameled strands, are preferred for winding cores in high-frequency applications due to their ability to mitigate copper losses caused by skin and proximity effects. The total winding loss in a Litz-wired transformer or inductor can be expressed as follows:

$$P_{\mathrm{w}} = \sum_{i=1}^{n_{\max}} F_{\mathrm{r},i} \cdot R_{\mathrm{dc}} \cdot I_{\mathrm{rms},i}^{2} \tag{26}$$

where $F_{\mathrm{r},i}$ is the ac-to-dc winding resistance ratio for the ith harmonic, $n_{\max}$ is the maximum harmonic order considered, R_{dc} is the dc resistance of the winding, and $I_{\mathrm{rms},i}$ denotes the root-mean-square (RMS) value of the nth-order harmonic current.

The dc resistance of a Litz-wire winding is determined by

$$R_{\mathrm{dc}} = \mathrm{MLT} \cdot N_{\mathrm{w}} \cdot \varepsilon_0 \cdot \frac{1}{\sigma \cdot N_0 \cdot \pi d_0^2/4} \tag{27}$$

where d_0 represents the diameter of a single bare strand, N_0 accounts for the number of strands in a Litz wire, σ is the electrical conductivity, ε_0 is the twisting length factor of the Litz wire indicating the elongation of a single strand due to twisting, and MLT represents the mean length turn of the winding, approximated as (28) for the EE cores [33]

$$\mathrm{MLT} \approx 2W_{\mathrm{leg}} + 2t_{\mathrm{core}} + 2.82W_{\mathrm{win}}. \tag{28}$$

Regarding the calculation of $F_{\mathrm{r,n}}$, Tourkhani's formula [34] developed for Litz wires is widely acknowledged. First, the skin depth is determined by

$$\delta = 1/\sqrt{\pi \cdot \sigma \cdot \mu \cdot f} \tag{29}$$

where μ represents the magnetic permeability, and f denotes the frequency of the winding current. Subsequently, the winding resistance ratio is given by

$$F_{\mathrm{r}} = \frac{\zeta}{2\sqrt{2}} \left[\psi_1(\zeta) - \frac{\pi^2 N_0 \beta_{\mathrm{w}}}{24} \left(16m_{\mathrm{w}}^2 - 1 + \frac{24}{\pi^2} \right) \psi_2(\zeta) \right] \tag{30}$$

where β_{w} denotes the winding packing factor defined as the copper-to-winding ratio, m_{w} indicates the layer number, and $\zeta = d_0/\delta$. $\psi_1(\zeta)$ and $\psi_2(\zeta)$ are combinations of Bessel functions and can be approximated by the first terms of their Taylor expansion, as shown in the following:

$$\begin{cases} \psi_1(\zeta) \approx 2\sqrt{2} \left(\frac{1}{\zeta} + \frac{1}{3 \cdot 2^8}\zeta^3 - \frac{1}{3 \cdot 2^{14}}\zeta^5 \right) \\ \psi_2(\zeta) \approx \frac{1}{\sqrt{2}} \left(-\frac{1}{2^5}\zeta^3 + \frac{1}{2^{12}}\zeta^7 \right). \end{cases} \tag{31}$$

Additionally, in (30), β_{w} is determined by

$$\beta_{\mathrm{w}} = \beta_0 \cdot \frac{N_{\mathrm{w}} \cdot \pi {d_{\mathrm{w}}}^2/4}{[m_{\mathrm{w}} \cdot d_{\mathrm{w}} + (m_{\mathrm{w}} - 1) \cdot \Delta d] \cdot [n_{\mathrm{w}} \cdot d_{\mathrm{w}} + (n_{\mathrm{w}} - 1) \cdot \Delta d]} \tag{32}$$

where β_0 is the fill factor of the Litz wire typically ranging from 0.5 to 0.6, d_{w} is the diameter of the Litz wire, n_{w} is the number of turns per layer, and Δd is the distance between wires.

When calculating F_{r} for the inductor, use half of the winding for the calculation since the position with zero magnetic field is located in the middle of the winding. More specifically, both m_{w} and N_{w} should be halved before being substituted into (30) and (32). Moreover, m_{w} needs to be rounded up if it is not an integer. As for the DAB transformer, calculate the winding loss of each layer separately by substituting m_{w} with 1, assuming the primary and secondary windings are interleaved to mitigate proximity effects [33], [35].

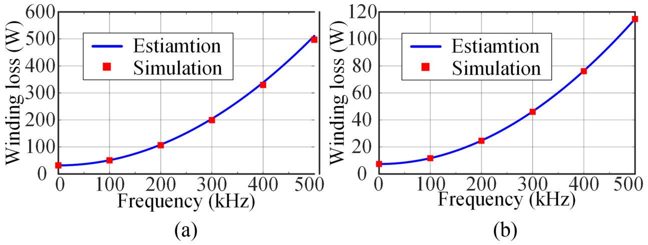


Fig. 11. Comparisons of simulated and estimated winding losses. (a) Transformer winding loss versus the frequency. (b) Inductor winding loss versus the frequency.

TABLE III
PARAMETERS OF THE MMC-BASED PET

Parameter		Symbol	Value
Port voltage	MVDC	V_{MVDC}	10 kV
	MVAC	V_{MVAC}	5 kV
	LVDC	V_{LVDC}	1 kV
Port power	MVDC	P_{MVDC}	2.5 MW
	MVAC	P_{MVAC}	1.75 MW
	LVDC	P_{LVDC}	0.75 MW
MMC	Number of HBs per arm	N	10
	Arm inductance	L_{arm}	1 mH
	Switching frequency	f_{MMC}	2 kHz
DC-link	DC voltage	V_{c0}	1 kV
	Voltage ripple factor	δ_{v}	10%
	Submodule capacitance	C_{sm}	**Undetermined**
DAB	Transformer turn ratio	n_{T}	1:1
	Switching frequency	f_{sw}	**Undetermined**
	Auxiliary inductance	L_{p}	**Undetermined**
	Secondary-side capacitance	C_{s}	32 μF

To verify the accuracy of the winding loss model, finite element simulations are conducted in Ansys Maxwell. The RMS winding current is set to 30 A. The winding parameters of the transformer are: $d_0 = 0.1$, $N_0 = 450$, $\varepsilon_0 = 1.1$, $\beta_0 = 0.5$, $d_{\mathrm{w}} = 2.98$ mm, $m_{\mathrm{w}} = 2$, $n_{\mathrm{w}} = 10$, $\Delta d = 0.05$ mm, and MLT = 81 mm, while those of the inductor are set as: $d_0 = 0.1$, $N_0 = 300$, $\varepsilon_0 = 1.1$, $\beta_0 = 0.5$, $d_{\mathrm{w}} = 2.98$ mm, $m_{\mathrm{w}} = 2.5$, $n_{\mathrm{w}} = 8$, $\Delta d = 0.08$ mm, and MLT = 50 mm. The simulated and estimated winding losses for the transformer and inductor, illustrated in Fig. 11(a) and (b), respectively, demonstrate high estimation accuracy.

IV. ESTABLISHMENT OF THE MOO PROGRAM FOR THE PET OPERATING IN THE RPT MODE

A. Overview

In later sections, the MOO for the MMC-based PET will be discussed to explore the design principles of this topology. This discussion is exemplified by a PET used in a ship power supply system, originating from a research project involving the authors. The parameters are listed in Table III. The input port interfaces with a 10-kV/2.5-MW MVDC bus, while the output ports connect to a 5-kV/1.75-MW MVAC bus and a

1-kV/0.75-MW LVDC bus. The dc-link voltage equals 1 kV, calculated by V_{MVDC}/N. The transformer turn ratio of the DAB is configured as $V_{\mathrm{c0}}/V_{\mathrm{LVDC}} = 1{:}1$ to match its input and output voltages.

In Table III, the parameters that belong solely to the MMC, including the number of HBs per arm, arm inductance, and switching frequency, are predetermined in the MOO program. On one hand, this article focuses on the impact of RPT on the design and optimization of the MMC-based PET; however, the design of these parameters has little relevance to RPT. On the other hand, their design is relatively mature [15], [16], [17], and delving into their design would detract from the main focus.

In contrast, parameters including the submodule capacitance, the DAB's switching frequency and auxiliary inductance are closely related to RPT and thus remain to be determined in the MOO program. Meanwhile, only the volumes and losses of the submodule capacitor and DAB within the submodule in Fig. 1(b) need to be considered in the MOO program of this study.

B. Definition of Objective Functions

The primary performance indicators for PETs are typically efficiency and power density. However, instead of directly optimizing them, we simplify calculations by using the sum of losses (P_Σ) to represent efficiency and the sum of volumes (V_Σ) to represent power density.

Notably, those loss and volume components that are unrelated to RPT and do not vary with decision variables, such as auxiliary circuit losses and insulation space, are excluded from the objective functions for simplicity as they do not affect optimization results. Additionally, components with minimal contributions to total loss/volume, like the diode conduction loss, capacitor losses, and the volume of the DAB output capacitors, are also excluded for simplicity since they have little impact on optimization results.

Consequently, P_Σ is given by the following:

$$P_{\sum} = 8 \cdot P_{\mathrm{MOS,\,avg}} + P_{\mathrm{c,T}} + P_{\mathrm{c,L}} + P_{\mathrm{w,T}} + P_{\mathrm{w,L}} \tag{33}$$

where the average power loss of MOSFETs ($P_{\mathrm{MOS,avg}}$) is estimated by the models in Section III-B, the core losses ($P_{\mathrm{c,T}}$ and $P_{\mathrm{c,L}}$) are estimated by the models in Section III-D, and the winding losses ($P_{\mathrm{w,T}}$ and $P_{\mathrm{w,L}}$) are estimated by the models in Section III-E.

Furthermore, V_Σ can be expressed as follows:

$$V_{\sum} = V_{\mathrm{hs}} + V_{\mathrm{T}} + V_{\mathrm{L}} + V_{\mathrm{cap}} \tag{34}$$

where the volume of heatsinks (V_{hs}) is estimated by the models in Section III-C and the Appendix. The volumes of the DAB transformer and inductor, comprising both core and winding parts, are estimated based on the dimensions in Fig. 8 as follows [35]:

$$V_{\mathrm{T}} \text{ or } V_{\mathrm{L}} = W_{\mathrm{core}} \cdot H_{\mathrm{core}} \cdot t_{\mathrm{core}} + 2W_{\mathrm{core}} \cdot H_{\mathrm{core}} \cdot W_{\mathrm{win}} \tag{35}$$

where the first term on the right side represents the core volume, and the second term represents the volume of windings.

Regarding the estimation of the capacitor volume, metalized poly-propylene film (MPPF) capacitors are preferred for the dc link in PETs due to their high voltage and current tolerance, long lifetime, low equivalent series impedance, and self-healing properties. For a PET with a 1-kV dc link, a 1200-V MPPF capacitor is appropriate. The volume-to-capacitance ratio for commercially available MPPF capacitors at this voltage is around 2 cm^3/μF, allowing for an estimation of V_{cap} by

$$V_{\mathrm{cap}} = 2\mathrm{cm}^3/\mu\mathrm{F} \cdot C_{\mathrm{sm}}. \tag{36}$$

C. Determination of Constraints

First, the temperature rise of the heatsink must be greater than zero to ensure that a suitable heatsink is available to keep $T_{\mathrm{j}} \leq T_{\mathrm{j,max}}$. Accordingly

$$\Delta T_{\mathrm{hs}} = T_{\mathrm{j,max}} - T_{\mathrm{a,max}} - P_{\mathrm{MOS,avg}} \cdot (R_{\mathrm{th,jc}} + R_{\mathrm{TIM}}) > 0. \tag{37}$$

Second, the maximum flux density of the DAB transformer and inductor must be constrained to avoid saturation, i.e.

$$B_{\mathrm{m,T}} = \frac{V_2}{4N_{w,\mathrm{T}} f_{\mathrm{sw}} A_{\mathrm{c,T}}} \leq B_{\max} \tag{38}$$

$$B_{\mathrm{m,L}} = \frac{L_{\mathrm{p}} \cdot I_{\mathrm{L,max}}}{N_{\mathrm{w,L}} A_{\mathrm{c,L}}} \leq B_{\max}. \tag{39}$$

The Mn-Zn ferrite PC95 from TDK, selected as the core material in this study due to its low core loss density, demonstrates a saturation flux density of 0.41 T at 100 °C. Consequently, $B_{\max}$ is set as 0.3 T to maintain a safe margin.

Thirdly, the limited window area constrains the winding fill factor, as delineated in (40) and (41). For the DAB transformer, $k_{\mathrm{cT,max}}$ is empirically set as 0.6 [33]. For the DAB inductor, air gaps can cause fringing fields, leading to increased winding losses [36]. Consequently, $k_{\mathrm{cL,max}}$ is further restricted to 0.3 in this study so as to position the windings away from air gaps

$$k_{\mathrm{c,T}} = \frac{2N_{\mathrm{w,T}} \cdot \pi \cdot d_{\mathrm{w,T}}^2/4}{A_{\mathrm{w,T}}} \leq k_{\mathrm{cT,max}} \tag{40}$$

$$k_{\mathrm{c,L}} = \frac{N_{\mathrm{w,L}} \cdot \pi \cdot d_{\mathrm{w,L}}^2/4}{A_{\mathrm{w,L}}} \leq k_{\mathrm{cL,max}}. \tag{41}$$

D. Selection of Decision Variables

Considering all the equations mentioned in preceding sections, the variables required to calculate the objective functions and constraints include global parameters (λ_{r}, C_{sm}, f_{sw}, L_{p}), core dimensions, and winding parameters.

1) Global Parameters: As indicated by Fig. 3, once C_{sm} is determined, λ_{r} can be uniquely identified to meet the predetermined voltage ripple factor. Therefore, λ_{r} is regarded as an intermediate variable rather than a decision variable.

The per-unit value of L_{p} is chosen as a decision variable instead of L_{p} directly due to its closely related value range with other decision variables. First, the maximum transmission power-to-input voltage ratio for the DAB is calculated by

$$r_{\mathrm{pv}} = \max\left\{\left|\frac{p_{\mathrm{T,pa}}(\omega t)}{N \cdot V_{\mathrm{c,pa}}(\omega t)}\right|\right\}, \quad \omega t \in [0, 2\pi). \tag{42}$$

TABLE IV
DECISION VARIABLES SELECTED FOR THE MULTIOBJECTIVE OPTIMIZATION

Symbol	Meaning	Symbol	Meaning
C_{sm}	Submodule capacitance	$d_{\mathrm{w,T}}$	Transformer wire diameter
f_{sw}	Switching frequency	$W_{\mathrm{core,L}}$	Inductor core width
$L_{\mathrm{p}}^{\mathrm{pu}}$	Per-unit inductance	$t_{\mathrm{core,L}}$	Inductor core thickness
$W_{\mathrm{core,T}}$	Transformer core width	$m_{\mathrm{w,L}}$	Inductor winding layers
$t_{\mathrm{core,T}}$	Transformer core thickness	$n_{\mathrm{w,L}}$	Winding turns per layer
$N_{\mathrm{w,T}}$	Transformer winding turns	$d_{\mathrm{w,L}}$	Inductor wire diameter

Then, the maximum value of L_{p} is determined by (43), yielding the per-unit value $L_{\mathrm{p}}^{\mathrm{pu}} = L_{\mathrm{p}}/L_{\mathrm{p,max}}$

$$L_{\mathrm{p}} \leq L_{\mathrm{p,max}} = \frac{V_2 \cdot D_{\mathrm{max}}(1 - D_{\mathrm{max}})}{r_{\mathrm{pv}} \cdot 2 f_{\mathrm{sw}}}. \tag{43}$$

2) Core Dimensions: Among the core dimensions shown in Fig. 8, W_{core} indicates the part number of the core, while the other dimensions except t_{core} are linearly related to W_{core} according to the homothetic law [37]. Based on manufacturers' datasheets, these dimensions can be approximated as follows:

$$\begin{cases} H_{\mathrm{core}} \approx 1.0629 \cdot W_{\mathrm{core}} - 3.9842 \\ W_{\mathrm{lag}} \approx 0.3119 \cdot W_{\mathrm{core}} - 1.2538 \\ H_{\mathrm{win}} \approx 0.7638 \cdot W_{\mathrm{core}} - 3.5180 \\ W_{\mathrm{win}} \approx 0.1885 \cdot W_{\mathrm{core}} + 0.8449 \end{cases} \tag{44}$$

with all measurements in millimeters.

In contrast, t_{core} depends on both the thickness of a single core and the number of cores. Additionally, multiple thickness options may exist for a same core width. t_{core} is therefore considered as an independent decision variable in the MOO program. Thus, assigning two decision variables (W_{core} and t_{core}) for the core dimensions is sufficient.

3) Winding Parameters: Regarding the winding turns, as explained in Section III-E, the winding loss calculation for the inductor requires both $m_{\mathrm{w,L}}$ and $n_{\mathrm{w,L}}$, necessitating two decision variables assigned. For the transformer, nevertheless, only $N_{\mathrm{w,T}}$ is needed.

Among the Litz wire parameters (ε_0, d_0, N_0, β_0, and d_{w}), ε_0 and β_0 are usually constant for a fixed series of Litz wires, and d_0 is recommended to be 0.1 mm for the frequency range of 20–100 kHz. Additionally, the above parameters have the following dependence according to the area equivalence principle:

$$\frac{\pi}{4} d_{\mathrm{w}}^2 \cdot \beta_0 = N_0 \cdot \frac{\pi}{4} d_0^2. \tag{45}$$

Thus, it is sufficient to assign only one of these parameters, N_0 or d_{w}, as an independent decision variable in the MOO program. In this study, the diameters of Litz wires, $d_{\mathrm{w,T}}$ and $d_{\mathrm{w,L}}$, are selected as decision variables.

Table IV summaries the decision variables selected for the MOO. All the objective functions and constraints can be calculated once these decision variables are specified.

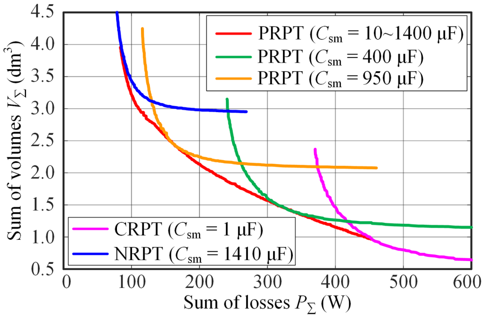


Fig. 12. Pareto front curves obtained from the MOO program.

V. ANALYSIS OF MOO RESULTS AND DISCUSSION ABOUT DESIGN PRINCIPLES

A. Overview of the Pareto-Optimal Solutions and Discussion of the Optimal Operation Mode

The nondominated sorting genetic algorithm II (NSGA-II) [38] is employed to solve the MOO problem described in Section IV. The resulting Pareto front curves are illustrated in Fig. 12, where the abscissa is the sum of losses representing efficiency, and the ordinate is the sum of volumes representing power density. Initially, with C_{sm} set to 1410 and 1 μF, the Pareto fronts for the NRPT and CRPT modes are obtained, respectively. Subsequently, C_{sm} is treated as a decision variable ranging from 10 to 1400 μF, resulting in the PRPT Pareto front. In particular, the Pareto fronts for the PRPT mode with C_{sm} fixed at 400 and 950 μF are also presented. A comparison of these curves reveals that the overall Pareto front of the MOO is composed of the PRPT curve and segments from the NRPT and CRPT curves. Moreover, the overall PRPT Pareto front acts as the envelope of the PRPT curves for fixed capacitances.

From Fig. 12, it is evident that the Pareto fronts obtained from the established MOO program intuitively illustrate the optimal designs of the PET. This enables designers to more flexibly balance efficiency and power density, thereby picking the most suitable design point according to practical needs.

Through comparison, it can be concluded that the RPT mode (including CRPT and PRPT modes) indeed reduces the sum of volumes relative to the NRPT mode, thereby helping to enhance the overall power density of the PET. Despite substantially reducing V_Σ, the CRPT mode also notably increases P_Σ, which inevitably leads to a low-efficiency design. In contrast, the proposed PRPT technology expands the optimization space and can strike a better balance between power density and efficiency. Thus, the PRPT-based design method is highly recommended when designing the MMC-based PET.

B. Discussion of the Optimal RPT Proportion and Submodule Capacitance

The variations of the optimal submodule capacitance and RPT proportion along the overall Pareto front are illustrated in Fig. 13, where the abscissa denotes the position on the Pareto front. Consistent with Section II, there is a one-to-one correspondence

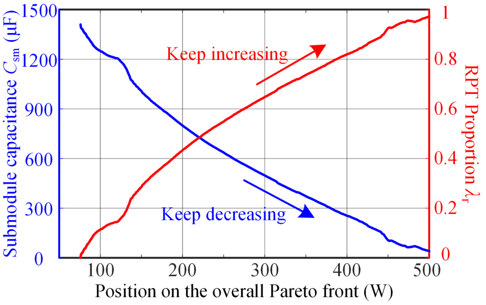


Fig. 13. Variations of the optimal submodule capacitance and RPT proportion along the overall Pareto front.

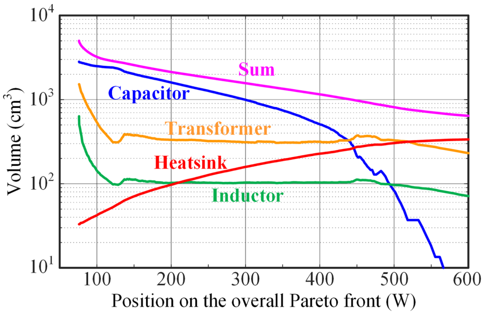


Fig. 14. Variations of component volumes along the overall Pareto front.

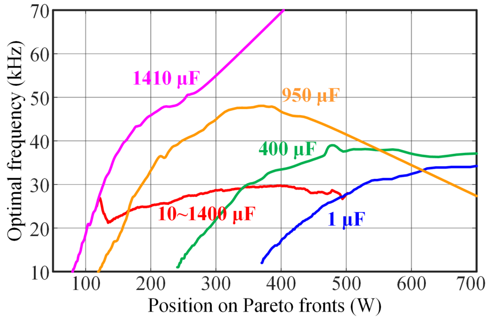


Fig. 15. Variations of optimal switching frequencies along Pareto fronts.

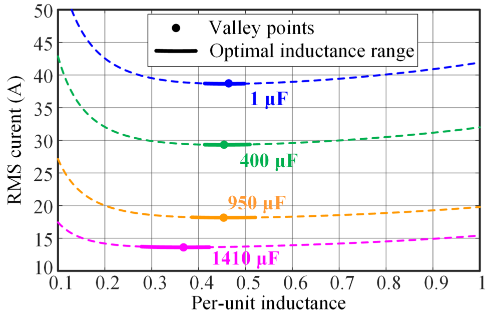


Fig. 16. Variations of the RMS inductor current with the per unit inductance.

between λ_r and the required C_{sm} when the capacitor voltage ripple factor is prespecified.

As stated in Section I, RPT can reduce the required capacitor size while increasing the transmission power of DABs. As a result, people may speculate that there exists a value of λ_r at which the total volume of the PET submodule is minimized. As evident in Fig. 13, however, the optimal λ_r keeps increasing along the overall Pareto front, indicating that the minimum V_Σ decreases monotonically with the increase of λ_r. To explore the reasons, Fig. 14 depicts the variations of the component volumes along the overall Pareto front. With the increase of λ_r, the submodule capacitor volume decreases while the heatsink volume increases. Overall, V_Σ exhibits a consistently declining trend since the capacitor volume is dominant. This is reasonable given the relatively low capacitance density of the MPPF capacitors that are most suitable for the dc link in PETs.

The observations from Figs. 12–14 indicates that the more ripple power transferred by DABs, the more beneficial it is for the overall power density. Therefore, λ_r can be regarded as the weight coefficient of power density. A larger λ_r as well as a smaller C_{sm} should be selected for higher power density. Conversely, if the efficiency is prioritized, a larger C_{sm} should be chosen to reduce λ_r. The Pareto front obtained from the MOO can help balance power density and efficiency when determining λ_r and C_{sm}.

C. Discussion of the Optimal Switching Frequency and Inductance of the DAB

The variations of the optimal switching frequencies derived from the Pareto-optimal solutions are depicted in Fig. 15, where all the curves correspond directly to those in Fig. 12. For both the NRPT mode ($C_{sm} = 1410\ \mu$F) and CRPT mode ($C_{sm} = 1\ \mu$F), high-power-density design requires higher f_{sw}, while high-efficiency design necessitates lower f_{sw}. This is because the rise in f_{sw} decreases the volume of magnetic components but increases the MOSFET switching losses, as well as the core and winding losses of magnetic components.

For the PRPT mode, however, the optimal switching frequencies are narrowly ranged between 20 and 30 kHz. Designs with excessively low or high switching frequencies do not appear on the PRPT Pareto front. This indicates that in the PRPT mode, regulating λ_r or C_{sm} to enhance power density or efficiency is more cost-effective than altering f_{sw}. This phenomenon can be attributed to two factors. First, due to the dominant capacitor volume, enhancing power density by reducing C_{sm} is more significant than increasing f_{sw}. Second, the reduction in λ_r directly lowers the transmission power of DABs, contributing more to overall efficiency enhancement than reducing f_{sw}.

Therefore, we can infer that when the type of power semiconductor devices and the core and winding materials are fixed, the optimal frequency is approximately constant with a small fluctuation range. The Pareto front derived from the MOO can help identify this optimal frequency. In particular, for scenarios similar to the discussed system, where SiC MOSFETs, ferrite cores, and Litz wires are most applicable, the recommended switching frequency range is 20–30 kHz.

To explore the design principle of the DAB inductance, Fig. 16 plots the variations of the RMS inductor current ($i_{L,RMS}$) with the per-unit inductance, using the steady-state models established in Section III-A. The filled dots indicate the valley points where $i_{L,RMS}$ is minimized, while the solid lines represent the

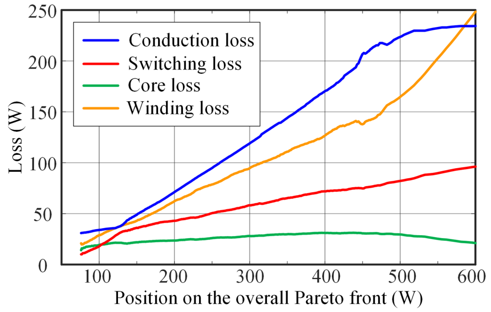


Fig. 17. Variations of component losses along the overall Pareto front.

range of the optimal inductances derived from Pareto-optimal solutions. As illustrated, irrespective of C_{sm}, the optimal inductances are consistently located near the valley points.

To explore the reasons, Fig. 17 depicts the variations of the component losses along the overall Pareto front. Obviously, the conduction loss and winding loss, which are directly related to $i_{\mathrm{L,RMS}}$, are dominant. This fact accounts for the observations in Fig. 16. The low switching loss in Fig. 17 is attributed to the zero-voltage switching capability of the DAB and the high switching speed of SiC MOSFETs. Additionally, low core loss is achievable with commonly-used magnetic materials, whereas reducing the winding loss remains challenging, even with Litz wires that are designed to minimize skin and proximity effects.

The above discussion suggests the selection principle for the DAB inductance. Once λ_{r} as well as C_{sm} is determined, the variation of $i_{\mathrm{L,RMS}}$ with the per-unit inductance can be plotted, allowing for the determination of the optimal inductance by minimize $i_{\mathrm{L,RMS}}$.

D. Summary of Design Procedure for the MMC-Based PET

This section begins by summarizing the MOO-based design procedure for the MMC-based PET operating in the RPT mode. Subsequently, this procedure is simplified according to the design principles identified earlier.

The left part of Fig. 18 illustrates the complete MOO-based design procedure, divided into six steps. First, specify the power and voltage of each port. Next, design the MMC parameters except submodule capacitance. Then, an MOO program is established, as described in Section IV. The NSGA-II [38] is employed to solve this MOO problem and obtain Pareto front curves. An appropriate point on the Pareto front is then selected to achieve a tradeoff between power density and efficiency, allowing the values of all the decision variables in Table IV to be determined. Following this, the submodule capacitor, heatsinks, the DAB transformer and inductor are designed. Finally, the whole design is verified through simulations or experiments.

Among the six steps, Step 3 involves extensive computations and is relatively time-consuming. Owing to the design principles identified in Sections V-B and V-C, the procedure can be simplified, as shown in the right part of Fig. 18. Among these steps, the first three and the final steps remain unchanged, while Steps 3 to 5 are modified as follows.

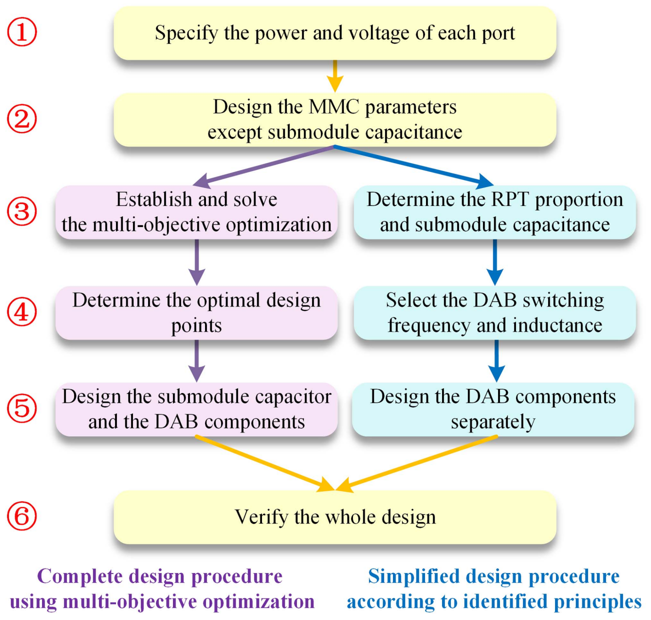


Fig. 18. Design procedures for the MMC-based PET operating in the RPT mode. The left part illustrates the complete design procedure using MOO, while the right part illustrates the simplified design procedure according to the identified design principles.

Step 3: Determine the RPT proportion and required submodule capacitance. First, select an appropriate RPT proportion based on the system's prioritization of power density versus efficiency. Then, the submodule capacitance required to keep the voltage ripple within an allowable range can be uniquely determined, as indicated in Fig. 3.

Step 4: Select the DAB switching frequency and inductance. As demonstrated in Section V-C, the variation range of the optimal switching frequencies for the PRPT mode is quite narrow. When the type of power semiconductor devices and the core and winding materials are fixed, it is possible to estimate the optimal switching frequency. Then, the optimal inductance can be determined to minimize the RMS inductor current.

Step 5: Design the DAB components separately. Once completing Steps 3 and 4, the DAB components, including heatsinks, the transformer and inductor, can be designed separately. The heat sinks can be optimized under known thermal resistance constraints using the method in Section III-C or through finite element simulations. The transformer and inductor can be designed using the AP method [33] or through their individual multiobjective optimization [35].

VI. EXPERIMENTAL VERIFICATIONS

To validate the feasibility and benefit of RPT, particularly the proposed PRPT technique in the MMC-based PET, a scaled-down but complete PET prototype is constructed. Additionally, a full-scale PET submodule (30 kW/1 kV) is built to verify the proposed design and optimization method of the MMC-based PET considering RPT.

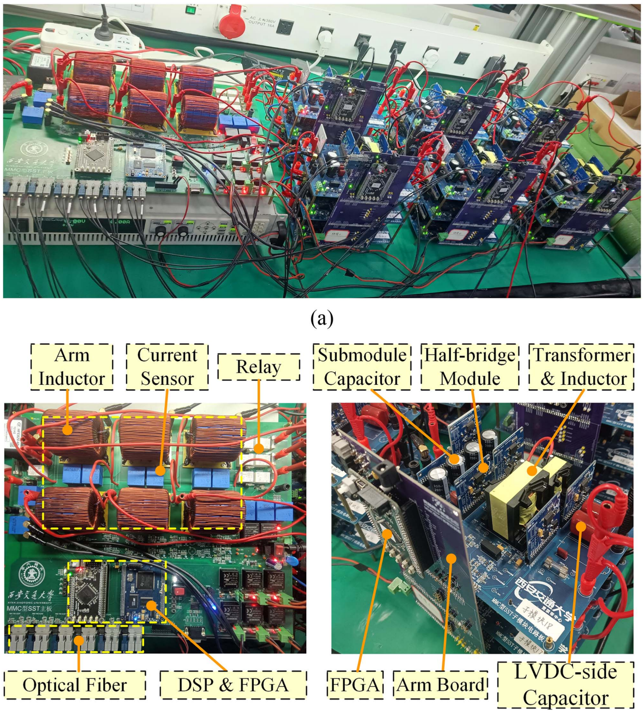


Fig. 19. Scaled-down MMC-based PET platform. (a) Overall platform. (b) Main board. (c) Arm board and submodule board.

TABLE V
PARAMETERS OF THE SCALED-DOWN MMC-BASED PET PROTOTYPE

Parameter		Symbol	Value
Port voltage	MVDC	V_{MVDC}	150 V
	MVAC	V_{MVAC}	75 V
	LVDC	V_{LVDC}	50 V
Port power	MVDC	P_{MVDC}	1000 W
	MVAC	P_{MVAC}	500 W
	LVDC	P_{LVDC}	500 W
MMC	Number of HBs per arm	N	3
	Arm inductance	L_{arm}	5 mH
	Switching frequency	f_{MMC}	10 kHz
DC-link	DC voltage	V_{c0}	50 V
	Voltage ripple factor	δ_{v}	5%
	Submodule capacitance	C_{sm}	600 μF
DAB	Transformer turn ratio	n_{T}	1:1
	Switching frequency	f_{sw}	10 kHz
	Auxiliary inductance	L_{p}	260 μH
	Secondary-side capacitance	C_{s}	20 μF

A. Verification of RPT Through a Scaled-Down PET Prototype

Fig. 19 shows the photographs of the constructed scaled-down PET prototype, which includes six arms, with each arm equipped with three half-bridge modules and three DABs. The key parameters of this prototype are listed in Table V.

As illustrated in Fig. 19(b), a digital signal processor (DSP), model TMS320F28335, and a field-programmable gate array (FPGA), model EP4CE10E22, together serve as master controllers where control strategies are implemented. Meanwhile, as shown in Fig. 19(c), each arm is equipped with an FPGA as the auxiliary controller to collect voltages/currents and generate driving signals for MOSFETs. The communication between the host and auxiliary controllers occurs via optical fibers.

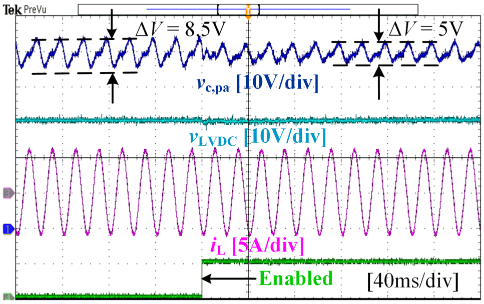


Fig. 20. Waveforms before and after enabling RRT control.

The control system of the MMC-based PET consists of the MMC control, the DAB control, and the RPT control described in Section II. The MMC control primarily contains ac current control, capacitor voltage averaging control, circulating current suppression control, and submodule balancing control [39], [40]. The control system of DABs includes output voltage control and input voltage sharing control [41]. Notably, both the MMC and DAB controls affect only the dynamic values of electrical quantities without altering their steady-state values. Consequently, they do not affect component volumes and losses, and thus have no impact on the PET design. As for the impact of the RPT control, the MMC-based PET exhibits different performances in different operation modes, as revealed in Section V-A.

Fig. 20 displays the PET waveforms of the PET before and after enabling the RPT control composed by (4)–(6). The maximum allowable voltage ripple factor is set at 5%, corresponding to a peak-to-peak voltage of 5 V. The peak-to-peak submodule capacitor voltage is initially 8.5 V and soon drops to 5 V, demonstrating the feasibility of the RPT control.

Furthermore, Fig. 21 shows the steady-state waveforms of the DAB in three operation modes: NRPT, CRPT, and PRPT. As shown in Fig. 21(b), although the voltage ripple is suppressed completely in the CRPT mode, the RMS inductor current increases from 359 to 705 mA, leading to additional power loss and reduced efficiency. In contrast, the RMS inductor current increases only slightly—from 359 to 418 mA—in the PRPT mode, as shown in Fig. 21(c). Therefore, the adoption of PRPT mode can significantly reduce power loss while keeping the voltage ripple within an allowable range. These observations support the analysis in Section V-A.

B. Verification of the Proposed Design and Optimization Method Through a Full-Scale PET Submodule

To validate the effectiveness of the proposed analysis and design methods, this section presents a design example of the PET submodule, which serves as a building block for constructing the MMC-based PET with the parameters listed in Table III.

The optimal decision variables derived from the MOO are listed in Table VI, with some adjustments for practical

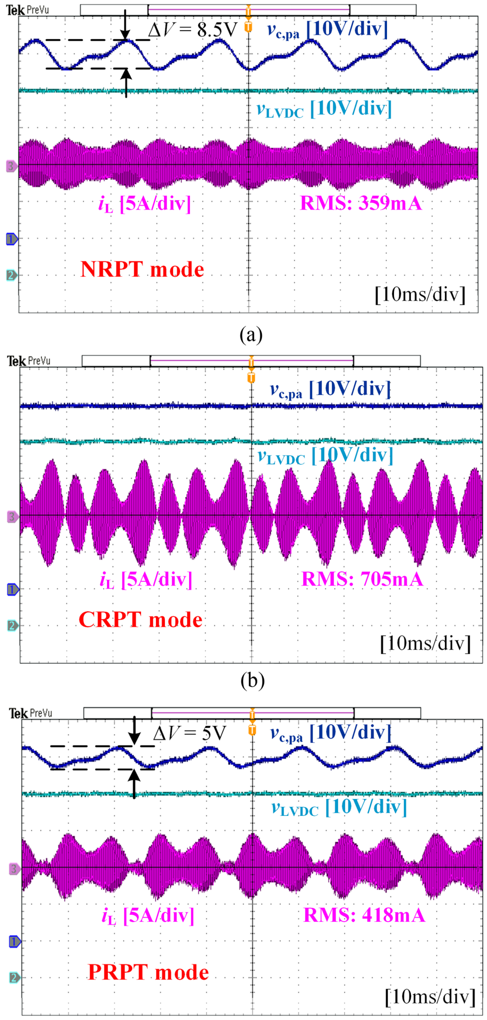


Fig. 21. Steady-state waveforms of the DAB in three operation mode. (a) In the NRPT mode. (b) In the CRPT mode. (c) In the PRPT mode.

TABLE VI
OPTIMAL DECISION VARIABLES DETERMINED BY THE MOO

DECISION VARIABLES	Optimization results	Adjusted results	Notes
C_{sm}	420 μF	420 μF	Unchanged
f_{sw}	29 kHz	30 kHz	Rounded
$L_{\mathrm{p}}^{\mathrm{pu}}$	0.4189	46 μH	Converted to the actual value
$W_{\mathrm{core,T}}$	64 mm	65 mm	Three pairs of EE65B cores
$t_{\mathrm{core,T}}$	79 mm	81mm	
$N_{\mathrm{w,T}}$	20	20	Unchanged
$d_{\mathrm{w,T}}$	3 mm	2.97 mm	450 strands, 0.1 mm
$W_{\mathrm{core,L}}$	49 mm	50 mm	Three pairs of EE50 cores
$t_{\mathrm{core,L}}$	42 mm	43.8 mm	
$m_{\mathrm{w,L}}$	1.389	15 turns	8 turns in the first layer and 7 turns in the second layer
$n_{\mathrm{w,L}}$	11		
$d_{\mathrm{w,L}}$	2.4 mm	2.42 mm	300 strands, 0.1 mm

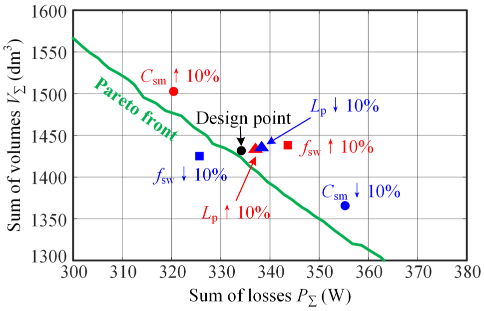


Fig. 22. Changes in the sums of volumes and losses when the global parameters are varied by ±10%.

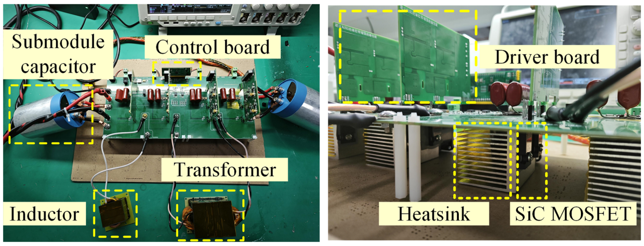


Fig. 23. Photographs of the PET submodule prototype.

conditions. These values correspond to the point with a 70% RPT proportion on the PRPT Pareto front in Fig. 12.

To verify whether the obtained results are correct and represent the optimal design, the global parameters in Table III, including the submodule capacitance, switching frequency, and inductance, are varied by ±10%. The resulting changes in the sums of volumes and losses are illustrated in Fig. 22, where the solid line represents the Pareto front, and the black dot marks the design point selected in this article. As shown, modifying the submodule capacitance or inductance, or increasing the switching frequency, causes the design points to shift towards the upper right of the Pareto front, indicating a decline in PET performance. Although reducing the switching frequency shifts the design point to the lower left, the maximum flux density at this time exceeds the constraints specified in (38) and (39). These observations confirm the correctness and optimality of the selected design point.

The PET submodule prototype, constructed based on the parameters in Table III and the decision variables in Table VI, is shown in Fig. 23. An MPPF capacitor (420 μF, 1200 V) from EACO's SHP series has been selected for the submodule. As mentioned in Section III, the power devices are 1.7-kV SiC MOSFETs (NTH028N170M1) from Onsemi. The core material is the Mn-Zn ferrite PC95 from TDK, and Litz wires are utilized for the windings. Additionally, the microcontroller STM32G431 serves as the controller of this PET submodule.

Given the high power of the designed submodule, a back-to-back test is conducted to alleviate the demand on the dc source and load. Specifically, the input and output ports of the DAB are first connected together, and then connect to a dc source. In this way, the dc source only needs to supply the difference between the input and output power, i.e., the power losses.

First, the port voltage is set to the rated 1000 V and the phase-shift ratio (D) of the DAB is fixed at 0.08 to test the

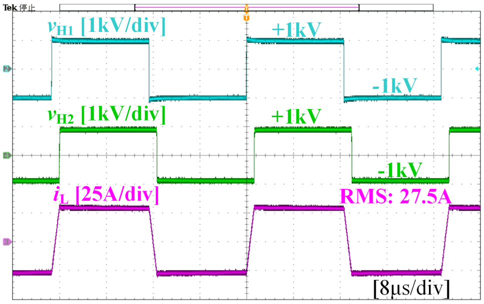


Fig. 24. Steady-state waveforms when $P_T > 0$ and $D = 0.08$.

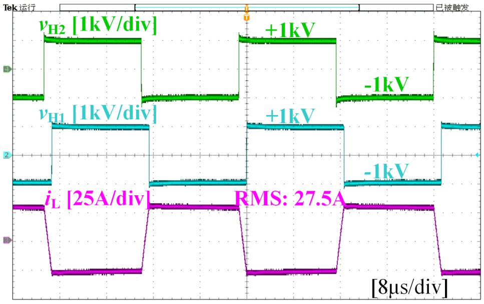


Fig. 25. Steady-state waveforms when $P_T < 0$ and $D = –0.08$.

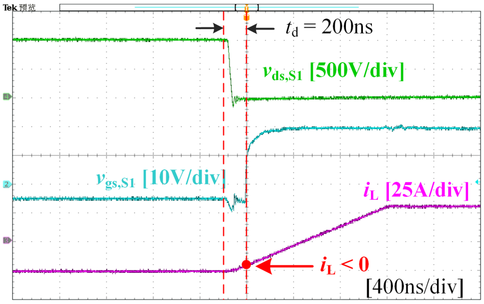


Fig. 26. Illustration of the zero-voltage switching of S_1.

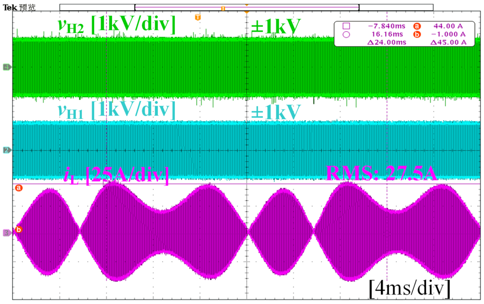


Fig. 27. Steady-state waveforms when the DAB transfer the ripple power.

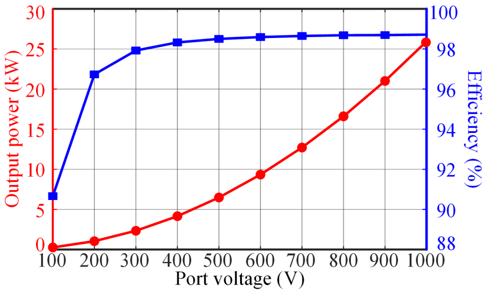


Fig. 28. Efficiency curve of the PET submodule.

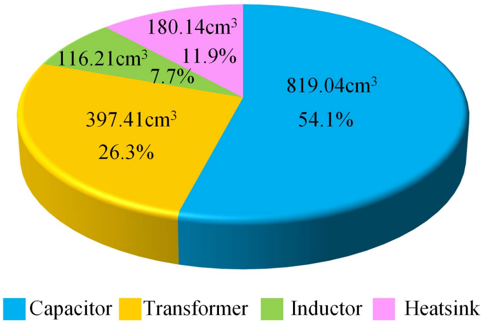


Fig. 29. Volume proportion of each component within the submodule prototype.

steady-state performance of the prototype. Under these conditions, the RMS inductor current is comparable to that under the rated conditions where the transmission power comprises both dc and ripple components. Figs. 24 and 25 show the steady-state waveforms for forward and reverse transmission power, respectively. Evidently, the prototype operates normally in both cases.

Fig. 26 illustrates the realization of zero-voltage switching for S_1 by zooming in on the time axis of Fig. 24. When the drive signal of S_1 transitions from low to high, the inductor current is reverse, and the voltage drop across S_1 has decreased to zero, indicating a successful zero-voltage turn-ON.

Then, let D fluctuate to implement RPT. The time series data for D are calculated using the steady-state models established in Section III-A. This approach ensures that the steady-state waveforms of the PET submodule match the waveform it would exhibit when operating within the complete PET system. Fig. 27 presents the corresponding steady-state waveforms, indicating normal operation under this condition.

When the PET operates in the RPT mode, it is hard to define the efficiency of the individual DAB due to its simultaneous transfer of dc and ripple power. Therefore, the efficiency of the constructed submodule prototype is tested with D set to the constant 0.08, given the comparable RMS inductor current. The efficiency curve is depicted in Fig. 28, demonstrating that the prototype achieves a peak efficiency exceeding 98%.

Finally, Fig. 29 presents the volume proportion of each component within the submodule prototype, which is consistent with the results in Fig. 14. As shown, the capacitor volume is dominant, implying that λ_r can be further increased to enhance power density. Nevertheless, as shown in Fig. 12, this increase will come at the expense of reduced efficiency.

VII. CONCLUSION

This article presents the first comprehensive investigation into the design and optimization of the MMC-based PET operating in the RPT mode through the MOO technique. The Pareto-optimal solutions reveal the principles of operation mode selection and parameter design. The conclusions drawn from this study can be summarized as follows.

1) The MOO program established in this article and the resulting Pareto fronts can intuitively illustrate the optimal design results, making them highly suitable for addressing the complex optimization issues of the MMC-based PET operating in the RPT mode. Moreover, they also play a significant role in supporting the parameter selection.
2) The RPT indeed contributes to enhancing the power density of the MMC-based PET. While CRPT inevitably results in a low-efficiency design, the proposed PRPT technique strikes a better balance between power density and efficiency and is thus highly recommended when designing this topology.
3) The RPT proportion (λ_{r}) introduced in this article can be regarded as the weight coefficient of power density. A larger λ_{r} as well as a smaller C_{sm} should be selected for higher power density. Conversely, if the efficiency is prioritized, a larger C_{sm} is necessary to reduce λ_{r}.
4) In the PRPT mode, the variation range of the optimal switching frequencies is quite narrow. When the type of power semiconductor devices and the core and winding materials are fixed, therefore, it is possible to estimate the optimal switching frequency. Additionally, the optimal DAB inductance is near the value that minimizes the RMS inductor current.

The research presented in this article seeks to provide guidance for the optimal operation mode selection and parameter design of the MMC-based PET, thereby facilitating full play of its advantages and promoting its practical application.

APPENDIX

As stated in Section III-C, estimating the volume of a heatsink hinges on developing a model that relate its thermal resistance to its dimensions, necessitating modeling the pressure drop and thermal resistance related to the airflow rate. The detailed modeling process are presented in the following.

A. Thermal Resistance Calculation With the Airflow Rate

The total thermal resistance for air-cooled heatsinks comprises the baseplate conduction resistance ($R_{\mathrm{hs,b}}$), convection resistance ($R_{\mathrm{hs,cr}}$), and spreading resistance ($R_{\mathrm{hs,sp}}$) [42].

The heat transfer through the baseplate can be considered as a one-dimensional conduction process. Accordingly

$$R_{\mathrm{hs,b}} = \frac{t_{\mathrm{b}}}{k \cdot W_{\mathrm{hs}} \cdot L_{\mathrm{hs}}} \tag{46}$$

where k denotes the thermal conductivity.

The Newton cooling formula [42] provides the expression for the convection resistance as

$$R_{\mathrm{hs,cr}} = \frac{1}{h \cdot A_{\mathrm{hs}}} \tag{47}$$

where h is called convection heat transfer coefficient, and A_{hs} is the equivalent surface area of the heatsink.

Teertstra et al. [43] developed the following expression to estimate h for the air-cooled plate-fin heatsink:

$$\begin{aligned} \mathrm{Nu} &= \frac{h \cdot s_{\mathrm{fin}}}{k_{\mathrm{f}}} \\ &= \left[\left(\frac{\mathrm{Re}_s^* \cdot \mathrm{Pr}}{2} \right)^{-3} \right. \\ &\quad \left. + \left(0.664 \sqrt{\mathrm{Re}_s^*} \mathrm{Pr}^{1/3} \sqrt{1 + \frac{3.65}{\sqrt{\mathrm{Re}_s^*}}} \right)^{-3} \right]^{-1/3} \end{aligned} \tag{48}$$

where k_{f} is the thermal conductivity of air, and Pr is the Prandtl number. The channel Reynolds number Re_s^* is defined by

$$\mathrm{Re}_s^* = \mathrm{Re}_s \cdot \frac{s_{\mathrm{fin}}}{L_{\mathrm{hs}}} = \frac{U_{\mathrm{f}} s_{\mathrm{fin}}}{\mu_{\mathrm{f}}} \cdot \frac{s_{\mathrm{fin}}}{L_{\mathrm{hs}}} \tag{49}$$

where μ_{f} is the dynamic viscosity of air, and U_{f} is the average wind speed between fins. U_{f} can be determined using the airflow rate and the total cross-sectional area of N_{fin} fins as follows:

$$U_{\mathrm{f}} = \frac{Q}{(N_{\mathrm{fin}} - 1) \cdot s_{\mathrm{fin}} \cdot H_{\mathrm{fin}}}. \tag{50}$$

Notably, Teertstra's model for calculating h assumes that fins are isothermal, which deviates from actual situations. To rectify the inaccuracies arising from this assumption, this article incorporates the fin efficiency [42], which accounts for the actual versus maximum possible heat transfer of the fin and is calculated by the following:

$$\eta_{\mathrm{fin}} = \frac{\tan \left[\sqrt{(h \cdot P_{\mathrm{c}})/(k \cdot A_{\mathrm{c}})} \cdot H_{\mathrm{fin}} \right]}{\sqrt{(h \cdot P_{\mathrm{c}})/(k \cdot A_{\mathrm{c}})} \cdot H_{\mathrm{fin}}} \tag{51}$$

where $P_{\mathrm{c}} = 2(t_{\mathrm{fin}} + L_{\mathrm{hs}})$ and $A_{\mathrm{c}} = t_{\mathrm{fin}} \cdot L_{\mathrm{hs}}$ denote the perimeter and area of the cross section of fins, respectively.

Subsequently, a precise convection resistance of the heatsink can be calculated by (52), where $A_{\mathrm{b}} = (N_{\mathrm{fin}}\text{-}1) \cdot s_{\mathrm{fin}} \cdot L_{\mathrm{hs}}$ and $A_{\mathrm{fin}} = 2(N_{\mathrm{fin}}\text{-}1) \cdot H_{\mathrm{fin}} \cdot L_{\mathrm{hs}}$ represent the convection heat transfer areas of the baseplate and fins, respectively

$$R_{\mathrm{hs,cr}} = \frac{1}{h \cdot (A_{\mathrm{b}} + \eta_{\mathrm{fin}} A_{\mathrm{fin}})}. \tag{52}$$

Another contribution to the total thermal resistance is the spreading resistance, which originates from the difference in area between the heat source and baseplate. This resistance can be calculated using equations provided in [44] for rectangular baseplates and heat sources, i.e.

$$\begin{aligned} \psi_{\mathrm{sp}} &= \frac{\rho}{\pi^2} \sqrt{\frac{\beta}{\alpha}} \sum_{l=1}^{\infty} \frac{1}{l^2} \sin(l\pi\alpha) \left[\frac{1 + \frac{Biot}{2l\pi} \cdot \tanh(2l\pi\tau)}{\frac{Biot}{2l\pi} + \tanh(2l\pi\tau)} \right] \\ &\quad + \frac{1}{\rho\pi^2} \sqrt{\frac{\alpha}{\beta}} \sum_{m=1}^{\infty} \frac{1}{m^2} \sin(m\pi\beta\rho) \left[\frac{1 + \frac{Biot}{2m\pi\rho} \cdot \tanh(2m\pi\rho\tau)}{\frac{Biot}{2m\pi\rho} + \tanh(2m\pi\rho\tau)} \right] \end{aligned}$$

$$+\frac{4}{\pi^2\sqrt{\alpha\beta}}\sum_{l=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{lm}\sin(l\pi a)\sin(m\pi\beta\rho)\frac{1}{2\pi\sqrt{l^2+m^2\rho^2}}$$
$$\cdot\left[\frac{1+\frac{Biot}{2\pi\sqrt{l^2+m^2\rho^2}}\cdot\tanh\left(2\pi\tau\sqrt{l^2++m^2\rho^2}\right)}{\frac{Biot}{2\pi\sqrt{l^2+m^2\rho^2}}+\tanh\left(2\pi\tau\sqrt{l^2++m^2\rho^2}\right)}\right] \quad (53)$$

$$R_{\text{th,sp}}=\frac{\psi_{\text{sp}}}{k\cdot\Delta x\cdot\Delta y} \quad (54)$$

where $\rho = L_{\text{hs}}/W_{\text{hs}}$, $\alpha = \Delta x/L_{\text{hs}}$, $\beta = \Delta y/L_{\text{hs}}$, and $\tau = t_{\text{b}}/L_{\text{hs}}$. Additionally, Δx and Δy represent the dimensions of the heat source along the baseplate's length and width, respectively, specifying the size of the MOSFET's metal case in this study.

In (53), the Biot number quantifies the effect of convection heat transfer on the spreading resistance, determined as follows:

$$\text{Biot}=\frac{h_{\text{eff}}\cdot L_{\text{hs}}}{k} \quad (55)$$

with the equivalent convection heat transfer coefficient calculated by

$$h_{\text{eff}}=\frac{1}{R_{\text{th,cr}}\cdot W_{\text{hs}}\cdot L_{\text{hs}}}. \quad (56)$$

B. Pressure Drop Calculation With the Airflow Rate

Referencing [45], the pressure drop through the heatsink is given by

$$\Delta p_{\text{hs}}=\left[f_{\text{app}}\frac{N_{\text{fin}}(2H_{\text{fin}}\cdot L_{\text{hs}}+s_{\text{fin}}\cdot L_{\text{hs}})}{W_{\text{hs}}\cdot H_{\text{fin}}}+K_{\text{c}}+K_{\text{e}}\right]$$
$$\cdot\frac{1}{2}\rho_{\text{f}}U_{\text{f}}^2 \quad (57)$$

where ρ_{f} is the air density.

The first term of (57) represents the frictional pressure loss, with f_{app} as the apparent friction factor. Given that the channels within the plate-fin heatsink can be regarded as multiple rectangular channels, the calculation of f_{app} can refer to the model proposed by Muzychka and Yovanovich for rectangular channels [46], as shown in the following:

$$f_{\text{app}}=\left[\left(\frac{3.44}{\sqrt{L_{\text{hs}}/(D_{\text{h}}\cdot\text{Re}_{D_{\text{h}}})}}\right)^2+f\text{Re}^2\right]^{1/2}/\text{Re}_{D_{\text{h}}} \quad (58)$$

where

$$D_{\text{h}}=\frac{2s_{\text{fin}}\cdot H_{\text{fin}}}{s_{\text{fin}}+H_{\text{fin}}} \quad (59)$$

$$\text{Re}_{D_{\text{h}}}=\frac{D_{\text{h}}\cdot U_{\text{f}}}{\mu_{\text{f}}} \quad (60)$$

$$f\text{Re}=24-32.527\left(\frac{s_{\text{fin}}}{L_{\text{hs}}}\right)+46.721\left(\frac{s_{\text{fin}}}{L_{\text{hs}}}\right)^2$$
$$-40.829\left(\frac{s_{\text{fin}}}{L_{\text{hs}}}\right)^3+22.954\left(\frac{s_{\text{fin}}}{L_{\text{hs}}}\right)^4-6.089\left(\frac{s_{\text{fin}}}{L_{\text{hs}}}\right)^5. \quad (61)$$

The second and third terms of (57) account for the contraction and expansion pressure drops at the inlet and exhaust, respectively, with K_{c} and K_{e} given as follows [47]:

$$K_{\text{c}}=0.42\left[1-\left(N_{\text{fin}}t_{\text{fin}}/W_{\text{hs}}\right)^2\right] \quad (62)$$

$$K_{\text{e}}=\left[1-\left(N_{\text{fin}}t_{\text{fin}}/W_{\text{hs}}\right)^2\right]^2. \quad (63)$$

REFERENCES

[1] S. J. Ul Hassan, A. Mehdi, Z. Haider, and J.-S. Song, "Towards medium voltage hybrid AC/DC distribution systems: Architectural topologies, planning and operation," *Int. J. Elect. Power Energy Syst.*, vol. 159, Aug. 2024, Art. no. 110003.

[2] J. E. Huber and J. W. Kolar, "Solid-state transformers: On the origins and evolution of key concepts," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, Sep. 2016.

[3] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: Modular multilevel converter versus cascaded H-bridge solutions," *IEEE Ind. Electron. Mag.*, vol. 10, no. 4, pp. 6–19, Dec. 2016.

[4] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[5] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, Jan. 2015.

[6] M. A. Perez, D. Arancibia, S. Kouro, and J. Rodriguez, "Modular multilevel converter with integrated storage for solar photovoltaic applications," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc.*, 2013, pp. 6993–6998.

[7] L. Chen, J. Wang, Z. Li, C. Guo, B. Zhang, and Z. Li, "Steady-state analysis of the DR-MMC based hybrid topology for offshore wind power transmission," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 3177–3188, Feb. 2005.

[8] S. Castellan, R. Menis, A. Tessarolo, and G. Sulligoi, "Power electronics for all-electric ships with MVdc power distribution system: An overview," in *Proc. 9th Int. Conf. Ecological Veh. Renewable Energies*, 2014, pp. 1–7.

[9] Z. Li, P. Wang, Z. Chu, H. Zhu, Z. Sun, and Y. Li, "A three-phase 10 kVAC-750 VDC power electronic transformer for smart distribution grid," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–9.

[10] Z. Jianqiao, Z. Jianwen, C. Xu, W. Jiacheng, and Z. Jiajie, "Family of modular multilevel converter (MMC) based solid state transformer (SST) topologies for hybrid AC/DC distribution grid applications," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–5.

[11] J. Zhou et al., "Design and control of power fluctuation delivery for cell capacitance optimization in multiport modular solid-state transformers," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1412–1427, Feb. 2021.

[12] M. Saeed, M. R. Rogina, M. López, A. Rodríguez, M. Arias, and F. Briz, "Design and construction of a DAB using SiC MOSFETs with an isolation of 24 kV for PET applications," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.10.

[13] N. Fritz, M. Rashed, S. Bozhko, F. Cuomo, and P. Wheeler, "Analytical modelling and power density optimization of a single phase dual active bridge for aircraft application," in *Proc. 9th Int. Conf. Power Electron., Mach. Drives*, 2018, pp. 3671–3676.

[14] H. Jin, Y. Pei, L. Wang, J. Wen, C. Yang, and X. Dong, "Achieving rated power and ZVS for dual active bridge converter considering the interaction of nonidealities," *IEEE Trans. Ind. Electron.*, vol. 70, no. 8, pp. 7867–7878, Aug. 2023.

[15] Z. Li, Y. Pei, L. Chen, L. Wang, and J. Wang, "A novel inductance and capacitance selection method for modular multilevel converters based on modulation margin considerations," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 12, no. 3, pp. 2431–2445, Jun. 2024.

[16] Z. Xu, H. Xiao, and Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renewable Power Gener.*, vol. 10, no. 6, pp. 788–797, Jul. 2016.

[17] J. Kang, D.-W. Kang, J.-P. Lee, D. W. Yoo, and J. W. Shim, "Design procedure of MMC-HVDC system: Comprehensive consideration of internal and external dynamics," *IEEE Access*, vol. 8, pp. 157437–157450, 2020.

[18] H. Lin, Z. Wang, X. Guo, Z. Lin, and G. Chen, "A 380 V/50 kVar SiC-SVG achieving a power density of 1.652 kVar/L with the optimization of heatsink and output filter volume," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 4634–4648, Aug. 2022.

[19] D. Ahmed, L. Wang, Z. Dai, and M. Wu, "Pareto-optimal design of litz-wire gapped-core high-frequency transformer for LLC converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 8883–8894, Sep. 2022.

[20] P. Chen, J. Liu, F. Xiao, Z. Zhu, and Q. Ren, "Multi-objective optimization design of modular multilevel multi-port DC-DC converter assessing efficiency, volume and reliability," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 2749–2756.

[21] B. Chen, X. Liang, and N. Wan, "Design methodology for inductor-integrated litz-wired high-power medium-frequency transformer with the nanocrystalline core material for isolated DC-link stage of solid-state transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11557–11572, Nov. 2020.

[22] B. Li et al., "An improved circulating current injection method for modular multilevel converters in variable-speed drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7215–7225, Nov. 2016.

[23] Z. Wang, J. Chen, K. Liao, J. Xiong, and K. Zhang, "Review on low-frequency ripple suppression methods for MMCs for medium-voltage drive applications," *IET Power Electron.*, vol. 11, no. 15, pp. 2403–2414, Dec. 2018.

[24] X. Cai et al., "Fluctuation power control strategy for MMC-based SST to reduce the submodule capacitor voltage oscillation," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 2430–2435.

[25] Z. Li, Y. Pei, L. Wang, L. Zhao, L. Pei, and W. Cao, "A comprehensive closed-loop voltage ripple control scheme for modular multilevel converter-based power electronic transformers," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15225–15241, Dec. 2023.

[26] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC–DC converter," *IET Power Electron.*, vol. 1, no. 4, pp. 507–517, Mar. 2008.

[27] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[28] Z. Ma, Y. Pei, L. Wang, Q. Yang, Z. Qi, and G. Zeng, "An accurate analytical model of SiC MOSFETs for switching speed and switching loss calculation in high-voltage pulsed power supplies," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3281–3297, Mar. 2023.

[29] J. Reinert, A. Brockmeyer, and R. W. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, Jul./Aug. 2001.

[30] J. Li, T. Abdallah, and C. R. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf.*, 2001, vol. 4, pp. 2203–2210.

[31] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. Workshop Comput. Power Electron.*, 2002, pp. 36–41.

[32] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 964–973, Feb. 2012.

[33] C. W. T. McLyman, *Transformer and Inductor Design Handbook*, 4rd ed. Boca Raton, FL, USA: CRC Press, 2011.

[34] F. Tourkhani and P. Viarouge, "Accurate analytical model of winding losses in round litz wire windings," *IEEE Trans. Magn.*, vol. 37, no. 1, pp. 538–543, Jan. 2001.

[35] E. L. Barrios, A. Ursúa, L. Marroyo, and P. Sanchis, "Analytical design methodology for litz-wired high-frequency power transformers," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2103–2113, Apr. 2015.

[36] N. H. Kutkut and D. M. Divan, "Optimal air-gap design in high-frequency foil windings," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 942–949, Sep. 1998.

[37] F. Forest, E. Labouré, T. Meynard, and M. Arab, "Analytic design method based on homothetic shape of cores for high frequency transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2070–2080, Sep. 2007.

[38] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Trans. Evol. Comput.*, vol. 6, no. 2, pp. 182–197, Apr. 2002.

[39] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017.

[40] F. Deng, Y. Lü, C. Liu, Q. Heng, Q. Yu, and J. Zhao, "Overview on submodule topologies, modeling, modulation, control schemes, fault diagnosis, and tolerant control strategies of modular multilevel converters," *Chin. J. Elect. Eng.*, vol. 6, no. 1, pp. 1–21, Mar. 2020.

[41] Z. Li, Y. Pei, L. Wang, J. Liu, and Y. Gao, "A novel linearization control strategy to improve the dynamic performance of DC solid-state transformers under all working conditions," *Trans. China Electrotech. Soc.*, vol. 39, no. 20, pp. 6475–6487, Oct. 2024.

[42] Y. Shabany, *Heat Transfer: Thermal Management of Power Electronic Devices*. Boca Raton, FL, USA: CRC Press, 2009.

[43] P. Teertstra, M. Yovanovich, and J. Culham, "Analytical forced convection modeling of plate fin heatsinks," *J. Electron. Manuf.*, vol. 10, no. 4, pp. 253–261, 2000.

[44] G. N. Ellison, "Maximum thermal spreading resistance for rectangular sources and plates with nonunity aspect ratios," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 2, pp. 439–454, Jun. 2003.

[45] J. R. Culham and Y. S. Muzychka, "Optimization of plate fin heatsinks using entropy generation minimization," *IEEE Trans. Compon. Packag. Technol.*, vol. 24, no. 2, pp. 159–165, Jun. 2001.

[46] Y. S. Muzychka and M. M. Yovanovich, "Modeling friction factors in non-circular ducts for developing laminar flow," in *Proc. 2nd AIAA Theor. Fluid Mech. Meeting*, 1998, Art. no. 2492.

[47] F. M. White et al., *Fluid Mechanics*, vol. 7. New York, NY, USA: McGrawHill, 2003.

Zhixiang Li (Graduate Student Member, IEEE) was born in Shandong, China, in 1996. He received the B.S. degree in electrical engineering in 2019 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include the topology, control, and design of multilevel converters and isolated dc/dc converters, especially the control and design of power electronic transformers, the modular multilevel converter and the dual active bridge converter.

Yunqing Pei (Member, IEEE) was born in 1969. He received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in power electronics from Xi'an Jiaotong University, Xi'an, China in 1991, 1994, and 1999, respectively.

He became a Faculty Member with Xi'an Jiaotong University, where he is currently a Professor. From February 2006 to February 2007, he was a Visiting Scholar with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University. His research interests include the high-power inverters, switch mode power supply, and converters in distributed generation systems.

Jiahao Liu was born in Xi'an, China, in 1999. He received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2017 and 2021, respectively.

He is currently working as an electronic Engineer with the Shanghai Huawei Technologies Company Ltd, Shanghai, China. His research interests include high-power-density resonant topologies and high-frequency magnetic and winding structures.

Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Department of Electrical Engineering, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Kingston. In 2017, he became a Full Professor with Xi'an Jiaotong University. His research interests include wide bandgap power semiconductors, packaging and integration, and high-density power conversion.

Dr. Wang is an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Co-Chair of System Integration and Application in International Technology Roadmap for Wide Band-Gap Power Semiconductor, the Chair of IEEE PELS and CPSS Joint Chapter in Xi'an, and the Vice Chair of IEEE PELS Membership Committee-China and the four committees in China Power Supply Society.

Zesong Leng was born in Guizhou, China, in 2001. He received the B.S. degree in electrical engineering from Chongqing University, Chongqing, China, in 2023. He is currently working toward the M.S. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His current research interests include the topology, control, and design of dc/dc converters, especially the control and design of resonant converters and dual active bridge converters.