DC-Link Capacitance Online Estimation Based on Current Hybrid Reconstruction by Charge Equivalence for Boost PFC Converters

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***Abstract*—The different operating modes of the boost power factor correction converter pose a challenge to accurately estimate dc-link capacitance across a wide power range. In order to meet the requirement of the mixed conduction mode (MCM) and the continuous conduction mode (CCM), an online estimation strategy of dc-link capacitance based on current hybrid reconstruction by charge equivalence is proposed. For obtaining the second harmonic component of capacitor current to estimate capacitance, the current reconstruction models are established in CCM and discontinuous conduction mode (DCM) within a switching cycle based on charge equivalence. By analyzing the effect of the voltage division of boost inductor internal resistance and the misjudgment of operating mode on the current reconstruction within a switching cycle, the capacitor current is reconstructed in different operating modes by the hybrid strategy based on error minimization. In this way, the estimation accuracy of dc-link capacitance can be improved across a wide power range without additional hardware and increasing sampling frequency. Finally, the effectiveness of the proposed strategy is verified on the experimental platform.**

***Index Terms*—Boost power factor correction (PFC) converter, capacitor current reconstruction, electrolytic capacitor, online capacitance estimation, wide power range.**

I. Introduction

SINGLE-PHASE boost power factor correction (PFC) converters are extensively utilized in ac/dc systems due to their simple structure, lower cost, and higher efficiency [1], [2], [3], [4], [5], [6]. In order to balance power and stabilize output voltage, the low-cost and high-capacity aluminum electrolytic capacitors are usually used on the dc side of the converter [7], [8], [9], [10]. In addition, the capacitance can also guide the design of voltage loop controller. However, aluminum electrolytic capacitors have become one of the weakest components in power electronic systems. According to the statistics, about 30% of converter failures are caused by the aging of electrolytic capacitors [11], [12], [13]. Therefore, in order to ensure the reliable operation of the system, it is necessary to estimate the status of electrolytic capacitors in boost PFC converters.

In recent years, lots of research has been conducted to achieve the state estimation of electrolytic capacitors. Adaptive filtering algorithms, such as the recursive least squares (RLS) algorithm [14], [15], [16], [17], the least mean squares algorithm [18], [19], [20], and the iterative least squares algorithm [21] are widely used. The capacitance and equivalent series resistance (ESR) are the important health indicators of electrolytic capacitors. Usually, once the capacitance decreases to 80% of the initial value or the ESR increases to twice the initial value, it is considered that the electrolytic capacitor has failed [13], [22], [23]. On this basis, the estimation methods of capacitor parameters can be divided into the offline methods, the quasi online methods, and the online methods. Among them, the online methods are currently research hotspots since they do not require dismantling capacitors or special testing conditions. For boost converters, based on the time scale, the online methods can be further divided into the wavelet transform methods, the steady-state ripple methods, and the capacitor charge-discharge methods.

The wavelet transform methods extract the frequency domain information of dc-link voltage at the time of power device shutdown to calculate ESR. In [16], an estimation strategy based on an improved hybrid model was proposed, which could simultaneously estimate the boost inductance and dc-link capacitance by the wavelet denoising (WTD) and the RLS algorithm. On the basis of WTD, the influence of sampling noise and voltage spikes was further considered [24]. In [25], the first derivative of Gaussian function was used as the wavelet basis, and the effect of different dc-link capacitance, boost inductance, switching devices, and loads on the accuracy of ESR estimation was discussed. In [26], an ESR estimation strategy based on compressive sensing and discrete wavelet transform was proposed to reduce the sampling frequency. However, in order to ensure

Received 25 June 2024; revised 30 September 2024; accepted 11 November 2024. Date of publication 14 November 2024; date of current version 28 January 2025. This work was supported in part by the Research Fund for the National Natural Science Foundation of China under Grant 52307198 and Grant 52125701, in part by the Fundamental Research Funds for the Central Universities, the Postdoctoral Fellowship Program of CPSF under Grant GZC20233437, in part by the Fellowship of China Postdoctoral Science Foundation under Grant 2024M754183, and in part by Heilongjiang Postdoctoral Financial Assistance under Grant LBH-Z23152. Recommended for publication by Associate Editor F. D. Freijedo. *(Corresponding author: Binxing Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3498332.

Digital Object Identifier 10.1109/TPEL.2024.3498332

the estimation accuracy, the sampling frequencies are usually required to be higher, which is difficult to achieve in some platforms.

The steady-state ripple methods employ the ripples of dc-link voltage and capacitor current to estimate capacitance and ESR. The capacitor current could be obtained through additional sensor [27], [28]. The short time least square Prony's algorithm [27] and the short time Fourier transform [28] were used to estimate capacitance and ESR in the low and medium frequency ranges, respectively. In order to avoid the additional capacitor current sensor, the dc-link voltage was sampled at two specific moments during the line cycle to calculate capacitance and ESR [29]. In addition, the capacitor current could also be reconstructed according to the inductor current and switch state [17], [19]. In [17], the Kalman filter was used to estimate capacitance and ESR. In [19], capacitance was estimated in the on state, and ESR was calculated by the estimated capacitance in the off state. However, in order to obtain capacitor current information, the additional hardware or sampling times are usually required.

The capacitor charge-discharge methods use the charging and discharging process of dc-link capacitors to estimate capacitance, which require a lower sampling frequency but a longer estimation time. For the uncertain operating conditions such as the dynamic loads, an estimation strategy based on the transient charging profile was proposed, which calculated the change in the capacitor charge to estimate capacitance [20]. In [30], the load current was calculated based on the power balance, and capacitance could be estimated through the changes in the dc-link voltage and the capacitor current. In [31], the damping factor was used as a health standard for capacitors, and the variation of dc-link voltage was characterized by the zero-state response of a parallel resistor-inductor-capacitor circuit during the transient period. The sampling frequency was as low as one fortieth of the switching frequency, but the pretest was required to obtain the capacitance.

In summary, existing capacitors estimation strategies are usually confronted with challenges such as high sampling frequency, increased hardware costs, or complex algorithm implementation. In addition, the capacitance estimation strategies for an operating mode are difficult to meet the application requirements, because the boost PFC converter operates in mixed conduction mode (MCM) and continuous conduction mode (CCM) across a wide power range [32], [33], [34]. Therefore, it is necessary to conduct further in-depth research on capacitance estimation strategies with the low hardware requirements, the simple algorithm implementation, and the wide power range.

This article proposes an online estimation strategy of dc-link capacitance based on current hybrid reconstruction by charge equivalence for boost PFC converters, which has the strong adaptability across a wide power range. In order to avoid the additional current sensor, the reconstruction principle of capacitor current based on charge equivalence is revealed by the discrete Fourier transform (DFT). According to the current characteristics of different operating modes, the current reconstruction models are established in CCM and discontinuous conduction mode (DCM) within a switching cycle based on charge equivalence, respectively. Furthermore, the effect of the voltage division of boost inductor internal resistance and the misjudgment of operating mode on the current reconstruction is analyzed within a switching cycle. Based on error minimization, the two current reconstruction strategies are integrated to improve the reconstruction accuracy of capacitor current across a wide power range. Finally, the effectiveness of the proposed strategy is verified on the experimental platform of permanent magnet compressor system driven by boost PFC converter.

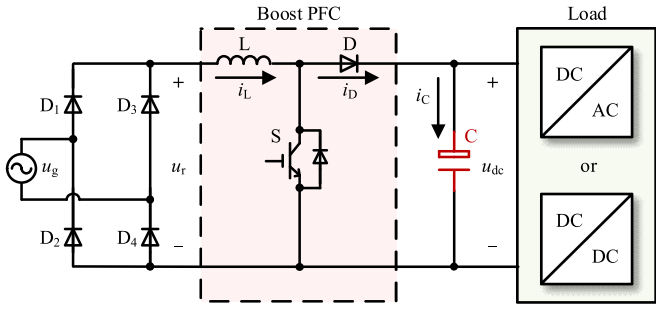

Fig. 1. Topology of single-phase boost PFC converter.

II. Proposed Online Capacitance Estimation Strategy Based on Current Reconstruction

The topology of single-phase boost PFC converter is shown in Fig. 1, and the capacitance can be calculated by the dc-link voltage and the capacitor current. At the second harmonic frequency of the grid, the ESR is much smaller than the capacitive reactance, so the capacitance C can be calculated as

$$C = \frac{1}{200\pi X_{\mathrm{C}}} \approx \frac{I_{\mathrm{C\_2}}}{200\pi U_{\mathrm{dc\_2}}} \tag{1}$$

where X_{C} represents the capacitive reactance and $U_{\mathrm{dc\_2}}$ and $I_{\mathrm{C\_2}}$ represent the amplitudes of the second harmonic components of dc-link voltage and capacitor current, respectively.

According to (1), in order to calculate capacitance, the capacitor current information is necessary. But there are generally only the inductor current sensor, the rectifier voltage sensor, and the dc-link voltage sensor in the boost PFC converter. In order to avoid the additional current sensor, it is significant to reconstruct the capacitor current, and the amplitude of the second harmonic component of capacitor current $I_{\mathrm{C\_2}}$ can be expressed as

$$I_{C\_2} = I_{D\_2} = \sqrt{\mathrm{Re}[\boldsymbol{I}_{D\_2}]^2 + \mathrm{Im}[\boldsymbol{I}_{D\_2}]^2} \tag{2}$$

where I_{D_2} represents the amplitude of the second harmonic component of diode current, $\boldsymbol{I}_{D\_2}$ represents the phasor form of I_{D_2}, $\mathrm{Re}[\boldsymbol{I}_{D\_2}]$ and $\mathrm{Im}[\boldsymbol{I}_{D\_2}]$ represent the real and imaginary parts of $\boldsymbol{I}_{D\_2}$, respectively.

As shown in Fig. 2, the DFT is used to analyze the second harmonic component of diode current within half a grid cycle. In Fig. 2, M represents the number of sample points for DFT within half a grid cycle, and P represents the number of sample points for DFT within a switching cycle defined by

$$P = \frac{T_{\mathrm{s}}}{T_2} M = \frac{M}{N} \tag{3}$$

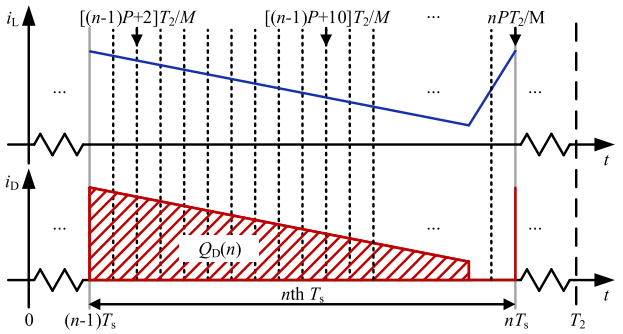

Fig. 2. DFT analysis for the second harmonic component of diode current.

where N represents the ratio of the half a grid cycle to the switching cycle, T_2 and T_s represent the half a grid cycle and the switching cycle, respectively.

The real and imaginary parts of $\boldsymbol{I}_{D\_2}$ can be expressed as

$$\begin{cases} \mathrm{Re}\left[\boldsymbol{I}_{D\_2}\right] = \dfrac{2}{M}\sum_{m=0}^{M-1} i_D(m)\cos\dfrac{2\pi m}{M} \\ \mathrm{Im}\left[\boldsymbol{I}_{D\_2}\right] = -\dfrac{2}{M}\sum_{m=0}^{M-1} i_D(m)\sin\dfrac{2\pi m}{M} \end{cases} \tag{4}$$

where i_D represents the diode current.

In addition, $m = (n\text{-}1)N, (n\text{-}1)N{+}1, \ldots, nN\text{-}1$ within the nth switching cycle. When the switching cycle is much smaller than the half a grid cycle, the following equation is approximately satisfied:

$$\begin{cases} \cos\dfrac{2\pi m}{M} = \cos\dfrac{2\pi m}{NP} \approx \cos\dfrac{2\pi(n-1)}{P} \\ \sin\dfrac{2\pi m}{M} = \sin\dfrac{2\pi m}{NP} \approx \sin\dfrac{2\pi(n-1)}{P} \end{cases}. \tag{5}$$

According to (3), (4), and (5), the real and imaginary parts of $\boldsymbol{I}_{D\_2}$ can be expressed as

$$\begin{cases} \mathrm{Re}\left[\boldsymbol{I}_{D\_2}\right] = \dfrac{2}{M}\sum_{n=1}^{N} Q_D(n)\cos\dfrac{2\pi(n-1)}{N} \\ \mathrm{Im}\left[\boldsymbol{I}_{D\_2}\right] = -\dfrac{2}{M}\sum_{n=1}^{N} Q_D(n)\sin\dfrac{2\pi(n-1)}{N} \end{cases} \tag{6}$$

where Q_D represents the amount of charge flowing through the diode within a switching cycle, which can be expressed as within the nth switching cycle

$$Q_D(n) = \sum_{m=(n-1)P}^{nP-1} i_D(m). \tag{7}$$

According to (2) and (6), when the switching frequency is much higher than twice the grid frequency, the second harmonic component of capacitor current can be accurately reconstructed by characterizing the amount of charge flowing through the diode within a switching cycle.

As a consequence, the proposed online estimation strategy of dc-link capacitance based on current hybrid reconstruction by charge equivalence is shown in Fig. 3. The strategy can be mainly divided into two parts: the capacitor current reconstruction and the dc-link capacitance calculation. Firstly, the diode current within a switching cycle is reconstructed based on the proposed hybrid strategy by charge equivalence. Then, the BPF and DFT

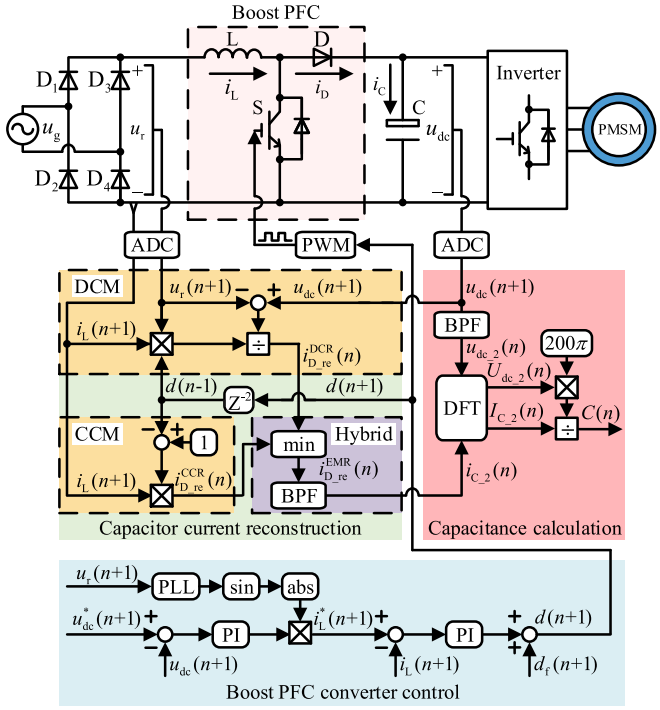

Fig. 3. Block diagram of the proposed online estimation of dc-link capacitance.

are used to extract the second harmonic components of the dc-link voltage and the capacitor current, respectively. Finally, the dc-link capacitance can be calculated according to (1).

III. Capacitor Current Hybrid Reconstruction in Different Operating Modes

For different operating modes, the continuous conduction reconstruction (CCR) strategy for CCM and the discontinuous conduction reconstruction (DCR) strategy for DCM within a switching cycle are proposed based on charge equivalence, respectively. By analyzing the effect of the voltage division of boost inductor internal resistance and the misjudgment of operating mode on the current reconstruction within a switching cycle, the hybrid reconstruction of capacitor current in different operating modes is achieved based on error minimization.

A. Single Switching Cycle Current Reconstruction in CCM

Considering the control timing of the boost PFC converter, the relationship between inductor current and diode current in CCM is shown in Fig. 4. The inductor current is sampled within the nth switching cycle, and the sampling value is updated at the beginning of the $(n{+}1)$th switching cycle. The duty cycle is calculated and the corresponding comparison value is generated within the $(n{+}1)$th switching cycle, the comparison value is updated at the beginning of the $(n{+}2)$th switching cycle, and the PWM is outputted within the $(n{+}2)$th switching cycle.

It can be seen that there is a switching cycle delay from the inductor current sampling to the sampling value update and from the duty cycle calculation to the PWM output, respectively.

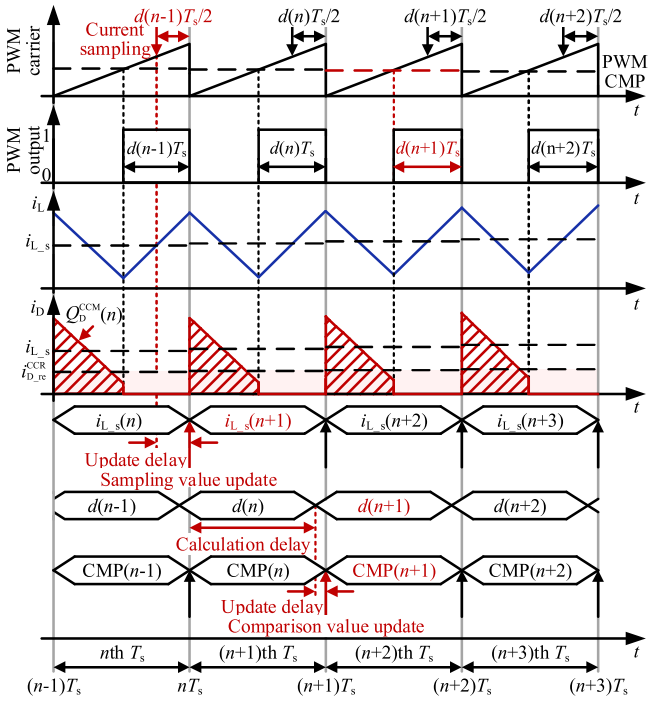

Fig. 4. Relationship between the inductor current and the diode current in CCM.

Therefore, the amount of charge flowing through the diode in CCM Q_D^{CCM} within the nth switching cycle can be expressed as

$$Q_D^{\mathrm{CCM}}(n) = i_{L\_s}(n+1)\left[1-d(n-1)\right]T_s \tag{8}$$

where $i_{L\_s}(n+1)$ represents the inductor current updated at the beginning of the $(n+1)$th switching cycle (sampled within the nth switching cycle), and $d(n\text{-}1)$ represents the duty cycle outputted within the nth switching cycle (calculated within the $(n\text{-}1)$th switching cycle).

According to (8), the diode current reconstructed by the CCR strategy $i_{D\_\mathrm{re}}^{\mathrm{CCR}}$ within the nth switching cycle can be obtained as

$$i_{D\_\mathrm{re}}^{\mathrm{CCR}}(n) = i_{L\_s}(n+1)\left[1-d(n-1)\right]. \tag{9}$$

According to (9), it can be seen that the single switching cycle current in CCM can be reconstructed only by the inherent inductor current sensor and the duty cycle information without any additional sensors.

B. Single Switching Cycle Current Reconstruction in DCM

The current characteristic diagram of DCM is shown in Fig. 5. It can be seen that the sampling value of inductor current is larger than the average value of inductor current within the nth switching cycle, which can be expressed as

$$i_{L\_s}(n+1) = \frac{i_{L\_a}(n)\,T_{\mathrm{s}}}{d(n-1)\,T_s + T_d(n)} \tag{10}$$

where i_{L_a} and T_d represent the average value and the decrease time of inductor current, respectively.

Based on the principle of voltage-second balance, the duty cycle and the decrease time of inductor current within the nth switching cycle can be calculated respectively as

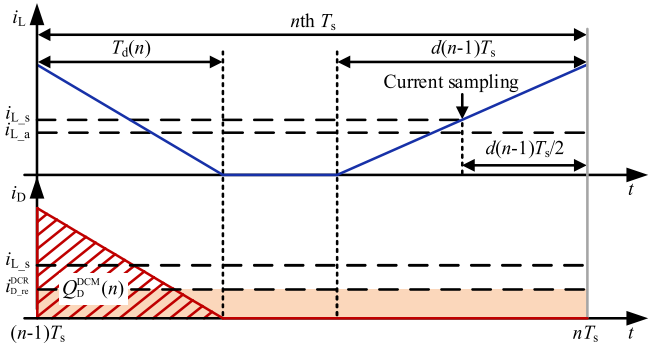

Fig. 5. Current characteristic diagram of DCM.

$$\begin{cases} d(n-1) = \dfrac{2Li_{L\_s}(n+1)}{u_{r\_s}(n+1)\,T_s} \\ T_d(n) = \dfrac{d(n-1)\,u_{r\_s}(n+1)\,T_s}{u_{\mathrm{dc\_}s}(n+1) - u_{r\_s}(n+1)} \end{cases} \tag{11}$$

where L represents the boost inductance and u_{r_s} and $u_{\mathrm{dc\_}s}$ represent the sampling values of rectifier voltage and dc-link voltage, respectively.

And the amount of charge flowing through the diode in DCM Q_D^{DCM} within the nth switching cycle can be expressed as

$$Q_D^{\mathrm{DCM}}(n) = \frac{i_{L\_s}(n+1)\,d(n-1)\,u_{r\_s}(n+1)\,T_s}{u_{\mathrm{dc\_}s}(n+1) - u_{r\_s}(n+1)}. \tag{12}$$

Therefore, the diode current reconstructed by the DCR strategy $i_{D\_\mathrm{re}}^{\mathrm{DCR}}$ within the nth switching cycle can be obtained as

$$i_{D\_\mathrm{re}}^{\mathrm{DCR}}(n) = \frac{i_{L\_s}(n+1)\,d(n-1)\,u_{r\_s}(n+1)}{u_{\mathrm{dc\_}s}(n+1) - u_{r\_s}(n+1)}. \tag{13}$$

Combining (13) with (9), similar to CCM, the single switching cycle current in DCM can also be reconstructed without any additional sensors. The difference is that (13) needs rectifier voltage and dc-link voltage, which may further cause the current reconstruction error.

C. Extraction and Error Analysis of the Capacitor Current

In practical systems, the inductance voltage u_L is lower than the boost inductor voltage u_{BL} due to the voltage division of inductor internal resistance. In addition, when the operating mode is misjudged, the CCR strategy and the DCR strategy are used in DCM and CCM, respectively. They decrease the reconstruction accuracy of capacitor current, therefore, it is important to analyze the reconstruction error of capacitor current considering the above effect. The equivalent circuit of boost PFC converter considering the effect of voltage division of internal resistance is shown in Fig. 6, and the internal resistance voltage u_{RL} within the nth switching cycle can be approximately expressed as

$$u_{RL}(n) = i_{L\_a}(n)\,R_L \tag{14}$$

where R_L represents the boost inductor internal resistance.

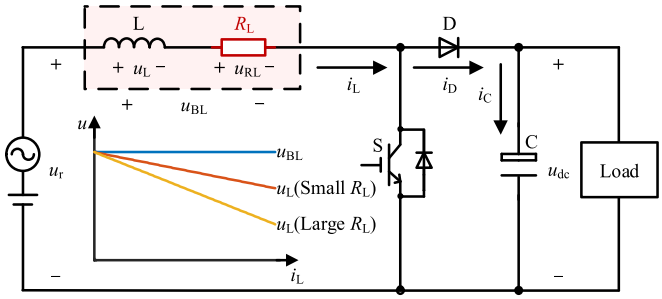

Fig. 6. Equivalent circuit of boost PFC converter considering the effect of voltage division of internal resistance.

According to (13) and (14), considering the effect of the voltage division of internal resistance, the actual diode current in DCM i_D^{DCM} within the nth switching cycle can be expressed as

$$i_D^{\mathrm{DCM}}(n)=\frac{i_{L\_s}(n+1)\,d(n-1)\,[u_{r\_s}(n+1)-i_{L\_a}(n)\,R_L]}{u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)+i_{L\_a}(n)\,R_L}. \tag{15}$$

Combining (9), the actual diode current within the nth switching cycle can be approximately expressed as

$$i_D(n)=\begin{cases} i_D^{\mathrm{DCM}}(n) \\ i_D^{\mathrm{CCM}}(n)=i_{L\_s}(n+1)\,[1-d(n-1)] \end{cases} \tag{16}$$

where i_D^{CCM} represents the actual diode current in CCM.

Therefore, according to (9) and (16), within the nth switching cycle, the reconstruction error of diode current for the CCR strategy E_{iD}^{CCR} in CCM is approximately zero, and E_{iD}^{CCR} in DCM can be calculated as

$$E_{iD}^{\mathrm{CCR}}(n)=\frac{i_{D\_\mathrm{re}}^{\mathrm{CCR}}(n)}{i_D^{\mathrm{DCM}}(n)}-1$$
$$=\frac{[1-d(n-1)]\,[u_{r\_s}(n+1)-i_{L\_a}(n)\,R_L]}{d(n-1)\,[u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)+i_{L\_a}(n)\,R_L]}-1. \tag{17}$$

According (10), (11), and (14), the duty cycle in DCM within the nth switching cycle can be derived as

$$d(n-1)=$$
$$\sqrt{\frac{2Li_{L\_a}(n)\,[u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)+i_{L\_a}(n)\,R_L]}{u_{\mathrm{dc\_s}}(n+1)\,[u_{r\_s}(n+1)\,T_s-i_{L\_a}(n)\,R_L]}}. \tag{18}$$

In addition, the duty cycle in CCM within the nth switching cycle can be expressed as

$$d(n-1)=1-\frac{u_{r\_s}(n+1)-i_{L\_a}(n)\,R_L}{u_{\mathrm{dc\_s}}(n+1)}. \tag{19}$$

Substituting (19) into (16) and combining with (15), the actual diode current in CCM and DCM within the nth switching cycle can be uniformly expressed as

$$i_D(n)=\frac{i_{L\_s}(n+1)\,d(n-1)\,[u_{r\_s}(n+1)-i_{L\_a}(n)\,R_L]}{u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)+i_{L\_a}(n)\,R_L}. \tag{20}$$

According to (13) and (20), within the nth switching cycle, the reconstruction error of diode current for the DCR strategy E_{iD}^{DCR} in CCM and DCM can be calculated as

$$E_{iD}^{\mathrm{DCR}}(n)=\frac{i_{D\_\mathrm{re}}^{\mathrm{DCR}}(n)}{i_D(n)}-1$$
$$=\frac{[u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)+i_{L\_a}(n)\,R_L]\,u_{r\_s}(n+1)}{[u_{r\_s}(n+1)-i_{L\_a}(n)\,R_L]\,[u_{\mathrm{dc\_s}}(n+1)-u_{r\_s}(n+1)]}-1. \tag{21}$$

And the sampling value of rectifier voltage within the nth switching cycle can be obtained

$$u_{r\_s}(n+1)=U_r\,|\sin\theta_{ur}(n+1)| \tag{22}$$

where U_r and θ_{ur} represent the amplitude and the phase of rectifier voltage, respectively.

The converter parameters are given in Table I, the amplitude of inductor current at the rated speed of the compressor is approximately 8 A, and R_L is set to 0.2 0.3, and 0.4 Ω, respectively. According to (17), (18), (21), and (22), under different θ_{ur} and i_{L_a}, the reconstruction errors of diode current can be obtained for two strategies in DCM and CCM within a switching cycle, respectively, as shown in Fig. 7. In Fig. 7(a), when the converter operates in DCM, E_{iD}^{DCR} is much smaller than E_{iD}^{CCR}. When θ_{ur} is between 0 and $\pi/2$, with θ_{ur} increases, E_{iD}^{CCR} first increases and then decreases, and with i_{L_a} decreases, E_{iD}^{CCR} increases. In Fig. 7(b), when the converter operates in CCM, E_{iD}^{CCR} is close to zero. With θ_{ur} increases, E_{iD}^{DCR} first increases and then

TABLE I
PARAMETERS OF EXPERIMENTAL PLATFORM

Parameter	Value
Grid voltage	220 Vrms
Grid frequency	50 Hz
Switching frequency	40 kHz
DC-link voltage	350 V
Boost inductance	500 μH
Rated speed	3000 r/min

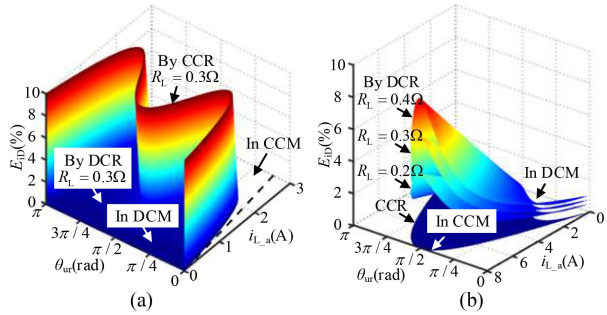

Fig. 7. Single switching cycle current reconstruction errors in different operating modes. (a) Discontinuous conduction mode. (b) Continuous conduction mode.

decreases, which reaches the maximum when θ_{ur} is $\pi/2$, and with i_{L_a} and R_L increase, E_{iD}^{DCR} increases.

According to the above analysis, considering the effect of the voltage division of boost inductor internal resistance and the misjudgment of operating mode, within a switching cycle, the currents reconstructed by the CCR strategy in DCM and the DCR strategy in CCM are both larger than the actual value. On this basis, in order to reduce the effect of the above factors on the reconstruction accuracy of diode current, the smaller value of the currents reconstructed by two strategies is selected as the final diode current. The current reconstruction strategy based on error minimization (EMR) avoids the judgment of operating modes and automatically adopts the better one between the CCR strategy and the DCR strategy. And the diode current reconstructed by the EMR strategy $i_{D\_\mathrm{re}}^{\mathrm{EMR}}$ within the nth switching cycle can be expressed as

$$i_{D\_\mathrm{re}}^{\mathrm{EMR}}(n) = \min\left[i_{D\_\mathrm{re}}^{\mathrm{CCR}}(n), i_{D\_\mathrm{re}}^{\mathrm{DCR}}(n)\right]. \tag{23}$$

Assuming the feedback value completely tracks the reference value in the current loop, the sampling value of inductor current within the nth switching cycle can be directly written as

$$i_{L\_s}(n+1) = I_{L\_s}\left|\sin\theta_{\mathrm{ur}}(n+1)\right|. \tag{24}$$

Substituting (24) into (10), the average value of inductor current can be expressed as

$$i_{L\_a}(n) = \begin{cases} I_{L\_s}\left|\sin\theta_{ur}(n+1)\right|, \mathrm{CCM} \\ I_{L\_s}\left|\sin\theta_{\mathrm{ur}}(n+1)\right|\dfrac{d(n-1)T_s + T_d(n)}{T_{\mathrm{s}}}, \mathrm{DCM}. \end{cases} \tag{25}$$

And the grid power P_g can be derived as

$$P_g = \frac{1}{N}\sum_{n=1}^{N} u_{r\_s}(n+1)\, i_{L\_a}(n). \tag{26}$$

The second harmonic component of capacitor current can be extracted by the BPF and DFT. According to (9), (13), (20), and (23), the amplitudes of the reconstructed second harmonic component and the actual second harmonic component can be expressed, respectively, as

$$\begin{cases} I_{C\_2}^{X} = \mathrm{DFT}\left[i_{C\_2\_\mathrm{re}}^{X}(n)\right] = \mathrm{DFT}\left[\mathrm{BPF}\left[i_{D\_\mathrm{re}}^{\mathrm{X}}(n)\right]\right] \\ I_{C\_2} = \mathrm{DFT}\left[i_{C\_2}(n)\right] = \mathrm{DFT}\left[\mathrm{BPF}\left[i_D(n)\right]\right] \end{cases} \tag{27}$$

where X = CCR, DCR, and EMR, $i_{C\_2\_\mathrm{re}}^{X}$ represents the second harmonic component of capacitor current reconstructed by the X strategy, and i_{C_2} represents the actual second harmonic component of capacitor current.

According to (27), the reconstruction error of the second harmonic component of capacitor current can be calculated as

$$\mathrm{err}_{iC\_2}^{X} = \frac{I_{C\_2}^{X}}{I_{C\_2}} - 1 = \frac{\mathrm{DFT}\left[\mathrm{BPF}\left[i_{D\_\mathrm{re}}^{X}(n)\right]\right]}{\mathrm{DFT}\left[\mathrm{BPF}\left[i_D(n)\right]\right]} - 1. \tag{28}$$

The converter parameters are shown in Table I, and R_L is set to 0.3 Ω. The base value of the root-mean-square value of grid voltage is set to 220 V, and the unit value is defined as k. Under different k and P_g, the reconstruction errors of the second

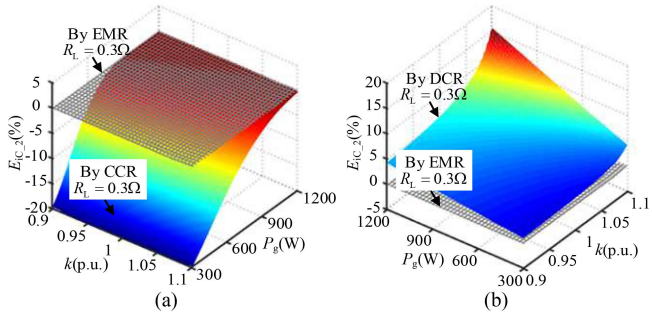

Fig. 8. Analysis of capacitor current reconstruction errors. (a) CCR and EMR. (b) DCR and EMR.

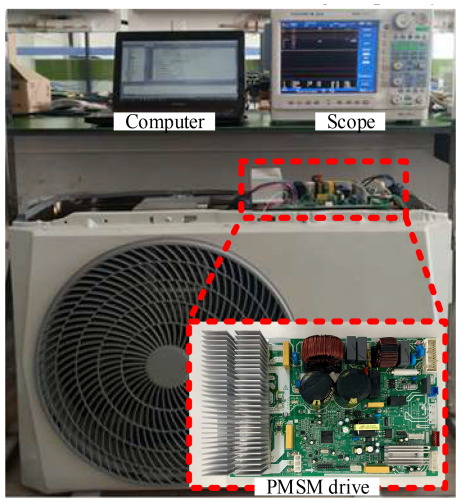

Fig. 9. Experimental platform of permanent magnet compressor system driven by boost PFC converter.

harmonic component for the CCR strategy, the DCR strategy, and the EMR strategy can be obtained, respectively, as shown in Fig. 8. In Fig. 8(a), the second harmonic component of capacitor current reconstructed by the CCR strategy is smaller than the actual value and $E_{iC\_2}^{\mathrm{CCR}}$ is negative. When P_g remains unchanged, $E_{iC\_2}^{\mathrm{CCR}}$ is less influenced by k, and when k remains unchanged, with P_g decreases, the absolute value of $E_{iC\_2}^{\mathrm{CCR}}$ increases. In Fig. 8(b), the second harmonic component of capacitor current reconstructed by the DCR strategy is larger than the actual value and $E_{iC\_2}^{\mathrm{CCR}}$ is positive. When P_{g} remains unchanged, $E_{iC\_2}^{\mathrm{DCR}}$ increases with k increases, and when k remains unchanged, $E_{iC\_2}^{\mathrm{DCR}}$ increases with P_{g} increases. In addition, it can be seen that $E_{iC\_2}^{\mathrm{EMR}}$ remains near zero under different k and P_g, so the reconstruction accuracy of the second harmonic component of capacitor current can be effectively improved by the EMR strategy across a wide power range.

IV. Experimental Results

The proposed strategy was verified on the experimental platform of permanent magnet compressor system driven by boost PFC converter, as shown in Fig. 9. The parameters of experimental platform are given in Table I. The proposed strategy utilizes

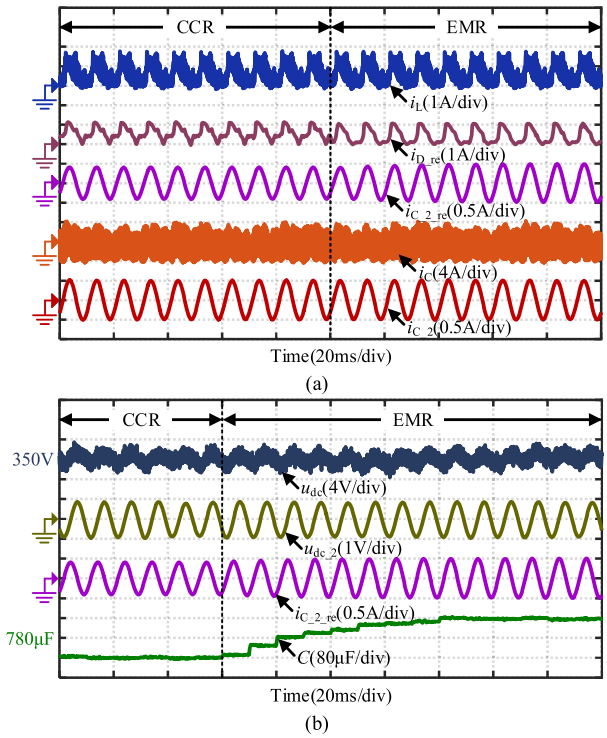

Fig. 10. Experimental results under light load (MCM, 863.1 μF and 150 W). (a) Current reconstruction waveforms. (b) Capacitance estimation waveforms.

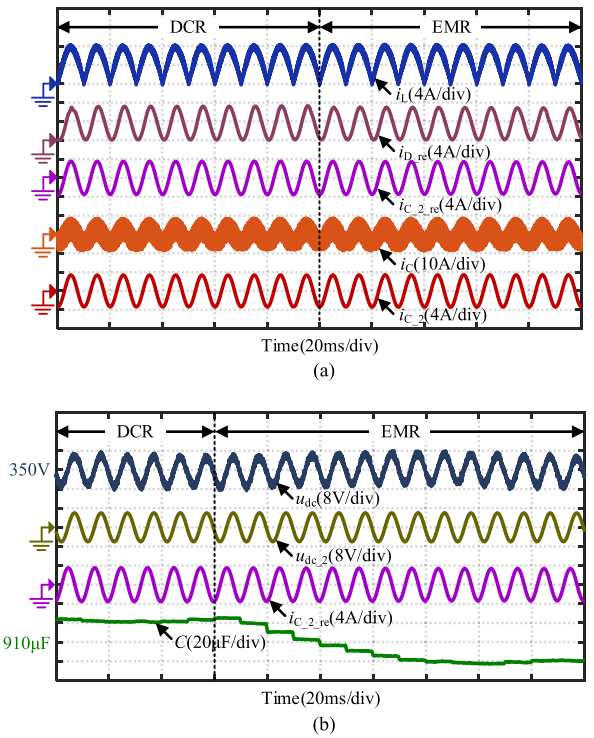

Fig. 11. Experimental results under heavy load (CCM, 863.1 μF and 1200 W). (a) Current reconstruction waveforms. (b) Capacitance estimation waveforms.

the existing resources in the boost PFC converter to estimate the dc-link capacitance, and the control algorithm is executed by the R5F562T7DDF microcontroller of Renesas RX62T series with the switching frequency of 40 kHz.

In order to verify the effectiveness of the proposed strategy under light load (MCM), the experimental results when the dc-link capacitance is 863.1 μF and the grid power is 150 W are shown in Fig. 10. In Fig. 10(a), when adopting the CCR strategy, the reconstructed diode current is larger in DCM within a switching cycle, which results in a smaller reconstructed second harmonic component of capacitor current than the actual value. After adopting the EMR strategy, with the reconstructed diode current decreases, the reconstructed second harmonic component of capacitor current increases and is closer to the actual value. In Fig. 10(b), when adopting the CCR strategy, due to the smaller reconstructed second harmonic component of capacitor current, the estimated dc-link capacitance is smaller and stabilizes at 700.6 μF. After adopting the EMR strategy, the estimated dc-link capacitance increases and stabilizes at 858.6 μF after a transition time of 80 ms. Therefore, the capacitance estimation error decreases from 18.8% to 0.5%.

In order to verify the effectiveness of the proposed strategy under heavy load (CCM), the experimental results when the grid power is 1200 W are shown in Fig. 11. In Fig. 11(a), when adopting the DCR strategy, the reconstructed diode current is larger within a switching cycle at the peak, which results in a larger reconstructed second harmonic component of capacitor current than the actual value. After adopting the EMR strategy, with the reconstructed diode current at the peak decreases, the reconstructed second harmonic component of capacitor current decreases and is closer to the actual value. In Fig. 11(b), when adopting the DCR strategy, due to the larger reconstructed second harmonic component of capacitor current, the estimated dc-link capacitance is larger and stabilizes at 932.4 μF. After adopting the EMR strategy, the estimated dc-link capacitance decreases and stabilizes at 889.4 μF after a transition time of 80 ms. Therefore, the capacitance estimation error decreases from 8.0% to 3.0%.

When the grid power changes between 150 and 250 W, the experimental results adopting the EMR strategy in MCM are shown in Fig. 12. In Fig. 12(a), during the dynamic process of power change, the estimated dc-link capacitance is between 861.1 μF and 882.2 μF, and the capacitance estimation error is 2.2%. In Fig. 12(b), when the grid power stabilizes at 150 W, the estimated dc-link capacitance is between 846.3 μF and 874.1 μF, and the capacitance estimation error is 1.9%. In Fig. 12(c), when the grid power stabilizes at 250 W, the estimated dc-link capacitance is between 869.1 μF and 881.9 μF, and the capacitance estimation error is 2.2%. Therefore, the capacitance estimation error when the grid power changes in MCM is less than 3%.

When the dc-link capacitance changes to 608.7 μF and the grid power changes between 200 W and 400 W, the experimental results adopting the EMR strategy in MCM and CCM are shown in Fig. 13. In Fig. 13(a), during the dynamic process of power change, the estimated dc-link capacitance is between 621.6 μF and 636.4 μF, and the capacitance estimation error is 4.6%. In Fig. 13(b), when the grid power stabilizes at 200 W, the estimated dc-link capacitance is between 613.7 μF and 625.7 μF, and the capacitance estimation error is 2.8%. In Fig. 13(c), when the grid

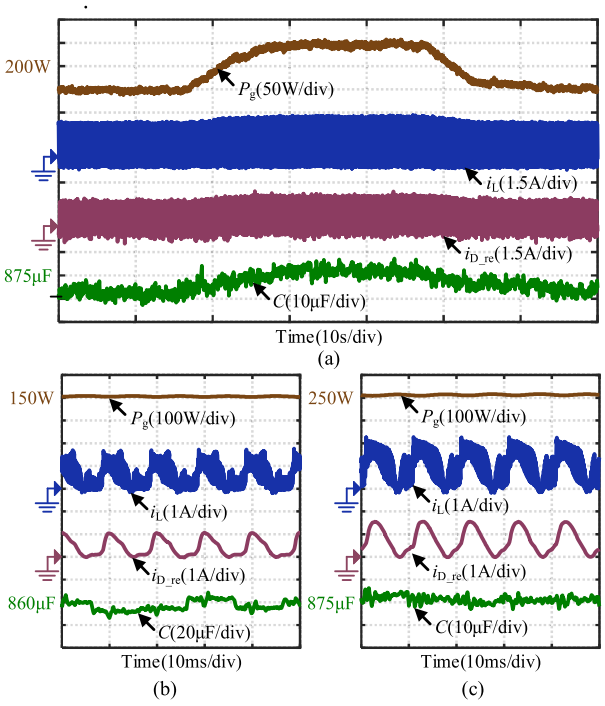

Fig. 12. Experimental results when the power changes in MCM (863.1 μF). (a) Dynamic waveforms. (b) Steady-state waveforms (150 W). (c) Steady-state waveforms (250 W).

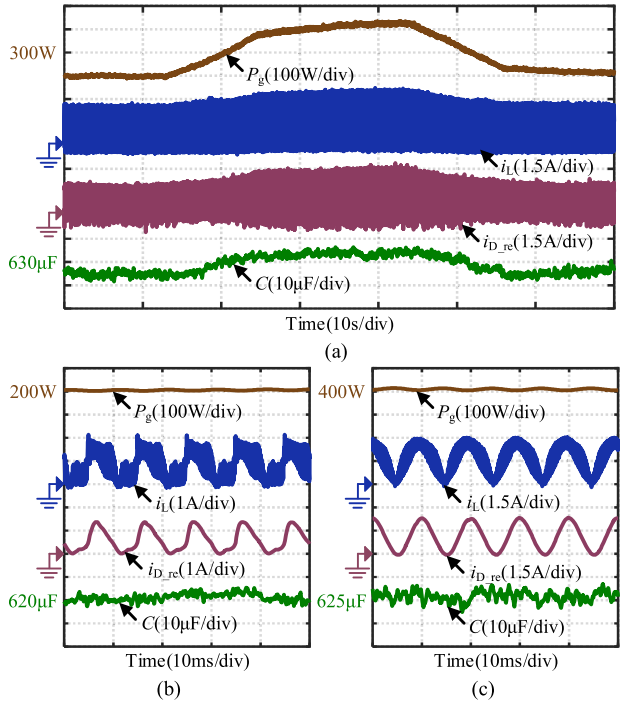

Fig. 13. Experimental results when the power changes between MCM and CCM (608.7 μF). (a) Dynamic waveforms. (b) Steady-state waveforms (200 W). (c) Steady-state waveforms (400 W).

power stabilizes at 400 W, the estimated dc-link capacitance is between 618.1 μF and 631.9 μF, and the capacitance estimation error is 3.8%. Therefore, the capacitance estimation error when the grid power changes between MCM and DCM is less than 5%.

When the dc-link capacitance changes to 1263.5 μF and the grid power changes between 800 W and 1000 W, the experimental results adopting the EMR strategy in CCM are shown in Fig. 14. In Fig. 14(a), during the dynamic process of power change, the estimated dc-link capacitance is between 1282.0 μF and 1294.2 μF, and the capacitance estimation error is 2.4%. In Fig. 14(b), when the grid power stabilizes at 800 W, the estimated dc-link capacitance is between 1284.8 μF and 1292.7 μF, and the capacitance estimation error is 2.3%. In Fig. 14(c), when the grid power stabilizes at 1000 W, the estimated dc-link capacitance is between 1289.1 μF and 1299.5 μF, and the capacitance estimation error is 2.8%. Therefore, the capacitance estimation error when the grid power changes in CCM is less than 3%.

The smaller the capacitance, the deeper the aging degree of dc-link capacitors. To verify the effectiveness of the proposed strategy when dc-link capacitors age deeply (379.3 μF), the experimental results in MCM (150 W) and CCM (1200 W) are shown in Fig. 15. In Fig. 15(a), when the grid power stabilizes at 150 W, the estimated dc-link capacitance is between 370.4 μF and 387.2 μF, and the capacitance estimation error is 2.3%. In Fig. 15(b), when the grid power stabilizes at 1200 W, the estimated dc-link capacitance is between 376.3 μF and 397.8 μF, and the capacitance estimation error is 4.9%. Therefore, the proposed strategy can effectively estimate the capacitance when dc-link capacitors age deeply (379.3 μF) and the capacitance estimation error is less than 5%.

To verify the practicality of the proposed strategy under grid conditions, the experimental results in MCM (150 W) and CCM (1200 W) are shown in. In Fig. 16(a), the grid voltage contains many harmonics, and the amplitude of the fundamental component of grid voltage is 321 V, which is greater than the theoretical value (311 V). In Fig. 16(b), the grid power stabilizes at 150 W, the estimated dc-link capacitance is between 821.4 μF and 843.1 μF, and the capacitance estimation error is 4.8%. In Fig. 16(c), the grid power stabilizes at 1200 W, the estimated dc-link capacitance is between 850.6 μF and 873.7 μF, and the capacitance estimation error is 1.5%. Therefore, the proposed strategy can effectively estimate the capacitance under grid conditions, and the capacitance estimation error is less than 5%.

The dc-link capacitance is usually implemented by two electrolytic capacitors in parallel to enhance both capacitance and ripple current handling capacity. To verify the adaptability of the proposed strategy, when the dc-link capacitance is implemented by a single capacitor (700.5 μF), the experimental results in MCM (150 W) and CCM (1200 W) are shown in Fig. 17. In Fig. 17(a), when the grid power stabilizes at 150 W, the estimated dc-link capacitance is between 673.1 μF and 694.8 μF, and the capacitance estimation error is 3.9%. In Fig. 17(b), when the grid power stabilizes at 1200 W, the estimated dc-link capacitance is between 695.3 μF and 714.2 μF, and the capacitance estimation error is 2.0%. Therefore, when the dc-link capacitance is implemented by a single capacitor, the proposed strategy can still effectively estimate the capacitance and the capacitance estimation error is less than 4%.

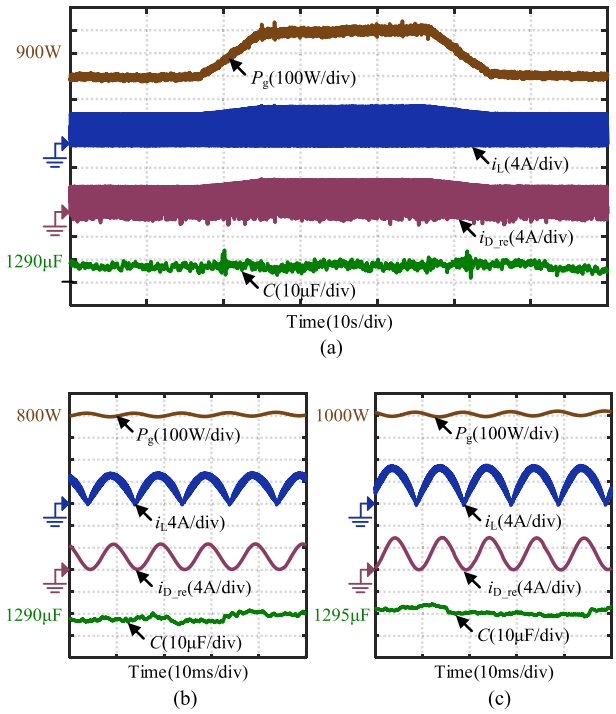

Fig. 14. Experimental results when the power changes in CCM (1263.5 μF). (a) Dynamic waveforms. (b) Steady-state waveforms (800 W). (c) Steady-state waveforms (1000 W).

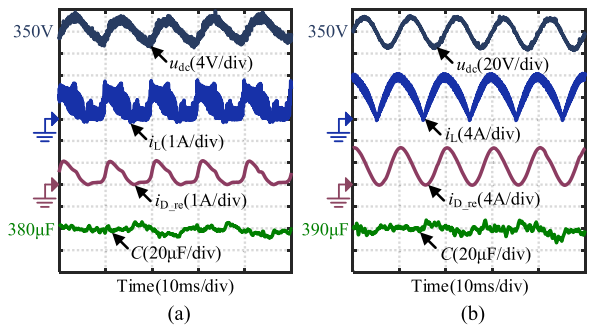

Fig. 15. Experimental results when dc-link capacitors age deeply (379.3 μF). (a) MCM (150 W). (b) CCM (1200 W).

In addition, to further verify the effectiveness of the proposed capacitance estimation strategy under different powers, when the grid power changes from 150 to 400 W in steps of 50 W and from 400 to 1200 W in steps of 200 W, the experimental results adopting the EMR strategy are shown in Fig. 18. And in order to minimize the error, the experimental waveforms within 0.1 s are analyzed. In Fig. 18, the capacitor current can be effectively reconstructed and the dc-link capacitance can be accurately estimated under different powers. And the current reconstruction error is less than 2.5% and the capacitance estimation error is less than 4%. The second harmonic component of inverter current, which is ignored in capacitance estimation, increases with grid power, so the estimation error increases with grid power. Besides, the estimation accuracy may also be affected by the nonideal factors, such as the parasitic capacitance, switch

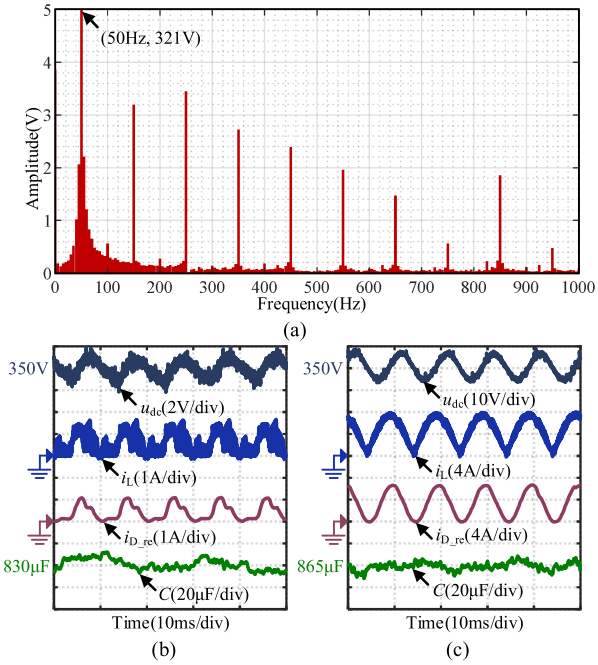

Fig. 16. Experimental results under grid conditions (863.1 μF). (a) Harmonic analysis results of grid voltage. (b) MCM (150 W). (c) CCM (1200 W).

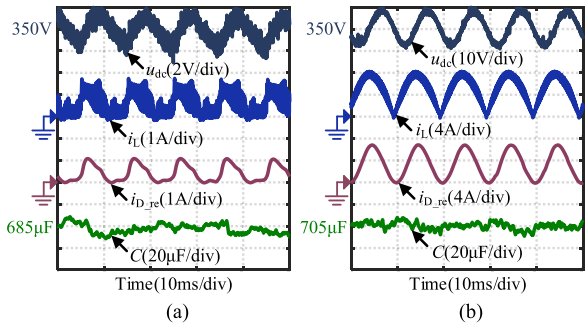

Fig. 17. Experimental results when the dc-link capacitance is implemented by a single capacitor (700.5 μF). (a) MCM (150 W). (b) CCM (1200 W).

TABLE II
TYPICAL DC-LINK CAPACITORS ESTIMATION SCHEMES

Reference	N_s	Additional devices	Errors
Lu et al. [25]	53	Trigger circuit, ripple extraction circuit, current amplifying circuit, and PC	ESR:<10%
Yao et al. [29]	1	Trigger circuit, ripple extraction circuit, isolated amplifier, and microcontroller	C:<2% ESR:<5%
Zhao et al. [30]	1	N/A	C:<3.5%
Proposed	1	N/A	C:<4%

delay and sampling delay, as well as the nonlinearity of capacitance including the dc bias characteristic and temperature characteristics.

The typical dc-link capacitors estimation schemes for boost PFC converters are given in Table II, where N_s and PC are the average number of sampling points per switching cycle and the personal computer, respectively. The strategy in [30] and the proposed strategy can estimate the capacitance without

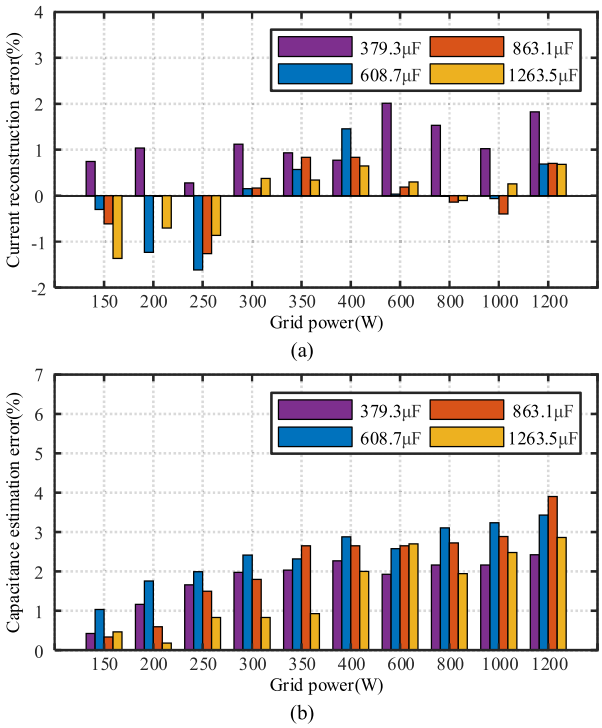

Fig. 18. Experimental results under different powers. (a) Current reconstruction error. (b) Capacitance estimation error.

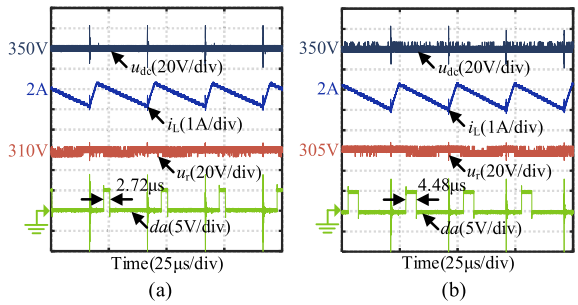

Fig. 19. Experimental comparison results of algorithm running time. (a) Strategy in [30]. (b) Proposed strategy.

additional sampling times and devices. To further verify the superiority of the proposed strategy, the experimental comparison results are tested between the strategy in [30] and the proposed strategy when the dc-link capacitance is 863.1 μF. The transient experimental condition required in [30] is implemented by a resistance box, and the load power suddenly drops from 500 to 250 W.

The experimental comparison results of algorithm running time are shown in Fig. 19, where *da* is the output of digital-to-analog converter. The algorithm running time is tested by the IO port and the digital-to-analog converter. The IO port is set to 1 when the algorithm starts and the IO port is set to 0 when the algorithm ends, and the digital signal 1 corresponds to the analog signal 5 V. In Fig. 19(a), the algorithm running time of the strategy in [30] is 2.72 μs. In Fig. 19(b), the algorithm running time of the proposed strategy is 4.48 μs. Although the proposed

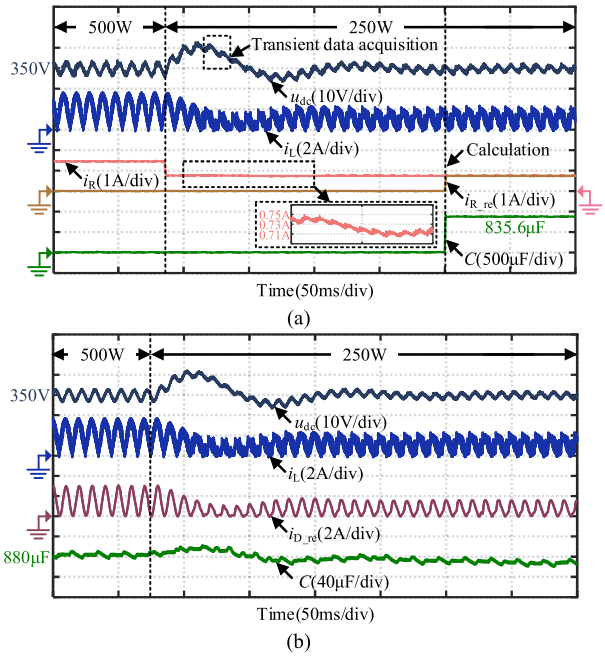

Fig. 20. Experimental comparison results of waveforms. (a) Strategy in [30]. (b) Proposed strategy.

strategy requires slightly longer algorithm running time, it is still easy to implement in a microcontroller.

The experimental comparison results of waveforms are shown in Fig. 20, where i_R and i_{R_re} are the load current and the reconstructed load current, respectively. In Fig. 20(a), the strategy in [30] is suitable for transient, the estimated dc-link capacitance is 835.6 μF, and the capacitance estimation error is 3.2%. In the strategy, the load current fluctuation in transient is ignored and the load current is approximated by the calculated value in steady-state, which may reduce the estimation accuracy under heavy load conditions. In Fig. 20(b), the proposed strategy is suitable for steady-state, the estimated dc-link capacitance is between 860.1 μF and 891.3 μF in steady state, and the capacitance estimation error is 3.3%. Therefore, the estimation accuracy of two strategies is similar, and both can effectively estimate the dc-link capacitance.

Compared with the strategy in [30], the proposed strategy does not require the pre-testing for efficiency, setting voltage thresholds to determine transient and steady state, and setting a power threshold to determine the operating mode. Therefore, the proposed strategy is simpler to implement and has better adaptability to different boost PFC converters. In addition, the estimation time of the strategy in [30] is over ten line cycles, but the estimation time of the proposed strategy is only one line cycle, so the proposed strategy has better real-time performance.

V. Conclusion

In this article, an online estimation strategy of dc-link capacitance based on current hybrid reconstruction by charge equivalence for boost PFC converters is proposed. In order to obtain capacitor current, the CCR strategy and DCR strategy

are proposed to reconstruct the diode current within a switching cycle based on charge equivalence, respectively. The effect of the voltage division of boost inductor internal resistance and the misjudgment of operating mode on two strategies is analyzed. The hybrid EMR strategy is generated by combining two strategies based on error minimization, which avoids judging the operating mode and effectively improves the reconstruction accuracy of capacitor current. The experimental results indicate that the average current reconstruction error and the average capacitance estimation error are less than 2.5% and 4% across a wide power range, respectively. Compared with the existing estimation strategies, the proposed strategy has the advantages of low cost and easy implementation, because it does not require additional sampling times, hardware devices, and data processing tools.

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