Current Ripple Prediction and ZVS-Based Variable Switching Frequency Control for Interleaved Multiphase Three-Level DC–DC Converter

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***Abstract*—For high-power applications, the interleaved three-level dc–dc converter is a preferred topology to meet high voltage and high current demands. However, due to the coupling effect of multiple switches, the inductor current is not a standard triangular waveform, complicating analysis and control in near-critical conduction mode (near-CRM). This article proposes an inductor current ripple prediction method and establishes a unified current ripple expression for an interleaved *n*-phase three-level dc–dc converter. The unified expression for predicting current ripple is applicable to any multiphase, eliminating the traditional cumbersome solution using segmented duty cycles and case-by-case analysis for each interleaved phase number. Based on the current ripple prediction, a variable switching frequency control method is proposed that does not require additional high-frequency sensors or auxiliary circuits, enabling zero-voltage switching (ZVS) in near-CRM. The required switching frequency is calculated within a digital controller based on current ripple prediction instead of current zero-crossing detection. The proposed current ripple prediction and ZVS-based variable switching frequency control are validated in an IGBT-based 15.6-kW three-phase interleaved three-level dc–dc converter, achieving maximum efficiency of 98.03%.**

***Index Terms*—Interleaved three-level dc–dc converter, near-critical conduction mode (near-CRM), variable switching frequency control, zero-voltage switching (ZVS).**

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I. Introduction

DC microgrid technology holds significant research value as an optimal means to fully utilize the efficiency of distributed power sources. The dc microgrid system, shown in Fig. 1, comprises various dc–dc converters connecting energy storage batteries, photovoltaic systems, electric vehicle charging piles, fuel cells, hydrogen electrolyzers, and other dc loads [1], [2], [3], [4]. These dc–dc converters serve as crucial interfaces between the dc bus and the power equipment [5], [6].

To achieve high efficiency, high power, compact size, and low current ripple in dc–dc converters for dc microgrid applications, interleaving and three-level techniques are widely favored [7], [8], [9], [10], [11]. One such example is the interleaved three-level dc–dc converter topology. This topology not only reduces the required voltage and current stress of power semiconductor devices but also diminishes the volume of passive components [12], [13], [14]. Additionally, the scalability and modularity of the interleaved three-level topology are advantageous in meeting various power-grade application demands [15].

Typically, interleaved three-level dc–dc converters operate in continuous conduction mode with hard-switching, leading to substantial switching losses and electromagnetic interference. To mitigate these issues, soft-switching technology is employed, particularly zero-voltage switching (ZVS) [16], [17], which effectively eliminates turn-ON losses and the body diode reverse recovery losses of power semiconductor devices. Conventionally, some auxiliary circuits or components are added to the main power topology to realize ZVS [18], [19]. For instance, some inductors, capacitors, and power semiconductor switches are added in [20], [21], and [22] to build a resonant transition for ZVS. However, these methods increase the hardware complexity and cost of the converter, limiting their application in high-power scenarios.

To eliminate additional auxiliary circuits, an effective way to achieve ZVS is to make the inductor current have both positive and negative peak values in each switching cycle. The operating principle of this idea is known as triangular current mode (TCM) or near-critical conduction mode (near-CRM) [23], [24], [25]. It has been successfully applied in buck/boost dc–dc converters [26], single-phase and three-phase inverters [19], [27], power factor correction rectifiers [28], and three-level dc–dc converters [25], [29]. To enable ZVS, it must take some effective means to

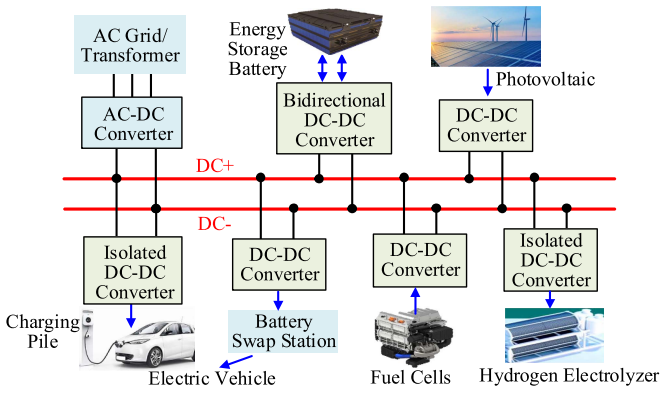

Fig. 1. Configuration diagram of a microgrid system with common DC buses.

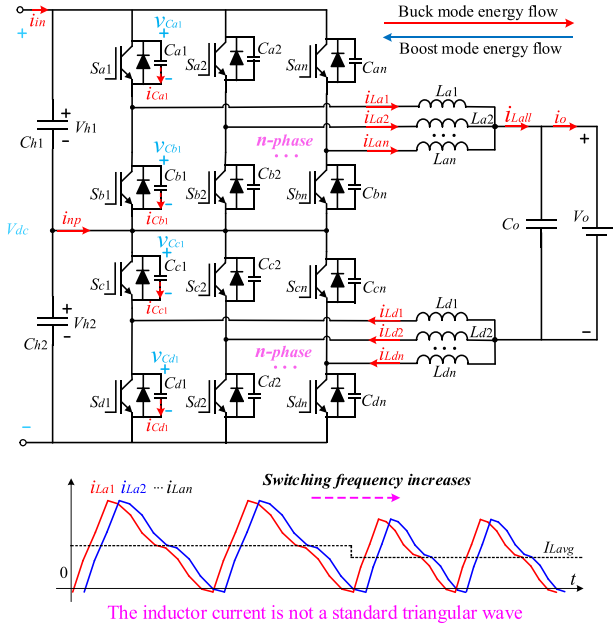

Fig. 2. Main topology of the interleaved n-phase three-level bidirectional DC–DC converter. Due to the coupling effect of multiple switches, the inductor current is not a standard triangular wave.

ensure that these converters work in TCM or near-CRM. Active zero-crossing detection methods are used in [30], [31], and [32] by adding some auxiliary hardware, such as a voltage sensing circuit, current sensor, or electroluminescence detection circuit. To avoid the complicated auxiliary hardware for current zero-crossing detection, the variable switching frequency method based on the measurement of input/output voltage and average current is adopted in [7], [29], and [33] to make the converter in near-CRM to realize ZVS. These methods mainly focus on two-level and noninterleaved three-level dc–dc converters with conventional triangular inductor current waveforms.

Unfortunately, ensuring ZVS in an interleaved three-level dc–dc converter is challenging because all the switches are mutually coupled, resulting in nonstandard triangular inductor current waveforms except at a few specific duty cycle points [13]. Although zero-crossing detection can be applied to each inductor current, the switching frequency can only be determined by one of them to maintain the interleaving advantage. In [13] and [14], the inductor current ripple is solved by using segmented duty cycles for two-phase and three-phase interleaved three-level dc–dc converters. However, this method requires case-by-case analysis and a cumbersome solution for each case of interleaved phase number, which cannot be extended to any n-phase interleaved three-level topology.

In this article, the inductor current ripple prediction method for interleaved n-phase three-level dc–dc converter is proposed and its unified current ripple expression is derived. The unified expression for predicting current ripple is applicable to any multiphase, eliminating the traditional cumbersome case-by-case analysis and solution. A variable switching frequency control method based on the current ripple prediction is proposed to enable ZVS in near-CRM. Using this method, any n-phase interleaved three-level dc–dc converter can be effectively analyzed and controlled to achieve ZVS without the need for zero-crossing detection sensors or circuits. The working principle and ZVS implementation process are introduced in Section II. Section III details the proposed method for current ripple prediction and variable switching frequency control. Experimental verification of this current ripple prediction and control method is presented in Section IV. Finally, Section V concludes this article.

II. Basic Working Principle and ZVS in Near-CRM

The main topology of the interleaved multiphase three-level bidirectional dc–dc converter is shown in Fig. 2, which is operated in near-CRM to achieve ZVS. Due to the coupling effect of multiple switches, the inductor current is not a standard triangular wave. This converter mainly consists of n upper and n lower switched half-bridges. C_{a1}–C_{an}, C_{b1}–C_{bn}, C_{c1}–C_{cn}, and C_{d1}–C_{dn} in parallel with each IGBT are output parasitic capacitors or additional resonance capacitors.

A. Basic Working Principle

In the interleaved multiphase three-level bidirectional dc–dc converter, S_{a1}–S_{an} and S_{d1}–S_{dn} are considered as the main switches. Additionally, S_{a1}–S_{an} and S_{b1}–S_{bn}, as well as S_{d1}–S_{dn} and S_{c1}–S_{cn}, function as complementary switches. The triangular carrier of each switched half-bridge is phase-shifted by $2\pi/(2n)$. Specifically, the carrier phase degree of the main switch S_{ai} is $\pi(2i\text{-}2)/n$, and the carrier phase degree of the main switch S_{di} is $\pi(2i\text{-}1)/n$. Consequently, the inductor current ripples of the corresponding $2n$ inductors are staggered by $2\pi/(2n)$, so that the total output current ripple is $2n$ times the switching frequency. The basic operating waveforms in buck mode are analyzed as an example, as shown in Fig. 3, and the analysis of the operating process in boost mode is similar. The duty cycles of the main switches S_{a1}–S_{an} and S_{d1}–S_{dn} are D_{a1}–D_{an} and D_{d1}–D_{dn}, respectively.

The average output voltage derived from the volt–second balance and the superposition theorem is

$$V_o = \frac{V_{h1}}{n}\sum_{i=1}^{n} D_{ai} + \frac{V_{h2}}{n}\sum_{i=1}^{n} D_{di} \tag{1}$$

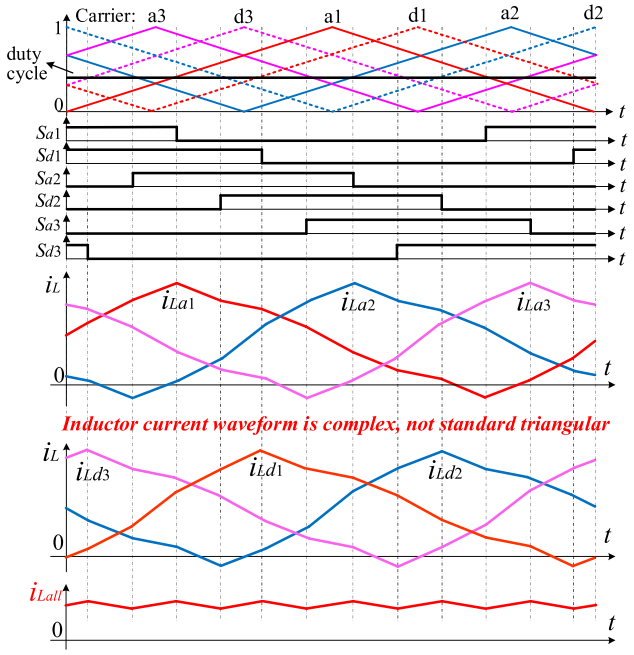

Fig. 3. Typical modulation waveforms for an interleaved three-phase (using $n = 3$ as an example) three-level bidirectional DC–DC converter.

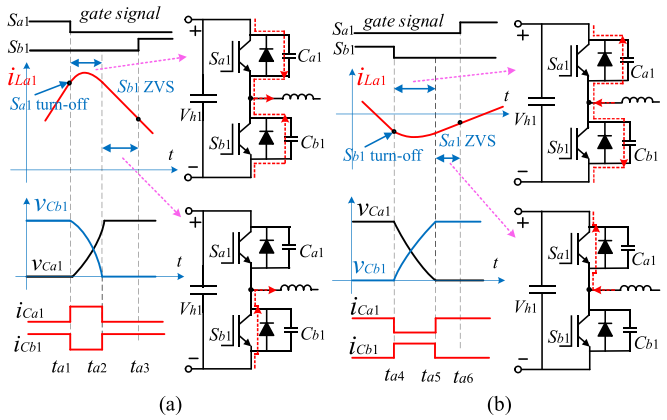

Fig. 4. ZVS turn-ON process of switches S_{a1} and S_{b1} at (a) positive peak current and (b) negative valley current.

where D_{ai} is the duty cycle of the main switch S_{ai}, and D_{di} is the duty cycle of the main switch S_{di}, $i = 1, 2, \ldots, n$.

If the duty cycles of all $2n$ main switches are equal to D, the output voltage can finally be written as

$$V_o = DV_{h1} + DV_{h2} = DV_{\rm dc}. \tag{2}$$

B. ZVS Implementation in Near-CRM

As shown in Fig. 3, when the main switch is ON, the corresponding inductor current rises from a negative value to a positive value. The ZVS and resonance process occur at both the peak and valley of the inductor current. Due to the symmetrical topology of the converter circuit, the equivalent circuits and resonant processes are similar for all half-bridges. Therefore, to simplify the analysis, only the first upper half-bridge, consisting of S_{a1} and S_{b1}, is shown in Fig. 4.

At the positive peak inductor current, as shown in Fig. 4(a), the main switch S_{a1} turns OFF and triggers a resonant transition during the interval t_{a1}–t_{a2}. The inductor $L_{\rm a1}$ resonates with the parasitic capacitors C_{a1} and C_{b1} until the voltage of C_{b1} is clamped to zero by the antiparallel diode of the main switch S_{b1}. As long as the inductor current at t_{a1} is greater than zero, meaning the current flows through the antiparallel diode of S_{b1}, S_{b1} will be turned ON with ZVS.

Similarly, at the negative valley inductor current, as shown in Fig. 4(b), the resonant transition is triggered at the turn-OFF moment t_{a4} of the main switch S_{b1}. During the resonance interval t_{a4}–t_{a5}, the capacitor C_{b1} is gradually charged to V_{h1} and the capacitor C_{a1} is gradually discharged to 0. If the inductor current at t_{a6} is less than zero, meaning the current flows through the antiparallel diode of S_{a1}, S_{a1} can also be turned ON with ZVS.

To achieve ZVS for all switches, referring to the detailed resonance process in [7], [14], and [34], each peak and valley current at the turn-OFF moment of the main switch must satisfy

$$\begin{cases} I_{p+} > \sqrt{\frac{CV_{\rm dc}(2V_o - V_{\rm dc})}{2L}} \\ I_{p-} < -\sqrt{\frac{CV_{\rm dc}(V_{\rm dc} - 2V_o)}{2L}} \end{cases} \tag{3}$$

where C represents the charge-equivalent capacitance from 0 to $0.5V_{\rm dc}$ for the output parasitic capacitor of the power switch [34].

The worst case scenario for holding the ZVS condition in (3) is $V_o = 0$ or $V_o = V_{\rm dc}$. Specifically, $V_o = 0$ is the worst case scenario for buck mode, and $V_o = V_{\rm dc}$ is the worst case scenario for boost mode. To mitigate the effect of the tolerance in capacitance and inductance values (e.g., $\pm 10\%$ tolerance), larger current limits of $I_{p+} = +1.5$ A and $I_{p-} = -1.5$ A are used as margins in the experiment, with $L = 380$ μH and parasitic $C_{\rm oes} = 0.58$ nF given in the datasheet of IGBT 39AC12T4V1.

III. Proposed Method for Current Ripple Prediction and Variable Switching Frequency Control

A. Current Ripple Analysis

Conventionally, the inductor currents in two-level and three-level dc–dc converters are standard triangle waves. However, the inductor current of the interleaved multiphase three-level dc–dc converter is affected not only by the switching state of its own half-bridge but also by the switching states of the other half-bridges, so that the waveform of the inductor current is not a standard triangular wave, as shown in Fig. 3. To control the converter to operate in near-CRM by adjusting the switching frequency in real time, it is important to derive a unified analytical equation for the inductor current ripple in full duty cycle ranges.

Taking the three-phase interleaved three-level dc–dc converter with a duty cycle range of $2/6 < D < 3/6$ as an example, based on the interleaved phase-shift modulation, the inductor current during one switching cycle can be divided into 12 segments, as shown in Fig. 5. Ignoring the nonlinear inductance problem [35],

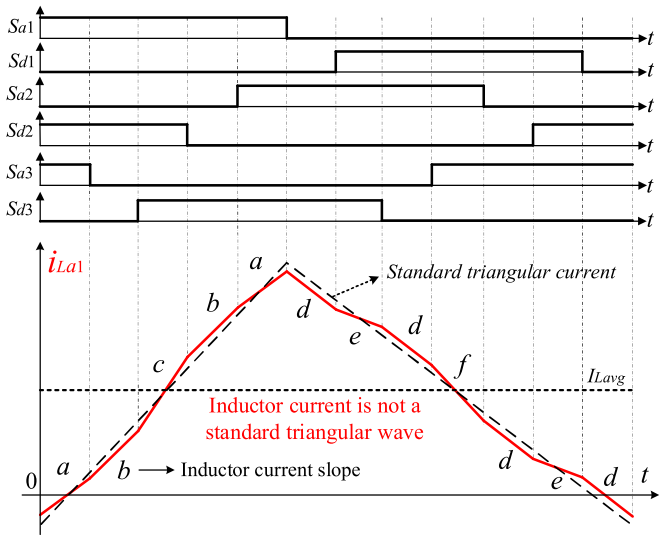

Fig. 5. Inductor current waveform during $2/6 < D < 3/6$ using a three-phase interleaved three-level bidirectional DC–DC converter as an example.

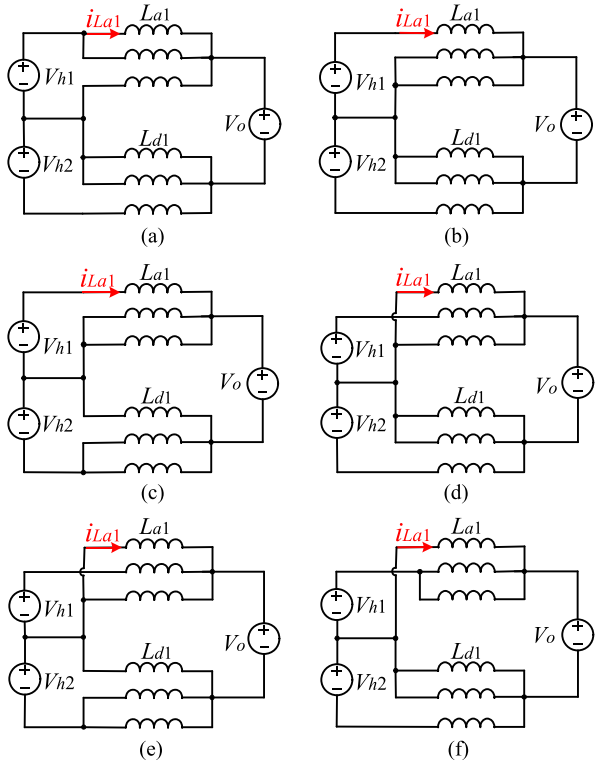

Fig. 6. Equivalent circuits corresponding to the slopes of the inductor current waveforms in Fig. 5.

the slope of the inductor current waveform is mainly determined by the switch combination.

The slopes of the inductor current in Fig. 5 correspond to six types of equivalent circuits shown in Fig. 6, where the inductor current follows the slope order: *abcba-dedfded*.

To handle such a complex inductor current waveform consisting of multiple line segments, the superposition principle is

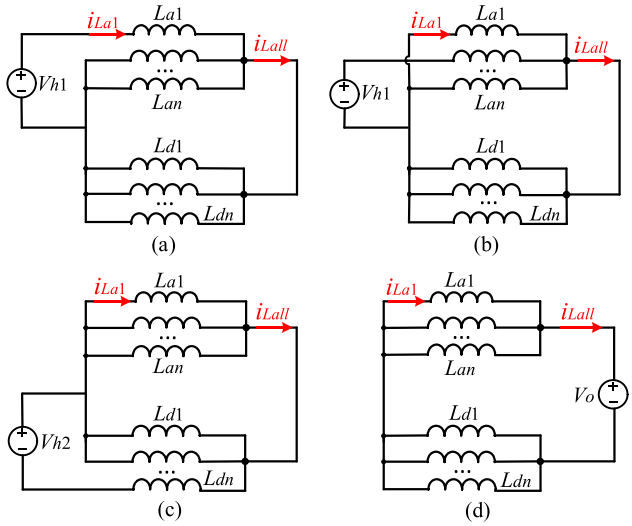

Fig. 7. Time-division equivalent circuits with the independent action of each voltage source with (a) only $S_{a1} = 1$, (b) only $S_{ai} = 1$ ($i = 2, 3, \ldots, n$), (c) only $S_{di} = 1$ ($i = 1, 2, \ldots, n$), and (d) only considering V_o.

used in this article to simplify these different types of switching states. Each segment of the inductor current slope in Fig. 5 can be viewed as a superposition of the effects of the main switch acting individually on the inductor L_{a1}.

B. Proposed Current Ripple Prediction Method for n-Phase

By distinguishing the role of the $2n$ main switches in the interleaved n-phase three-level dc–dc converter, they can be divided into four types of time-division equivalent circuits with the independent action of each voltage source, as shown in Fig. 7.

When only $S_{a1} = 1$ in these main switches, as shown in Fig. 7(a), the slope of the inductor current i_{La1} is

$$k_1 = \frac{di_{La1\_Sa1}}{dt} = \frac{(2n-1)\,V_{h1}}{2nL}. \tag{4}$$

When only $S_{ai} = 1$ ($i = 2, 3, \ldots, n$) in these main switches, as shown in Fig. 7(b), the slope of the inductor current i_{La1} is

$$k_2 = \frac{di_{La1\_Sai}}{dt} = \frac{-V_{h1}}{2nL}, i = 2, 3, \ldots, n. \tag{5}$$

When only $S_{di} = 1$ ($i = 1, 2, \ldots, n$) in these main switches, as shown in Fig. 7(c), the slope of the inductor current i_{La1} is

$$k_3 = \frac{di_{La1\_Sdi}}{dt} = \frac{V_{h2}}{2nL}, i = 1, 2, \ldots, n. \tag{6}$$

When all the main switches are OFF and only V_o is considered, as shown in Fig. 7(d), the slope of the inductor current i_{La1} is

$$k_4 = \frac{di_{La1\_Vo}}{dt} = \frac{-V_o}{2L}. \tag{7}$$

For any linear segment of the inductor current i_{La1} shown in Fig. 5, its slope can be expressed as a superposition of the above four inductor current slopes associated with the main switching

function, i.e.,

$$\frac{di_{La1}}{dt} = k_1 S_{a1} + k_2 \sum_{i=2}^{n} S_{ai} + k_3 \sum_{i=1}^{n} S_{di} + k_4 \tag{8}$$

where S_{a1}, S_{ai}, and S_{di} are the switching functions of the main switches; ON is 1 and OFF is 0.

According to (8), the inductor current ripple can be calculated by multiplying this slope by its duration time. If the duty cycle of all main switches is D, the duty cycle for simultaneous ON of S_{a1} and S_{ai} is

$$D_{ai} = \left(D - \frac{i-1}{n}\right) \text{ceil}\left(D - \frac{i-1}{n}\right) + \left(D - \frac{n-i+1}{n}\right) \text{ceil}\left(D - \frac{n-i+1}{n}\right) \tag{9}$$

where ceil(x) function is the smallest integer greater than or equal to the specified expression x, for example, ceil(-0.2) = 0.

During the time S_{a1} is ON, the total duty cycle for S_{ai}, $i = 2, 3, \ldots, n$, can be summed as

$$D_{a2-an} = \sum_{i=2}^{n} D_{ai}. \tag{10}$$

The duty cycle for simultaneous ON of S_{a1} and S_{di} can be formulated as

$$D_{di} = \left(D - \frac{2i-1}{2n}\right) \text{ceil}\left(D - \frac{2i-1}{2n}\right) + \left(D - \frac{2n-2i+1}{2n}\right) \text{ceil}\left(D - \frac{2n-2i+1}{2n}\right). \tag{11}$$

During the time S_{a1} is ON, the total duty cycle for S_{di}, $i = 1, 2, \ldots, n$, can be summed as

$$D_{d1-dn} = \sum_{i=1}^{n} D_{di}. \tag{12}$$

Applying the superposition principle to model the effect of $2n$ main switches on L_{a1}, the inductor current ripple, i.e., the variation of the inductor current during the time S_{a1} is ON, can be expressed as

$$\Delta i_{La1} = \left(k_1 D_{a1} + k_2 D_{a2-an} + k_3 D_{d1-dn} + k_4 D_{a1}\right) T_{\text{sw}}. \tag{13}$$

Finally, based on the equal voltage of the two input series capacitors, i.e., $V_{h1} = V_{h2} = 0.5V_{\text{dc}}$, and $D_{a1} = D$, the inductor current ripple, expression (13), can be simplified as

$$\begin{aligned}\Delta i_{La1} &= \left(\frac{(2n-1)\,V_{\text{dc}}}{4nL} D - \frac{V_{\text{dc}}}{4nL} D_{a2-an} + \frac{V_{\text{dc}}}{4nL} D_{d1-dn} - \frac{V_{\text{dc}}}{2L} D^2\right) \frac{1}{f_{\text{sw}}} \\ &= \left[\frac{(2n-1)\,D}{2n} - \frac{D_{a2-an}}{2n} + \frac{D_{d1-dn}}{2n} - D^2\right] \frac{V_{\text{dc}}}{2Lf_{\text{sw}}}.\end{aligned} \tag{14}$$

Based on (14), the relationship between the inductor current ripple and the duty cycle is shown in Fig. 8. The inductor current ripple does not exceed the current ripple of an equivalent two-level buck/boost converter with $V_{\text{dc}}/2$ on the high voltage side. As the number of interleaved phases increases, the inductor current ripple gradually approaches the inductor current ripple of the two-level buck/boost converter.

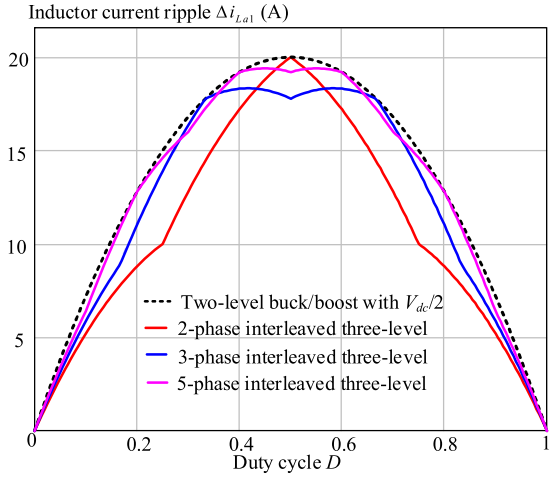

Fig. 8. Relationship between the inductor current ripple and the duty cycle, where the black dotted line is an equivalent two-level buck/boost converter with $V_{\text{dc}}/2$ on the high voltage side. The basic parameters are $L = 380\ \mu$H, $f_{\text{sw}} = 11.8$ kHz, and $V_{\text{dc}} = 720$ V for example.

For a given duty cycle D, the maximum number of main switches that can be simultaneously turned ON in an n-phase interleaved three-level dc–dc converter can be formulated as

$$K_{\text{ON}} = \text{ceil}\left(D \cdot 2n\right). \tag{15}$$

Meanwhile, the duration of holding the K_{ON} value is

$$\Delta T_{\text{ON}} = \frac{D \cdot 2n - \text{floor}\left(D \cdot 2n\right)}{2nf_{\text{sw}}} \tag{16}$$

where floor(x) function is the smallest integer less than or equal to the specified expression x, for example, floor(1.6) = 1.

When the voltage source V_{h1} acts alone, as shown in Fig. 7(a), the total inductor current increment is

$$\Delta I_{r1} = \left(\frac{2n-1}{2n} V_{h1} - \frac{n-1}{2n} V_{h1}\right) \frac{\Delta T_{\text{ON}}}{L} = \frac{V_{h1} \Delta T_{\text{ON}}}{2L}. \tag{17}$$

When the output voltage source V_o acts alone, as shown in Fig. 7(d), the total inductor current increment is

$$\Delta I_{r2} = -\frac{nV_o \Delta T_{\text{ON}}}{2L}. \tag{18}$$

When the voltage source V_{h2} acts alone, as shown in Fig. 7(c), the total inductor current increment is

$$\Delta I_{r3} = \frac{V_{h2}}{2n} \frac{\Delta T_{\text{ON}}}{L} n = \frac{V_{h2} \Delta T_{\text{ON}}}{2L}. \tag{19}$$

If the two input series capacitor voltages are balanced, i.e., $V_{h1} = V_{h2} = 0.5V_{\text{dc}}$, it can be obtained that

$$\Delta I_{r1} = \Delta I_{r3} = \frac{V_{\text{dc}} \Delta T_{\text{ON}}}{4L}. \tag{20}$$

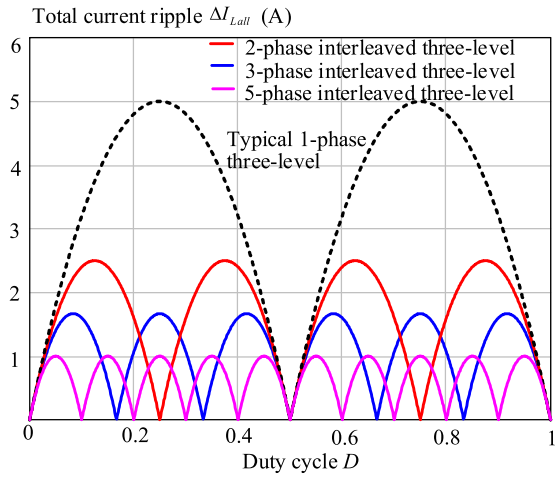

Fig. 9. Relationship between the output total inductor current ripple and the duty cycle for an example with $L = 380\ \mu$H, $f_{\rm sw} = 11.8$ kHz, and $V_{\rm dc} = 720$ V.

Applying the superposition principle to solve the effect on total current ripple of $2n$ main switches, the output total inductor current ripple can be obtained as

$$\Delta i_{L\rm all} = K_{\rm ON}\Delta I_{r1} + \Delta I_{r2} = \frac{K_{\rm ON}V_{\rm dc}\Delta T_{\rm ON}}{4L} - \frac{nV_o\Delta T_{\rm ON}}{2L} = (K_{\rm ON} - 2nD)\frac{V_{\rm dc}\Delta T_{\rm ON}}{4L}. \quad (21)$$

Substituting (15) and (16) into (21), the final expression of the output total inductor current ripple for any n-phase interleaved three-level dc–dc converter is

$$\Delta i_{L\rm all} = [\text{ceil}(2nD) - 2nD]\frac{2nD - \text{floor}(2nD)}{2n}\frac{V_{\rm dc}}{4Lf_{\rm sw}} \quad (22)$$

where $n \geq 2$ and it represents the phase number of interleaved three-level dc–dc converter, ceil(x) function is the smallest integer greater than or equal to x, and floor(x) function is the smallest integer less than or equal to x.

Based on (22), the relationship between the output total inductor current ripple and the duty cycle can be obtained as shown in Fig. 9. It can be clearly seen that the total inductor current ripple decreases rapidly as the number of interleaved phases increases. The curves of (14) and (22) are in perfect agreement with the current ripple results of two-phase and three-phase interleaved three-level dc–dc converter in [13], which verifies the correctness of these equations.

C. Proposed Variable Switching Frequency Control Method

To eliminate the zero-crossing detection and additional high-frequency sensors in the traditional method, this article proposes a variable switching frequency control method based on the current ripple prediction to realize ZVS. The required switching frequency can be directly calculated from (14), i.e.,

$$f_{\rm sw} = \left[\frac{(2n-1)D}{2n} - \frac{D_{a2-an}}{2n} + \frac{D_{d1-dn}}{2n} - D^2\right]\frac{V_{\rm dc}}{2L\Delta i_{La1}}. \quad (23)$$

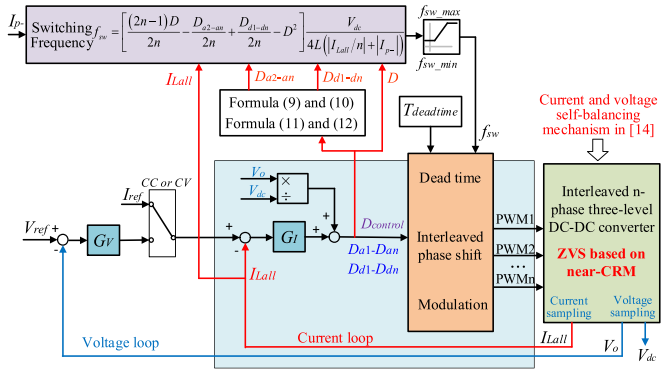

Fig. 10. Proposed variable switching frequency control method based on the inductor current ripple prediction to achieve ZVS for interleaved n-phase three-level DC–DC converter.

In near-CRM, the inductor current has both positive and negative values in each switching cycle, so the inductor current ripple can also be expressed as

$$\Delta i_L = 2\left(|I_{L\rm all}/n| + |I_{p-}|\right). \quad (24)$$

Substituting (24) into (23), the final expression for the switching frequency can be obtained as

$$f_{\rm sw} = \left[\frac{(2n-1)D}{2n} - \frac{D_{a2-an}}{2n} + \frac{D_{d1-dn}}{2n} - D^2\right] \times \frac{V_{\rm dc}}{4L\left(|I_{L\rm all}/n| + |I_{p-}|\right)}. \quad (25)$$

where $I_{L\rm all} = nI_{L\rm avg}$ is the average current of $i_{L\rm all}$ and is also equal to the output current I_o, and $I_{p\text{-}}$ is the reverse valley current.

Using the switching frequency expression (25), a variable switching frequency control based on current ripple prediction is proposed, as shown in Fig. 10, which only requires sampling the average value of $V_{\rm dc}$, V_o, and $i_{L\rm all}$ instead of zero-crossing detection and additional high-frequency sensors. The control diagram mainly consists of the output voltage outer loop, the current inner loop for $I_{L\rm all}$, and the switching frequency calculation. G_V and G_I represent the voltage loop controller and the current loop controller, respectively. The balancing measures for current and voltage are not required, because the interleaved inductor currents and the input series capacitor voltages are inherently self-balancing in near-CRM, as verified in [13]. Moreover, the inductor value can withstand $\pm 10\%$ tolerance by setting a larger reverse current as a margin based on (3).

According to (25), the switching frequency can be calculated by sampling the input/output voltage and total output current for a given interleaving phase number n. The 3-D relationship surface is shown in Fig. 11 for an example of $n = 3$. It can be seen that as the inductor output current increases, the required switching frequency must decrease to achieve ZVS. Due to the limitations of the gate driver hardware for IGBTs, the maximum switching frequency is limited to 30 kHz in the following experiments. The minimum switching frequency is set at 6 kHz based on experience with the IGBT module 39AC12T4V1, as

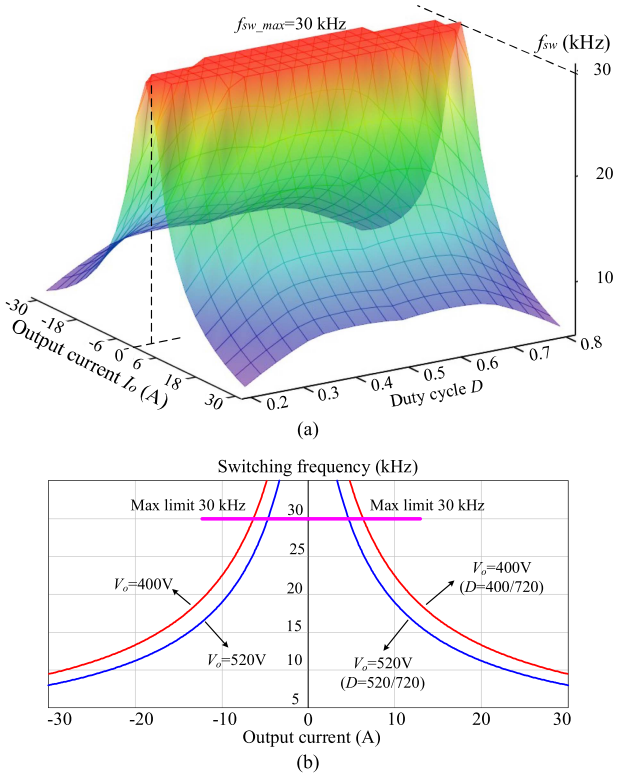

Fig. 11. (a) 3-D relationship and (b) 2-D relationship of the switching frequency versus the output current and duty cycle in near-CRM with $n = 3$, $I_{p-} = -1.5$ A, $L = 380$ μH, and $V_{\rm dc} = 720$ V.

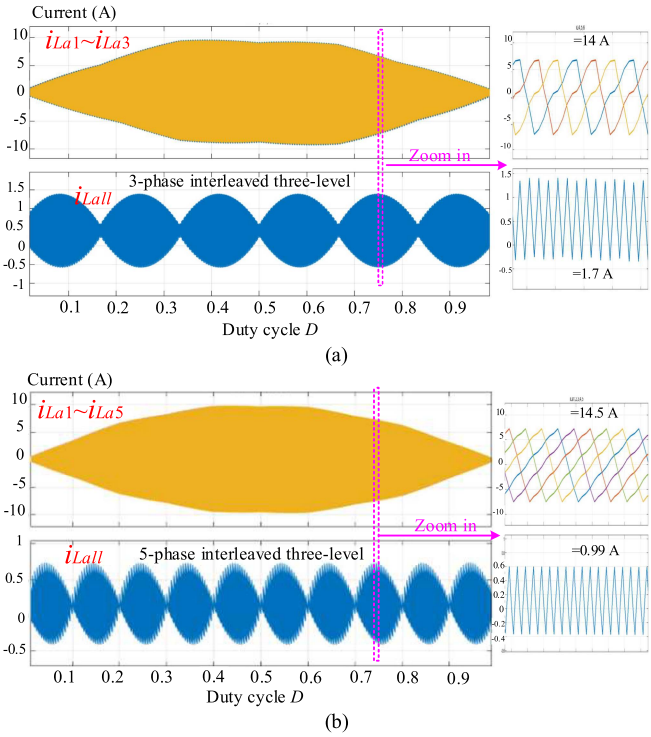

Fig. 12. Simulation results of the inductor current and output total current for interleaved (a) 3-phase and (b) 5-phase three-level DC–DC converters. The simulation parameters are the same as in Figs. 8 and 9.

lower switching frequencies necessitate larger filter inductors and capacitors.

In our experiment, the switching frequency of 6–30 kHz is only an example based on experience. However, the contribution and method of this article are not limited by the switching frequency and can be applied to various power semiconductor switches with their appropriate switching frequencies.

It is important to design the inductor value based on a reasonable switching frequency operating range. In addition, the design of the inductance value must also take into account the input/output voltage range, output current, negative valley current, and duty cycle in practical operation. Based on (25), the inductance value can be solved as

$$L = \left[\frac{(2n-1)\,D}{2n} - \frac{D_{a2-an}}{2n} + \frac{D_{d1-dn}}{2n} - D^2\right] \times \frac{V_{\rm dc}}{4f_{\rm sw}\left(|I_{\rm Lall}/n| + |I_{p-}|\right)}. \tag{26}$$

Take the three-phase interleaved three-level dc–dc converter as an example: $V_{\rm dc} = 720$ V, $V_o = 200$–560 V, $f_{\rm sw} = 6$–30 kHz, and the maximum average inductor current is 10 A, i.e., the output current can reach to ± 30 A. To mitigate the tolerance effect of inductance and capacitance, a larger reverse current ($I_{p-} = -1.5$ A) is selected to satisfy (3). Using (26), the inductance value can be calculated as 395 μH. To maintain some margin for adjusting the switching frequency, the inductance is selected at 380 μH with a minimum of 6.3 kHz. The interrupt program frequency is the same as the switching frequency.

IV. Simulation and Experimental Results

To verify the correctness of the current ripple solution proposed in Section III, the interleaved 3-phase and 5-phase three-level dc–dc converters are simulated as shown in Fig. 12. Fig. 12(a) shows that the inductor current ripple is 14 A at $D = 0.75$ and the maximum output total current ripple is 1.7 A for interleaved 3-phase three-level, whereas the corresponding theoretical values, calculated using (14) and (22), are 13.94 A and 1.67 A, respectively. Fig. 12(b) shows the inductor current ripple is 14.5 A at $D = 0.75$ and the maximum output total current ripple is 0.99 A for interleaved 5-phase three-level, whereas the corresponding theoretical values are 14.65 A and 1.0 A, respectively. These simulation results verify that the inductor current ripple and the output total current ripple agree well with the theoretical calculation results in Figs. 8 and 9 and (14) and (22).

An interleaved three-phase ($n = 3$) three-level dc–dc converter prototype is constructed, as shown in Fig. 13, to verify the proposed variable switching frequency control method based on current ripple prediction. The part number of the IGBT module is SKiiP 39AC12T4V1, the high dc-link capacitors C_{h1} and C_{h2} are 360 μF, the low dc-link capacitor C_o is 60 μF, and the DSP controller is TMS320F28377D. The inductor is wound using a High Flux magnetic core CH467060 to obtain 380 μH with $\pm 8\%$ tolerance. Based on typical IGBT operation, the switching

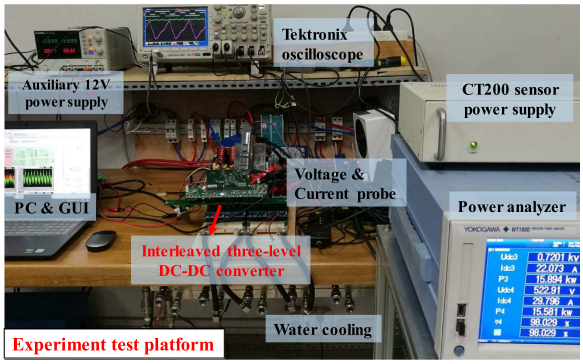

Fig. 13. Experimental prototype test bench of the interleaved three-phase ($n = 3$) three-level DC–DC converter.

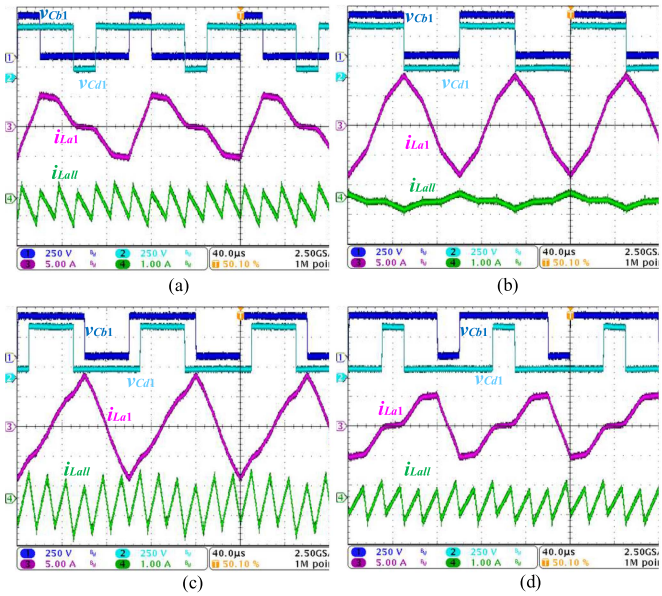

Fig. 14. Waveforms of the inductor current and the total output current for $n = 3$ with $V_{\rm dc} = 600$ V and $f_{\rm sw} = 10$ kHz at different duty cycles. (a) $D = 0.2$. (b) $D = 0.5$. (c) $D = 0.6$. (d) $D = 0.8$.

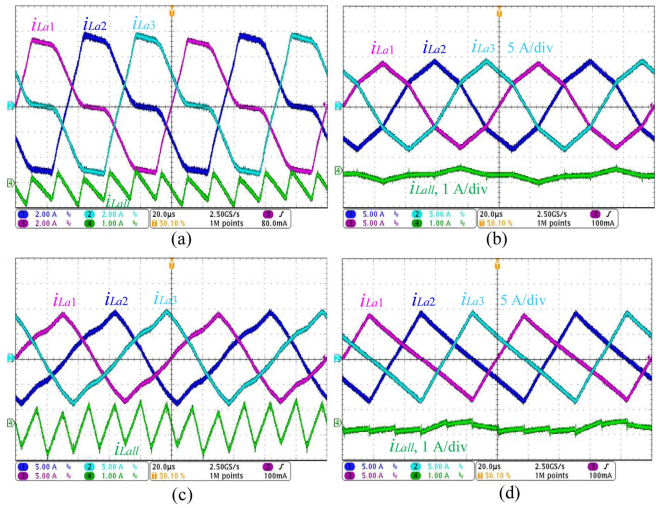

Fig. 15. Waveforms of interleaving inductor currents and the total current with $V_{\rm dc} = 600$ V and $f_{\rm sw} = 10$ kHz at different duty cycles. (a) $D = 0.2$. (b) $D = 0.5$. (c) $D = 0.6$. (d) $D = 0.667$.

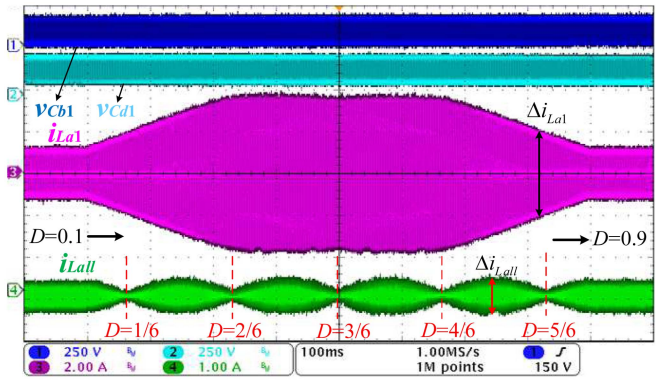

Fig. 16. Inductor current and total current waveforms with the duty cycle D sweeping from 0.1 to 0.9 with $V_{\rm dc} = 380$ V and $f_{sw} = 15$ kHz, which can reflect the current ripple Δi_{La1} and Δi_{La11} due to no-load testing.

frequency is selected in the range of 6–30 kHz and the dead time is set to 3 μs.

A. Current Ripple Verification

To verify the current ripple equation in Section III, the inductor current ripples corresponding to different duty cycles are experimentally tested, as shown in Fig. 14. The waveforms show the inductor current and the total output current at different duty cycles: (a) $D = 0.2$, (b) $D = 0.5$, (c) $D = 0.6$, and (d) $D = 0.8$. It can be seen that the inductor current is not a standard triangular waveform, and the frequency of the total output current ripple is six times that of the inductor current ripple. In addition, the inductor current waveforms at $D = 0.2$ and $D = 0.8$ are symmetrical.

Fig. 15 shows the waveforms of interleaving inductor currents and the total current at different duty cycles: (a) $D = 0.2$, (b) $D = 0.5$, (c) $D = 0.6$, and (d) $D = 0.667$. After interleaving, the total output current ripple is greatly reduced. At the special point $D = 0.667$, the total output current ripple is almost zero, where the total output current ripple is exactly zero due to the inductance tolerance and nonlinearity. These waveforms demonstrate the benefits of reducing inductor current ripple by combining interleaving and three-level technology.

To verify the relationship between the inductor current ripple and the duty cycle shown in Fig. 8, as well as the current ripple cancellation illustrated in Fig. 9, the duty cycle D is swept from 0.1 to 0.9, as shown in Fig. 16. The ripple envelope of the current i_{La1} is consistent with the theoretical analysis result. The output total current ripple is almost zero for $D = 1/6$, 2/6, 3/6, 4/6, and 5/6. At $D = 2.5/6$, the inductor current ripple is 7.6 A and the maximum output total current ripple is 0.7 A, whereas the corresponding theoretical values, calculated using (14) and (22), are 7.64 A and 0.69 A, respectively. Considering the measurement tolerance, these experimental results are in agreement with the theoretical calculation results.

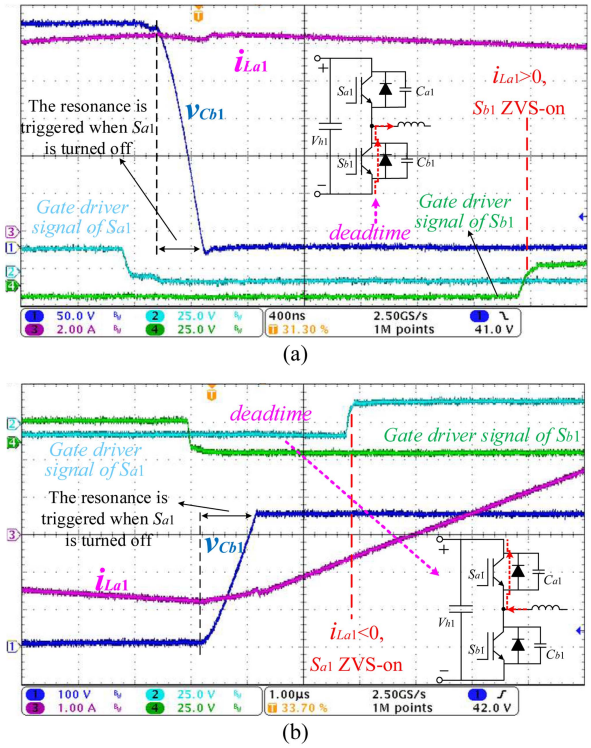

Fig. 17. ZVS waveforms in near-CRM. (a) S_{b1} turns ON with ZVS at a positive peak current. (b) S_{a1} turns ON with ZVS at a negative valley current of $i_{La1}<0$.

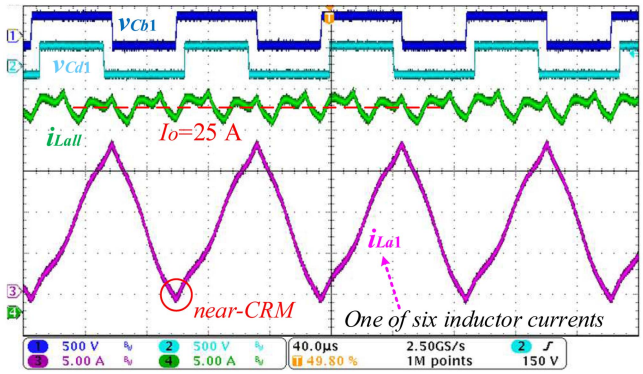

Fig. 18. Basic waveforms in near-CRM with $V_{\rm dc} = 720$ V, $V_o = 400$ V, and $P_o = 10$ kW.

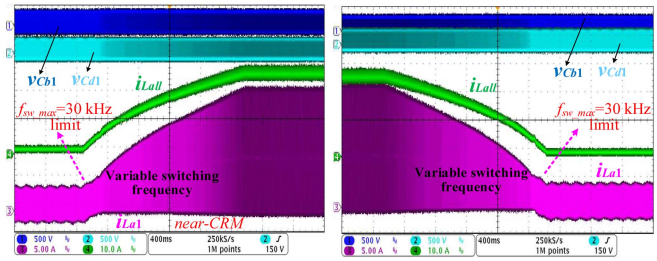

Fig. 19. Dynamic test waveforms as the output current sweeps from 2 to 30 A and from 30 to 2 A with $V_{\rm dc} = 720$ V and $V_o = 520$ V.

B. ZVS Transition Waveforms

Fig. 17 shows the ZVS transition process in near-CRM. At the peak of the inductor current, S_{a1} turns OFF, causing the voltage v_{Cb1} to gradually decrease until it is clamped by the antiparallel diode of S_{b1}, as shown in Fig. 17(a). S_{b1} will turn ON with ZVS as long as i_{La1} remains greater than zero at this turn-ON moment. Similarly, at the valley of the inductor current, the resonance process is triggered when S_{b1} turns OFF, and S_{a1} turns ON with ZVS as long as $i_{La1}<0$ at the turn-ON moment of S_{a1}. Due to the symmetry of the interleaved topology, the other switches have also the same theory to achieve ZVS in near-CRM.

C. Waveforms in Proposed Variable Switching Frequency Control Based on Current Ripple Prediction

Using the proposed switching frequency control method, this converter can work in near-CRM even though the inductor current is not a standard triangular wave, as shown in Fig. 18. This test result verifies that the inductor current i_{La1} is in near-CRM with a small negative value of approximately -1.5 A. Thanks to ripple cancellation in interleaving, the output total current ripple remains very small relative to the average current of 25 A.

In buck mode, with a voltage source on the output side simulating a battery, the dynamic test waveforms as the output current sweeps from 2 to 30 A and from 30 to 2 A with $V_{\rm dc} = 720$ V and $V_o = 520$ V are shown in Fig. 19. The maximum switching frequency is limited by 30 kHz. As the output current increases from 2 to 30 A, the switching frequency gradually decreases to enable ZVS based on near-CRM.

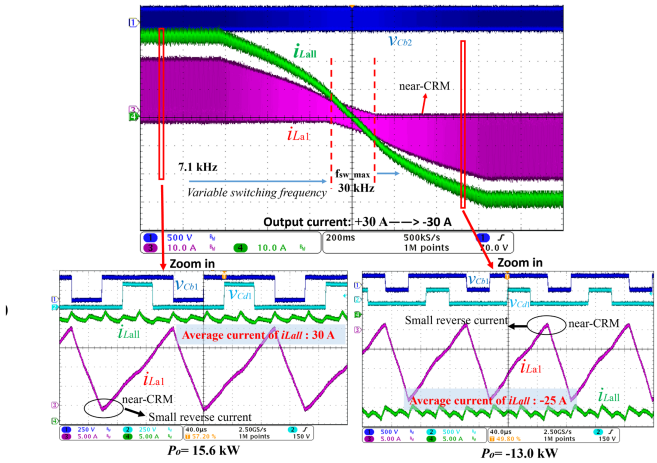

Fig. 20. Dynamic test waveforms as the output current sweeps from $+30$ A (buck mode) to -30 A (boost mode) with $V_{\rm dc} = 720$ V and $V_o = 520$ V.

Fig. 20 shows the dynamic test waveforms of the current bidirectional function. As the output current changes from $+30$ A in buck mode to -30 A in boost mode, the inductor current ripple is adjusted by the proposed variable switching frequency control to maintain this converter in near-CRM. Although the inductor current ripple is quite large, the output total current ripple remains small due to interleaving. Around the interval where the average current is 0 A, the inductor current ripple remains unchanged because of the fixed switching frequency, which is limited to a maximum of 30 kHz.

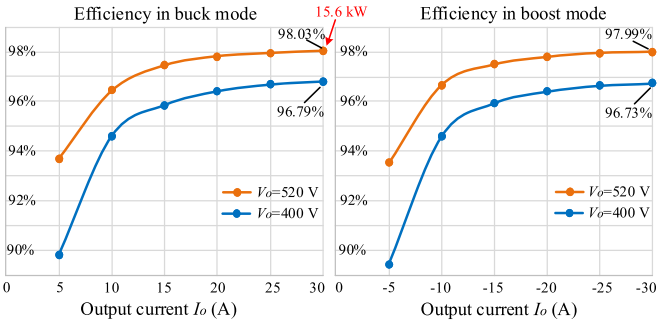

Fig. 21. Efficiency test results of the experimental prototype with IGBT device in buck and boost mode at $V_{\rm dc} = 720$ V, maximum test power at 15.6 kW.

The efficiency results in buck and boost mode for the experimental prototype using IGBT devices are tested at $V_{\rm dc} = 720$ V, as shown in Fig. 21. This converter is still operated in near-CRM to achieve ZVS. The maximum efficiency is 98.03% for buck mode at 15.6 kW, and 97.99% for boost mode at -15.6 kW with an output current of -30 A. The efficiency can be further optimized using the power loss minimization method in [36].

V. Conclusion

This article proposes a method for current ripple prediction and variable switching frequency control in an interleaved n-phase three-level dc–dc converter. A unified current ripple expression is established, which is applicable to any multiphase three-level dc–dc converter for predicting the complex inductor current ripple, thus eliminating the traditional cumbersome case-by-case analysis and solution. The required switching frequency to maintain ZVS under near-CRM can be calculated directly in a digital controller based on current ripple prediction.

Using this method, any n-phase interleaved three-level dc–dc converter can be effectively analyzed and controlled to achieve ZVS without the need for zero-crossing detection sensors or circuits. Therefore, compared to the traditional zero-crossing detection method, the proposed current ripple prediction-based variable switching frequency control reduces the hardware complexity and cost of the converter. The theoretical analysis and proposed method are verified using an IGBT-based three-phase interleaved three-level dc–dc converter, achieving a maximum efficiency of 98.03% at 15.6 kW.

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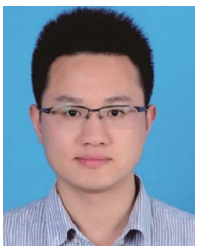

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