Letters

Compact Rectifier With Wide Range of Output Load Based on Self-Bias Impedance Compensation

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***Abstract*—One of the challenges in rectifiers is that their efficiency is significantly affected by variations in output load and input power. In this brief, we propose a compact rectifier based on dynamic self-bias impedance compensation (SBIC) between two subrectifiers operating in low-load and high-load regions. Their input impedance can dynamically compensate for each other as the output load increases. Consequently, the impact of the nonlinear effect of the diode, caused by the biasing of the dc output voltage, can be reduced. Theoretical analyses were carried out, and corresponding equations were formulated for designing the SBIC. For validation, a prototype was simulated, fabricated, and characterized. At 0-dB·m input power, the rectifier demonstrated a measured efficiency of over 50% with the output load from 0.4 to 9 kΩ, achieving up to 21% improvement in the load range compared to that of a single-diode rectifier. The reflection coefficient remains below −10 dB with an output load between 0.5 and 9 kΩ, and at the same time, good performance can be maintained in the range of input power from −15 to 10 dB·m.**

***Index Terms*—Impedance compensation, rectifying circuit, wide input power range, wide output-load range, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) has, rightly, been receiving increasing attention from researchers [1]. The rectifier, which converts RF energy into dc output, is a key device in WPT systems and has been extensively studied. However, in real-world applications, the available electromagnetic energy and system load are generally not constant but vary with operating conditions. The fluctuating input power and output load lead to impedance mismatching since the rectifying device is nonlinear. Therefore, as a key component of WPT systems, it is crucial to design rectifiers with a wide range of output load and input power [2], [3].

Resistive compression networks (RCNs) can reduce the sensitivity and nonlinearity of electronic devices such as amplifiers, dc–dc converters [4], and rectifiers [5]. In [6], multiway transmission-line RCNs were implemented with a 4-W rectifier for maintaining near-constant input impedance over a load resistance of 18–170 Ω. Similarly, in [7], a broadband impedance matching network is mixed with an RCN to form a hybrid resistance compression technique, so the rectenna can maintain high efficiency with a load impedance ranging from 5 to 80 kΩ. However, for complex impedances, neither the RCN nor the TRCN can simultaneously compress the real and imaginary parts of the complex impedance [8].

One possible solution to address impedance variation is the incorporation of a power recycling or self-matching network. In [9], an integrated hybrid coupler with a phase shifter was utilized to mitigate the nonlinear effects caused by changes in input power and load impedance. In [10], a self-matching rectifier was realized through an artificial transmission line biased by its output voltage. It is noticed that this coupler-based recycling structure requires more circuit area, and the power loss introduced by the recycling or self-matching network cannot be neglected.

For output load impedance matching, a dc–dc converter with maximum power point tracking (MPPT) is commonly used for the receiving side of a WPT system [11]. In [12], a load-modulated rectifier for RF micropower harvesting was presented using dc–dc converters activated by a start-up stage. Huang et al. [13] used a buck–boost converter with the MPPT method, achieving an almost steady PCE when the load resistance varied from 0.1 to 5 kΩ. While a dc–dc converter can match the rectifier with an optimal output load, it is an active circuit that requires some energy to startup and operate.

In this brief, we proposed a novel compact topology using self-bias impedance compensation (SBIC). As shown in Fig. 1, the proposed rectifier consists of two parallel rectifier cells directly connected to the input port without any circuits. The main branch, Cell M, and the self-bias compensation branch,

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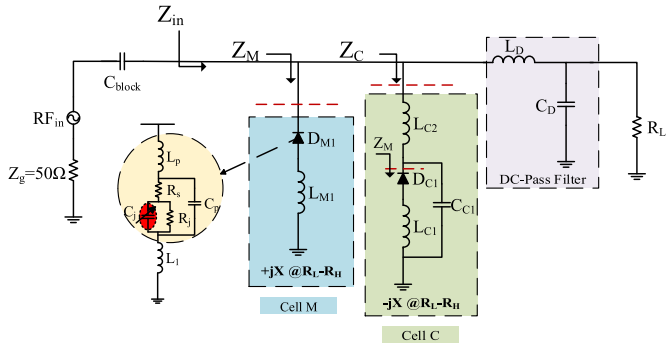


Fig. 1. Schematic of the proposed rectifier with wide output load range, the main branch is named as Cell M, and the self-bias compensation branch is denoted as Cell C.

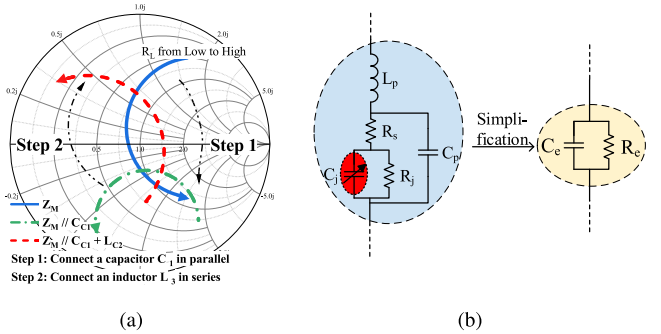


Fig. 2. Operating principle of the proposed rectifier with two subrectifiers designed to be approximately conjugate. (a) Realization of Cell C through a rotation of Z_{M} by λ/4. (b) Equivalent circuit model of a Schottky diode.

Cell C, are designed for complementary operations. This approach allows both the real and imaginary parts of the complex impedance to be compressed, enabling the rectifier to maintain stable RF– dc conversion over a wide range of output loads.

II. Design of the Microwave Rectifier

A. Principle

As shown in Fig. 1, the input impedance of the main branch and the self-bias compensation branch are denoted as Z_{M} and Z_{C}, respectively. To suppress the variation of input impedance with the output load R_{L}, Z_{M} and Z_{C} are designed to be approximately conjugate

$$Z_{\mathrm{C}}(R_{\mathrm{L}}) = Z_M^*(R_{\mathrm{L}}). \tag{1}$$

Thus, the input matching of is achieved with $\mathrm{Im}\{Z_{\mathrm{in}} = Z_{\mathrm{M}} \parallel Z_{\mathrm{C}}\} \approx 0$ for extending the range of output loads.

In Cell M, inductor L_{M1} is used to compensate for the capacitive impedance of the diode, making the imaginary part of Z_{M} symmetrical with respect to the output load, which is indicated by the solid line in Fig. 2(a). As to Cell C, a λ/4 rotation of Z_{M} can be realized through the parallel connections of C_{C1} and the serial connection of L_{C2} to Z_{M}, labeled as steps 1 and 2 in Fig. 2(a), respectively. In the following section, Z_{M} and Z_{C} versus dc load will be analyzed through their equivalent circuits.

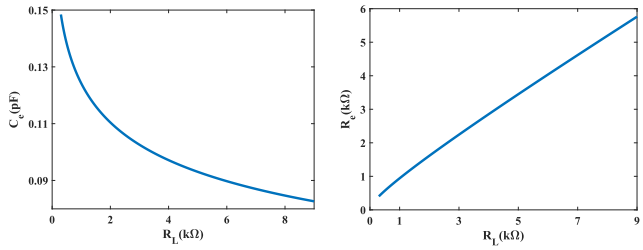


Fig. 3. Equivalent junction capacitance and resistance versus output load with a given input power. (a) Calculated C_e and (b) calculated R_e ($C_{\mathrm{j0}} = 0.18$ pF, $V_{\mathrm{bi}} = 0.6$ V, $\eta = 0.6$, and $P_{\mathrm{in}} = 0$ dB·m).

B. Variation of Diode Impedance

Based on the rectification cycle represented by the input fundamental and diode junction voltage waveforms impressed on the diode *I–V* curve, closed-form equations for the diode's efficiency and input impedance are derived in [14]. Using those equations, the diode impedance can be described by the parallel connection of a nonlinear junction capacitance C_e and a nonlinear junction resistance R_e [see Fig. 2(b)], C_e and R_e can be expressed as

$$C_e = C_j \frac{\pi - \theta_{\mathrm{on}} + \frac{1}{2}\sin 2\theta_{\mathrm{on}}}{\pi};\ R_e = \frac{\pi R_{\mathrm{s}}}{\theta_{\mathrm{on}} - \sin\theta_{\mathrm{on}}\cos\theta_{\mathrm{on}}} \tag{2}$$

where θ_{on} is the forward-bias turn-ON angle and R_{s} is the diode's series resistance. The junction capacitance C_j in (2) is defined as $C_j = C_{\mathrm{j0}}/\sqrt{1 + (V_o/V_{\mathrm{bi}})}$ where C_{j0} is the zero bias junction capacitance, V_{bi} is the diode's built-in voltage in the forward bias, and V_o is the output dc voltage. θ_{on} used in (2) is a dynamic variable dependent on V_o and output load R_{L}, and is derived as

$$\frac{\pi R_{\mathrm{s}}}{R_{\mathrm{L}}\left(1 + \frac{V_{\mathrm{bi}}}{V_0}\right)} = \tan\theta_{\mathrm{on}} - \theta_{\mathrm{on}}. \tag{3}$$

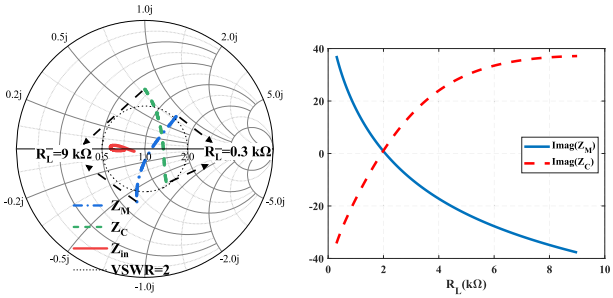
Assuming the rectifier maintains good matching conditions despite variations in the dc load, η can be fixed at a reasonable value for a given input power P_{in} based on the simulation results. In this case, the output voltage V_o equals to $\sqrt{\eta \cdot P_{\mathrm{in}} \cdot R_{\mathrm{L}}}$, and θ_{on} could be determined by (3), then C_e and R_e variation over R_{L} can be obtained using (2).

We calculated the C_e and R_e of an HSMS-286 diode when $\eta = 0.6$ and $P_{\mathrm{in}} = 0$ dB·m, and the results are shown in Fig. 3. The C_e decreases steadily from 0.148 to 0.08 pF and the R_e increases from 0.5 to 5.7 kΩ when R_{L} grows from 0.3 to 9 kΩ.

C. Main Branch-Cell M

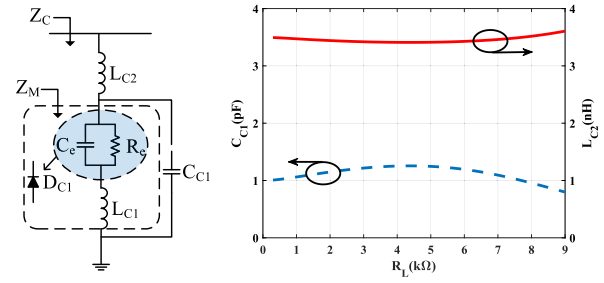
As shown in Fig. 1, in Cell M, the diode has an inductance L_{M1} for impedance matching, so Z_{M} can be expressed as

$$\begin{aligned} Z_{\mathrm{M}} &= \frac{1}{1 + (\omega R_e C_e)^2} - j\frac{\omega {R_e}^2}{1/C_e + C_e(\omega R_e)^2} + j\omega L_{\mathrm{M1}} \\ &= R_{\mathrm{M}} + jX_{\mathrm{M}} \end{aligned} \tag{4}$$



(a) (b)

Fig. 4. Calculated input impedance Z_{M}, Z_{C}, and Z_{in} using the results of C_e and R_e. (a) Impedance on the Smith chart. (b) Imaginary parts of Z_{M} and Z_{C} are moving in opposite directions.



(a) (b)

Fig. 5. Determine the parameters of Cell C. (a) Schematic of Cell C. (b) Calculated L_{C2} and C_{C1} with the increase of R_{L}.

where R_{M} and X_{M} are the real part and imaginary part, respectively. As seen in (4), Im(Z_{M}) can be zeroed by tuning L_{M1}. When the output load R_{L} increases, V_o increases and C_e decreases. The value of $1/C_e + C_e(\omega R_e)^2$ decreases as C_e decreases $(C_e > 1/(\omega R_e))$, which leads to an increase in the second term in (4), making Z_{M} capacitive.

Using (2) and (4), calculated Z_{M} is plotted in Fig. 4(a) with considerations of increase of R_e and decrease of C_e, L_{M1} is 16.5 nH and the operating frequency is 2.2 GHz. It is observed that Z_{M} varies from $(68.9 + j39.7)\ \Omega$ to $(30.3 - j33.8)\ \Omega$ with the increase of R_{L}, and the imaginary part of Z_{M} is nearly symmetrical to 2 kΩ output load [see Fig. 4(b)].

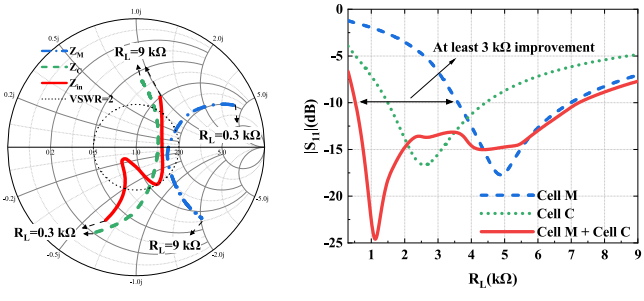
D. Compensation Branch-Cell C

As shown in Fig. 5(a), the self-bias compensation branch, Cell C, is realized by the parallel connection of C_{C1} and the serial connection of L_{C2} to Z_{M}. Z_{C} can be expressed as

$$Z_{\mathrm{C}} = (R_{\mathrm{M}} + jX_{\mathrm{M}}) \| \frac{1}{j\omega C_{\mathrm{C1}}} + j\omega L_{\mathrm{C2}}. \tag{5}$$

Z_{C} is designed to be conjugated with Z_{M}, so we have

$$Z_{\mathrm{C}} = Z_{\mathrm{M}}^{*} = R_{\mathrm{M}} - jX_{\mathrm{M}}. \tag{6}$$



(a) (b)

Fig. 6. Simulated Z_{M}, Z_{C}, and Z_{in} using harmonic balance simulation. (a) Input impedance on the Smith chart. (b) Input reflection coefficient $|S_{11}|$ of Cell M, Cell C, and Cell M+Cell C.

Combining (5) and (6) gives an expression for C_{C1} as

$$C_{\mathrm{C1}} = \frac{X_{\mathrm{M}} \pm \sqrt{(X_{\mathrm{M}}{}^2 + R_{\mathrm{M}}{}^2) - R_{\mathrm{M}}{}^2}}{\omega(X_{\mathrm{M}}{}^2 + R_{\mathrm{M}}{}^2)}. \tag{7}$$

Once C_{C1} is solved, L_{C2} is derived as

$$L_{\mathrm{C2}} = \frac{-X_{\mathrm{M}} - \dfrac{(1 - \omega X_{\mathrm{M}} C_{\mathrm{C1}})X_{\mathrm{M}} - \omega R_{\mathrm{M}}{}^2 C_{\mathrm{C1}}}{(1 - \omega X_{\mathrm{M}} C_{\mathrm{C1}})^2 + (\omega R_{\mathrm{M}} C_{\mathrm{C1}})^2}}{\omega}. \tag{8}$$

From (7) and (8), the calculated C_{C1} and L_{C2} versus R_{L} are plotted in Fig. 5(b). It is observed that C_{C1} and L_{C2} fluctuate with R_{L}, but the slope of change is very small. Considering $Z_{\mathrm{M}} \parallel Z_{\mathrm{C}}$ for the input matching of the rectifier, the strict conjugation condition of (6) can be relaxed to satisfy voltage standing wave ratio (VSWR) ≤ 2. Thus, the average values of C_{C1} and L_{C2}, 1.12 pF and 3.45 nH, are considered for the calculation of Z_{C} over 0.3–9 kΩ .

To verify the calculation results, Z_{M}, Z_{C}, and Z_{in} for different R_{L} values are simulated in Advanced Designed System (ADS, keysight) based on a nonlinear SPICE model, and the results are shown in Fig. 6. It is observed that the simulated $Z_{\mathrm{M}} \parallel Z_{\mathrm{C}}$ move in opposite directions with the increase of the output load. As a result, the curve of Z_{in} is folded in the middle region over R_{L} ranging from 0.3 to 9 kΩ. In addition, Fig. 6(b) shows that the $|S_{11}|$ curve of the proposed SBIC ($Z_{\mathrm{M}} \parallel Z_{\mathrm{C}}$) achieves better input matching than the Cell M, with its $|S_{11}|$ below -10 dB across 0.3 to 7 kΩ. Notably, a significant improvement of $|S_{11}|$ over 0.5–3.5 kΩ can be achieved by this SBIC.

III. Design and Implementation

A rectifier operating at 2.2 GHz is designed, optimized, and fabricated. The proposed rectifier is designed on a Rogers 4350B ($\epsilon_r = 3.66$ and $\tan\delta = 0.002$) with a height of 0.76 mm. The parameters and design of the proposed rectifier circuit are optimized in ADS. The layout and a photograph of the fabricated rectifier are shown in Fig. 7.

Fig. 8(a) shows the simulated input reflection coefficient $|S_{11}|$ versus frequency with $R_{\mathrm{L}} = 3$ kΩ. The frequency range for $|S_{11}| \leq -10$ dB is from 1.77 to 1.99 GHz, which gives a center frequency of 1.88 GHz. The measured center frequency

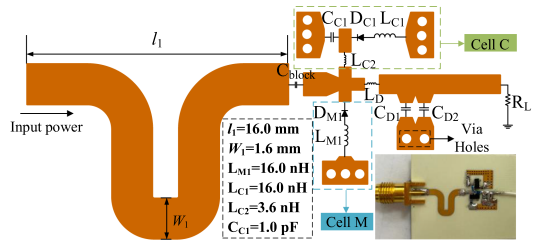


Fig. 7. Circuit layout, component values, and a photo of the proposed rectifier.

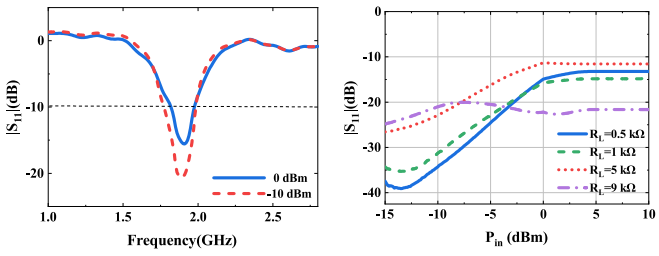


Fig. 8. Measured $|S_{11}|$ versus (a) frequency and (b) RF input power.

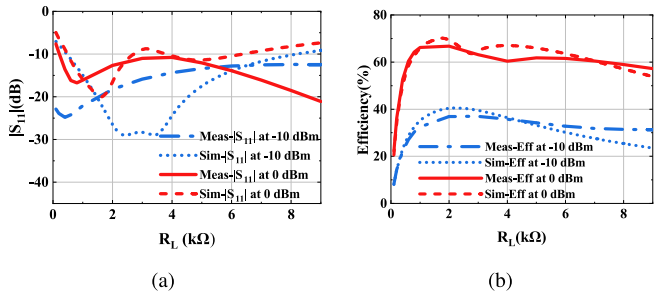


Fig. 9. Simulated and measured (a) $|S_{11}|$ and (b) PCE versus R_{L} at different input power.

deviates slightly from the simulation, which may be caused by the lumped components and the SPICE mode of the diode. We also measured $|S_{11}|$ versus input power at 1.88 GHz, which is shown in Fig. 8(b). One can see that the input power range for $|S_{11}| \leq -10$ dB is greater than 25 dB·m (-15 to 10 dB·m) with a wide range of output loads from 0.5 to 9 kΩ .

The measured $|S_{11}|$ and PCE versus R_{L} at -10 and 0 dB·m are depicted in Fig. 9. These results show that the circuit remains matched under a large variation of output loads from 0.3 to 9 kΩ. As shown in Fig. 9(b), the PCE remains nearly constant over a wide range of R_{L} for low levels of harvested power. This circuit preserves an efficiency higher than 50% over 0.4–9 kΩ at 0 dB·m input power, and it also presents a PCE stability that is above 30% over 0.8–9 kΩ at -10 dB·m.

To prove the effectiveness of the proposed SBIC, we measured the $|S_{11}|$ for Cell M, Cell C, and the proposed rectifier, the results are shown in Fig. 10(a). Improvements in the $|S_{11}|$ over 0.2–3 kΩ can be observed, the load range for $|S_{11}| \leq -10$ dB shows an increase of 46% when compared to that of Cell M (3–9 kΩ). Besides, Fig. 10(b) shows the measured PCE of the proposed

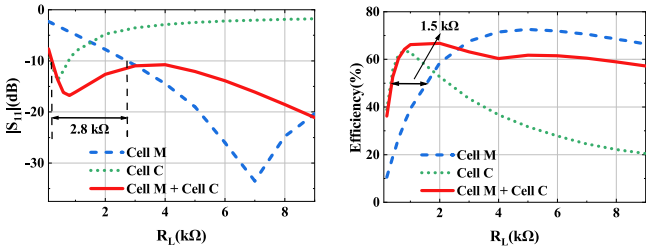


Fig. 10. Measured $|S_{11}|$ and PCE of Cell M, Cell C, and Cell M+Cell C at 0 dB·m RF power. (a) $R_L(k\omega)$. (b) $R_L(k\omega)$.

TABLE I
COMPARISON WITH THE PREVIOUS WORKS ON WIDE LOAD RANGE

Reference		[9]	[15]	[16]	**This work**
Eff.≥50%	Load (kΩ)	8-97	2-30	0.01–10	0.4–9
	Load ratio*	12.125	15	1000	**22.5**
	Pow (dB·m)	10	6	32	0
Peak Eff.	Eff.	74.2%	75.5%	73%	67%
	Load (kΩ)	40	7.6	0.4	2
	Fre.(GHz)	0.915	0.86	2.45	1.8
Tech.		Coupler	Voltage Multiplier	DC–DC Converter	SBIC
Diode num.		12	4	1	2
Diode Type		HSMS 2852	HSMS 286P	HSMS 2818	HSMS 286
Size(mm×mm)		110×63	39×34	37×25	21×10

*Load ratio: Max (R_L) / Min (R_L)

rectifier compared with Cell M and Cell C. As R_{L} increases, Cell C is deactivated and Cell M is in charge of operation. The PCE of the rectifier (Cell M+Cell C) remains over 50% with the output load from 0.4 to 9 kΩ, achieving up to 21% improvement compared to that of Cell M (1.9–9 kΩ).

Table I shows a comparison of the performances between the proposed rectifier and some previous rectifiers focusing on output load range extension. Except for the design using a dc–dc converter at a relatively high RF input power, the proposed rectifier shows the widest output load range for PCE >50%, where the load ratio (max/min) can reach 22.5.

IV. CONCLUSION

In this brief, a novel design of SBIC has been presented to broaden the high-efficiency range of the rectifying circuit under different incident power and load impedance simultaneously. By utilizing SBIC, the input impedance variations of two subrectifiers are neutralized so that good input impedance matching is maintained when the input power and the output load vary dynamically. The proposed SBIC features a simple circuit structure and a low insertion loss with impedance variation, which helps to ensure a high efficiency over a wide power range and load variation.

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