Approximate SPICE Modeling of SiC MOSFETs

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***Abstract*—The recent adaptation of wide bandgap (WBG) semiconductors pushes the SPICE circuit simulation software to the very edge, requiring computationally light and accurate assessment of rapid and oscillatory transients. One of the main limitations in SPICE modeling of WBG semiconductors is the lack of built-in models in the available software, forcing usage of behavioral modeling with heavily nonlinear equations. Using such implementation leads to high computational costs and convergence issues. This work presents a general approach to the approximate modeling of WBG semiconductors, leveraging the functionality of modern open-source SPICE software to improve convergence by decoupling nonlinear model formulation from the SPICE model formulation and to move the computational cost of nonlinear model updates outside the SPICE software. The proposed modeling approach is suitable for further acceleration by FPGA implementation and machine learning surrogate modeling. To investigate the accuracy of the approximate modeling, the approximations are derived for charge and channel equations of two silicon carbide MOSFETs and compared in a double pulse test against the original simulation model and experimental results. It is shown that the approximate implementation maintains the accuracy of the original model in the transient simulation and improves the convergence, leading up to 59% acceleration.**

***Index Terms*—Circuit simulation, silicon carbide (SiC), spice modeling, wide bandgap (WBG) semiconductors.**

I. Introduction

FAST and accurate simulation of wide bandgap (WBG) devices is a challenging task. First, the effect of parasitic elements of the layout has a significantly higher impact compared to silicon devices. Due to the fast switching transients, layout parasitics can introduce undesired oscillations potentially leading to instability issues in, for example, parallel-connected switches [1]. Quantifying these effects requires a detailed parasitic equivalent model simulated together with the rest of the circuit. However, this approach significantly increases the computational cost and poses challenges related to the convergence of device models. Second, there is a lack of built-in models suitable for accurate representation of silicon carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs) and other WBG semiconductor devices. The built-in SPICE models were originally developed over a long period to accurately represent silicon devices [2], [3], [4]. The material and structure differences between WBG and silicon devices render those models less applicable, forcing the manufacturers and users to rely on behavioral models. Creating new built-in models requires an in-depth knowledge of semiconductor physics, computer science, and advanced circuit theory. In addition, most prevalent SPICE software, such as PSPICE and LTSPICE, is distributed as closed-source, hence even the researchers and engineers with adequate skills and knowledge cannot introduce new models into the source code. Therefore, it is rare for such models dedicated to power devices to emerge.

There is a fundamental difference between the built-in and behavioral models. The former uses a simplified linear companion model with an update equation, which allows to avoid deriving the partial differential equations of the nonlinear models at every timestep. On the other hand, the behavioral models require deriving the linear companion at every time step with the assumption of model continuity [5]. The more complicated the nonlinear equations are, the more computational power has to be used to derive the linear approximation. Discontinuities, which are quite common in the models, contribute further to the convergence issues. This effect becomes even more apparent when the models are surrounded by highly oscillatory parasitic equivalent circuits, forcing the solver to use a smaller timestep.

There is also another important phenomenon to be addressed in simulating heavily nonlinear and discontinuous models with the parasitic equivalent circuits, namely, the false convergence [6]. Overly relaxed solver parameters, combined with the complex circuit behavior can easily lead to convergence to a local minimum of the residual. The results of such simulation are unusable, and noticing a nonobvious false convergence requires an in-depth knowledge of the simulated circuit combined with long troubleshooting. Usage of overly complex, heavily nonlinear behavioral models leads to false convergence being quite prevalent, and therefore to a decrease of trust in the circuit simulation.

Despite the computational disadvantages, the flexibility of behavioral models makes them convenient to use and easy to implement. Utilizing behavioral sources, a new model can be implemented as a mathematical equation requiring no advanced programming skills from the model developer, which has been widely exploited by the researchers in both industry and

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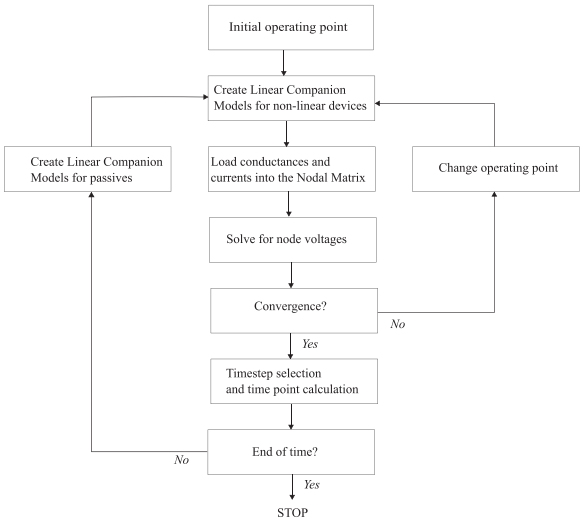


Fig. 1. SPICE algorithm for transient simulation, adapted from [5].

academia [7], [8], [9], [10]. This approach results in oftentimes more accurate models compared to fine-tuning of the built-in models [11].

The main contribution of this article is the introduction of a novel SPICE model implementation method to improve convergence and decrease simulation time by replacing complex, non-linear formulas with well-established linearized Taylor series approximations. The proposed approximate SPICE modeling approach leverages the capabilities of open-source SPICE software (NGSpice), enabling updates to the approximation coefficients at every time step, and therefore reducing the need for deriving linearizations for overly complex formulas. This type of implementation separates the full model equations and the SPICE implementation. Utilizing this approach, the implementation of well-conditioned approximations can improve SPICE convergence, while the costly approximation updates can be performed outside the SPICE software, with a possibility for further acceleration. Such acceleration has the potential of significantly lowering the computational cost of simulating multiple SiC MOSFET devices, which currently proves to be challenging in the low and medium voltage packaging applications [12], [13], [14], [15].

II. SPICE MODELLING FOR WBG DEVICES

The family of SPICE circuit solvers is probably the most successful circuit simulation software for power electronics applications up to this date. It is based on the modified nodal analysis (MNA). The MNA provides an intuitive method of formulating and solving the differential equations at a single time point. In combination with the modified Newton–Raphson and iterative linear companion modeler, it offers a powerful algorithm for analyzing nonlinear circuits. The SPICE simulation algorithm is depicted in Fig. 1.

To fully understand the difference between the built-in and behavioral models, it is important to note that the creation of linear companion models is performed at every timestep. The behavioral models require symbolic derivation of the linear companion model based on the expression provided in the behavioral source definition. This is a costly operation, that becomes problematic when very stiff problems are encountered, and a high number of timesteps have to be taken to properly evaluate all of the time constants. When the circuit is relatively simple, the overhead from linear companion model derivation for behavioral sources is negligible, becoming potentially significant only with the increase of the timestep number. The built-in models use a predefined linear companion, effectively avoiding the repeated derivation. An additional advantage of using a predefined linear companion model is the possibility of simplifying the update equation, further decreasing the computational cost.

Having established the background of good performance of built-in models, the lack of their usage in the power electronics industry has to be addressed. The main reason is clear and explored since the emergence of WBG devices, as the characteristic of SiC MOSFETs and Gallium nitride (GaN) high-electron mobility transistors face difficulty to be accurately represented accurately represented using the available built-in models, such as Berkeley short-channel insulated gate field-effect transistor (IGFET) Mode family. In the former case, the device structure differences result in a higher drift region contribution to the on-state resistance [16] and a soft threshold behavior [17]. In the literature, multiple approaches to the SPICE modeling of SiC power MOSFETs were presented. Starting with the works of McNutt et al. [17], where the material differences of SiC were first introduced in the context of SPICE models. The development of models until the year 2014 has been well-documented by Mantooh et al. [18]. In the last decade, the convergence and computational cost issues have been addressed by proposing compact models [19], building models using a combination of built-in models in [20], and proposing extending the built-in models in [16]. It is also worth noting, that due to the convergence problems, alternatives to SPICE have been proposed using neural network models [21] or real-time models implemented on field-programmable gate arrays (FPGAs) [22]. Convergence issues associated with SPICE simulation of WBG devices were also addressed by proposing alternative formulations of discontinuous equations [23], [24], and by deploying solver parameter adaptation [12]. The computational efficiency has also been discussed in [25] and [26], including the topic of convergence.

To achieve a reliable, fast and accurate simulation of circuits with WBG devices, implementation of dedicated built-in models would be required. As most of the SPICE software is distributed as a closed source, modifications to the source code in the development of the new built-in models can only be performed by the software distributors. Free, closed-source SPICE software retains most of its value from using the built-in models to promote the products of the owner, therefore only SiC and GaN device manufacturers would have an incentive to develop such models. The models would probably not be customizable enough to work well for third-party products. For the commercial SPICE software distributors, the key issue is likely the lack of standardization in WBG models. The models used vary strongly between the manufacturers, and implementing one of them might impose a risk of wasting resources on

a potentially short-lived implementation, as the research area of WBG power device modeling remains relatively active and develops significantly fast.

The open-source SPICE software offers more flexibility in terms of custom modeling, as each user can alter the source code. Some of the open-source distributions (e.g., NGSpice) also enable including precompiled custom verilog models and usage of external voltage and current sources in the netlists. This work uses the functionality of the latter to provide an alternative modeling approach, as the custom Verilog models do not seem to provide additional options of accelerating the device evaluation aside from improved compilation.

In the SiC MOSFET behavioral models, the main convergence and computational challenge is connected to the channel and charge equations and the body diode model. Those parts describe the nonlinear behavior of the device, with the rest of the model corresponding to the parasitic elements and thermal networks, as it can be seen, e.g., in the manufacturer model of CREE CMP-1200-160B available at [27]. The body diode is often modeled using the built-in diode model with a satisfactory performance. On the other hand, the channel and charge equations presented in the Appendix remain an issue from the performance and formulation, due to the heavy utilization of conditional terms along with a number of logarithmic and exponential functions. For this reason, those two equations are considered to form the bulk of computational complexity of SiC MOSFET models.

In this article, the external voltage sources are used to update approximations of the nonlinear channel and charge equations to improve the convergence and decrease the simulation time, by enabling the behavioral models to utilize predefined linear companion models. This is expected to prove beneficial for applications in the optimization of circuits containing multiple parallel devices, where the device models strongly contribute to the overall computational cost [25]. When running hundreds or thousands of simulations, the optimization runs can in turn take hours or days to complete making computational cost a crucial aspect.

III. Approximate Model Formulation and Implementation

The approximate modeling approach proposed in this work follows the following set of steps. The first step is replacing the nonlinear behavioral source formulas, with the linear approximation based on the well-established first-order multivariate Taylor series expansion form

$$T(x_1,\ldots,x_d)=f(a_1,\ldots,ad)+\sum_{j=1}^{d}\frac{\delta f(a_1,\ldots,ad)}{\delta x_j}(x_j-a_j). \tag{1}$$

This formulation requires providing a linearization point for each of the variables and calculating the terms associated with a function value at the linearization point and partial derivatives. This is implemented using an NGSpice feature, that allows voltage sources with a value provided by the external process controlling the simulation.

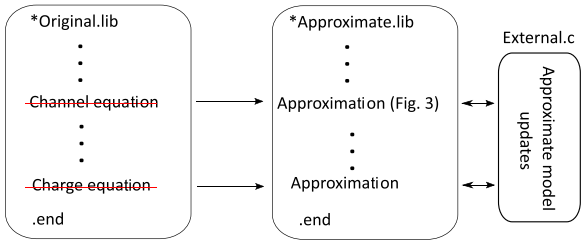


Fig. 2. Difference between the original SPICE models and proposed implementation.

```
Va1   a1   0   external
Va2   a2   0   external                    Linearization point

Vf0   f0   0   external
Vf1   f1   0   external
Vf2   f2   0   external                    Linearization coefficients

G     g0   d1   value = 'V(f0) +
+     (V(d1,g)-V(a1))*V(f1) +
+     (ddt(V(g,d1))-V(a2))*V(f2)'         Approximate model
                                          (V(d1,g) = x1, ddt(v(g,d1)) = x2)
```

Fig. 3. Netlist implementation of a two-variable linear approximation of charge equation.

In this way, each of the linearization points and values are represented as a voltage source with the value calculated externally. The NGSpice uses a callback function, called at every timestep to update the values of the external sources. Therefore, the calculation of the Taylor series expansion terms is performed in the external software controlling the simulation. Since NGSpice is compiled as a dynamic link library, the additional computational cost of calling it from the external process is comparable to a normal function call and originates from calling an additional cache table.

Having moved the linear companion derivation and computation to the external C program, the next step is formulating the nonlinear function and its partial derivatives and implementing them as functions to be used inside the previously mentioned callback function. Alternatively, the C program can be interfaced with higher level languages, such as Python, Julia, or Matlab, using pipes, however, those implementations are out of the scope of this work. The flowchart of approximate model operation in conjunction with the SPICE algorithm has been depicted in Fig. 4.

The last issue to be discussed is finding the initial operating point for this type of model. For simplicity, the original subcircuit model is used to compute the operating point at the start of the simulation.

The proposed method offers the following benefits.

1) Improved convergence, due to the simplified implementation in SPICE.
2) Faster evaluation, due to the improved convergence.
3) Possibility of further acceleration by modifying the external C program.
4) Possibility of operating directly on the measured device characteristic if needed, without introducing the discontinuities potentially present in e.g. derivatives in LUT-based approaches.

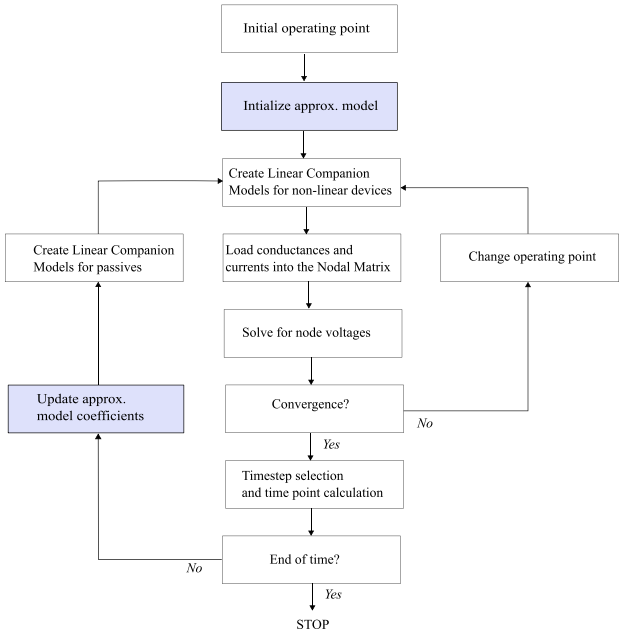


Fig. 4. SPICE algorithm for transient simulation with approximate models.

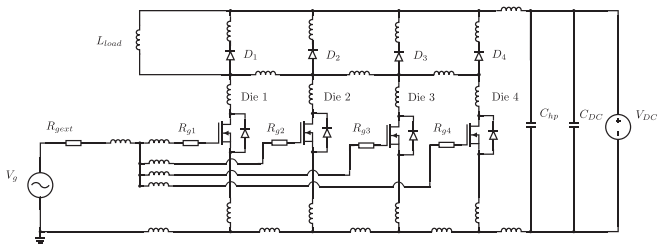


Fig. 5. Simplified schematic of the DPT circuit.

The proposed implementation method has been applied to the CREE CPM2-1200-0160B and ROHM SCT4018K bare die models, with the original and proposed model equation netlist implementations available in the Appendix, and full code available in the CoDE project GitHub repository [29].

IV. Simulation Results

The proposed modeling approach was assessed in a double-pulse test (DPT) case of a power module with four parallel dies. The module is a custom-made design deploying the CPM2-1200-0160B dies. The layout was evaluated using Ansys Q3D Extractor, and full parasitic equivalent circuit has been extracted at the frequency of 200 MHz and imported to SPICE. A simplified circuit schematic of the circuit considered has been depicted in Fig. 5. To provide additional means for validation of the proposed modeling method, ROHM SCT4018K dies have been included in the numerical comparison.

The relevant parameters of the circuits used are summarized in Table I. Aside from the elements depicted in Fig. 5, the parasitic equivalent circuit using in the numerical comparison contains a full RLGC representation.

To guide the potential model users on the expected model accuracy, the differences between the original model and the approximate implementation were quantified using the standard switching waveform metrics. This means rise and fall times, percentage overshoot, and switching loss. The calculation of switching metrics for the turn-ON transient have been depicted in Fig. 6.

In calculation of rise and fall times, standard transition between 10% and 90% of the steady state value were used. The switch turn-ON has been simulated in the presented circuits at four different current and voltage levels to quantify the behavior differences between the original and approximate models over a wider range. Due to the convergence issues with the original model, more favorable matrix conditioning has been applied in the simulations including it, using the.rshunt command. This move was necessary to enable a direct comparison between the models.

Tables II and III summarize the solver settings used to reach acceptable accuracy for original and approximate models of the

TABLE I
Relevant Circuit Parameters and Their Variation in This Work

Parameter	Value
Dies	CREE CPM2-1200-0160B, ROHM SCT4018K
Diodes	CREE CPW41200S010B
Vdc	200, 500, 700, 1200 V
Vg	-5/15 V
Rgext	30, 82 Ω
Rg1-4	10 Ω
Cdc2	4.7 uF
Chp	100 nF
Lload	103 μ H
Iload	4, 10, 16, 28.5 A

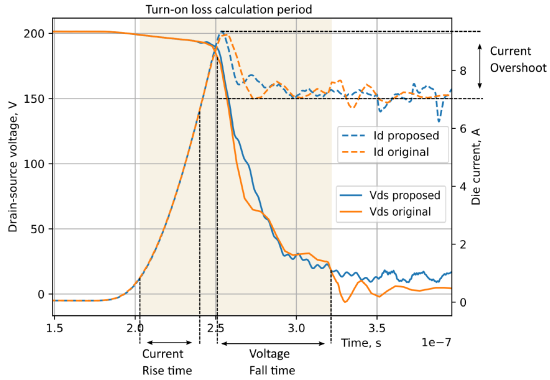


Fig. 6. Visualization of the turn-ON switching metrics used for model comparison.

TABLE II
SPICE Solver Settings for Reaching an Acceptable Accuracy for CMP2-1200-0160B, at V_{DS} = 100 V, I_D = 28 A and R_G = 82 Ω

Parameter	Baseline	Original	Approximate
Max. timestep	0.2 ns	0.7 ns	4 ns
reltol	0.001	0.001	0.004
abstol	1e-12	1e-10	1e-10
chgtol	1e-12	1e-10	1e-10
gmin	1e-12	1e-12	1e-18
vntol	1e-12	1e-10	1e-10
trtol	1	2	2
rshunt	1MEG	1MEG	-

TABLE III
SPICE SOLVER SETTINGS FOR REACHING AN ACCEPTABLE ACCURACY FOR SCT4018K, AT V_{DS} = 1000 V, I_D = 28 A AND R_G = 30 Ω

Parameter	Baseline	Original	Approximate
Max. timestep	0.4 ns	5 ns	6 ns
reltol	0.001	0.01	0.01
abstol	1e-12	1e-10	1e-10
chgtol	1e-12	1e-10	1e-10
gmin	1e-12	1e-12	1e-14
vntol	1e-12	1e-10	1e-10
trtol	1	2	4
rshunt	1MEG	1MEG	1MEG

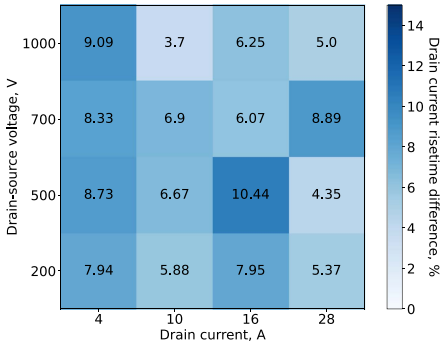


Fig. 7. Current rise time difference between original and approximate model, at different voltage and current levels for CREE CMP-1200-0160B.

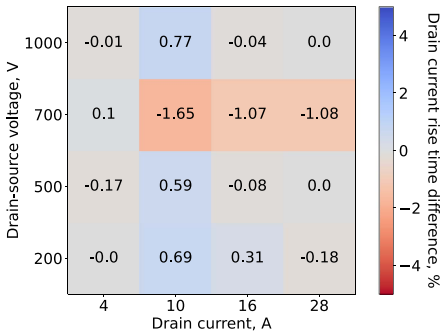


Fig. 8. Current rise time difference between original and approximate model, at different voltage and current levels for ROHM SCT4018K.

selected switches. The base parameters have been chosen to guarantee consistent convergence across the whole voltage and current range for the minimal external gate resistance achievable, corresponding to the fastest transients for which this comparison was found to be feasible. In the case of CREE CPM-2-1200-0160B, consistent convergence was found to be achievable only at higher gate resistance values, such as 82 Ω. The resistance of 30 Ω has been used for the SCT4018K. The achieved solver setting relaxation can vary with the application case and is provided as a means of quantifying the impact of approximate model implementation.

Fig. 7 depicts the percentage difference in current rise time simulated with the original and the approximate model. The agreement between the models is generally good and appears to be improving with the drain current level. In the case of SCT4018K the agreement is even better, as depicted in Fig. 8.

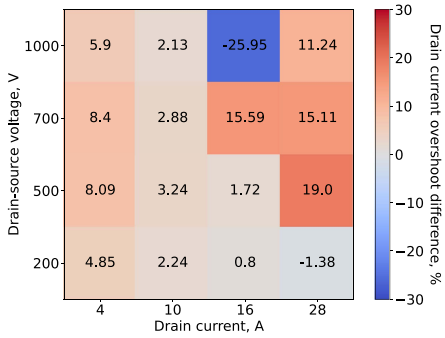


Fig. 9. Current overshoot difference between original and approximate model, at different voltage and current levels for CREE CMP-1200-0160B.

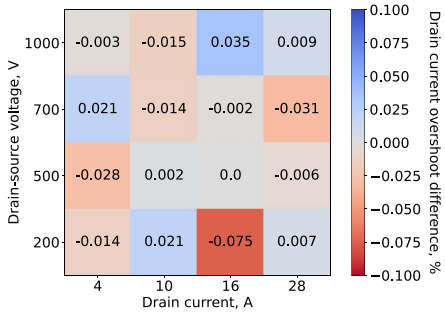


Fig. 10. Current overshoot difference between original and approximate model, at different voltage and current levels for ROHM SCT4018K.

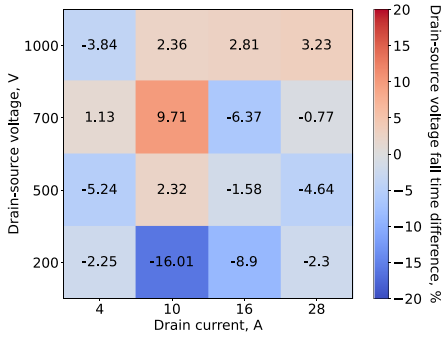


Fig. 11. Drain-source voltage fall time difference between original and approximate model, at different voltage and current levels for CREE CMP-1200-0160B.

Fig. 9 shows the opposite trend compared to Fig. 7, where the difference in predicted current overshoot increases at higher drain-source voltage and drain current levels. This difference could potentially originate from SPICE relative tolerance adjustment, allowing for a larger error margins at proportionally larger magnitudes.

Fig. 10 depicts the current overshoot difference between original and approximate models for ROHM SCT4018K. The matching between the models is close, and no particular error trends are observed.

In general, the approximate model shows a good agreement with the original model in current rise time and overshoot prediction.

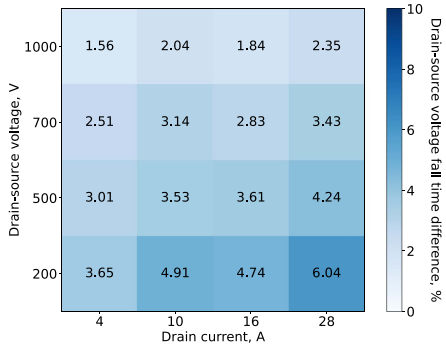


Fig. 12. Drain-source voltage fall time difference between original and approximate model, at different voltage and current levels for ROHM SCT4018K.

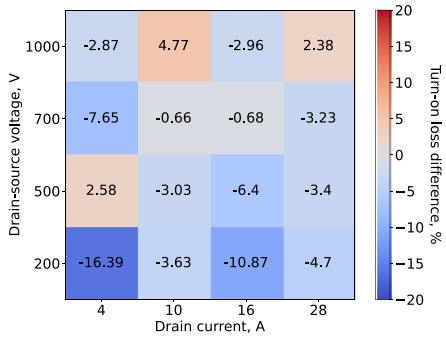


Fig. 13. Turn-ON loss difference between original and approximate model, at different voltage and current levels for CREE CMP-1200-0160B.

Fig. 11 depicts the difference in voltage fall time simulated using both models for CREE CMP-1200-0160B. Once again, a close agreement is observed, regardless of the voltage and current levels.

For ROHM SCT4018K, the drain-source voltage fall time difference between both models shows a clear trend depicted in Fig. 12. The discrepancy increases with drain current magnitude, and decreases with the drain-source voltage magnitude.

The difference in CREE CMP-1200-0160B turn-on loss estimation in both models is shown in Fig. 13, showing a good agreement between both of the models. The estimation diverges slightly more at the lower voltage levels, however not at all current levels. The low voltage area experienced generally higher convergence issues, therefore it could be a potential culprit behind this inconsistency. As for the ROHM SCT4018K, the turn-ON loss estimation difference between approximate and original models is lower than in the case of CREE CMP-1200-0160B, and does not show clear trends.

Finally, the acceleration of simulation time with the application of approximate models has been quantified in Figs. 15 and 16. Overall, an acceleration of 5%–20% is observed in the most of the operating range, with exception in the low voltage high current region. This acceleration showcases the improved convergence properties, even without the additional acceleration methods.

As for the approximate model of ROHM SCT4018K acceleration of simulation times up to 60% is observed, performing even better than in the case of CREE CMP-1200-0160B. In the case of

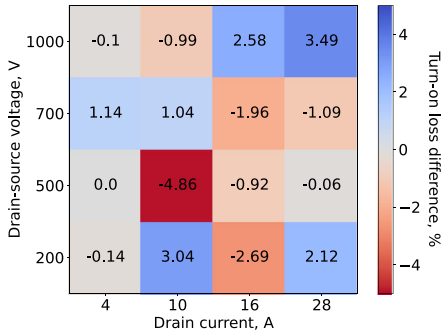


Fig. 14. Turn-ON loss difference between original and approximate model, at different voltage and current levels for ROHM SCT4018K.

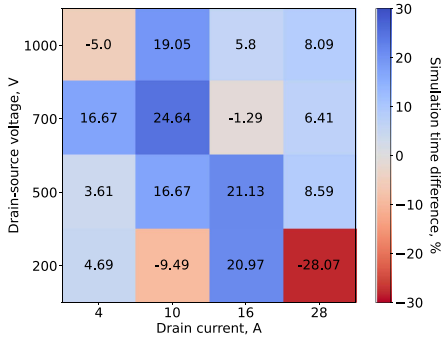


Fig. 15. CMP-1200-0160B simulation time acceleration at different voltage and current levels, positive values signifying shorter simulation time.

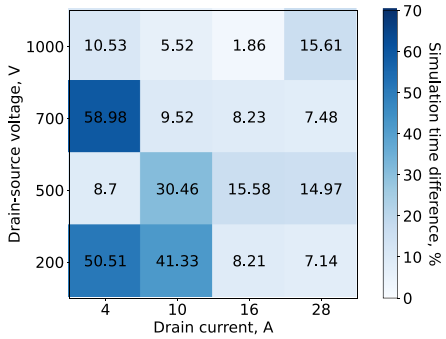


Fig. 16. SCT4018K simulation time acceleration at different voltage and current levels, positive values signifying shorter simulation time.

ROHM SCT4018K the observed simulation times are generally longer, which may have provided more room for computational cost savings by using the approximate model implementation. The absolute simulation times for the original and approximate models of Cree CMP-1200-0160B and ROHM SCT4018K are presented in Tables IV and V.

To provide additional validation, approximate modeling concept has been evaluated at a wide range of junction temperatures, with the results presented in Figs. 18 and 19.

The approximate model of CREE CMP-1200-0160B accurately captures the temperature dependency, matching the original manufacturer-provided model. A slight discrepancy can be observed in the decay phase of the turn-ON current transient at 125°.

TABLE IV
ABSOLUTE SIMULATION TIME COMPARISON FOR CREE CPM2-1200-0160B, AT RG = 82 Ω AND TJ = 25 °C

Id \Vd		200 V	500 V	700 V	1000 V
4A	Original:	64 s	66.4 s	84 s	60.6 s
	Proposed:	61 s	64 s	70 s	63 s
10A	Original:	54.8 s	71 s	69 s	84.25
	Proposed:	60 s	56 s	52 s	68.8
16A	Original:	94.1 s	92.5 s	70 s	69 s
	Proposed:	73.5 s	67 s	70.9 s	65 s
28A	Original:	57.9 s	71 s	78 s	81.6 s
	Proposed:	75.3 s	64.9 s	73 s	75 s

TABLE V
ABSOLUTE SIMULATION TIME COMPARISON FOR ROHM SCT4018K, AT RG = 30 Ω AND TJ = 25 °C

Id \Vd		200 V	500 V	700 V	1000 V
4A	Original:	198 s	115 s	295 s	285 s
	Proposed:	98 s	105 s	121 s	255 s
10A	Original:	196 s	174 s	168 s	181 s
	Proposed:	115 s	121 s	152 s	171 s
16A	Original:	134 s	154 s	158 s	161 s
	Proposed:	123 s	130 s	145 s	158 s
28A	Original:	140 s	167 s	147 s	173 s
	Proposed:	130 s	142 s	136 s	146 s

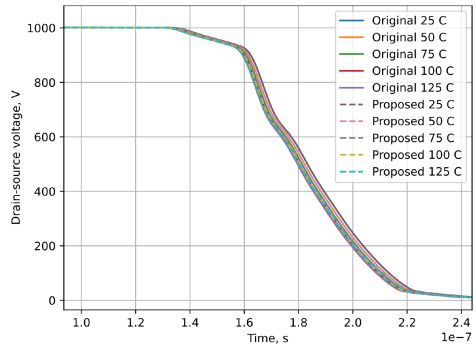


Fig. 17. Turn-ON voltage waveforms for CREE CMP-1200-0160B under a variation of temperature, at Rg = 30 Ω.

Similarly to the CREE CMP-1200-0160B, the approximate model of ROHM SCT4018K retains the accuracy in the modeling of temperature dependencies.

The proposed approximate modeling approach shows a good agreement with the original model, especially in the loss and voltage fall time estimation. It can therefore be assumed that the linear approximation is sufficiently valid for approximating the charge and channel equations between the time steps.

V. EXPERIMENTAL VALIDATION

The simulated cases have been verified against the experimental results in the system depicted in Fig. 21.

The power module populated with four parallel-connected CREE CMP-1200-0160B bare dies per switching position has been evaluated at a 28.5 A load and dc-bus voltage of 200 V. A comparison of voltage waveforms between the original SPICE model, the approximate model, and the experimental measurement is depicted in Fig. 22.

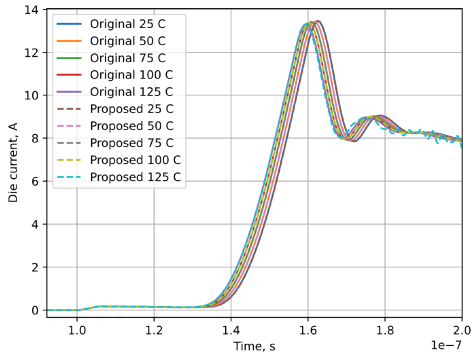


Fig. 18. Turn-ON current waveforms for CREE CMP-1200-0160B under a variation of temperature, at Rg = 30 Ω.

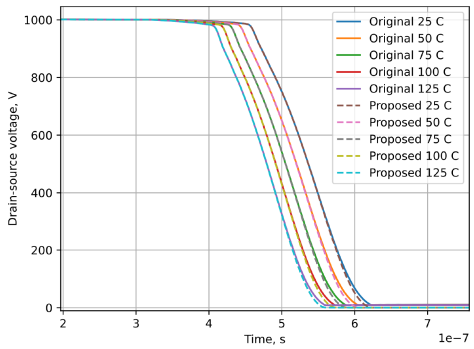


Fig. 19. Turn-ON voltage waveforms for ROHM SCT4018K under a variation of temperature, at Rg = 30 Ω.

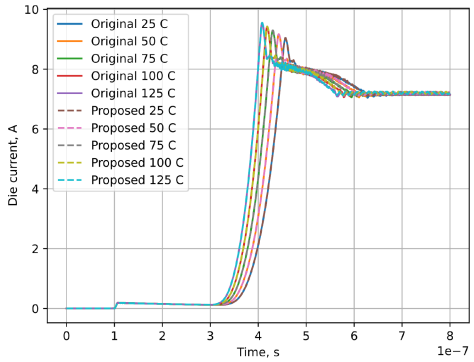
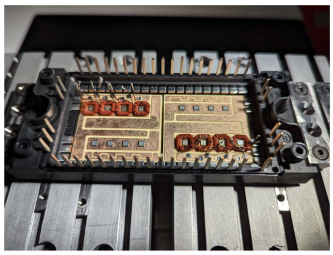
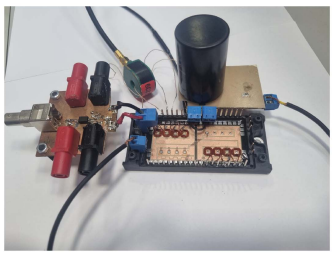


Fig. 20. Turn-ON current waveforms for ROHM SCT4018K under a variation of temperature, at Rg = 30 Ω.

The current measurement has been conducted using a two-stage current sensor that consists of a Pearson current monitor and current transformer that is embedded inside the power module [28]. The current transformer is encircling the die which behaves as its primary winding. During switching of the dies, a current is induced in the secondary winding of the current transformers which is obtained using the Pearson current monitor. By considering the turns ratio and magnetic coupling coefficient of the embedded current transformer, the read secondary winding current by the Pearson current monitor is converted to the actual die current. The sensor has been calibrated using a 30 MHz CWT mini Rogowski coil. The voltage has been measured at



(a)



(b)

Fig. 21. (a) Power module used and (b) setup with DC-link and driver board.

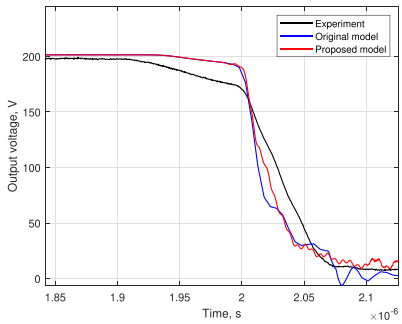


Fig. 22. Turn-ON voltage waveform comparison between the simulated models and experimental results.

the module output terminals, using Tektronix P6139B 500 MHz passive voltage problems. All of the measurements have been conducted using LeCroy HDO6054A oscilloscope.

Fig. 22 presents the comparison between experimental and simulated output voltage waveforms. A very close agreement is observed, with a slight difference at the end of the voltage fall phase.

Fig. 23 compares the experimental and simulated currents of one of the dies. A good agreement is observed through the most of the current rise phase. After the overshoot, a significant mismatch is observed. This mismatch is likely related to the die parameter distribution effect on the current sharing, particularly the gate threshold voltage as the device turn-ON seems to be only slightly accelerated compared to the simulation. This might cause it to conduct a larger part of the current until the rest of the parallel devices turn ON, resulting in the observed mismatch. In this case, the other dies would conduct significantly lower current than predicted, which can be seen in Fig. 24.

Contrary to Die 1, Die 4 current rise proceeds slower, and results in a much lower overshoot than predicted by the simulations.

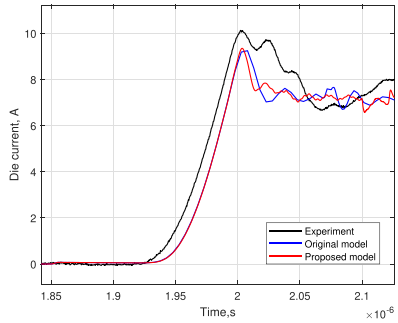


Fig. 23. Die 1 turn-ON current waveform comparison between the simulated models and experimental results.

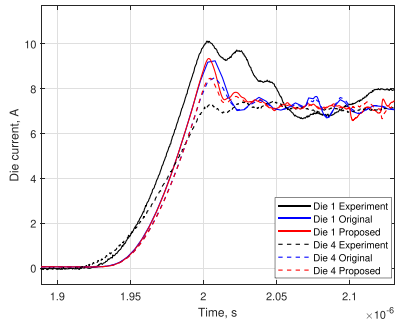


Fig. 24. Die 1 and 4 turn-ON current waveform comparison between the simulated models and experimental results.

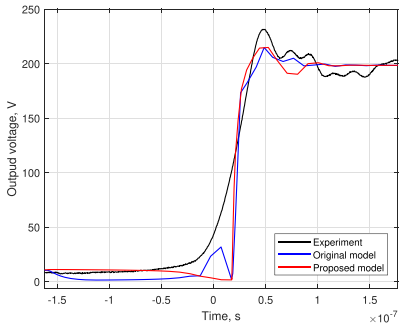


Fig. 25. Turn-OFF voltage waveform comparison between the simulated models and experimental results.

A comparison between the experimental and simulated voltage waveforms is presented in Fig. 25. An agreement is observed, with slight mismatches in the voltage overshoot and at the start of the transient.

The turn-OFF current waveforms of the first die are depicted in Fig. 26, showing a significant difference between the experiment, and both simulation models. The proposed model predicts a steeper transition, leading to a current undershoot while the original model predicts additional overshoot at the start of the transient. Both simulation models predict a jump in the middle of the transient, which was found to originate from the R_{ds} variation due to gate voltage oscillations at the Miller plateau. The measurement result shows a more damped transient, with slight oscillations at the end of it. It is likely that a part of the oscillations is not registered by the sensor.

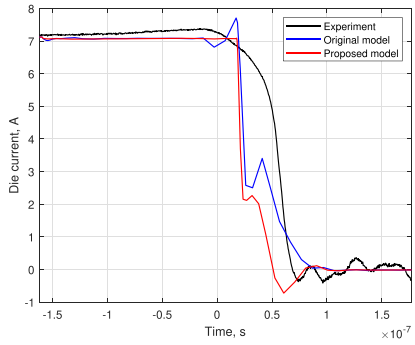


Fig. 26. Die 1 turn-OFF current waveform comparison between the simulated models and experimental results.

TABLE VI
SWITCHING METRICS COMPARISON BETWEEN THE PROPOSED AND ORIGINAL MODEL(TURN-ON)

Metric	Original	Proposed	Exp.	Diff.	Unit
Voltage fall time	88.7	86.6	90	1.4/3.8%	ns
Current rise time	37.82	37.80	40	5.4/5.5%	ns
Current overshoot	31.56%	30.58%	40%	21.1/23.6%	%

TABLE VII
SWITCHING METRICS COMPARISON BETWEEN THE PROPOSED AND ORIGINAL MODEL(TURN-OFF)

Metric	Original	Proposed	Exp.	Diff.	Unit
Voltage rise time	7.5	7.5	49	84.7%	ns
Current fall time	40.9	32.5	33	23.9/1.5%	ns
Voltage overshoot	7%	4.5%	15.5%	54.9/73.3%	%

The estimated sensor bandwidth is 35 MHz, while the duration of the turn-OFF current transient approaches 30 ns. Capturing the phenomenon lasting approximately 10–20 ns in measured waveforms would require a current sensor having a bandwidth of 100–200 MHz, which exceeds the bandwidth of both in-house developed and commercially available sensors applicable to die current measurement [30].

Finally, the switching metrics were calculated to provide a quantitative comparison between the simulation models and experiment.

Table VI shows a good match between the simulation models and the experiment. The biggest discrepancy can be observed for the current overshoot, as it could be noticed in the current waveforms.

The rapid turn-OFF leads to more significant differences between the simulation models and the experimental results. Voltage fall time and overshoot exhibits the highest mismatch, however the said difference appears to the same extent in both the approximate and original model. It worth noting, that the approximate model provided a much more accurate current fall time prediction at only 1.5% error compared to 23.9% in the case of the original model. It also captured the current undershoot, clearly present in the measurement results.

This proves that the approximate model formulation retains the accuracy of the behavioral SPICE model that served as a base for their formulation.

VI. CONCLUSION

This article presented a novel approximate SPICE modeling approach for transient simulation of nonlinear devices, such as SiC MOSFETs. The proposed approach allows to disconnect the model formulation in the netlist and the full nonlinear model formulation by utilizing a well-known multivariate Taylor approximation updated at each time step. This enables the behavioral models to utilize predefined linear companion models in a similar manner to the built-in models. This approach improves the convergence and moves the computation of nonlinear model updates outside the SPICE software, opening a path to future software and hardware acceleration, such as deployment of parameter updates on FPGA/GPU or replacement by a trained machine learning model. Without utilizing additional acceleration methods, the average acceleration of 7% and 36.8% has been observed, with the best case reaching up to 24.6% and 59% without additional acceleration measures. The accuracy of the approximate modeling is verified by modeling and simulating a power module populated with four parallel SiC MOSFET dies, showing a good agreement.

APPENDIX
SPICE IMPLEMENTATION

The original CMP-1200-0160B channel equations

```
G1 d1 s1 value = 'if(V(d1,s1)<0,-p10
+ *V(NET1,0)*((log(1+exp((v(g2,s1)
+ -V(NET2,0))/p9)))**p5)*(1+p8*v(s1,d1))
+ ,p10*V(NET1,0)*((log(1+exp((v(g2,s1)-
+ V(NET2,0))/p9)))**p5)*(1+p8*v(d1,s1)))'

G2 d1 s1 value = 'if(V(d1,s1)<0,
+ p10*V(NET1,0)*((log(1+exp((v(g2,s1)
+ -V(NET2,0)-p6*(v(s1,d1))**p7)/p9)))**p5)
+ *(1+p8*v(s1,d1)),-p10*V(NET1,0)*
+ ((log(1+exp((v(g2,s1)-V(NET2,0)-p6*
+ (v(d1,s1))**p7)/p9)))**p5)*(1+p8*v(d1,s1)))'
```

The proposed CMP-1200-0160B channel equation

```
G5 d11 s1 value = '(V(chan1)+V(chan11))+
+ (v(d1,s1)-V(x1))*(V(chan2)+V(chan21))+
+ (V(NET1,0)-V(x2))*(V(chan3)+V(chan31))+
+ (V(NET2,0)-V(x3))*(V(chan4)+V(chan41))+
+ (v(g2,s1)-V(x4))*(V(chan5)+V(chan51))'
Vx1 x1 0 external
Vx2 x2 0 external
Vx3 x3 0 external
Vx4 x4 0 external
Vchannel1 chan1 0 external
Vchannel2 chan2 0 external
Vchannel3 chan3 0 external
Vchannel4 chan4 0 external
Vchannel5 chan5 0 external
Vchannel11 chan11 0 external
Vchannel21 chan21 0 external
Vchannel31 chan31 0 external
Vchannel41 chan41 0 external
Vchannel51 chan51 0 external
```

The original CMP-1200-0160B charge equation
The proposed CMP-1200-0160B charge equation:

```
G11 g0 d1 value ='k1*((1+(limit(v(d1,g),0,420))*
+ (1+ka*(1+TANH(kb*V(d1,g)-kc))/2))**-k2)
+ *ddt(v(g,d1))'
```

```
G11 g0 d1 value ='V(ch1) + (v(d1,g)-V(x))
+ *V(ch2) + (ddt(v(g,d1))-V(y))*V(ch3)'
Vch1 ch1 0 dc 0 external
Vch2 ch2 0 dc 0 external
Vch3 ch3 0 dc 0 external
Vx x 0 dc 0 external
Vy y 0 dc 0 external
```

The original SCT4018K channel equation

```
.FUNC I1(V,W,Tj)
+ {V*(1+802m*(TANH((V-57.77)/57.77)+1)/
+ (10*EXP(-V/141.6)*EXP((Tj-T0)/95.44k)))*
+  W/(ABS(W)+802m*(TANH((V-57.77)/57.77)+1)*
+ EXP((Tj-T0)/-173.6))}
```

The proposed SCT4018K channel equation

```
.FUNC AI1(V,W,Tj,Chan,Chan1,Chan2,Chan3,V1,W1,Tj1)
+ {Chan + (V-V1)*Chan1 + (W-W1)*Chan2 +
+ (Tj-Tj1)*Chan3}
Vchv1 CHV1 0 external
Vchw1 CHW1 0 external
VchT1 CHT1 0 external
Vchan Chan 0 external
Vchan1 Chan1 0 external
Vchan2 Chan2 0 external
Vchan3 Chan3 0 external
```

The original SCT4018K charge equation

```
.FUNC C1(U,V,W,X) {((32.86k*(V-647.3m)+144.7k*
+ (1-317.5*TANH(W/317.5)/3.236)**-523.3m)*
+ (1+(TANH((U+2.871)/1.192)-1)/2.078))*
+ (376.8m*TANH(2.708*X-1.826)-121.9m*X+1.356)}
```

The proposed SCT4018K charge equation

```
.FUNC AC1(U,V,W,X,Char,Char1,Char2,Char3,Char4,
+ U1, V1, W1, X1)
+ {Char + (U-U1)*Char1 + (V-V1)*Char2 +
+ (W-W1)*Char3 + (X-X1)*Char4}

Vu1 U1 0 external
Vv1 V1 0 external
Vw1 W1 0 external
Vx1 X1 0 external
Vchar Char 0 external
Vchar1 Char1 0 external
Vchar2 Char2 0 external
Vchar3 Char3 0 external
Vchar4 Char4 0 external
```

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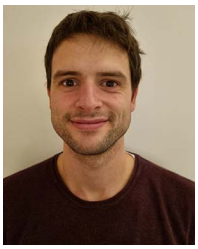

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