An Ultrawide Range Pulse Width Modulated LLC Converter With Voltage Multiplier Rectifiers

Zhengming Hou, *Graduate Student Member, IEEE*, Dong Jiao, *Graduate Student Member, IEEE*, and Jih-Sheng Lai, *Life Fellow, IEEE*

***Abstract*—This article presents a voltage multiplier rectifier-based LLC resonant converter that achieves an ultrawide range of the output voltage with pulse width modulation (PWM) of the auxiliary switches on the secondary side. Compared with the pulse frequency modulated LLC topologies, the proposed topology operates at a fixed frequency and features a bounded voltage gain range. Thus, the resonant tank design can be optimized at one frequency, and high efficiency can be realized throughout the output voltage range. Furthermore, the proposed topology greatly extends the maximum PWM normalized voltage gain range to 4.0 with two-mode operations. Meanwhile, zero-voltage switching is realized for all the switches, and a seamless mode transition is achieved by the proposed converter. At last, a time-domain-based analysis and optimization methodology are proposed. A 300 kHz, 1 kW, 400 V input/250–1000 V output prototype demonstrates high efficiency through the output range and achieves 97.69% peak efficiency.**

***Index Terms*—Isolated dc–dc converter, LLC, pulse width modulation (PWM), seamless transition, high efficiency, ultrawide range, voltage multiplier rectifiers, zero-voltage switching (ZVS).**

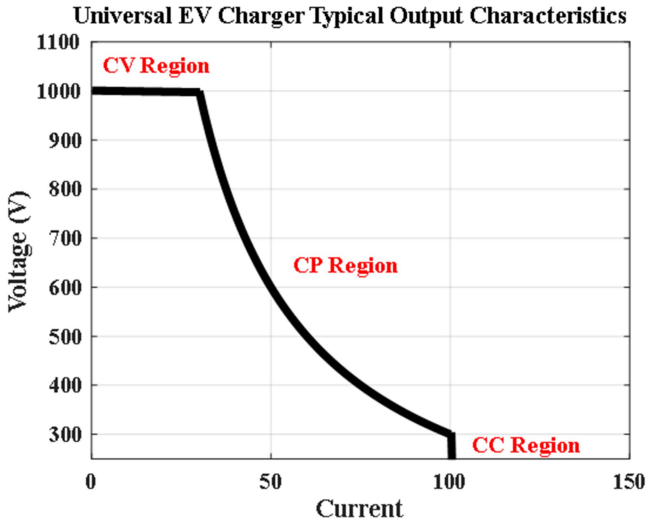

Fig. 1. Typical universal EV charger output characteristics.

I. Introduction

THE emergence of electric vehicles (EVs) and renewable energy battery storage systems aims to reduce greenhouse gas emissions for sustainable development. As the EV market booms, numerous automotive original equipment manufacturers (OEMs) have their own EV designs. However, the battery voltage varies from 250 to 1000 V between different OEMs and EV models. Although the nonisolated pulse width modulation (PWM) converter proposed in [1], [2], and [3] demonstrates high efficiency, high power density, and wide output range, galvanic isolation is preferred for safety considerations. Consequently, an ultrawide range isolated dc–dc converter is desired to meet the requirements of different EVs, as depicted in Fig. 1.

To achieve high efficiency, the LLC resonant converter has been widely adopted for battery charging applications due to its soft switching capability in [4], [5], and [6]. Unfortunately, the conventional LLC resonant converter fails to regulate the output voltage over an ultrawide range. On the other hand, the significant efficiency drop of the LLC converter is inevitable in achieving a wide regulation range as its operating point deviates far from its series resonant frequency. At last, the load-dependent characteristic of the LLC resonant converter makes it difficult to optimize the resonant tank throughout the regulation range. A variable dc-link voltage regulated by the front end power factor correction stage is proposed in [7] and [8] to extend the output voltage range. However, the voltage stress on the dc-link side is increased as well. Consequently, it is more beneficial to extend the voltage range of the LLC resonant converter stage.

Different techniques have been proposed to resolve the disadvantages of the conventional LLC resonant converter. All the proposed techniques can be arranged into the following four categories.

1) Multimode LLC topology.
2) Multiresonant tank topology.
3) Partial power series resonant converter (SRC)-based topology.
4) Hybrid resonant converter strategy.

The conventional LLC converter voltage gain depends on the resonant tank parameters. Hence, the first category introduces additional operation modes to extend the voltage regulation range. In [9], different operation modes are realized by switching around the odd-order subharmonic modes to extend the output

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voltage range. In [10], [11], [12], and [13] the relays or auxiliary switches are implemented on the output side to reconfigure the output series and parallel connections to extend the output voltage range. In [14], [15], [16], and [17], the adjustable turns-ratio transformer LLC topologies, realized by the relays or auxiliary switches to alter the turns ratio among different windings, are proposed to extend the voltage regulation range. In [18], an adjustable magnetizing LLC resonant converter is proposed to realize the wide regulation range. In [19] and [20], a symmetrical split resonant tank approach is adopted to generate three different operation modes. In [21], [22], [23], [24], and [25], different operation modes are realized by reconfiguring between half-bridge, full-bridge, and voltage multiplier rectifiers. To further extend the voltage range, an H5 bridge with asymmetrical resonant tank topology is proposed in [26] and [27], which can be reconfigured up to six different modes. Although the voltage regulation range is extended via multimode operations, the wide switching frequency range still exists. Furthermore, mode transitions raise concerns about the dynamic stress of the resonant components.

The second category reshapes the gain curve to extend the voltage range by implementing a higher order resonant tank. In [28], [29], and [30], the LCLCL resonant topologies are proposed by placing an additional L and C to the LLC resonant tank. In [31], an LLC-type converter with paralleling two different *LC* resonant tanks is proposed. Although zero gain can be achieved in the multiresonant tank topologies, higher costs, and larger sizes are inevitable with the additional *LC* resonant tank. Furthermore, the leakage inductance is no longer considered part of the resonant tank since it is impossible to parallel the *LC* tank with the leakage inductance.

The partial power concept is implemented on the SRC to improve efficiency and power density by regulating voltage through a partial voltage conversion cell in [32], [33], and [34]. The unregulated LLC-DCX with regulated buck cells system demonstrates great efficiency and power density improvement in [32] and [33]. However, the hard switching in the multiphase buck cell is inevitable. In [34], a fully soft-switching LLC-DCX integrated with full-bridge converter is proposed. Nevertheless, the partial power technique is not suitable for ultra-wide range applications because the partial power ratio is proportional to the output voltage range.

The hybrid resonant converter strategy is also applied to the wide range resonant converter for the efficiency improvement by shrinking the operation frequency range. A phase shift and dual resonant hybrid converter is proposed in [35]. A fixed frequency hybrid modulated resonant converter is proposed in [36]. The buck mode is realized by the primary phase shift while the boost mode is realized by the secondary phase shift. Nevertheless, the zero-voltage switching (ZVS) is not guaranteed for the entire load range with phase shift modulation. Furthermore, the PWM-based resonant converter topologies are proposed to enhance efficiency while achieving a bounded gain range. In [37], the inner synchronous rectifiers (SRs) of the voltage quadruple rectifier (VQR) are driven by PWM signals. However, the hard switching on the SRs prevents it from pushing to a higher switching frequency. In [38] and [39], several fully ZVS PWM-type LLC topologies are proposed. A 1.0–2.0 normalized gain range (respective to its minimum voltage) is achieved via the auxiliary MOSFETs switching between the voltage multiplier and full-bridge. A pulse frequency modulated (PFM) and PWM hybrid converter is proposed in [40] to achieve an ultrawide output range. While high efficiency is achieved in the PMW region, the converter struggles with efficiency when operating in the PFM region.

Among all the techniques, the PWM-type resonant topology is attractive because it is not only beneficial for the high efficiency, but also the bounded gain range. This article proposes a novel resonant converter with voltage multiplier rectifiers covering an ultrawide output voltage range only with PWM. The contributions of this article are summarized as follows.

1) The bounded gain range achieved by PWM is greatly extended from 2.0 to 4.0, ensuring high efficiency through an ultrawide output range.
2) A seamless mode transition is achieved on the proposed converter.
3) A time-domain-based analysis is presented for the resonant tank optimization.

The rest of this article is organized as follows. In Section II, the topology of the proposed converter and operation principles are explained. The time-domain-based resonant tank optimization methodology is presented in Section III. Sections IV and V discuss the impacts of tolerance on the resonant tank parameters and the digital control implementation, respectively. The experimental results are presented and discussed in Section VI. Finally, Section VII concludes this article.

II. Proposed Converter and Operation Principles

Fig. 2 shows the proposed LLC converter. The primary side consists of a full-bridge inverter (Q_1-Q_4), resonant inductor (L_r), resonant capacitor (C_r), and the transformer (L_m and T_1). The secondary rectifier is derived from a combination of a voltage doubler and a voltage quadrupler. The auxiliary switches Q_5 and Q_6 interconnect the switching nodes of the diode bridge and the middle point of the capacitor bridges ($C_{o1} - C_{o4}$). By examining the boundaries of D_{Q5} and D_{Q6}, the rectifier operates as a full-bridge rectifier, when $D_{Q5} \in [0, 0.5]$, $D_{Q6} \in [0, 0.5]$; a voltage doubler, when $D_{Q5} = 1$, $D_{Q6} \in [0, 0.5]$; a voltage quadrupler, when $D_{Q5} = 1$, $D_{Q6} = 1$. Consequently, the proposed converter operates at its resonant frequency to minimize the circulating energy while achieving a bounded gain range with soft switching turn-ON. By modulating the duty cycle of the auxiliary switches, the output voltage is regulated via controlling the V_{Co1} and V_{Co3} within $[0, \frac{V_{\text{in}}}{n}]$. In addition, it can be configurated into voltage doubler-PWM mode (VDM) and voltage quadrupler-PWM mode (VQM) to significantly extend the PWM gain range.

A. VDM Operation Principle

The normalized voltage gain defined in (1) is bound between 1.0 and 2.0 under PWM control in VDM

$$\text{Gain}_{\text{normalized}} = n\frac{V_{\text{out}}}{V_{\text{in}}}. \tag{1}$$

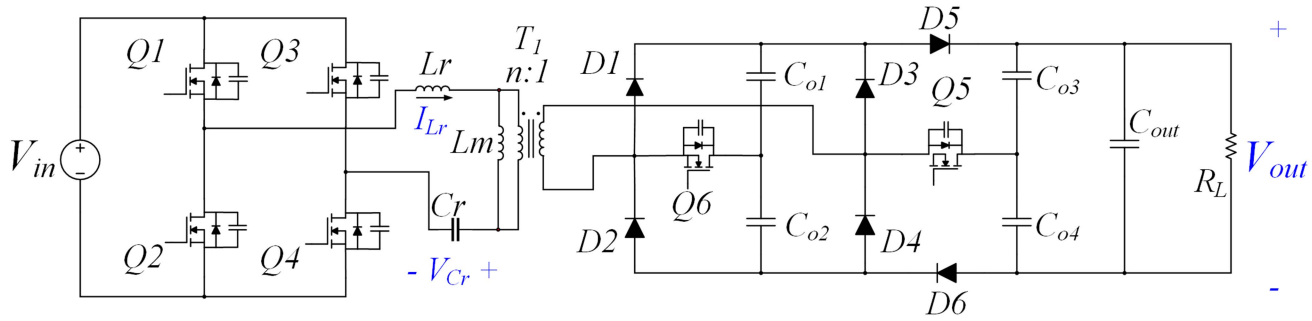

Fig. 2. Schematic of the proposed PWM LLC converter with voltage multiplier rectifiers.

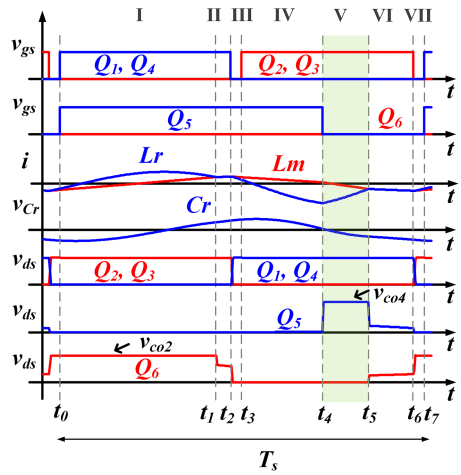

Fig. 3. Typical steady-state waveforms in VDM.

The primary full-bridge is driven by the fixed frequency complementary square waveforms with 50% duty cycle and certain dead time (t_d). The switching frequency is at its series resonant frequency f_r

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \ . \tag{2}$$

In VDM, Q_6 is OFF and Q_5 is switching at f_r with the rising edge alignment with respect to Q_1 as the waveforms depicted in Fig. 3. The asymmetrical resonant current waveform depicts that the positive cycle is "resonant cycle" and the negative cycle is "PWM cycle." Moreover, a small delay can be added between Q_1 and Q_5 to realize the ZVS turn-ON. It is worth mentioning that the voltage regulation functions only when the duty cycle of Q_5 ranges from 0.5 to 1.0. The secondary operates as a full-bridge rectifier (FBR) if the duty cycle of Q_5 is smaller than 0.5.

Fig. 4 displays the equivalent states in one switching cycle. The "body diode" symbol is utilized to distinguish the reverse conduction. The analysis is based on the following assumptions.

1) The voltage drops across the semiconductors are negligible.
2) The voltage ripples across $V_{Co1} - V_{Co4}$ are negligible.
3) The dead time is short enough to treat V_{Cr} and I_{Lm} as constants during dead time.

State I $[t_0 - t_1]$: Before t_0, all the FETs are OFF and the resonant current I_{Lr} is clamped by the magnetizing current I_{Lm}, which is negative. At t_0, the output capacitance of Q_1 and Q_4 are fully discharged and start conducting the reverse current through the channel. Hence, Q_1 and Q_4 are turned ON under ZVS. Meanwhile, the power is delivered to output via the resonant current I_{Lr}. Hence, Q_5 starts conducting the reverse current and achieves ZVS turn-ON as it functions as SR. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (3)–(5)

$$V_{Cr}(t) = (nV_{co5} + V_{cr0} - V_{\text{in}})\cos\left(\frac{t}{\sqrt{L_r C_r}}\right) - nV_{co5} + V_{\text{in}} + +I_{Lr0}\sqrt{\frac{L_r}{C_r}}\sin\left(\frac{t}{\sqrt{L_r C_r}}\right) \tag{3}$$

$$I_{Lr}(t) = -\sqrt{\frac{C_r}{L_r}}(nV_{co4} + V_{Cr0} - V_{\text{in}})\sin\left(\frac{t}{\sqrt{L_r C_r}}\right) + I_{Lr0}\cos\left(\frac{t}{\sqrt{L_r C_r}}\right) \tag{4}$$

$$I_{Lm}(t) = I_{Lm0} + \frac{nV_{co4}}{L_m}t \ . \tag{5}$$

State II $[t_1 - t_2]$: Q_1, Q_4, and Q_5 remains ON throughout this state. At t_1, the resonant current I_{Lr} is clamped by the magnetizing current I_{Lm} again. Hence, no energy is transferred to the secondary side and the output energy is provided by the output capacitors. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (6)–(8)

$$L_{\text{eq}} = L_r + L_m \tag{6}$$

$$V_{Cr}(t - t_1) = V_{\text{in}} + (V_{cr1} - V_{\text{in}})\cos\left(\frac{t - t_1}{\sqrt{L_{\text{eq}} C_r}}\right) + I_{Lr1}\sqrt{\frac{L_{\text{eq}}}{C_r}}\sin\left(\frac{t - t_1}{\sqrt{L_{\text{eq}} C_r}}\right) \tag{7}$$

$$I_{Lm}(t - t_1) = I_{Lr}(t - t_1) = \sqrt{\frac{C_r}{L_{\text{eq}}}}(-V_{Cr1} + V_{\text{in}})\sin\left(\frac{t - t_1}{\sqrt{L_{\text{eq}} C_r}}\right)$$

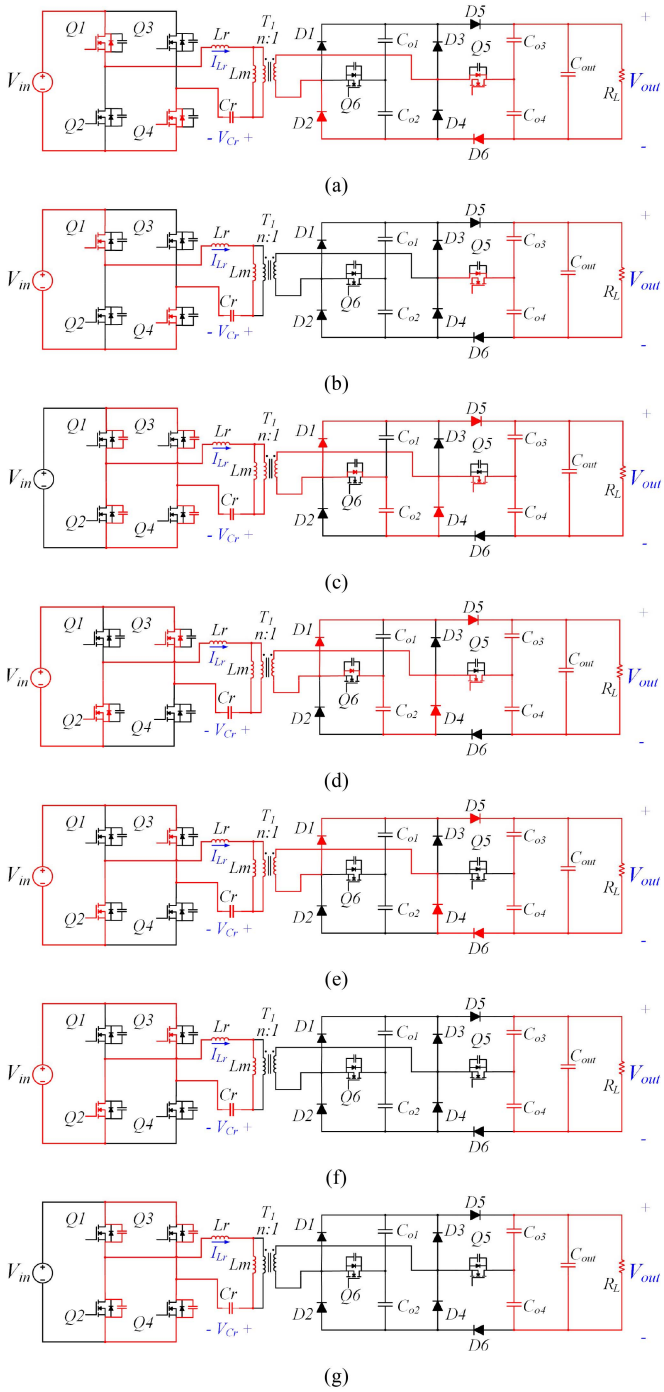

Fig. 4. Operation states in VDM. (a) State I $[t_0 - t_1]$. (b) State II $[t_1 - t_2]$. (c) State III $[t_2 - t_3]$. (d) State IV $[t_3 - t_4]$. (e) State V $[t_4 - t_5]$. (f) State VI $[t_5 - t_6]$. (g) State VII $[t_6 - t_7]$.

$$+ I_{Lr1} \cos\left(\frac{t - t_1}{\sqrt{L_{\text{eq}} C_r}}\right). \tag{8}$$

State III $[t_2 - t_3]$: Q_1, Q_4 are turned OFF while Q_5 remain ON and the primary entered the dead time for the ZVS realization. The resonant inductor is charged linearly. The output capacitance of Q_1, Q_4 (Q_2, Q_3) are charged (discharged) by the resonant current. At t_3, the output capacitance of Q_2 and Q_3 are fully discharged

$$V_{Cr2} = V_{Cr3} \tag{9}$$

$$I_{Lr3} = I_{Lr2} - \frac{n\left(V_{co4} - V_{\text{out}}\right) + V_{cr3} + V_{\text{in}}}{L_r} t_d \tag{10}$$

$$I_{Lm2} = I_{Lm3}\,. \tag{11}$$

State IV $[t_3 - t_4]$: At t_3, Q_2 and Q_3 are turned ON under ZVS. Q_5 remains on and the resonant current I_{Lr} is kept charging linearly until t_4. The power is transferred to the output side in this state. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (12)–(14)

$$V_{Cr}\ (t - t_3) = \left[n\left(V_{co4} - V_{\text{out}}\right) + V_{cr3} + V_{\text{in}}\right] \cos\left(\frac{t - t_3}{\sqrt{L_r C_r}}\right) - V_{\text{in}} + nV_{\text{out}} + I_{Lr3}\sqrt{\frac{L_r}{C_r}} \sin\left(\frac{t - t_3}{\sqrt{L_r C_r}}\right) \tag{12}$$

$$I_{Lm}\ (t - t_3) = I_{Lm3} - \frac{n\left(V_{\text{out}} - V_{co4}\right)}{L_m}(t - t_3) \tag{13}$$

$$I_{Lr}\ (t - t_3) = I_{Lr3} \cos\left(\frac{t - t_3}{\sqrt{L_r C_r}}\right) - \sqrt{\frac{C_r}{L_r}} - \left[n\left(V_{co4} - V_{\text{out}}\right) + V_{Cr3} + V_{\text{in}}\right] \sin\left(\frac{t - t_3}{\sqrt{L_r C_r}}\right). \tag{14}$$

State V $[t_4 - t_5]$: Q_2 and Q_3 remain ON in this state, while Q_5 is turned OFF at t_4. The resonant current I_{Lr} is discharged linearly until t_5. The power is transferred to the output side in this state until t_5. At t_5, the resonant current I_{Lr} equals to the magnetizing current I_{Lm}. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (15)–(17)

$$V_{Cr}\left(t - t_4\right) = \left(-nV_{\text{out}} + V_{cr4} + V_{\text{in}}\right) \cos\left(\frac{t - t_4}{\sqrt{L_r C_r}}\right) - V_{\text{in}} + nV_{\text{out}} + I_{Lr4}\sqrt{\frac{L_r}{C_r}} \sin\left(\frac{t - t_4}{\sqrt{L_r C_r}}\right) \tag{15}$$

$$I_{Lm}\ (t - t_4) = I_{Lm4} - \frac{nV_{\text{out}}}{L_m}(t - t_4) \tag{16}$$

$$I_{Lr}\left(t - t_4\right) = -\sqrt{\frac{C_r}{L_r}}\left(-nV_{\text{out}} + V_{Cr4} + V_{\text{in}}\right) \sin\left(\frac{t - t_4}{\sqrt{L_r C_r}}\right) + I_{Lr4} \cos\left(\frac{t - t_4}{\sqrt{L_r C_r}}\right). \tag{17}$$

State VI $[t_5 - t_6]$: At t_5, the resonant current I_{Lr} is clamped by magnetizing current I_{Lm} and the output energy is provided by the output capacitors. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (18)–(19)

$$V_{Cr}\ (t - t_5) = -V_{\text{in}} + \left(V_{cr5} + V_{\text{in}}\right) \cos\left(\frac{t - t_5}{\sqrt{L_{\text{eq}} C_r}}\right)$$

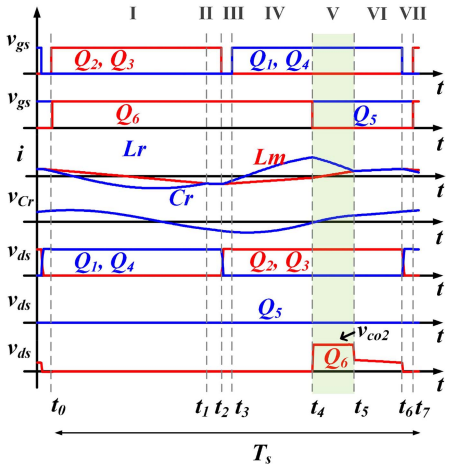

Fig. 5. Typical steady-state waveforms in VQM.

$$+ I_{Lr5}\sqrt{\frac{L_{\text{eq}}}{C_r}}\sin\left(\frac{t-t_5}{\sqrt{L_{\text{eq}}C_r}}\right) \tag{18}$$

$$I_{Lm}\ (t-t_5) = I_{Lr}\ \ (t-t_5) = I_{Lr5}\ \cos\left(\frac{t-t_5}{\sqrt{L_{\text{eq}}C_r}}\right) - \sqrt{\frac{C_r}{L_{\text{eq}}}}\,(V_{Cr5}+V_{\text{in}})\sin\left(\frac{t-t_5}{\sqrt{L_{\text{eq}}C_r}}\right). \tag{19}$$

State VII $[t_6 - t_7]$: Q_2, Q_3 are turned OFF and the primary entered the dead time for the ZVS realization. During this state, the resonant current I_{Lr} always equals the magnetizing current I_{Lm}. The output capacitance of Q_2, Q_3 (Q_1, Q_4) are charged (discharged) by the magnetizing current. At t_7 (t_0), the output capacitance of Q_1 and Q_4 are fully discharged. The resonant variables (I_{Lr}, V_{Cr}, and I_{Lm}) are expressed in (20)–(22)

$$V_{Cr6} = V_{Cr7} \tag{20}$$

$$I_{Lr6} = I_{Lr7} \tag{21}$$

$$I_{Lm6} = I_{Lm7}. \tag{22}$$

B. VQM Operation Principle

The normalized voltage gain lies within the range of 2.0–4.0 under PWM control in VQM. The primary operation is kept the same as in the VDM. Q_5 is always ON, forming a voltage doubler, in this mode. Q_6 will be aligned with Q_3 and it is modulated between 0.5 and 1.0 duty cycle for the voltage regulation. As the normalized voltage gain approaches 2.0 in VDM, the duty cycle of Q_5 also approaches to 1.0. There is no impact on Q_6 when it starts from the OFF state to 0.5 duty as Q_6 is clamped by D_1 when its duty is smaller than 0.5. Hence, seamless transitions can be achieved between VDM and VQM. The operation principle of VQM will be briefly explained because this mode can be considered as the mirror operation of Q_5 in VDM as shown in Figs. 5 and 6.

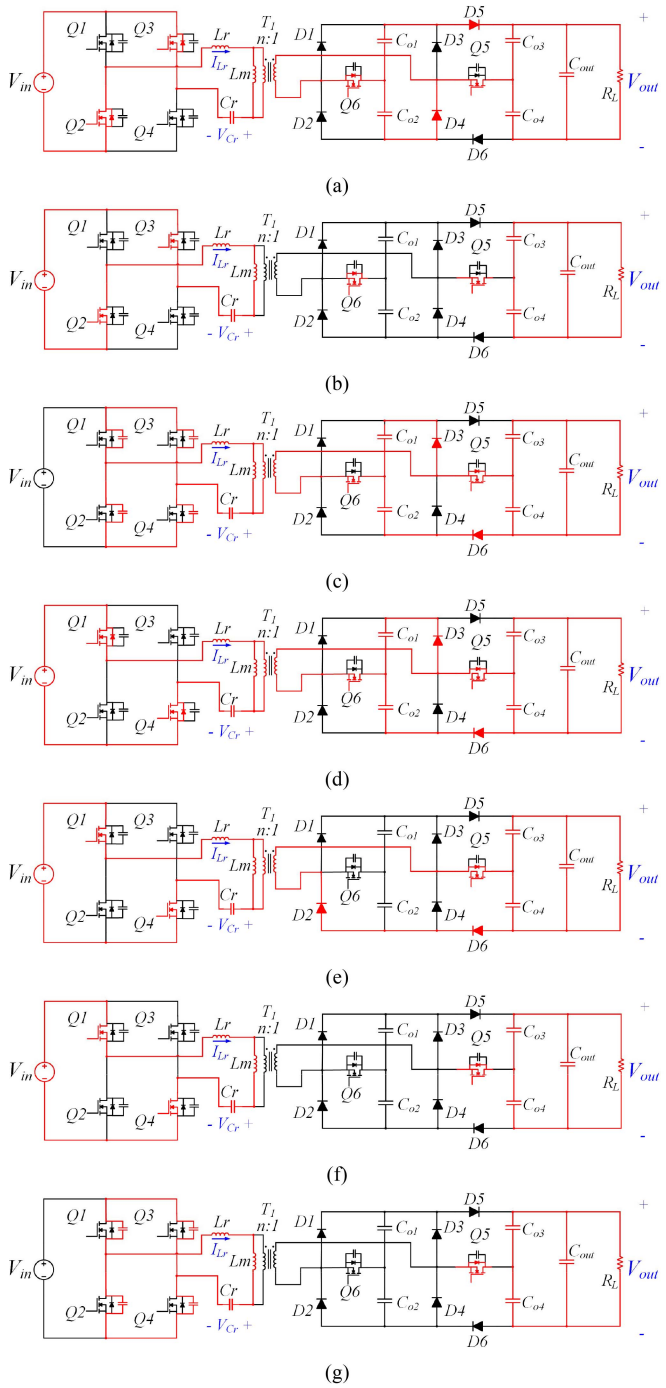

Fig. 6. Operation states in VQM. (a) State I $[t_0 - t_1]$. (b) State II $[t_1 - t_2]$. (c) State III $[t_2 - t_3]$. (d) State IV $[t_3 - t_4]$. (e) State V $[t_4 - t_5]$. (f) State VI $[t_5 - t_6]$. (g) State VII $[t_6 - t_7]$.

State I $[t_0 - t_1]$: Before t_0, all the primary FETs are OFF and the resonant current I_{Lr} is clamped by the magnetizing current I_{Lm}, which is positive. At t_0, the output capacitance of Q_2 and Q_3 are fully discharged and start conducting the reverse current through the channel. Hence, Q_2 and Q_3 are turned ON under ZVS. Meanwhile, the power is delivered to output via the resonant current I_{Lr}. Hence, Q_6 starts conducting the reverse current and achieves ZVS turn-ON as it functions as SR.

TABLE I
COMPARISONS OF THE NUMBER OF DIODE VOLTAGE DROPS

	Proposed		FBR	VQR
	VDM	VQM		
State I	$2V_F$	V_F		
State II	-	-		
State III	$2V_F$	V_F		
State IV	$2V_F$	V_F	$2V_F$	V_F
State V	$4V_F$	$2V_F$		
State VI	-	-		
State VII	-	-		

State II $[t_1 - t_2]$: Q_2, Q_3, and Q_6 remain ON through this state. At t_1, the resonant current I_{Lr} is clamped by the magnetizing current I_{Lm} again. Hence, no energy is transferred to the secondary side and the output energy is provided by the output capacitors.

State III $[t_2 - t_3]$: Q_2, Q_3 are turned OFF while Q_6remains ON and the primary entered the dead time for the ZVS realization. The resonant inductor is charged linearly. The output capacitance of Q_2, Q_3 (Q_1, Q_4) are charged (discharged) by the resonant current. At t_3, the output capacitance of Q_1 and Q_4 are fully discharged.

State IV $[t_3 - t_4]$: At t_3, Q_1 and Q_4 are turned ON under ZVS. Q_6 remains ON and the resonant current I_{Lr} is kept charging linearly until t_4. The power is transferred to the output side in this state.

State V $[t_4 - t_5]$: Q_1 and Q_4 remain ON in this state, while Q_6 is turned OFF at t_4. The resonant current I_{Lr} starts discharging linearly until t_5. The power is transferred to the output side in this state until t_5. At t_5, the resonant current I_{Lr} equals to the magnetizing current I_{Lm}.

State VI $[t_5 - t_6]$: At t_5, the resonant current I_{Lr} is clamped by magnetizing current I_{Lm} and the output energy is provided by the output capacitors.

State VII $[t_6 - t_7]$: Q_1, Q_4 are turned OFF and the primary entered the dead time for the ZVS realization. During this state, the resonant current I_{Lr} always equals to the magnetizing current I_{Lm}. The output capacitance of Q_1, Q_4 (Q_2, Q_3) are charged (discharged) by the magnetizing current. At t_7 (t_0), the output capacitance of Q_2 and Q_3 are fully discharged.

C. Diode Voltage Drop

Although multiple diodes conduct simultaneously, they primarily conduct with no more than two diodes in series for most of the time. Two diodes are conducted in series in VDM, and one diode is conducted in VQM. The only exception occurs during operation in state V. Four diodes are conducted in series in VDM, and two diodes are conducted in VQM which causes additional voltage drop losses, but this state only lasts for a short period, as highlighted in green in Figs. 3 and 5. Table I summarizes the number of diode voltage drops of the proposed rectifier compared to the conventional FBR and VQR. The diode voltage drop in VDM is akin to the FBR, while in VQM is akin to VQR.

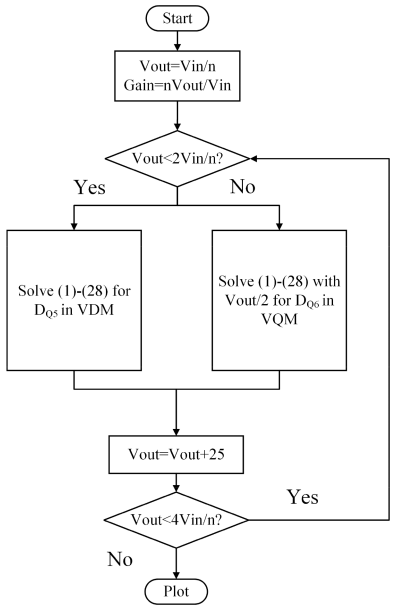

Fig. 7. Algorithm of deriving the corresponding duty for the gain curve.

D. Proposed Converter Steady State Gain Curve

The normalized voltage gain is bound between 1.0 and 4.0 by two independent control variables D_{Q5} and D_{Q6}. The duty cycle corresponding to the voltage gain in the steady state can be derived through time-domain-analysis. The starting point (t_0) and ending point (t_7) are consistent in the steady state. Within one switching cycle, the resonant current is clamped by the magnetizing current twice (t_1 and t_5). Moreover, the charge balance shall be achieved between the multiplier capacitors. Finally, energy conservation should be satisfied. According to these constraints, the equations are established in (23)–(28). Therefore, the voltage gain in VDM can be derived by solving (1)–(28) together. On the other hand, the voltage gain in VQM can be derived from VDM because one leg is configured as a voltage doubler. The derivation process is illustrated in Fig. 7. The normalized gain curve (voltage gain and duty cycle of Q_5 and Q_6) is plotted in Fig. 8

$$V_{Cr0} = V_{Cr7} \tag{23}$$

$$I_{Lm0} = I_{Lr0} = I_{Lr7} = I_{Lm7} \tag{24}$$

$$I_{Lr1} = I_{Lm1} \tag{25}$$

$$I_{Lr5} = I_{Lm5} \tag{26}$$

$$\int_{t_0}^{t_1} I_{Lr}(t) - I_{Lm}(t) = \int_{t_3}^{t_4} I_{Lm}(t) - I_{Lr}(t) \tag{27}$$

$$P_{\text{in}} = P_{\text{out}}. \tag{28}$$

III. RESONANT TANK OPTIMIZATION METHODOLOGY

Resonant tank optimization is the key design in the proposed converter to achieve high efficiency. To ensure the ZVS turn-ON in all conditions, the turn-OFF current shall provide enough

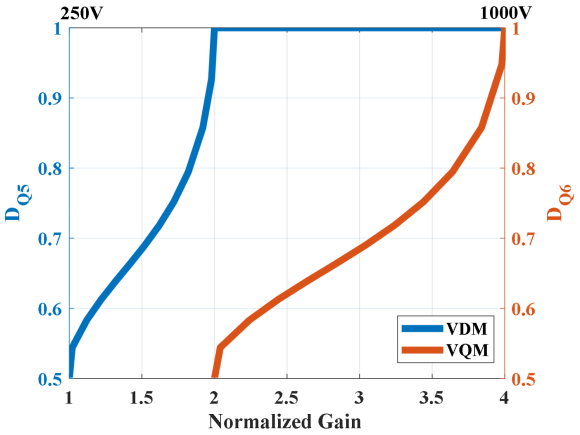

Fig. 8. Normalized gain curve of the proposed converter under 1 kW.

charge to fully discharge the output capacitance of the primary switches during the dead time. The ZVS realization mechanism during the "resonant cycle" depends on the magnetizing current, whereas the mechanism during the "PWM cycle" relies on the charge provided by the resonant inductor.

First, the transformer turns ratio can be determined according to the minimum output voltage

$$n = \frac{V_{\text{in}}}{V_{\text{out,min}}}. \tag{29}$$

The maximum magnetizing inductance is constrained by the ZVS condition in the "resonant cycle." In the proposed converter, the switching frequency f_s equals the resonant frequency f_r to minimize the circulating energy. Therefore, the voltage across the transformer equals the input voltage V_{in}

$$L_m = \frac{V_{\text{in}} t_d}{8 f_s Q_{\text{oss}}}. \tag{30}$$

The minimum resonant inductance is constrained by the ZVS condition in the "PWM cycle." Two constraints shall be satisfied as follows. 1) The charge provided by the resonant inductor shall be enough for the ZVS during dead time. 2) The resonant current direction cannot be changed before ZVS turn-ON

$$\int_0^{td} I_{Lr}(t)\, dt = \geq 2Q_{\text{oss}} \tag{31}$$

$$\begin{cases} I_{Lr}(t_3) \geq 0, & \text{in VDM} \\ I_{Lr}(t_3) \leq 0, & \text{in VQM.} \end{cases} \tag{32}$$

The resonant current charging slope in state V is determined by the voltage across the resonant inductor. The highest inductor voltage (worst condition) is when the duty approaches to 0.5 for two reasons as follows. 1) The voltage of V_{Co3} and $V_{Co4} - V_{co2}$ equal to zero as the duty is approaching 0.5. 2) The resonant capacitor voltage is around its peak value as a 90° phase shift to the resonant current

$$V_{Lr} = \begin{cases} -V_{\text{in}} - V_{Cr} + nV_{Co3}, & V_{Lr} < 0 \text{ in VDM} \\ V_{\text{in}} - V_{Cr} - n(V_{Co4} - V_{Co2}), & V_{Lr} > 0 \text{ in VQM.} \end{cases} \tag{33}$$

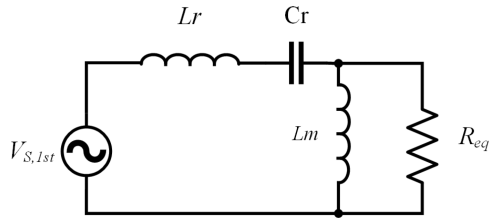

Fig. 9. FHA equivalent circuit when duty approaches 0.5.

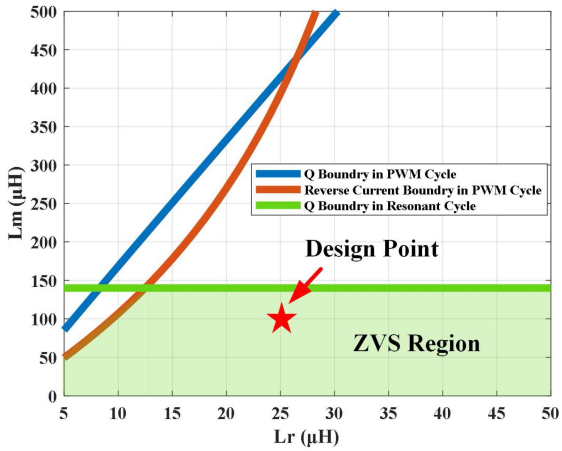

Fig. 10. ZVS constraint in terms of L_m and L_r.

The worst-case resonant capacitor peak voltage can be derived based on the first harmonic analysis (FHA), as shown in Fig. 9. It is worth mentioning that the worst-case R_{eq} are the same in both VDM and VQM under the same power level. It implies that the ZVS conditions are the same in both modes and the ZVS is guaranteed in VQM with the resonant inductor optimized in VDM when D_{Q5} is approaching 0.5

$$V_{s,1\text{st}} = \frac{2\sqrt{2}}{\pi} V_{\text{in}} \tag{34}$$

$$R_{\text{eq}} = \begin{cases} \frac{8n^2}{\pi^2} R_{\text{load,250V}}, & D_{Q5} \to 0.5 \\ \frac{2n^2}{\pi^2} R_{\text{load,500V}}, & D_{Q6} \to 0.5 \end{cases} \tag{35}$$

$$V_{Cr,pk} = \sqrt{2} \left| \frac{Z_{Cr}}{Z_{Lr} + Z_{Cr} + \frac{Z_{Lm} R_{\text{eq}}}{Z_{Lm} + R_{\text{eq}}}} \right| V_{s,1\text{st}}. \tag{36}$$

Eventually, the total charge provided during dead time in the "PWM cycle" can be calculated based on the volt–sec balance of the inductor

$$\int_0^{td} I_{Lr}(t)\, dt = \int_0^{td} \left(\frac{V_{\text{in}}}{4 f_s L_m} t - \frac{V_{\text{in}} + V_{Cr,pk}}{L_r} \right) dt. \tag{37}$$

The ZVS region constraint respective to L_m and L_r are plotted in Fig. 10 for a 300 kHz, 1 kW, 400 V input/250–1000 V output prototype. The maximum L_m is 140 μH to ensure the ZVS in the "resonant cycle" and the minimum Lr is 12.5 μH to ensure the ZVS in the "PWM cycle." Although a small Lr means smaller

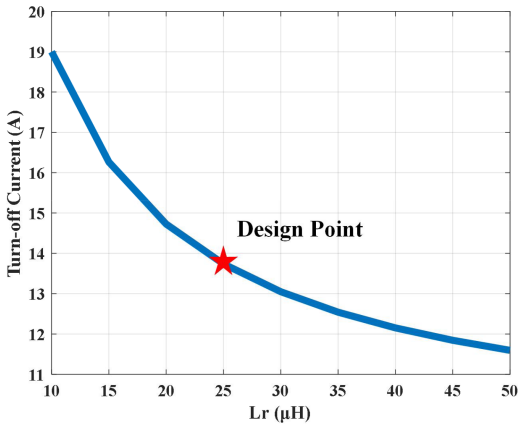

Fig. 11. L_r versus turn-OFF current plot.

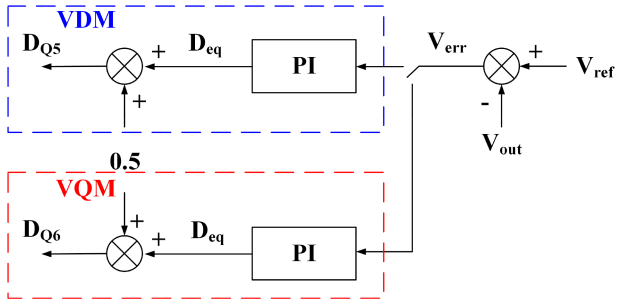

Fig. 12. Voltage loop control block diagram.

inductor size and less magnetic power loss, it also experiences a higher turn-OFF current on the auxiliary switches, as shown in Fig. 11 and the turn-OFF loss is exponential of the turn-OFF current as concluded in [41]. A 25 μH resonant inductance and a 100μH magnetizing inductance are selected to ensure enough margin for ZVS.

IV. Resonant Tank Parameter Tolerance

The unavoidable tolerance on the resonant tank parameters is the common consideration for the resonant converter. The effects are examined from two different perspectives as follows.

A. Voltage Gain

The conventional PFM LLC resonant converter voltage is volatile to the resonant tank parameters because the voltage gain is dependent on the switching frequency and the tank characteristic impedance. Especially, a small Lm/Lr value is typically designed in the conventional LLC resonant converter to achieve a steep gain curve within a narrow switching frequency range. This exacerbates susceptibility to the tolerance of the resonant tank components.

The proposed PWM LLC resonant converter operates at a fixed frequency and the voltage gain is bound between 1.0 and 4.0 by controlling the duty cycles, which are independent variables of the resonant frequency. Furthermore, as the gain range is bound, a larger Lm/Lr ratio can be selected to accommodate the tolerance of the resonant tank components, ensuring a robust gain when the switching frequency is not precisely equal to the resonant frequency.

B. ZVS Condition

The conventional LLC resonant converter ZVS is dependent on the magnetizing current. As shown in (30), f_s is a variable in the conventional LLC resonant converter. However, the proposed converter is modulated at a fixed frequency, so the magnetizing current is independent of the resonant frequency. On the other hand, a design margin is considered in the resonant tank design as presented in Fig. 10. Hence, the ZVS is guaranteed in the proposed converter while considering the tolerance on the resonant tank parameters.

Overall, the PWM resonant converter is more robust compared to the conventional PFM LLC resonant converter regarding the tolerance of the resonant tank components.

V. Digital Controller Implementation

The output voltage is regulated via the voltage across the high-side voltage multiplier capacitors (V_{co1} or V_{co3}) when the duty cycle is within [0.5, 1]. If the duty is below 0.5, the proposed converter operates as an LLC-DCX. It can be concluded that the output voltage is controlled by the effective duty (D_{eq}), as expressed in (38) in the "PWM cycle." Moreover, VDM and VQM exhibit the same operation principle, except the regulated output voltage change is twice as the voltage change of V_{Co1} as expressed in (39). The voltage control is implemented for the proposed converter as shown in the control block diagram, Fig. 12. Two identical PI controllers are implemented for each mode to achieve smooth mode transitions. When the mode transits from VDM to VQM, the PI output starts from 0 to 0.5 for D_{Q6}, while latching D_{Q5} to 1.0 in VQM. It is vice versa for the mode transition from VQM to VDM

$$D_{\text{eq}} = \begin{cases} D_{Q5} - 0.5, & \text{VDM} \\ D_{Q6} - 0.5, & \text{VQM} \end{cases} \tag{38}$$

$$V_{\text{out}} + \Delta\, V_{\text{out}} = \begin{cases} V_{co3} + \Delta V_{co3} + V_{co4}, & \text{VDM} \\ 2\left(V_{co1} + \Delta V_{co1} + V_{co2}\right), & \text{VQM}. \end{cases} \tag{39}$$

As shown in Figs. 3 and 5, the resonant current will be charged and discharged first and then clamped by the magnetizing current in the "PWM cycle." Consequently, the operation in the "PWM cycle" can be treated as discontinuous conduction mode (DCM). Similar to the conventional DCM PWM converter, the plant of the proposed converter exhibits as a single pole system as shown in Fig. 13. Hence, a simple PI controller is implemented to regulate the output voltage without the stability issue.

The controller of the proposed PWM converter is implemented on a TMS320F28377D board from Texas Instruments, as illustrated in Fig. 14. The primary switches Q_1 and Q_4 are driven by the output (Epwm1A) of the EPWM modules at f_r. The D_{Q5} is driven by Epwm2A with a short dead time relative to the rising edge of Epwm1A and D_{Q6} is driven by Epwm3A with a short dead time relative to the rising edge of Epwm1B. In

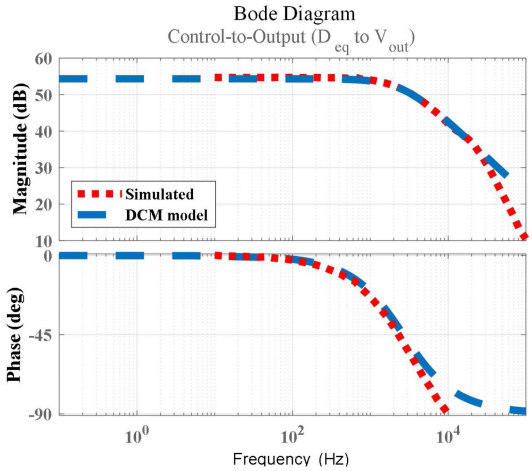

Fig. 13. Control-to-output frequency response in VDM with $D_{Q5} = 0.75$.

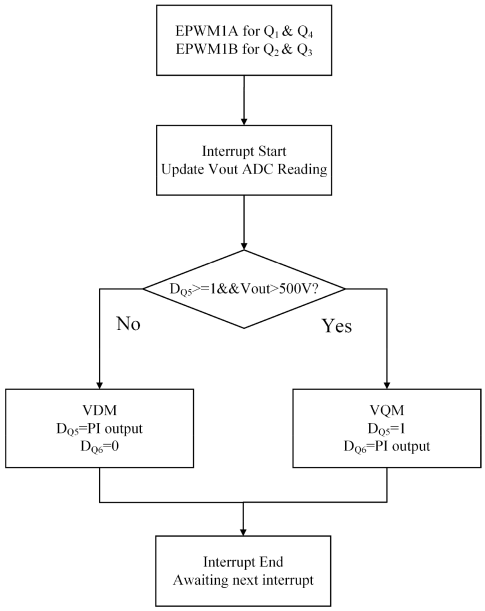

Fig. 14. Digital control algorithm of the proposed converter.

VDM, Epwm3A is forced low and only Epwm2A is modulated to control the output voltage. When the output voltage exceeds 500 V and D_{Q5} is over 1.0, the operating mode changes from VDM to VQM and Q_6 is activated. The mode transition from VQM to VDM is triggered under the opposite algorithm.

VI. Experimental Results

A 1 kW, 400 V input/250–1000V output prototype is built, as shown in Fig. 15. The key design parameters are summarized in Table II. All the experimental results are under voltage loop control. Fig. 16 are the waveforms captured in VDM under 1 kW from 250 to 500V. It is worth mentioning that Fig. 16(b) is the worst-case condition when D_{Q5} is approaching 0.5. It clearly shows that ZVS in the "resonant cycle" is achieved throughout the output voltage range in VDM. The smooth transition of the

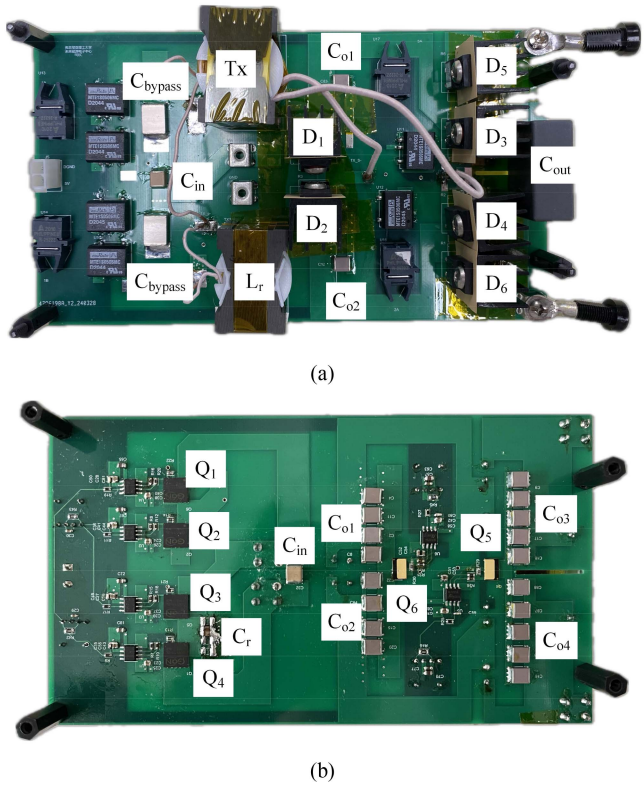

Fig. 15. 1 kW of the proposed PWM controlled LLC converter prototype. (a) Top side. (b) Bottom side.

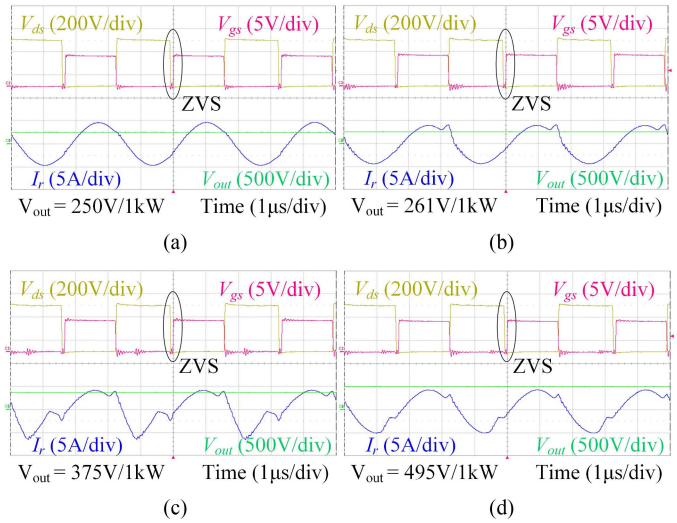

Fig. 16. Primary waveforms in VDM under 1 kW. (a) $V_{\text{out}} = 250$ V. (b) $V_{\text{out}} = 261$ V. (c) $V_{\text{out}} = 375$ V. (d) $V_{\text{out}} = 495$ V.

V_{ds} rising edge indicates that ZVS is also achieved in the "PWM cycle" in VDM.

Fig. 17 are the waveforms captured in VQM under 1 kW from 500 to 1000 V. It clearly shows that ZVS in the "PWM cycle" is achieved throughout the output voltage range in VQM. The smooth transition of the V_{ds} rising edge indicates that ZVS is also

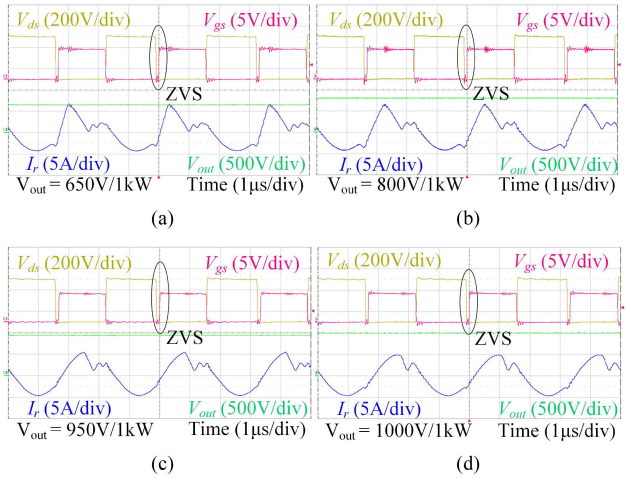

Fig. 17. Primary waveforms in VQM under 1 kW. (a) $V_{\text{out}} = 650$ V. (b) $V_{\text{out}} = 800$ V. (c) $V_{\text{out}} = 950$ V. (d) $V_{\text{out}} = 1000$ V.

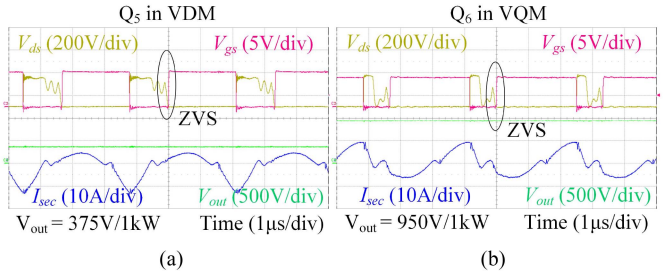

Fig. 18. PWM control switch and secondary current waveforms under 1 kW. (a) $V_{\text{out}} = 375$ V. (Q_5 in VDM). (b) $V_{\text{out}} = 950$ V. (Q_6 in VQM.)

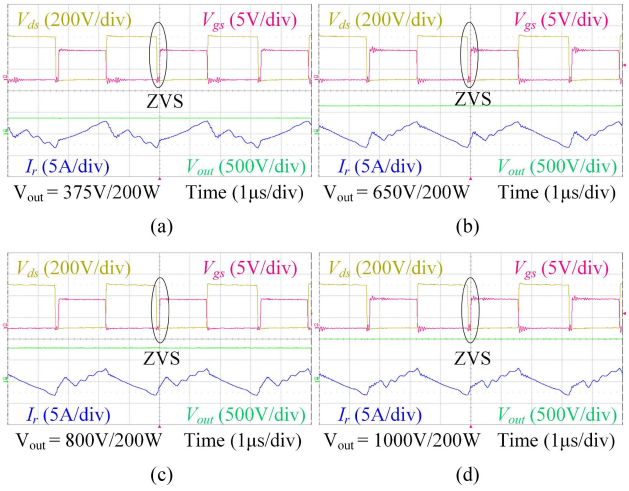

Fig. 19. Primary waveforms under 200 W. (a) $V_{\text{out}} = 375$ V. (b) $V_{\text{out}} = 650$ V. (c) $V_{\text{out}} = 800$ V. (d) $V_{\text{out}} = 1000$ V.

achieved in the "resonant cycle" in VQM. The nonsinusoidal resonant current waveform indicates PWM regulation. Ideally, the resonant current should exhibit a pure sinusoidal shape at output voltages of 250 V, 500 V, and 1000 V. However, a small notch observed on the resonant current in Fig. 17(d) suggests PWM regulation because of the tolerance on the resonant parameters.

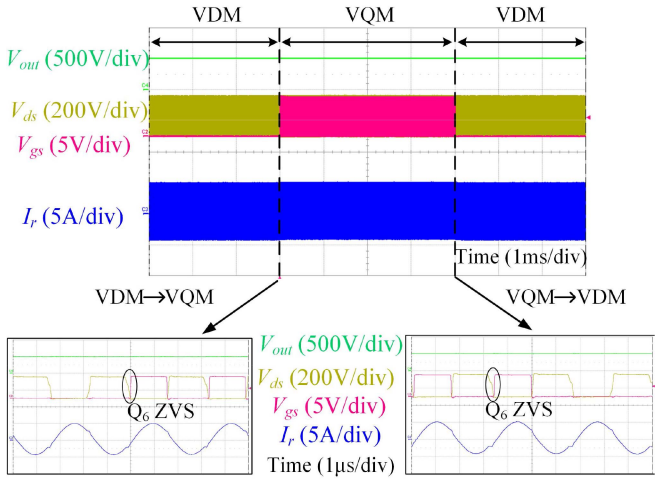

Fig. 20. Seamless mode transitions captured under 500 V/1 kW condition.

TABLE II
PARAMETERS OF THE 1 KW PROTOTYPE CONVERTER

Parameters	Values
Input voltage V_{in}	400 V
Output voltage V_{out}	250–1000 V
Rated power P	1000 W
Magnetizing inductance L_m	100 μH
Resonant inductance L_r	25 μH
Resonant capacitor C_r	2×5.6nF/630V/C0G/1206
Turn ratio of transformer n	24:15
Operating frequency f_s	300 kHz
Dead time t_d	100 ns
Transformer core	PQ32/35-3F36
Transformer winding	0.7mm airgap (0.35 mm each) Prim: 24 turns of 270/#46 Litz wire Sec: 15 turns of 660/#46 Litz wire
Inductor core	PQ32/20-3F36
Inductor winding	2mm airgap (1 mm each) 24 turns of 270/#46 Litz wire
Primary switches $Q_1 - Q_4$	GS-065-011-2-L (650 V/150 mΩ)
Secondary diodes $D_1 - D_6$	SCS215AMC (650 V/15 A)
Auxiliary switches Q_5, Q_6	GS66508T (650 V/50 mΩ)
Multiplier capacitors $C_{o1} - C_{04}$	5×0.1 μF/630 V/C0G/2220
Output capacitor C_{out}	2.7 μF/1.1 kV/film capacitor

In addition, a high-frequency ringing is observed in the "PWM cycle" which is caused by the resonance between the output capacitance of Q_6 and L_r. The waveforms of the control switches and the secondary current are captured under 1 kW as given in the Fig. 18. The waveforms clearly indicate the ZVS turn-ON of Q_5 and Q_6 in VDM and VQM, respectively. Fig. 19 are the waveforms captured with 200 W under different output voltages to verify the ZVS under light load conditions. The ZVS mechanism in light load depends on the magnetizing current, which is the same as the conventional LLC resonant converter.

The mode transitions only occur when the output voltage is at 500 V in the designed prototype. Fig. 20 shows that the mode was transited from VDM to VQM and back to VDM under 1 kW output condition. The Q_6 was inactive in VDM

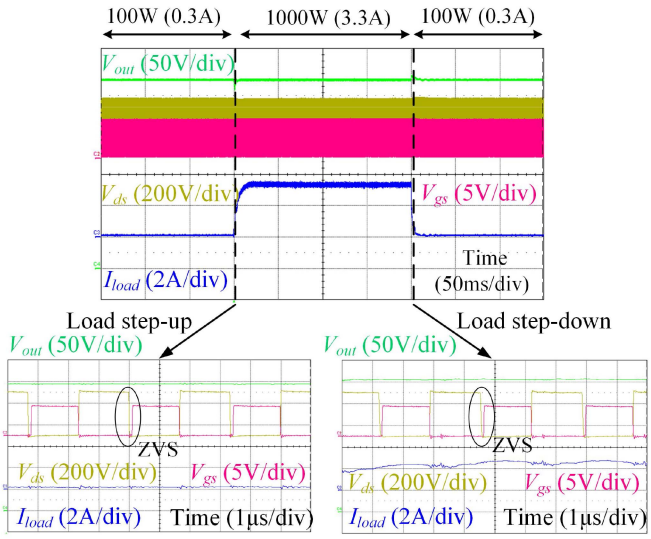

Fig. 21. Load transitions capture under 300 V output condition.

Udc1	400.106 V	P1	1.03069 kW
Udc2	1.00040 kV	P2	1.00688 kW
Idc1	2.57623 A	η1	97.690 %
Idc2	1.00638 A	P-loss	23.8130 W

Fig. 22. Peak efficiency measured by YOKOGAWA WT5000.

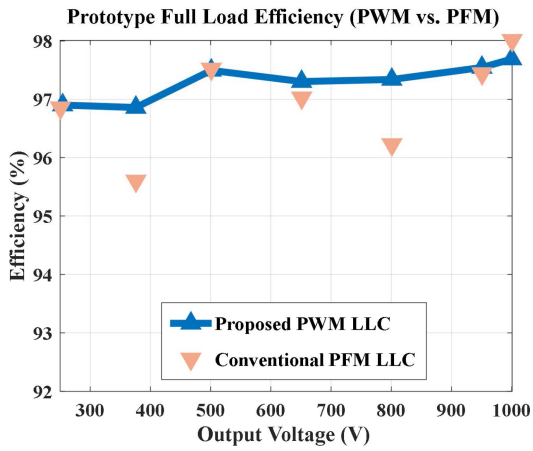

Fig. 23. Prototype full-load efficiency comparison (PWM and PFM).

and went to 50% duty in VQM. It is worth mentioning that although $V_{ds,Q6}$ is a pulsating waveform in VDM, Q_6 is not conducting current, because Q_6 is clamped to V_{co2} when D_2 (around 250 V) conducts in the positive half cycle and clamped to V_{co1} (around 0 V) when D_1 conducts in the negative half cycle. Hence, Q_6 achieves ZVS immediately during VDM to

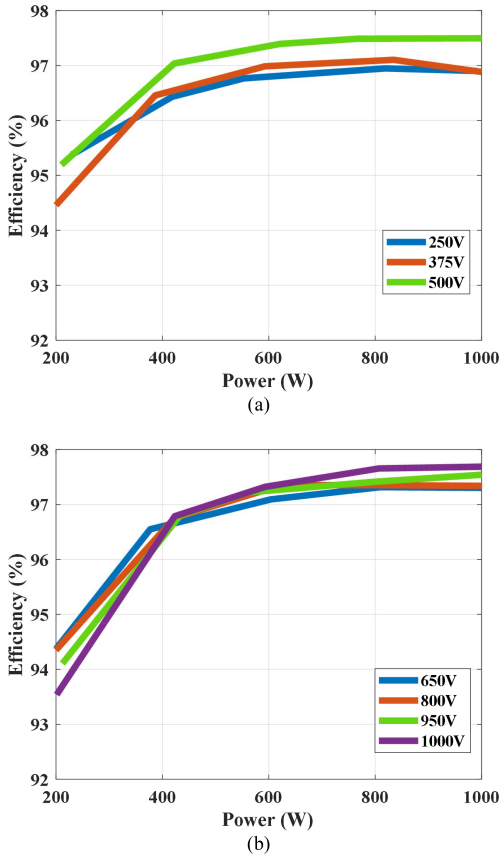

Fig. 24. Prototype measured efficiency curves. (a) VDM. (b) VQM.

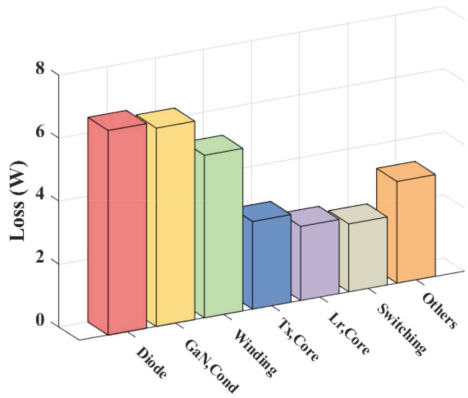

Fig. 25. Loss breakdown under 800 V/1 kW output.

VQM transition, as shown in the zoomed-in waveforms. The unchanged resonant current during the mode transition implies that ZVS is achieved on the primary side. Furthermore, both the output voltage and the resonant current are not affected during the mode transitions. Therefore, a seamless mode transition is achieved in the proposed converter.

A dynamic load-change was tested under 300 V,3 A load-step and step-down conditions. Fig. 21 depicts the voltage and current waveforms including output voltage $V_{\rm out}$, primary device drain-source voltage $V_{\rm ds}$, gate-source voltage $V_{\rm gs}$, and load current $I_{\rm load}$. Initially, the output load was 100 W. A 900 W load is applied to the full power of 1 kW and then dropped back to

TABLE III
COMPARISON WITH PREVIOUS PUBLICATIONS

Topologies	[23]	[37]	[38]	[39]	Proposed
Semiconductor devices	24	8	11	8	12
Rectifier voltage stress	Low	Low	Low	High	Low
Rectifier current stress	Low	High	Low	Low	Low
Magnetic components	3	2	2	2	2
Input voltage	750 V	220–420 V	390 V	390 V	400 V
Output voltage	200–700 V	400 V	250–420 V	250–420 V	250–1000 V
Switching frequency	31–70 kHz	100 kHz	100 kHz	100 kHz	300 kHz
Modulation	PFM	PWM	PWM	PWM	PWM
Normalized PWM gain	-	1.0–2.0	1.0–2.0	1.0–2.0	1.0–4.0
Gain range	1.0–3.5	1.0–2.0	1.0–2.0	1.0–2.0	1.0–4.0
ZVS	Yes	No	Yes	Yes	Yes
Power	3.5 kW	1 kW	1.3 kW	1 kW	1 kW
Full-load efficiency	93.8%–96.8%	89.0%–94.1%	92.5%–93.9%	94.7%–96.7%	96.9%–97.69%

100 W. Under both load transients, the output voltage $V_{\rm out}$ was well regulated, and ZVS was also well maintained as shown in the zoomed-in waveforms.

The peak efficiency is 97.69% measured under 1 kV and 1 kW conditions. Fig. 22 shows the screen capture result from the power meter YOKOGAWA WT5000. A flat full-load efficiency curve is achieved throughout the output range, as shown in Fig. 23. Moreover, a fair efficiency comparison is conducted between PWM and PFM using the same prototype. To achieve the same output voltage range under PFM, the prototype is reconfigured into three different modes, full-bridge (250 V), voltage doubler (500 V), and voltage quadrupler (1000 V). The proposed PWM converter demonstrates superior efficiency. Even though the PFM method shows a slightly better efficiency at 1 kV output, its efficiency significantly drops below 950 V output conditions. Fig. 24 demonstrates the load-efficiency curves in VDM and VQM.

The proposed converter loss breakdown has been analyzed and plotted under 800 V, 1 kW output condition. The top three losses come from diode conduction, FET conduction, and winding, as shown in Fig. 25. Although more than two diodes are conducted in the proposed converter, the total diode forward voltage drops are still maintained under a low level as they are conducted with no more than two in series during most of the time. The major switch conduction loss is on the primary side due to its larger ON-resistance $R_{\rm ds,on}$ compared to the PWM switch's (Q_5 and Q_6). Although Q_5 and Q_6 cause additional conduction loss, it is trivial compared to the diode conduction loss. The winding loss and core loss are determined by the number of turns ($B_{\rm peak}$) and the switching frequency that affects the ac resistance ($R_{\rm ac}$). The design tradeoff is necessary to minimize the total loss. A higher switching frequency can achieve higher power density, while a lower switching frequency can achieve higher efficiency. Thanks to the ZVS turn-ON of all switches, the switching loss is minimized, resulting in only turn-OFF loss.

Table III compares the key features and efficiency between the proposed converter and the other wide-range LLC converters from the existing publications. It can be seen that under strict PWM operation, the proposed converter achieves the highest full-load efficiency and widest voltage range. With the added PFM approach and SRs in secondary, the converter proposed in [40] achieves better peak efficiency, but its normalized PWM gain is limited to 2.375. The proposed approach extends the voltage gain to 4.0 strictly under PWM operation without losing ZVS and maintaining high efficiency throughout the entire output voltage range.

VII. CONCLUSION

In this article, an ultrawide range PWM controlled LLC resonant converter with voltage multiplier rectifiers is proposed. The PWM gain is significantly extended to encompass a broader output range through two operation modes, VDM and VQM. Meanwhile, the ZVS turn-ON for all switches and a seamless mode transition are achieved in the proposed converter topology. To achieve ZVS for the entire voltage and load range, a time-domain-based optimization methodology is presented. The experimental results confirm high efficiency across the output voltage range.

In addition to the verified voltage gain of 1.0–4.0, it is possible to further extend the normalized PWM gain to 0.5–4.0 by adopting the topology morphing proposed in [42] and [43] that switches the primary switching circuit between full-bridge and half-bridge.

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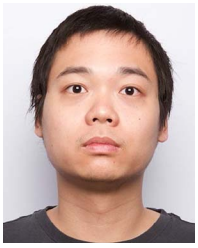

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