An Interline HVDC Power Flow Controller Based on Energy-Exchanging Arm

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***Abstract*—Meshed HVDC grid is instrumental in enhancing transmission capability and mitigating power fluctuations of renewable power generations. However, meshed dc grid cannot fully regulate the current flow through each line. To address the problem, this article presents a novel design for dc power flow controller (DCPFC) that enhances power flow control capability of meshed HVDC grid while minimizing the use of semiconductors. Benefits could be especially valuable in multiport applications. The circuit structure, operating waveforms, parameters, and control design are presented. The start process of the proposed DCPFC is also introduced. Simulation results and downscaled experimental tests are performed for demonstrating the effectiveness of the proposed topology.**

***Index Terms*—DC power flow controller (DCPFC), energy-exchanging arm, high-voltage direct-current (HVDC), meshed dc grid.**

I. Introduction

MESHED high voltage dc (HVDC) grids provide a solution for enhancing transmission capability and reducing power fluctuations of renewable power generation [1]. The world's first meshed flexible HVDC grid, the ZHANGBEI HVDC grid, has been put into operation in 2021 [2]. However, the dc power flow controllability of meshed dc grids remains a problem. The imbalanced current distribution arises in transmission lines, where some transmission lines suffer a higher current load, while others are underutilized [3], [4].

To address the problem, the implementation of dc power flow controller (DCPFC) is necessary [5]. According to the circuit configuration, DCPFCs can be classified into two types: 1) parallel and 2) series, [6], [7]. The parallel DCPFC is a high-voltage dc/dc converter, which is costly and suffers the voltage stress of the HVDC grid. Therefore, series DCPFCs have been extensively studied.

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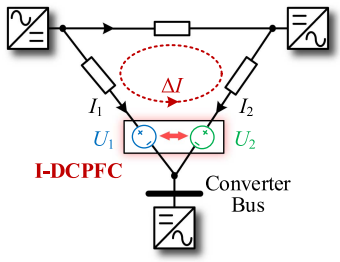

Fig. 1. Topology of DCPFC within meshed DC grid.

The series DCPFC connects within dc lines and generates dc flow control voltage. With line currents flowing through DCPFCs, therefore, the energy balance of DCPFCs is a key technical consideration. In [8] and [9], DCPFCs exchanged energy through external power sources. However, external sources are costly due to high voltage stress of HVDC grids. Other studies have proposed DCPFCs that exchange energy by integrating them within HVDC stations, as in [10] and [11]. However, this approach risks disrupting the operational and control mechanisms of HVDC voltage stations. To address energy balance of series DCPFCs, interline-DCPFCs have been proposed in [12] and [13]. As illustrated in Fig. 1, DCPFC connects with at least two dc lines of meshed dc grids, allowing current regulating and energy balance.

In [14] and [15], DCPFC topologies utilizing one capacitor were introduced. These designs involve periodically switching the capacitor within the DCPFC among different dc lines, enabling current regulating and energy balancing. However, this switching introduces voltage and current fluctuations. The authors in [16] and [17] presented a DCPFC implementation where capacitors are constant connected within the dc lines, while inductors are alternately coupled to the capacitors to facilitate energy exchange. This approach mitigates fluctuations in dc power flow control voltage and current. It is noted that both of these DCPFC designs rely on discrete semiconductors, which inherently limits their voltage capacity and potential applications within HVDC grids.

In [18], [19], and [22], DCPFCs designed for meshed HVDC grids were proposed, featuring a submodule (SM) arm topology. These topologies achieve energy balance through circulating current, which increases current stress and also requires additional costs associated with bulky ac current filters. To avoid the circulating current, [20] presented a thyristor-based hybrid

DCPFC. This hybrid DCPFC employs three interleaved arms connecting to dc lines, maintaining energy balance while reducing circulating current and eliminating the need for additional ac filters. Nevertheless, this approach has drawbacks, as the employment of thyristor groups elevates implementation costs. Furthermore, the interleaved connection of arms across all lines leads to a considerable demand of IGBTs for the entire DCPFC system.

This article presents a novel design for a DCPFC that enhances the power flow control capabilities of meshed HVDC grids while minimizing the use of semiconductors. This is achieved through the operating principle of energy-exchanging arm of the proposed DCPFC, which facilitates energy exchange between line arms across different dc lines, enabling effective energy balance. The proposed topology offers several key contributions as follows.

1) With the implementation of an energy-exchanging arm, thyristor valves are only positioned between the energy-exchanging arm and the line arms, rather than all arms, thereby reducing the number of thyristors required.
2) The proposed DCPFC connects all line arms to constant dc lines, rather than interconnecting and offer the flow control voltage of different lines, thus reducing the voltage requirement on individual line arms and decreases the number of IGBTs needed. In addition, the use of half-bridge in the line arms further results in reduction of IGBTs required.
3) The proposed DCPFC can be easily extended to multiport applications due to its operating principle of the energy-exchanging arm, serving as the power exchanging element among line arms, facilitating scalability and versatility.

In this article, we thoroughly introduce the topology of the proposed DCPFC, along with its operating principles, parameters design, control design, and start process. Comparison and multiport application are also discussed. In addition, experimental tests on a downscaled prototype are performed to further validate the effectiveness of the proposed circuit topology.

II. Topology and Operating Principle

A. Current Regulation and Energy Balance of Interline-DCPFCs

To understand the topology and operating of the proposed DCPFC, the principle of current regulating and energy balance of the interline-DCPFCs is first introduced.

As shown in Fig. 1, the line currents, I_1 and I_2, within the meshed HVDC loop can be regulated by the line voltages U_1 and U_2. The current regulating variation of I_1, ΔI, can be calculated as

$$\Delta I = \frac{U_2 - U_1}{R_{\text{loop}}} \tag{1}$$

where R_{loop} represents the loop resistance which is the sum of the resistances of all the dc lines in the meshed HVDC loop. In addition, to achieve the energy balance of DCPFC, the total power of the two voltages sources U_1 and U_2 should be

$$U_1 I_1 + U_2 I_2 = 0. \tag{2}$$

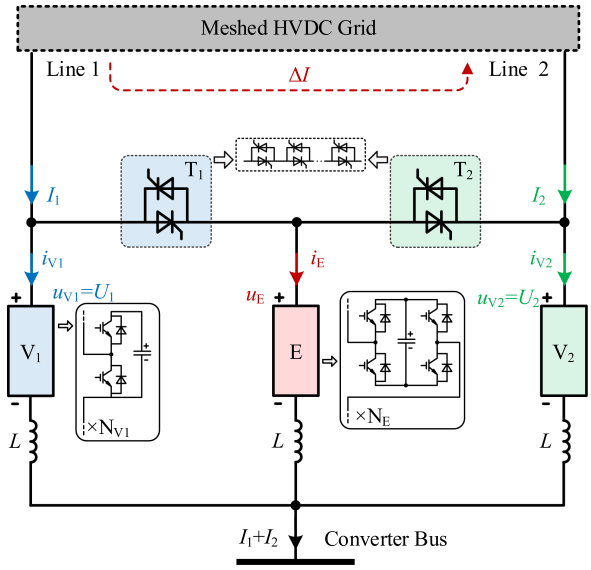

Fig. 2. Topology configuration of the proposed DCPFC.

Combining (2) with (1), the dc power flow control voltages U_1 and U_2 can be calculated

$$\begin{cases} U_1 = -\frac{I_2 \Delta I R_{\text{loop}}}{I_1 + I_2} \\ U_2 = \frac{I_1 \Delta I R_{\text{loop}}}{I_1 + I_2} \end{cases}. \tag{3}$$

Utilizing the voltage generated by DCPFC, as formulated in (3), current regulation and energy balance of the interline-DCPFCs can be achieved.

B. Topology

The topology of proposed DCPFC is illustrated in Fig. 2. It consists of one energy-exchanging arm, denoted as E, two line arms, denoted as V_1 and V_2, are series-connected in dc lines 1 and 2. The V_1 and V_2 act as two voltage sources that are responsible for regulating dc current control voltages U_1 and U_2, respectively. Energy-exchanging E interconnects with line arms through two groups of thyristors, namely T_1 and T_2. Each arm possesses an inductor, L, and all arms are linked to one converter bus.

C. Operating Principle

The operating principles of the proposed DCPFC are as follows.

1) The energy-exchanging arm E interconnects with line arms through thyristors valves. When energy-exchanging arm E connects with line arm j, it generates a voltage equal to U_j, controlling the current of arm E, denoted as i_{E}, to reach I_{E}, while the current of line arm, $i_{\text{V}j}$, becomes I_j-I_{E}. This ensures the total current remains constant at I_j, and enabling energy exchange between line arm j and the arm E without causing fluctuations in the HVDC grid's line currents. Positioning thyristors solely between the arm E and the line arms minimizes their usage and facilitates easy extension to multiport application.

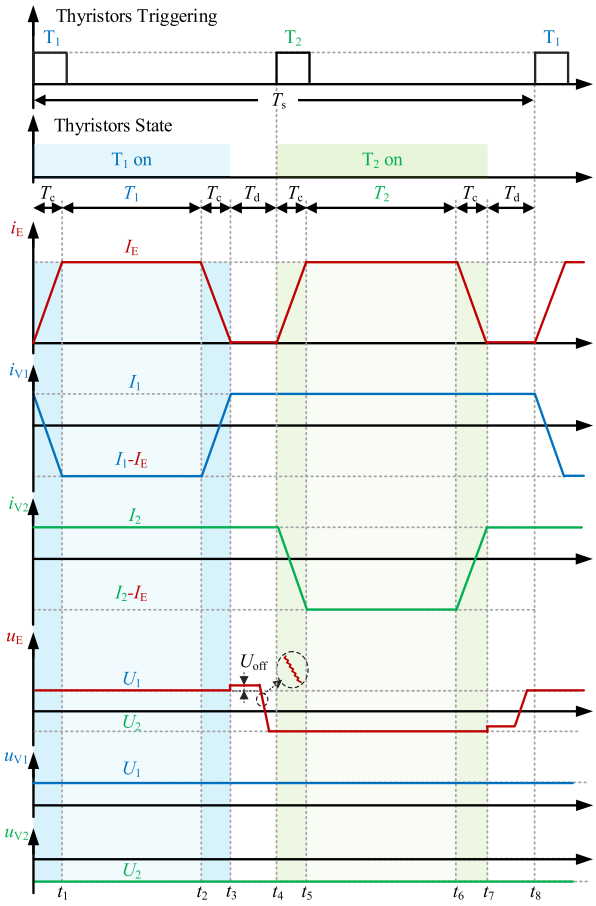

Fig. 3. Operating waveforms of the proposed DCPFC.

2) Line arms are constantly connected in the lines and generate the dc current control voltage specific to each line. This configuration ensures that line arms only provide the voltage for their respective lines, thereby reducing the voltage requirement on individual line arm and decreasing the number of IGBTs needed. Furthermore, using half-bridge topologies can further minimize the IGBT count. These advantages are particularly valuable in multiport application.

The key operating waveforms of the DCPFC are presented in Fig. 3. The voltages of all the line arms remain constant, and the voltage of arm E matches that of connected line arm. The current waveform of arm E has two distinct states, depending on which line arm it is connected to. For example, consider the state when the arm E connects with the line arm V_1.

1) Two Current Commutation Stages: During $[0, t_1]$, thyristor T_1 is first triggered and begins conducting. Current commutation occurs between arm E and line arm V_1. The current i_E is controlled to rise from 0 to I_E, while the current i_{V1} is controlled to decrease from I_1 to I_1-I_E. The current variations are controlled as a sloped wave to limit di/dt. The equivalent circuit of $[0, t_1]$ is shown in Fig. 4(a).

Similarly, during $[t_2, t_3]$, opposite current commutation occurs between the arm E and V_1. The current i_E is controlled to fall from I_E to 0, while i_{V1} is controlled to increase from I_1-I_E to I_1. The equivalent circuit is shown in Fig. 4(c).

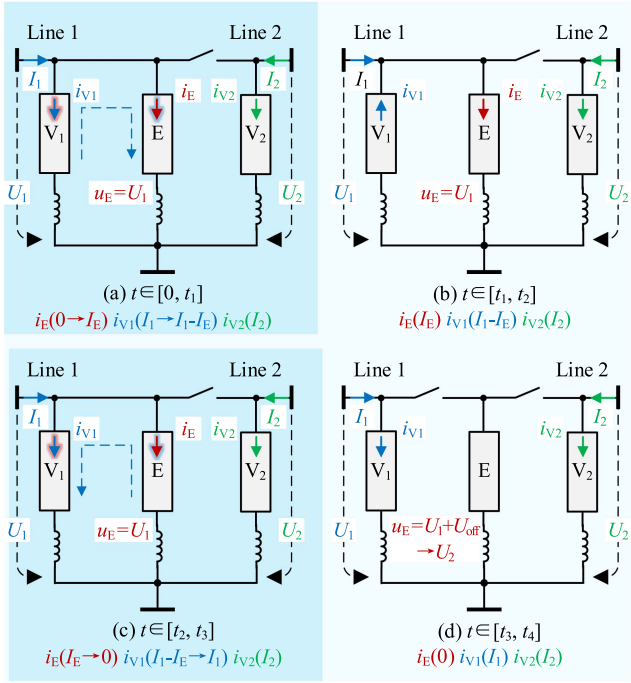

Fig. 4. Equivalent circuits of DCPFC when arm E connecting with arm V_1.

2) Steady Current Stage: During $[t_1, t_2]$, between two current commutation stages, there is a steady current stage (T_1) for energy exchanging. Within this time, the negative current flows through the line arm V_1 to maintain energy balance. The equivalent diagram of $[t_1, t_2]$ is shown in Fig. 4(b).

3) Delay Stage: During $[t_3, t_4]$, to ensure the reliable turn-off of thyristor T_1, arm E generates voltage equal to U_1+U_{off} for a time span. Then the voltage of arm E, u_E, is controlled as a sloped wave from U_1+U_{off} to U_2 for zero voltage switching of thyristor T_2. The equivalent diagram of $[t_3, t_4]$ is shown in Fig. 4(d).

The operating waveforms of the arm V_2 are similar to V_1, and the working stages are shown in Fig. 5. When arm E connects with arm V_2, energy is transferred from the arm V_2 to the arm E. Consequently, during the entire working cycle, energy is transferred from arm V_2 to arm V_1 through the arm E. Energy balance of line arms V_1 and V_2 is achieved based on the energy-exchanging arm E.

D. Operating Waveforms Designing

Based on the operating principle and the Fig. 3, the entire working cycle of the proposed DCPFC, denoted as T_s, can be expressed as

$$T_s = (T_1 + 2T_c + T_d) + (T_2 + 2T_c + T_d) \tag{4}$$

where T_j (j∈1, 2) is the time span of steady stage, T_c is the time span of current commutation stage, and T_d is the time span of delay stage. T_c and T_d are designed to ensure the reliability of thyristors

1) T_c is set to 200 μs to limit the di/dt of the current commutation stage and ensure thyristor safety. In this way, the

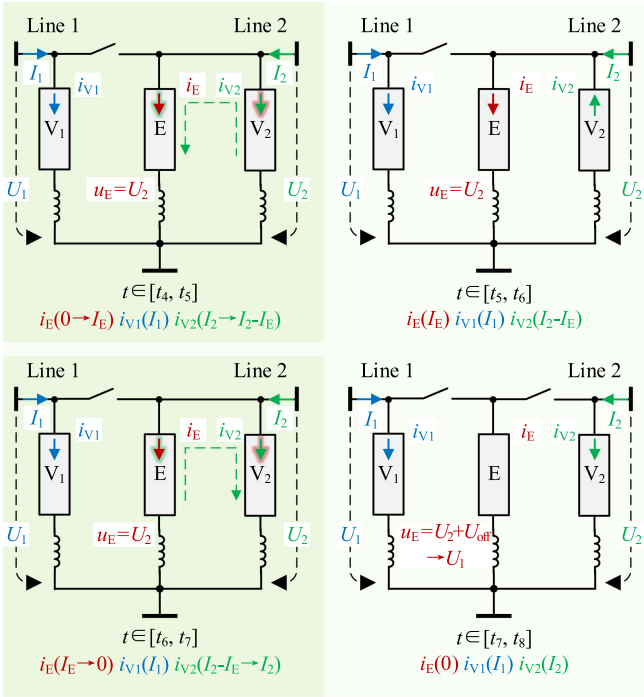

Fig. 5. Equivalent circuits of DCPFC when arm E connecting with arm V_2.

current falling rate of thyristor is restricted to a value less than 20 A/μs, which is the critical current falling rate.

2) T_d is governed by the turn-OFF time and the critical change rate of voltage across the thyristors. The thyristors valve assembly comprises multiple thyristors in series, this configuration results in a significant voltage change rate, with the turn-OFF time (t_q) being the primary factor. Currently, the turn-OFF time of high-speed thyristors ranges from 60 to 90 μs. Therefore, T_d is set to 200 μs to safely turn OFF thyristor.
3) T_s is set at 100 Hz (10 000 μs) in this manuscript. As T_s increases, the proportion of delay stages within a single working cycle decreases, thereby augmenting the utilization efficiency of the energy-exchanging arm. However, this prolongation also leads into heightened demands on the energy storage of capacitors within the DCPFC, ultimately requiring larger capacitors. Balancing these two aspects, T_s is set to 100 Hz, resulting in a mere 4% of the working cycle allocated to delay stages.
4) T_j should be designed in accordance with the principles of energy balance. In one entire working cycle, the energy of three arms shall be equal to zero and can be expressed as

$$E_E = \int_0^{T_s} u_E i_E dt = (|U_1(T_1+T_c)| - |U_2(T_2+T_c)|)$$
$$I_E = 0 \tag{5}$$

$$E_{V1} = \int_0^{T_s} u_{V1} i_{V1} dt = |U_1 I_1 T_s| - |U_1 I_E (T_1+T_c)|$$
$$= 0 \tag{6}$$

$$E_{V2} = \int_0^{T_s} u_{V2} i_{V2} dt = |U_2 I_2 T_s| - |U_2 I_E (T_2+T_c)|$$
$$= 0 \tag{7}$$

where E_j (j = E, V_1, V_2) is the energy of arm j in one working cycle. Combining (4) and (5), the T_j can be expressed as

$$T_1 = \frac{|U_2|}{|U_1|+|U_2|}(T_s - 2T_c - 2T_d) - T_c \tag{8}$$

$$T_2 = \frac{|U_1|}{|U_1|+|U_2|}(T_s - 2T_c - 2T_d) - T_c. \tag{9}$$

5) I_E, the current amplitude of the arm E should also be designed in accordance with the principles of energy balance. Combining (4), (6), and (7), I_E can be expressed as follows:

$$I_E = \frac{|I_1|+|I_2|}{T_s - 2T_c - 2T_d} T_s \tag{10}$$

III. Parameter Design

A. Submodules and IGBTs

With the operating principle of the proposed DCPFC, it is necessary for the arms V_1 and V_2 to provide the dc power flow control voltage U_1 and U_2, respectively. As a result, the numbers of SMs required in arms V_1 and V_2 can be calculated

$$N_{V1} \geq \frac{|U_1|}{(1-\varepsilon/2)U_C} N_{V2} \geq \frac{|U_2|}{(1-\varepsilon/2)U_C} \tag{11}$$

where N_{V1} and N_{V2} are the numbers of SMs in arm V_1 and V_2. U_C is the rated capacitor voltage of SMs, and ε is the peak-to-peak capacitor voltage ripple. In terms of arm E, it is expected to output not only the voltage as arms V_1 and V_2, but also a turn-OFF voltage for thyristor U_{off}

$$N_E \geq \frac{\max[|U_1|, |U_2|] + U_{off}}{(1-\varepsilon/2)U_C} \tag{12}$$

where N_E is the number of SMs in arm E.

The number of IGBTs of the proposed DCPFC can be calculated

$$N_{IGBTs} = 2(N_{V1} + N_{V2}) + 4N_E. \tag{13}$$

B. Thyristors

The thyristors are responsible for achieving alternate connections of arm E in the proposed DCPFC, which results in voltage stress between the two dc power flow control voltages, U_1 and U_2. Therefore, the number of series-connected thyristors, N_T, should be chosen as

$$N_T \geq \frac{|U_1 - U_2|}{\lambda_d U_T} \tag{14}$$

where U_T is the rated blocking voltage of thyristors, and λ_d is the derating factor [21].

C. Capacitance

The capacitor in SMs should buffer the energy fluctuations of arms. In one whole cycle, the absorbed energy should be equal to the released energy of one arm. Therefore, energy variations of each arm are (5)–(10). Supposing that the capacitor voltages in each arm are balanced, energy variation is evenly distributed among the N SMs, i.e.,

$$C_{\mathrm{E}} = \frac{U_1 U_2}{\varepsilon N_{\mathrm{E}} U_{\mathrm{C}}^2}\left(\frac{|I_1|+|I_2|}{|U_1|+|U_2|}T_{\mathrm{s}}\right) = \frac{U_1 U_2}{\varepsilon f N_{\mathrm{E}} U_{\mathrm{C}}^2}\left(\frac{|I_1|+|I_2|}{|U_1|+|U_2|}\right) \tag{15}$$

$$C_{\mathrm{V1}} = \frac{U_1 I_1}{\varepsilon N_{\mathrm{V1}} U_{\mathrm{C}}^2}\left(1-\frac{T_{\mathrm{c}}}{T_{\mathrm{s}}}\right)\left(T_{\mathrm{s}} - \frac{|U_2|}{|U_1|+|U_2|}(T_{\mathrm{s}}-2T_{\mathrm{c}}-2T_{\mathrm{d}})\right) = \frac{U_1 I_1}{\varepsilon N_{\mathrm{V1}} U_{\mathrm{C}}^2}\left(1-\frac{T_{\mathrm{c}}}{T_{\mathrm{s}}}\right)\left(T_{\mathrm{s}} - \frac{|I_1|}{|I_1|+|I_2|}(T_{\mathrm{s}}-2T_{\mathrm{c}}-2T_{\mathrm{d}})\right) \tag{16}$$

$$C_{\mathrm{V2}} = \frac{U_2 I_2}{\varepsilon N_{\mathrm{V2}} U_{\mathrm{C}}^2}\left(1-\frac{T_{\mathrm{c}}}{T_{\mathrm{s}}}\right)\left(T_{\mathrm{s}} - \frac{|U_1|}{|U_1|+|U_2|}(T_{\mathrm{s}}-2T_{\mathrm{c}}-2T_{\mathrm{d}})\right) = \frac{U_2 I_2}{\varepsilon N_{\mathrm{V2}} U_{\mathrm{C}}^2}\left(1-\frac{T_{\mathrm{c}}}{T_{\mathrm{s}}}\right)\left(T_{\mathrm{s}} - \frac{|I_2|}{|I_1|+|I_2|}(T_{\mathrm{s}}-2T_{\mathrm{c}}-2T_{\mathrm{d}})\right). \tag{17}$$

The energy variation is intricately related to the working point of DCPFC, necessitating the consideration of maximum energy variation during the capacitors design.

IV. Start Process of DCPFC

The start process of the interline DCPFC is pivotal to its operation, with the DCPFC start process primarily involving the charging of SM capacitors. The start process of the energy-exchanging arm E is introduced in detail, and followed by commutation stages identical to the operating principle of the proposed DCPFC, the start and charging process of other line arms can be achieved.

The start process of the energy-exchanging arm E is shown in Fig. 6, where the circuit of the arm E is shown in Fig. 6(a). The energy-exchanging arm E is isolated from the HVDC line through the switch $\mathrm{SW_E}$, with all the SM capacitor voltage at zero, and the current of line 1 flowing through the line switch $\mathrm{SW_1}$. During the start process, the thyristor valve group $\mathrm{T_1}$ is always triggered.

1) *Precharging:* First, one SM undergoes precharging with a dc source. The charging dc source does not have to suffer the high voltage stress of the HVDC grid, because of the isolation by the switch $\mathrm{SW_E}$. Moreover, since the voltage of one SM capacitor is much lower compared to the voltage of the HVDC grid, it is possible to charge one SM without the need for a high-voltage dc source, thereby reducing the demand on the charging power supply.
2) *Current commutation:* After isolated precharging, the switch $\mathrm{SW_E}$ is closed, the charged capacitor is put into the dc line in the reverse direction, while the other SMs are bypassed. Driven by the negative voltage, the line current is commutated from the $\mathrm{SW_1}$ to the energy-exchanging arm E. When the commutation is complete and the current through the $\mathrm{SW_1}$ drops to zero, the switch $\mathrm{SW_1}$ can be safely opened, allowing the line current flowing through the arm E.
3) *Charging:* Enabling the capacitor voltage control and modulation, the charging of SMs in the arm E is facilitated by the line current. Once all submodules reach the rated value U_{C} the start process is complete.

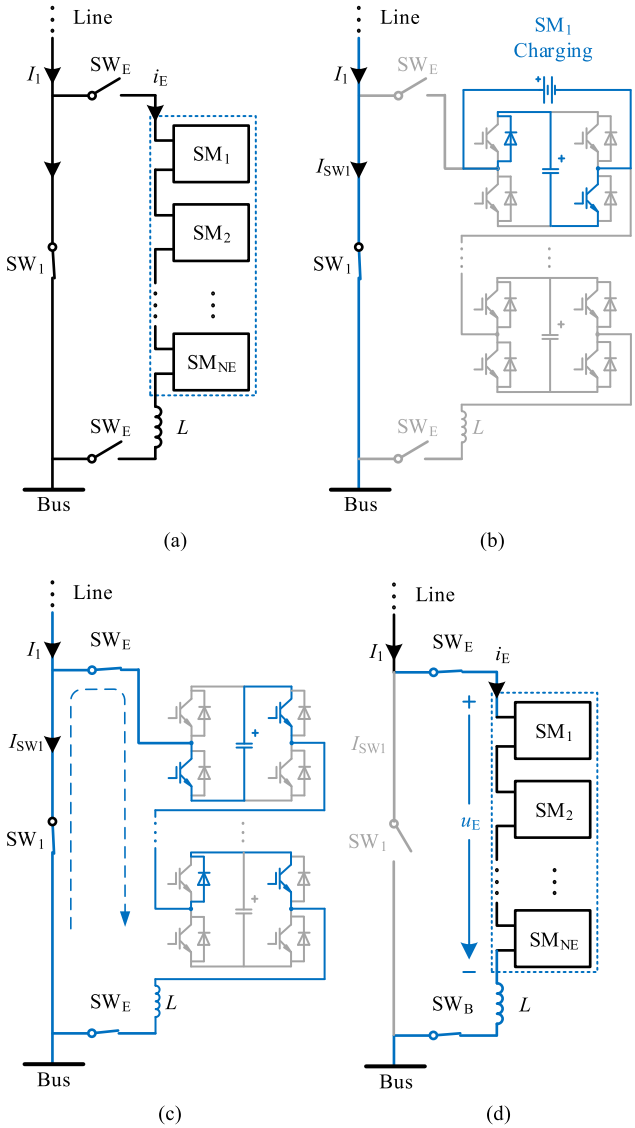

Fig. 6. Start processes of arm E. (a) Topology. (b) Pre-charge. (c) Curent commutating. (d) Charging.

The key design of start process is the current commutating. During commutating, the charged capacitor releases energy, and the capacitor voltage gradually decreases. Simultaneously, the current flowing through the inductor L increases. Consequently, there is an energy transfer between the capacitor and inductor. It can be expressed as

$$\Delta E_{\mathrm{cap}} = \frac{1}{2}C\left(U_{\mathrm{charged}}^2 - U_{\mathrm{end}}^2\right) = \Delta E_{\mathrm{L}} = \frac{1}{2}LI_1^2 \tag{18}$$

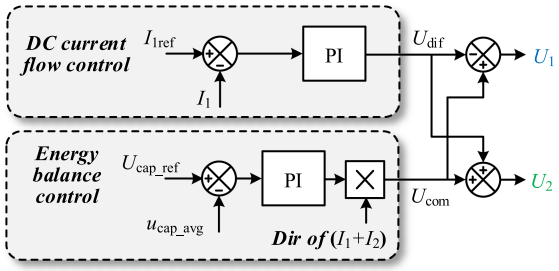

Fig. 7. Upper-level control scheme of DCPFC.

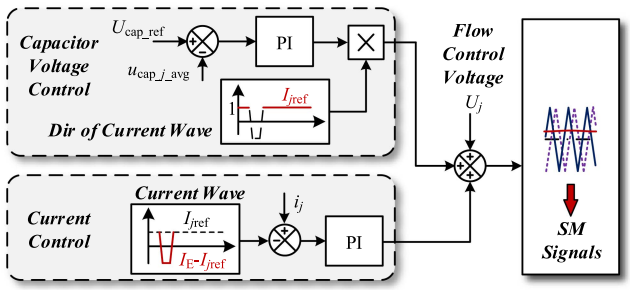

Fig. 8. Line arm control scheme of DCPFC.

where ΔE_{cap} is the energy variation of the charged capacitor, ΔE_{L} is the energy variation of the inductor, and U_{charged} and U_{end} are the precharged voltage and the capacitor voltage at the end of commutating. To reliably start and commutate, U_{end} should be bigger than zero. Therefore, the precharged voltage U_{charged} should be

$$U_{\text{charged}} \geq \sqrt{\frac{L}{C}} I_1. \tag{19}$$

V. Control Strategy

A. Upper-Level Control

Utilizing the line voltages generated by the line arms, current regulation and energy balance of the proposed DCPFC can be achieved. The line voltages are determined by (3), but two control aspects are coupled with two voltages. Moreover, it needs the information of impedance and current variation of HVDC grid. Therefore, in the upper-level control, a dual-mode voltage control approach is employed for regulating dc power flow and ensuring energy balance of the entire DCPFC, without relying on the impedance and current variation. This is achieved by adjusting both the differential and common voltages of DCPFC.

To realize the decoupling of two control aspects, the differential and common voltages of DCPFC are

$$\begin{cases} U_{\text{dif}} = \frac{U_2 - U_1}{2} \\ U_{\text{com}} = \frac{U_1 + U_2}{2} \end{cases} \tag{20}$$

where U_{dif} and U_{com} are the differential and common voltages of DCPFC, respectively. U_1 and U_2 can be calculated

$$\begin{cases} U_1 = U_{\text{com}} - U_{\text{dif}} \\ U_2 = U_{\text{com}} + U_{\text{dif}} \end{cases}. \tag{21}$$

DC current flow can be only regulated by the differential voltage

$$\Delta I = \frac{2U_{\text{dif}}}{R_{\text{loop}}}. \tag{22}$$

The energy balance can also be achieved by adjusting the common voltage

$$U_{\text{com}} (I_1 + I_2) + U_{\text{dif}} (I_2 - I_1) = 0. \tag{23}$$

Fig. 7 gives the upper-level control scheme for the DCPFC, which is based on the concept of dual-mode voltage control. In the control scheme, the differential voltage is derived from a feedback loop that controls the current I_1, with $I_{1\text{ref}}$ serving as the reference for the desired current flow. By adjusting the differential voltage in response to deviations from the reference current, the DCPFC is able to regulate the dc power flow. On the other control loop, the energy balance of the entire DCPFC is maintained through a separate feedback loop that controls the average capacitor voltage of DCPFC, $u_{\text{cap\_avg}}$. This common voltage control loop ensures that the total energy of the DCPFC remains constant. By separating the control of differential voltage and common voltage, the upper-level control strategy enables the DCPFC to independently optimize both the dc power flow and energy balance, without relying on the impedance and current variation of HVDC grid. Notably, the outputs generated by the upper-level control serve as the inputs for the arm control.

B. Arm Control

In the arm control, the arm current control and the arm capacitor voltage control are activated in different operating stages. Consequently, the different aspects of arm control can also be decoupled temporally.

The line arm control of DCPFC is given in Fig. 8. This incorporates three distinct control aspects: flow control, current control, and capacitor voltage control. The flow control voltages, denoted as U_j $(j = 1, 2)$, are derived from the upper-level control. The arm current and arm capacitor voltage controls are activated during different operating stages, where $u_{\text{cap\_}j\text{\_avg}}$ is the average capacitor voltage of line arm V$_j$, $I_{j\text{ref}}$ is the current reference of dc lines.

Specifically, the arm current control is only activated during the current commutation stages for driving the arm current. Conversely, the arm capacitor voltage control is activated all the working cycle except the current commutation stages. This approach allows for the decoupling and concordance of the various aspects associated with arm control. As for the capacitor voltage control, it is important to consider the directions of current for charging or discharging capacitors. To achieve this, the output of the capacitor voltage controller shall be multiplied by a sign formula based on the arm current.

Regarding the energy-exchanging arm in the proposed DCPFC, the flow control, arm current control, and arm capacitor voltage control are similar to those of the line arms. However,

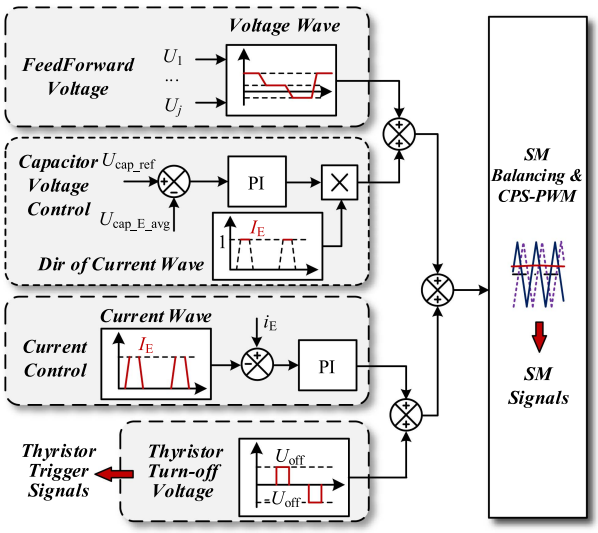

Fig. 9. Energy-exchanging arm control scheme of DCPFC.

TABLE I
SIMULATION PARAMETERS

Parameters	Values
SMs of strings	$N_E = 12$, $N_{V1} = N_{V2} = 10$
Capacitor voltage (U_C)	2500 V
SM capacitance ($C_E/C_{V1}/C_{V2}$)	11.9/7.5/7.5 mF
String inductance (L)	0.05 mH
Operation frequency ($1/T_s$)	100 Hz
CPS carrier frequency	1000 Hz
Current changing time (T_c)	200 μs
Transition time (T_d)	200 μs

it is important to note that the energy-exchanging arm also incorporates an additional thyristor control. This thyristor control is responsible for generating the trigger signals and turn-OFF voltage necessary for the proper triggering signals and turning-OFF of the thyristor valves. This ensures the reliable operation of the thyristors within the energy-exchanging arm. The control scheme of the energy-exchanging arm is illustrated in Fig. 9.

The voltage commands of all control parts are summed to get the final voltage reference for the arms. In order to realize SMs balance, the magnitude of carrier waves is adjusted based on the difference in average voltage of each SM. Then, the gating signals of SMs are processed by phase-shifted carrier pulse-width modulation (CPS-PWM).

VI. Simulation Verification and Discussion

To demonstrate the effectiveness of the proposed DCPFC, the simulation configuration of 500 kV ZHANGBEI four-terminal meshed HVDC grids is built and shown in Fig. 10. The parameters of four VSC stations and transmission lines are shown in Fig. 10. The resistance and inductance of per kilometer dc lines are 0.04 Ω and 1.02 mH. The natural dc current flow distribution of the grid is given in the Fig. 10. Without dc power flow control, the natural line currents I_1 and I_2 are 2515 A and 485 A, respectively. The proposed DCPFC is installed at the VSC1 within the line 21 and line 41. The parameters of DCPFC are listed in Table I.

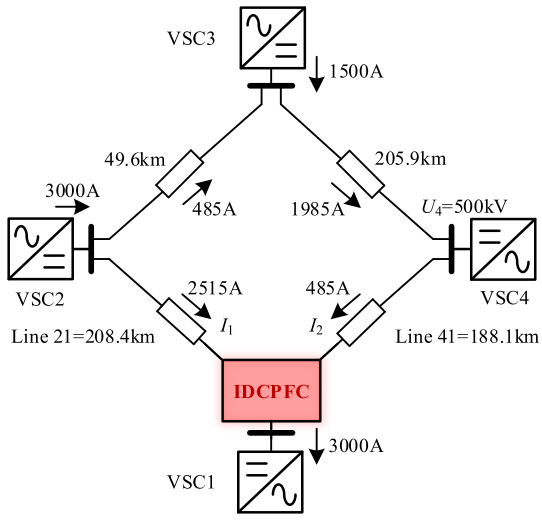

Fig. 10. Four-terminal meshed HVDC grids with proposed DCPFC.

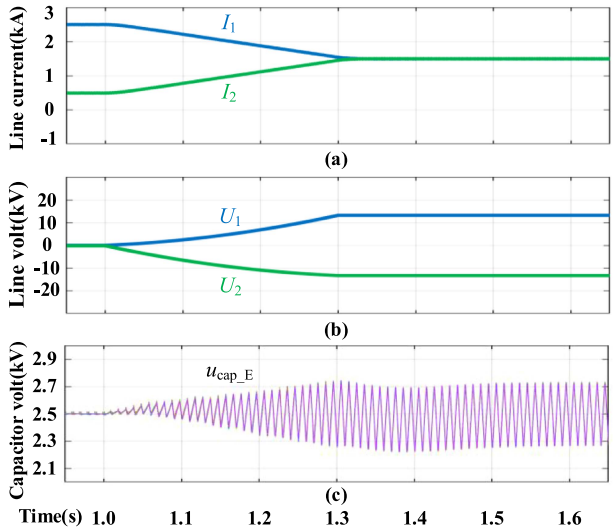

Fig. 11. Simulation results of dynamic dc power flow control. (a) The currents of line 1 and 2; (b) the DC power flow control voltages; and (c) the capacitors voltages of energy-exchanging arm.

A. Simulation Verification

Fig. 11 shows the results of the dynamic dc power flow control process. The line current I_1 is set as the control target of DCPFC. When the power flow control is active at 1s, I_1 is controlled to 1500 A gradually, and then remains at 1500 A. Correspondingly, I_2 is regulated to 1500 A (the total current of VSC1 is constant 3000 A). The dc power flow control voltages U_1 and U_2 are varying from 0 to 13.2 kV and to –13.2 kV, respectively. The total energy of DCPFC is balanced. Taking the capacitors voltages of energy-exchanging arm E as the example, the voltages are kept in well balanced around the rated value at 2.5 kV.

Fig. 12 specifically shows the zoomed waveforms of the proposed DCPFC during [1.58 s, 1.60 s]. The line currents I_1 and I_2 are stable and remain at 1500 A. The currents of line arms and energy-exchanging arm are trapezoids but composing the constant line currents, I_1 and I_2. The energy-exchanging arm

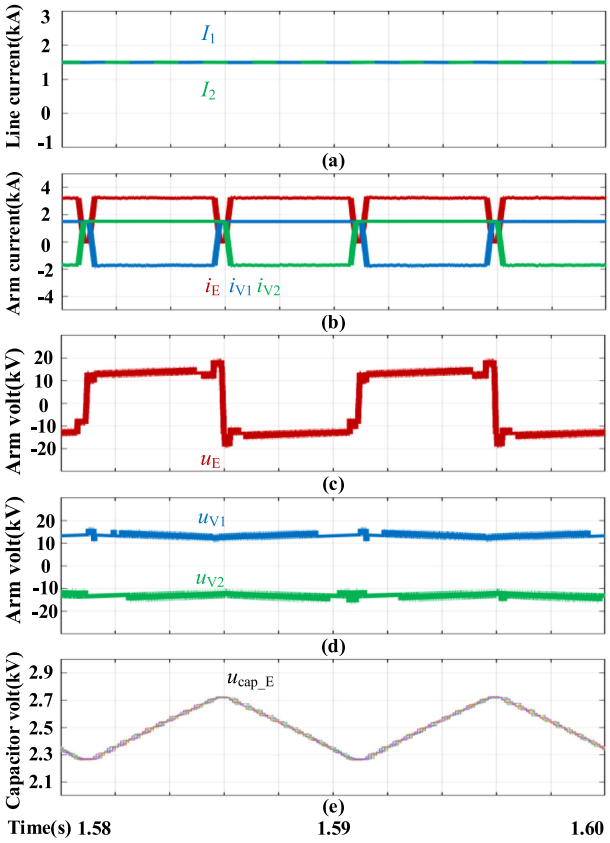

Fig. 12. Simulation results of proposed DCPFC [1.58 s, 1.60 s]. (a) The currents of line 1 and 2; (b) the currents of arm V_1, V_2 and E; (c) the voltage of energy-exchanging arm; (d) the voltages of line arms; and (e) the capacitors voltages of energy-exchanging arm.

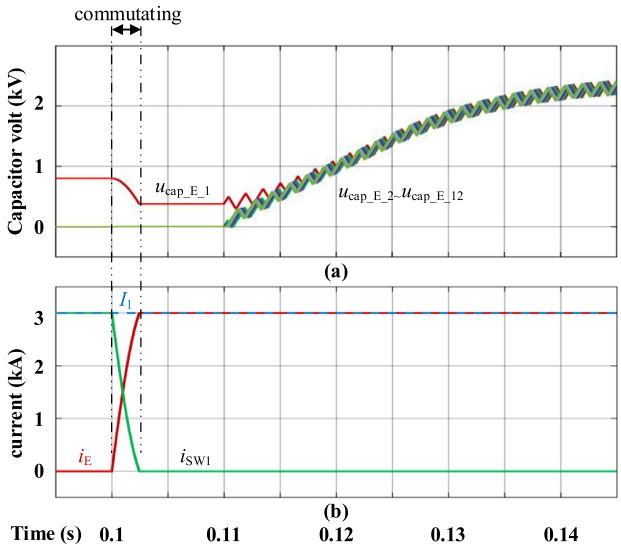

Fig. 13. Simulation results of the start process of DCPFC. (a) Voltages of capacitors in energy-exchanging arm; (b) the line current, the current of arm, and the current of line switch.

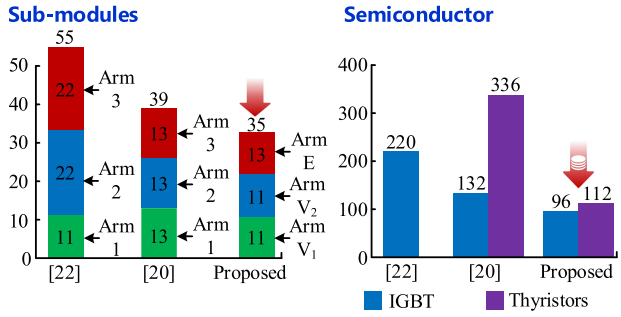

Fig. 14. Comparison results of submodules and semiconductors.

interleaving connects with line arms. There are slopes in the current waveforms to limit d*i*/d*t* during current commutation. The voltage of energy-exchanging arm is also a trapezoidal waveform. When the energy-exchanging arm parallel connects with line arm V_1, the energy-exchanging arm generates 13.2 kV and absorbs energy from the arm V_1. Conversely, when parallel connecting with line arm V_2, the energy-exchanging arm generates –13.2 kV and release energy to the arm V_2. The energy-exchanging arm generates the turn-OFF voltage at the end of current commutations stages for reliable closing thyristor valves. The voltages of line arms V_1 and V_2 are constant at 13.2 kV and –13.2 kV, respectively. With the interleaving connects, the energy of all arms is balanced. The capacitors voltages of energy-exchanging arm are rising when absorbing energy from arm V_1 and falling when releasing energy to arm V_2. During the whole working cycle, it is balanced and around at the rated voltage.

Fig. 13 shows the proposed start process of DCPFC. One SM is first isolated precharging to 800 V. Then, the precharged SM is put into the dc line in the reverse direction, and the current commutates from the line switch SW_1 to the arm. During current commutating, the voltage of precharged SM falls, and there is an energy transfer between the SM capacitor and arm inductor. After commutating, the current of SW_1 decreases to 0, the line switch can be safely opened, and the line current flows through the arm. With enabling the capacitor voltage control, all SMs absorbs energy from the line current and gradually reach the rated value U_C.

B. Comparison

To demonstrate the advantages and characteristics of the proposed DCPFC, it is compared with other IDCPFC topology, [20] and [22]. For a fair comparison, all topologies have same operation frequency, all the SMs in these topologies have the same voltage rating, and the design margin is not considered for all the parameters. The specific simulation study under the four-terminals meshed HVDC grids is selected as an example with calculated numbers, where the maximum power flow control voltage generated by the DCPFC is 25 kV (5% the rated voltage of meshed HVDC grids), the rated voltage of each SM is 2.5 kV, the operation frequency is 100 Hz, the capacitor voltage coefficient is $\varepsilon = 10\%$, the turn-OFF voltage of thyristors is 5 kV, and the derating factor of thyristors is 0.6.

Fig. 14 shows the comparison results of SMs and semiconductors counts. The proposed DCPFC reduces number of SMs and semiconductors over the most recent topologies [20] and [22]. In each arm of the three DCPFC topologies, the fundamental count

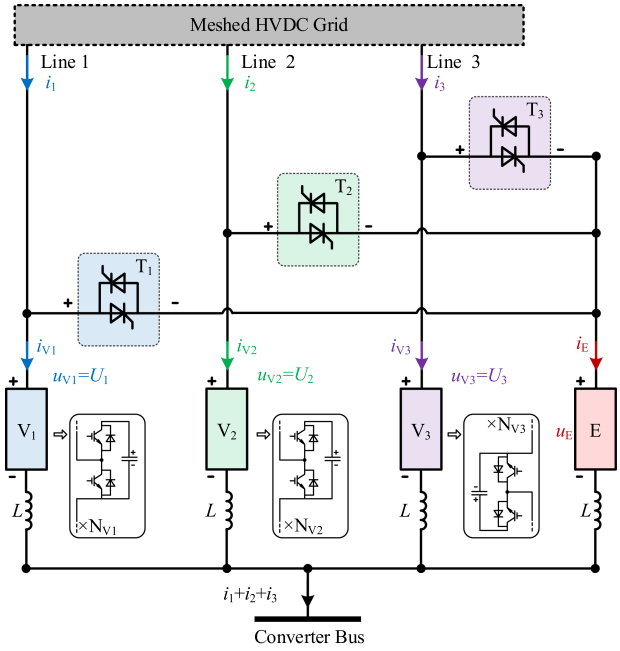

Fig. 15. Circuit configuration of the proposed DCPFC with three DC lines.

of SMs is consistent at 11. For topology [22], the inner-ac voltage for energy balance results in a doubling of the SM count in arms 2 and 3. The proposed DCPFC and [20] achieve a significant reduction in SM count by mitigating the ac voltage. Moreover, in the proposed DCPFC, the turn-OFF voltage for thyristors is generated solely by the energy-exchanging arm, which further minimizes the number of SMs required.

The proposed DCPFC achieves energy balance across the entire DCPFC by utilizing an energy-exchanging arm. The energy-exchanging arm is interconnected with different line arms and exchanges energy with them, eliminating the need for ac current and ac current loops. This results in fewer SMs and IGBTs. Moreover, the proposed DCPFC employs a constant series connection of line arms in the dc lines. Consequently, thyristor valves are only required between line arm and the energy-exchanging arm, resulting in fewer thyristors. The half-bridge SMs can be also used in the line arms of the proposed DCPFC, further reducing the number of IGBTs.

C. Multi-DC Lines Configuration

The proposed DCPFC possesses a versatile topology and operating principle suitable for complex network structure. Fig. 15 gives the circuit configuration of the proposed DCPFC with three dc lines. It comprises three line arms ($V_j, j = 1, 2, 3$) connected in series to dc-lines 1, 2, and 3, one energy-exchanging arm E, and three groups of thyristor valves connected between line arms V_j and energy-exchanging arm E.

Notably, as the number of lines increases, the working cycle and capacitance of multiline DCPFC rise. The proposed DCPFC still offers simplicity, lower costs, and fewer SMs, requiring only one additional thyristor valve set and one half-bridge line arm per extra dc-line. In contrast, the DCPFC in [20] for three dc-lines employs four full-bridge SM arms and 12 (4×(4-1)) thyristor valves. The proposed DCPFC connects all line arms to constant dc lines, rather than interconnecting and offer the flow control voltage of different lines, thus reducing the voltage requirement on individual line arms and decreasing the number of IGBTs needed. Moreover, for applications with n dc-lines, the control block diagrams for all line arms remain consistent with Fig. 8, simplifying the extension of the topology to more complex network structures.

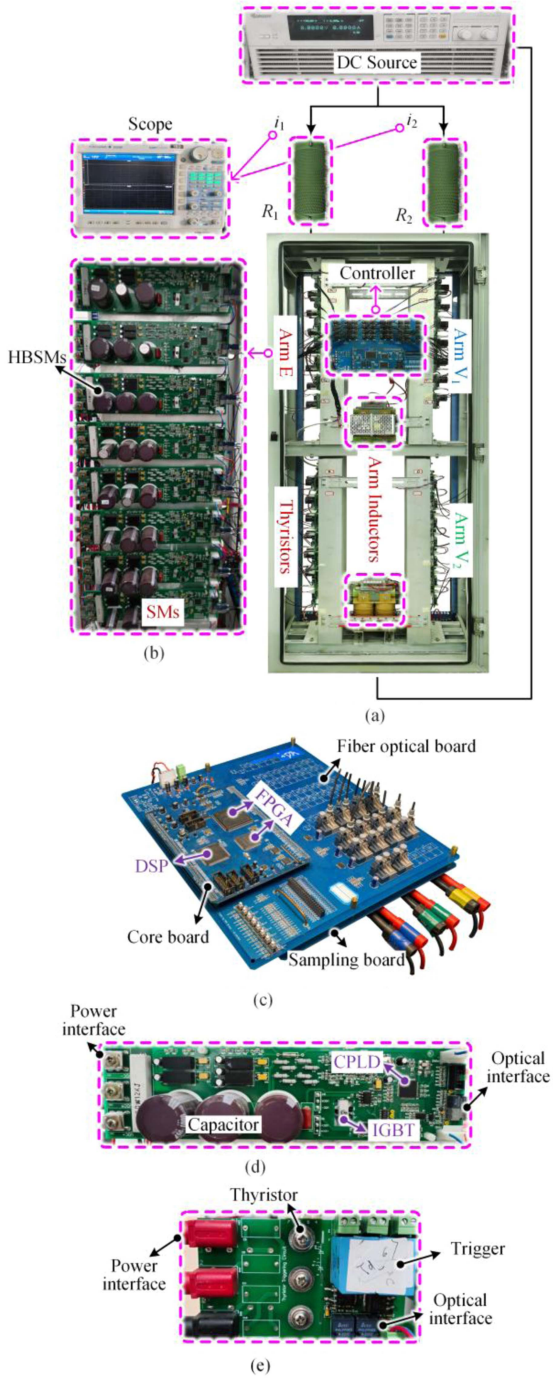

Fig. 16. Photo of experimental prototype. (a) Picture of the experimental protoype. (b) Picture of the arm. (c) Picture of the controller. (d) Picture of the HBSM. (e) Picture of the thyristor and trigger.

TABLE II
PARAMETERS OF EXPERIMENTAL PROTOTYPE

Parameters	Values
SMs of strings	$N_{V1}=N_{V2}=N_E=4$
Capacitor voltage	60 V
SM capacitance	6 mF
Arm inductance	2 mH
Operation frequency	100 Hz

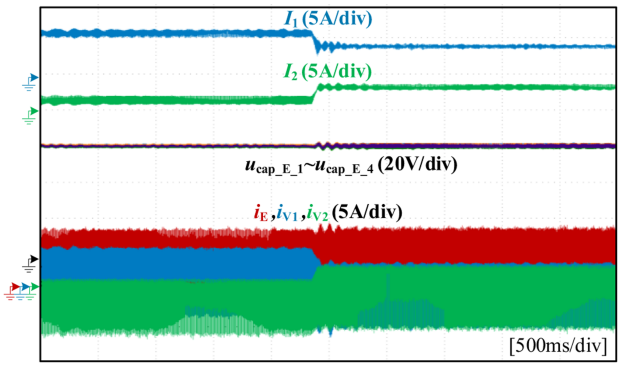

Fig. 17. Experimental results of dynamic process of DC power flow control.

VII. EXPERIMENTAL RESULTS

Experimental tests on a scaled-down prototype are given to demonstrate the effectiveness of the proposed topology. Fig. 16 shows the configuration of the experimental circuit. The dc current source outputs a constant line current, 6 A. The resistances of lines 1 and 2 are 10 Ω and 50 Ω, respectively. Therefore, the natural current flows are 5 A and 1 A. Each arm includes four SMs, and rated voltage of SMs is 60 V. The parameters of down-scaled prototype are given in Table II. The control schemes including a TMS320F28377 DSP for upper-level control and arm control, and two FPGAs for modulation and capacitor voltage balancing and sends the PWM signals to the SMs and triggering signals to thyristors.

Fig. 17 shows the experimental results of the dynamic process of dc power flow control. The proposed DCPFC regulates the current I_1 from 5 to 3 A. Meanwhile, the current I_2 increases from 1 to 3 A. During the control process, the voltages of capacitors are steady, and the currents in the arms change following the operating principle.

Fig. 18 shows the zoomed experimental results of the proposed DCPFC. The line currents I_1 and I_2 are controlled to 3 A. The current of arm E, I_E, is an 8.57 A trapezoidal waveform. The arm currents i_{V1} and i_{V2} change between 3 A and –5.57 A. The arm current waveforms have a slope during rising and falling for limiting di/dt. The voltages of capacitors are steady and balanced around 60 V. According to (3), the dc power flow control voltage U_1 and U_2 are 60 V and –60 V, respectively. The turn-OFF voltage can be founded in the voltage results of energy-exchanging arm at the end of current commutations stages for reliable closing thyristor valves.

Fig. 19(a) shows the experimental results of the start process of the DCPFC. In the beginning, the line current I_1 and the current of switch SW_1, i_{SW1}, are 3 A. The precharged voltage

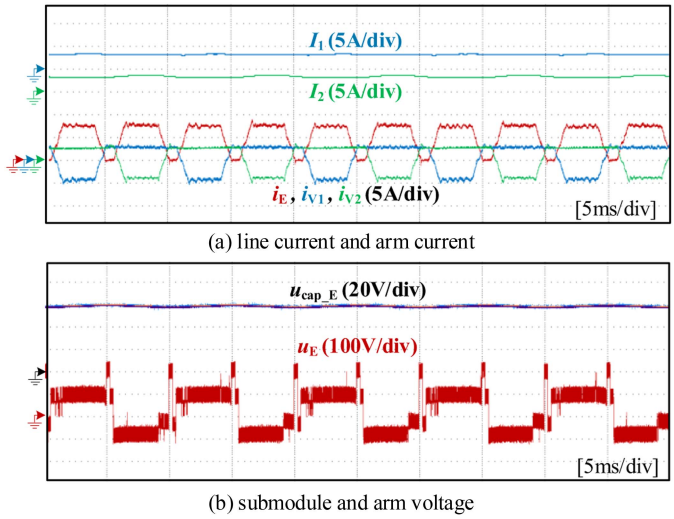

Fig. 18. Zoomed experimental results of DCPFC. (a) Line currents and arm currents; (b) voltages of SMs and energy-exchanging arm.

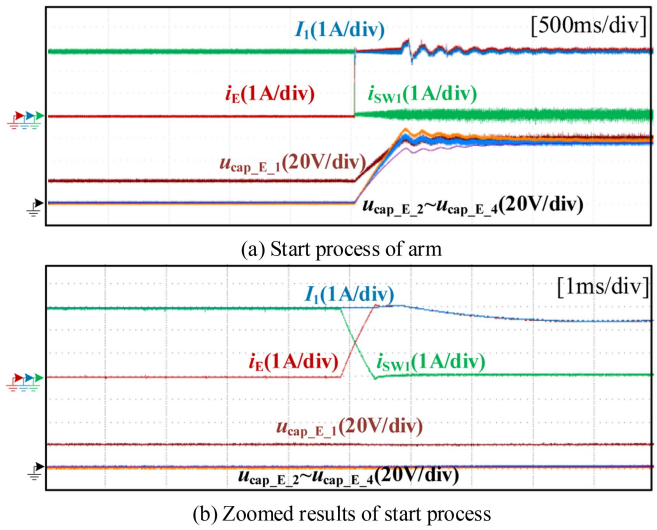

Fig. 19. (a) Experimental results of start process of DCPFC; (b) zoomed results of start process.

of capacitor is 20 V. After the current commutating, i_{SW1} falls to 0, and the switch SW_1 opened safely with zero current. The line current I_1 flows through the arm. Then, all capacitors are charged through line current under the voltage control. Fig. 19(b) gives the zoomed results.

VIII. CONCLUSION

This article presents an innovative design for a DCPFC that enhances power flow control capability of meshed HVDC grids while minimizing the use of thyristors and IGBTs. This is achieved through the implementation of an energy-exchanging arm in proposed DCPFC, which facilitates energy exchanging between line arms across different dc lines, enabling effective energy balance without the need for ac current. With the operating principle of energy-exchanging arm, thyristor valves are only positioned between the energy-exchanging arm and the

line arms, thereby reducing the number of thyristors required. The proposed DCPFC connects all line arms to constant dc lines, rather than interconnecting them among different DC lines. This approach mitigates voltage requirement on individual line arms and decreases the number of IGBTs needed. In addition, the use of line arms of the DCPFC further results in a reduction in the number of IGBTs required.

These benefits are particularly significant in multiport application. The start process for DCPFC is also carefully designed, and both parameter design and control strategies are developed to ensure the proper operation of the proposed DCPFC. Simulation and experimental testing have been performed to demonstrate the effectiveness of the proposed design in meshed HVDC grids.

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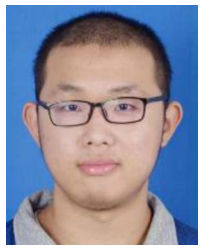

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