An Asymmetric Hybrid Phase-Leg Modular Multilevel Converter With Small Volume, Low Cost, and DC Fault-Blocking Capability

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***Abstract*—Hybrid modular multilevel converters (MMCs) have exhibited superior power density and cost-effectiveness than the conventional half-bridge submodule-based MMC (HB-MMC), while still maintaining the hassle of using high-voltage dc supporting capacitors or nonstandard transformers. To alleviate the hassle, an asymmetric hybrid phase leg MMC (AHPL-MMC) is proposed in this article. The presented AHPL-MMC consists of a half-bridge submodule-based phase leg and two full-bridge submodule-based hybrid phase legs. This asymmetric configuration reduces bridge arm inductance, the number of submodules, and total capacitance, thereby improving the converter's power density and cost-effectiveness. In addition, the proposed converter can operate across the full range of modulation indices and power factors with the features of dc fault blocking and low dc current ripples. The operating principles, parameter design, and performance comparison of the AHPL-MMC are provided in this article. Close-loop energy balancing control methods are further proposed for the hybrid phase legs and the conventional phase leg, respectively. The effectiveness of the proposed AHPL-MMC is validated by both simulation and experimental results.**

***Index Terms*—Asymmetric bridge arm, capacitor voltage balancing, hybrid multilevel converter (HMC), power density.**

I. Introduction

MODULAR multilevel converters (MMCs) have been extensively investigated due to their notable advantages, including high modularity, scalability, reliability, and power quality. These converters are increasingly employed in medium- and high-voltage applications, such as the interconnection of cross-regional power grids, flexible dc distribution grids, and the long-distance transmission of renewable energy [1]. However, the typical half-bridge submodule-based MMC (HB-MMC) has inherent limitations, including a large number of submodules (SMs), a high requirement of SM capacitance, and the need for dc circuit breakers, making it challenging to use HB-MMC in cost-, weight-, or space-sensitive applications [2].

Much research has been done to improve the power density and economics of MMCs. One promising topology is the hybrid MMCs [3], [4], which mainly consist of high-voltage direction switches (DSs) and wave-shaping circuits (WSCs). The DSs consist of series-connected semiconductor switches, while the WSCs consist of cascaded full-bridge SMs (FBSMs) or half-bridge SMs (HBSMs). The DSs are alternately switched at low frequencies to connect the WSCs, thereby forming multilevel voltages on the ac side. The hybrid MMCs can improve the utilization rate of SMs and compress the energy fluctuation of the SM capacitor [4], thus effectively reducing the capacity and quantity requirements of the SMs.

Hybrid MMCs can be classified into two primary types based on the connection pattern of the phase legs. One category consists of series-phase-leg-type hybrid MMCs [3], [5], [6], in which the three-phase legs are connected in series on dc side. Typically, a nonstandard open-winding ac transformer is necessary for this configuration [7], which may result in increased system cost and size. The series connection can reduce the number of SMs and switches, often accompanied by a decrease in SM capacitance. For instance, the chain-link parallel hybrid converter (PHC) can save approximately 1/4 of the switches and 4/5 of the SM capacitance [4], [8], [9]. However, the PHC has certain technical limitations. It can only operate at a fixed modulation index of $\pi/3$, with the dc current exhibiting a 6th-order ripple. Furthermore, it is unable to block the dc fault current. Although the 3rd harmonic injection method can marginally extend the operating range [9], [10], the current and voltage ratings will increase accordingly. To further achieve dc voltage filtering, a wider modulation index range, and dc fault blocking, additional cascaded FBSMs can be inserted into the dc side, the ac side, or the inner bridge arm of the PHC, thereby forming the series bridge converter [11], [12], hybrid series bridge converter [13], and hybrid phase converter [14]. However, the assembly of additional cascaded FBSMs will undoubtedly result in power loss, volume, and cost issues [15].

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TABLE I
BRIEF COMPARISON OF THE CONVERTERS

	AHPL-MMC	HB-MMC	PHC	AAC	HMC
SM number	Medium	Largest	Small	Large	Small
SM capacitance	Medium	Large	Small	Small	Small
Modulation index range	[0,1]	[0,1]	$\pi/3$	$4/\pi$	$4/\pi$
DC side harmonics	Tiny	Tiny	6^{th}	6^{th}	6^{th}
Bridge Arm inductor	Small	Large	N/A	N/A	N/A
DC fault-blocking capability	Yes	No	No	Yes	Yes
AC transformer	Y-Δ	Y-Δ	Open-winding	Y-Δ	Y-Δ
DC supporting capacitor	No	No	No	Yes	Yes

Another category is the parallel-phase-leg-type hybrid MMCs [16], in which the three-phase legs are connected in parallel on dc side. Typically, the cascaded SMs are alternatively connected to the dc side through DSs, it is often necessary to configure dc-supporting capacitors to maintain the dc voltage. The alternate arm converter (AAC) [17] and the hybrid multilevel converter (HMC) [18] are two typical examples of this type of converter. They have the capability to block dc faults, but they still face the problem of 6th-order dc current ripple and a fixed modulation index of $4/\pi$ [16]. To achieve a higher operating range of modulation index for the AAC, the upper and lower bridge arms are turned ON simultaneously during an overlapping period in [19] and [20], thus generating a circulating current to charge or discharge the WSC. For the HMC, the phase angle or pulsewidth of the DSs is used to adjust the energy balance of the WSC [21], allowing a full range of modulation indices. In addition, the time-sharing AAC (TS-AAC) [22], three-level hybrid MMC [23], [24], etc. are developed to reduce the SM number or SM capacitance. To meet the high-voltage criteria, the dc-supporting capacitor requires a significant number of series-connected split capacitors [25]. This results in cost and volume issues, along with challenges in maintaining dynamic voltage balance among the series-connected capacitors.

For three-phase converters, the phase legs are traditionally designed with symmetric structures to ensure consistency in terms of loss, lifetime, and layout. This article, however, introduces a new concept of asymmetric phase legs and presents an asymmetric hybrid phase leg MMC (AHPL-MMC). This new converter combines cost-effectiveness and high-power density with dc fault-blocking capability and can operate across the full range of modulation indices and power factor angles. It addresses the challenges associated with nonstandard ac transformers in series-phase-leg hybrid MMCs and the need for large-capacity dc-supporting capacitors in parallel-phase-leg hybrid MMCs. A brief comparison of the mentioned converters is listed in Table I.

The rest of this article is structured as follows. Section II introduces the operating principle, followed by the parameter design method in Section III, and performance comparison in Section IV. Section V presents the control strategies, while Section VI provides the simulation and experimental results for verification. Finally, Section VII concludes this article.

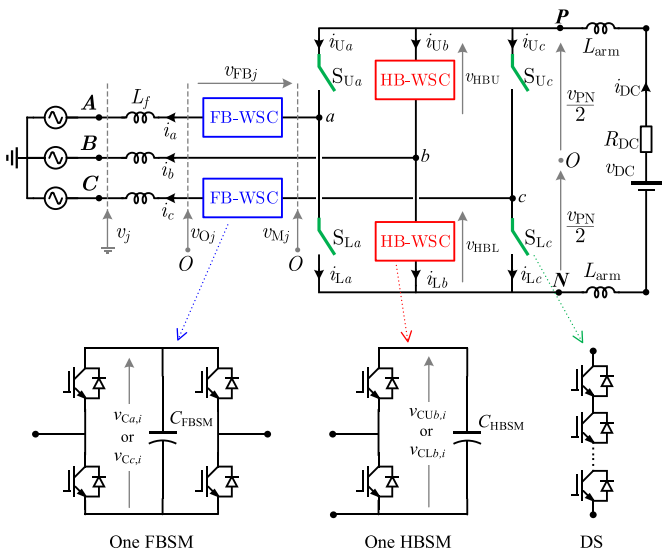

Fig. 1. Topology of AHPL-MMC.

II. OPERATION PRINCIPLE OF THE AHPL-MMC

A. Topology of the AHPL-MMC

Fig. 1 illustrates the topology of the proposed AHPL-MMC. Both phases a and c utilize a hybrid phase leg, which consists of upper and lower DSs (S_{Ua}, S_{Uc}, S_{La}, and S_{Lc}) and full-bridge submodule-based wave shaping circuits (FB-WSC). In contrast, phase b employs conventional upper and lower bridge arms, each consisting of half-bridge submodule-based wave shaping circuits (HB-WSC). A total of N_{FBSM} and N_{HBSM} SMs are employed in the FB-WSC and HB-WSC, respectively. C_{FBSM} and C_{HBSM} are the SM capacitance of the FBSM and HBSM, respectively. L_f is the ac filtering inductor, while L_{arm} is the bridge arm inductor that is symmetrically mounted on the dc side. Its purpose is to suppress dc current ripple, limit dc fault current, and prevent the direct connection between the phase leg of phase b and the dc voltage source. R_{DC} is the inner resistance of the equivalent dc source.

In Fig. 1, v_{PN} represents the voltage across ports P and N, and the neutral point O is defined as half of v_{PN}. On the dc side, v_{DC} refers to the voltage, and i_{DC} to the current. Meanwhile, v_j and i_j (where $j = a, b, c$) denote the ac side voltages and currents, respectively. The phase voltage of the converter is v_{Oj}, while v_{Mj} represents the voltage across the midpoint of the phase leg and the neutral point. In addition, v_{FBj} signifies the output voltage of the FB-WSC, while v_{HBU} and v_{HBL} are the output voltages of the upper and lower HB-WSCs. i_{Uj} and i_{Lj} stand for the branch currents of the upper and lower bridge arms. Finally, $v_{Ca,i}$ and $v_{Cc,i}$ are the capacitor voltage of the ith FBSM in phases a and c, respectively. $v_{CUb,i}$ and $v_{CLb,i}$ are the capacitor voltage of the ith HBSM in the upper and lower HB-WSCs, respectively.

B. Operation Principle of Hybrid Phase Leg (Phases a and c)

The three-phase ac voltages v_j and currents i_j in phase j are assumed to be

$$v_j = V_m \sin(\omega t + \theta_j), i_j = I_m \sin(\omega t + \theta_j + \varphi) \quad (1)$$

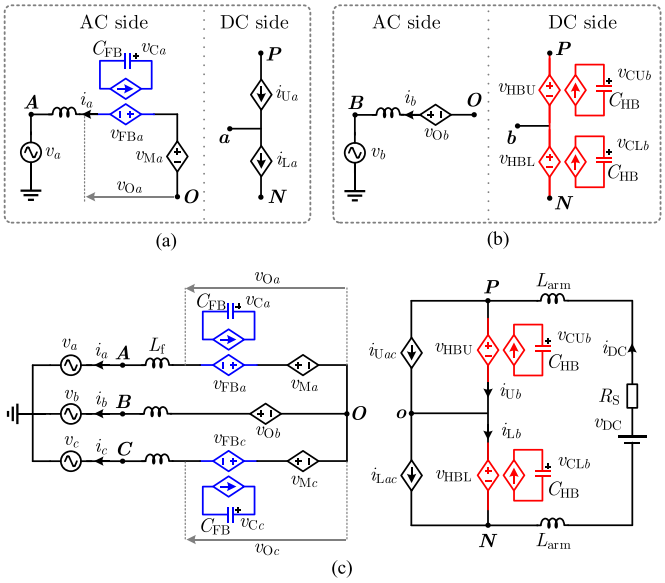

Fig. 2. Equivalent circuits of the (a) hybrid phase leg, (b) conventional phase leg, and (c) overall AHPL-MMC.

where V_m and I_m are the amplitudes. θ_j is the initial phase angle with $\theta_a = 0$, $\theta_b = -2\pi/3$, and $\theta_c = 2\pi/3$. ω is the angular frequency of the ac voltage, and $\varphi \in [-\pi/2, \pi/2]$ is the power factor angle.

Phases a and c follow a similar operation principle. Taking phase a as an example, the upper and lower DSs are alternately conducted for each half-fundamental cycle. The switching logic of the DSs is generated by

$$S_{\mathrm{U}a} = \bar{S}_{\mathrm{L}a} = \begin{cases} 1, & \sin(\omega t + \theta_a - \alpha_a) \geq 0 \\ 0, & \sin(\omega t + \theta_a - \alpha_a) < 0 \end{cases} \tag{2}$$

where $\alpha_a \in [-\pi/2, \pi/2]$ is the lagging phase angle relative to the initial phase angle of ac voltage. When $S_{\mathrm{U}a}$ is turned ON, $v_{\mathrm{M}a}$ is equal to $0.5v_{\mathrm{PN}}$ and i_a flows from port P. Conversely, when $S_{\mathrm{U}a}$ is turned OFF, $v_{\mathrm{M}a}$ equals $-0.5v_{\mathrm{PN}}$ and i_a flows from port N. Therefore, the switching characteristics of the DSs can be equivalent to a voltage source $v_{\mathrm{M}a}$ on the ac side and to two current sources, $i_{\mathrm{U}a}$ and $i_{\mathrm{L}a}$, on the dc side, as shown in Fig. 2(a). The expression of these voltage and current sources are as

$$v_{\mathrm{M}a} = \begin{cases} {}^1\!/_2 v_{\mathrm{PN}} \\ -{}^1\!/_2 v_{\mathrm{PN}} \end{cases}, i_{\mathrm{U}a} = \begin{cases} i_a \\ 0 \end{cases}, i_{\mathrm{L}a} = \begin{cases} 0, & S_{\mathrm{U}a}\mathrm{ON} \\ -i_a, & S_{\mathrm{U}a}\mathrm{OFF} \end{cases}. \tag{3}$$

According to the arm-level averaged modeling method [26], the cascaded FBSMs in FB-WSC can be regarded as an equivalent SM with capacitance and voltage equal to

$$C_{\mathrm{FB}} = C_{\mathrm{FBSM}}/N_{\mathrm{FBSM}}, v_{\mathrm{C}a} = \sum_{i=1}^{N_{\mathrm{FBSM}}} v_{\mathrm{C}a,i}. \tag{4}$$

The output of this equivalent SM can be represented by a voltage source $v_{\mathrm{FB}a}$. Thus, the voltage equation of the ac side

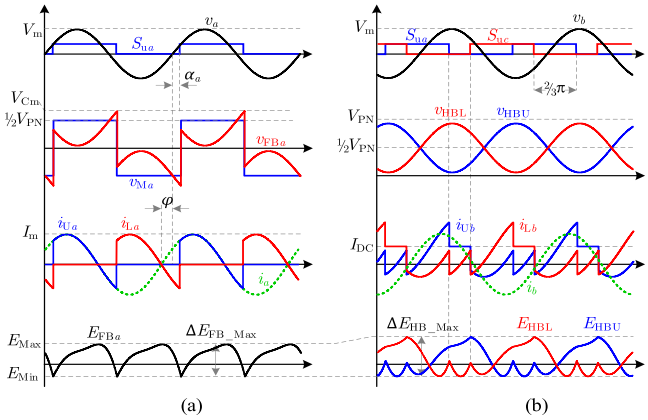

Fig. 3. Key waveforms of the AHPL-MMC.

in phase a can be expressed as

$$v_a + L_f \frac{\mathrm{d}i_a}{\mathrm{d}t} = v_{\mathrm{O}a}, v_{\mathrm{O}a} + v_{\mathrm{FB}a} = v_{\mathrm{M}a}. \tag{5}$$

Since the voltage drop on L_f is relatively small and can be neglected, $v_{\mathrm{FB}a}$ can be approximated as

$$v_{\mathrm{FB}a} = \begin{cases} {}^1\!/_2 v_{\mathrm{PN}} - V_{\mathrm{m}} \sin(\omega t + \theta_a), & S_{\mathrm{U}a}\mathrm{ON} \\ -{}^1\!/_2 v_{\mathrm{PN}} - V_{\mathrm{m}} \sin(\omega t + \theta_a), & S_{\mathrm{U}a}\mathrm{OFF} \end{cases}. \tag{6}$$

The typical waveforms of the hybrid phase leg of the AHPL-MMC are shown in Fig. 3(a), where $V_{\mathrm{C}m}$ is the maximum output voltage of the FB-WSC, E is the energy of the WSC, and ΔE_{Max} is the maximum energy fluctuation.

C. Operation Principle of Conventional Phase Leg (Phase b)

The upper or lower HB-WSCs in phase b can be also regarded as an equivalent SM with capacitance and voltage equal to

$$C_{\mathrm{HB}} = C_{\mathrm{HBSM}}/N_{\mathrm{HBSM}},$$
$$v_{\mathrm{CU}b} = \sum_{i=1}^{N_{\mathrm{HBSM}}} v_{\mathrm{CU}b,i},$$
$$v_{\mathrm{CL}b} = \sum_{i=1}^{N_{\mathrm{HBSM}}} v_{\mathrm{CL}b,i}. \tag{7}$$

The output of the equivalent SM can be represented by a voltage source, v_{HBU} or v_{HBL}. The operation principle of phase b is similar to that of a traditional MMC. The equivalent circuit is shown in Fig. 2(b).

The common mode voltage of v_{HBU} and v_{HBL} is equal to the P-N port voltage v_{PN}, i.e.,

$$v_{\mathrm{PN}} = v_{\mathrm{HBU}} + v_{\mathrm{HBL}}, v_{\mathrm{PN}} + 2L_{\mathrm{arm}} \frac{\mathrm{d}i_{\mathrm{DC}}}{\mathrm{d}t} + i_{\mathrm{DC}} R_{\mathrm{DC}} = v_{\mathrm{DC}}. \tag{8}$$

The differential mode voltage of v_{HBU} and v_{HBL} can be represented by another voltage source on the ac side, namely the phase voltage $v_{\mathrm{O}b}$ of the converter, and can be expressed as

$$v_{\mathrm{O}b} = {}^1\!/_2 (v_{\mathrm{HBL}} - v_{\mathrm{HBU}}). \tag{9}$$

The voltage equation of the ac side can be expressed as

$$v_b + L_f \frac{\mathrm{d}i_b}{\mathrm{d}t} = v_{\mathrm{Ob}}. \tag{10}$$

Consequently, when neglecting the voltage drop on L_f, the output voltages of the upper and lower HB-WSCs can be approximated as

$$\begin{cases} v_{\mathrm{HBU}} = {}^1\!/_2 v_{\mathrm{PN}} - V_m \sin(\omega t + \theta_b) \\ v_{\mathrm{HBL}} = {}^1\!/_2 v_{\mathrm{PN}} + V_m \sin(\omega t + \theta_b) \end{cases}. \tag{11}$$

Since the conventional phase leg acts as a series-connected voltage source on the dc side, the branch currents of the upper and lower HB-WSCs are determined by the dc current and the branch current of the other two hybrid bridge arms, which is

$$\begin{cases} i_{\mathrm{U}b} = i_{\mathrm{DC}} - S_{\mathrm{U}a} i_a - S_{\mathrm{U}c} i_c \\ i_{\mathrm{L}b} = i_{\mathrm{DC}} + \bar{S}_{\mathrm{U}a} i_a + \bar{S}_{\mathrm{U}c} i_c \end{cases}. \tag{12}$$

According to the conservation of the average active power on the ac and dc sides of the converter, we can obtain

$$V_{\mathrm{PN}} I_{\mathrm{DC}} = \frac{3}{2} V_m I_m \cos\varphi \Rightarrow I_{\mathrm{DC}} = \frac{3 V_m I_m \cos\varphi}{2 V_{\mathrm{PN}}} \tag{13}$$

where I_{DC} and V_{PN} are the nominal dc components of i_{DC} and v_{PN}. The typical waveforms of the conventional bridge arm of the AHPL-MMC are shown in Fig. 3(b).

To derive the overall equivalent circuit of the AHPL-MMC, the following steps are taken.

1) Connect the O points of the ac side equivalent circuits of different phases.
2) Connect the phase leg midpoints (points a, b, and c) of the dc side equivalent circuit, forming a new current node o.
3) Integrate the dc side equivalent circuits of phases a and c into two current sources based on

$$i_{\mathrm{U}ac} = i_{\mathrm{U}a} + i_{\mathrm{U}c}, i_{\mathrm{L}ac} = i_{\mathrm{L}a} + i_{\mathrm{L}c}. \tag{14}$$

The final equivalent circuit of the overall AHPL-MMC is illustrated in Fig. 2(c).

D. Energy Balancing Condition of Bridge Arms

Applying the energy conversation law to the FB-WSC and HB-WSC, we can obtain

$$v_{\mathrm{FB}a} i_a = C_{\mathrm{FB}} \frac{\mathrm{d}v_{\mathrm{C}a}}{\mathrm{d}t} v_{\mathrm{C}a} \Rightarrow v_{\mathrm{C}a} = \sqrt{\frac{2}{C_{\mathrm{FB}}} \int v_{\mathrm{FB}a} i_a \mathrm{d}t + V_{\mathrm{C}a0}^2} \tag{15}$$

$$\begin{aligned} v_{\mathrm{CU}b} i_{\mathrm{U}a} &= C_{\mathrm{HB}} \frac{\mathrm{d}v_{\mathrm{CU}b}}{\mathrm{d}t} v_{\mathrm{CU}b} \Rightarrow v_{\mathrm{CU}b} \\ &= \sqrt{\frac{2}{C_{\mathrm{HB}}} \int v_{\mathrm{HBU}} i_{\mathrm{U}b} \mathrm{d}t + V_{\mathrm{CU}b0}^2} \end{aligned} \tag{16}$$

$$\begin{aligned} v_{\mathrm{CL}b} i_{\mathrm{L}a} &= C_{\mathrm{HB}} \frac{\mathrm{d}v_{\mathrm{CL}b}}{\mathrm{d}t} v_{\mathrm{CL}b} \Rightarrow v_{\mathrm{CL}b} \\ &= \sqrt{\frac{2}{C_{\mathrm{HB}}} \int v_{\mathrm{HBL}} i_{\mathrm{L}b} \mathrm{d}t + V_{\mathrm{CL}b0}^2} \end{aligned} \tag{17}$$

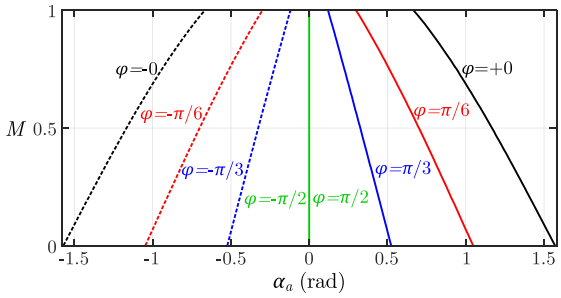

Fig. 4. Theoretical α_a for maintaining the total energy balancing of the hybrid phase leg under different M and φ.

where $V_{\mathrm{C}a0}$, $V_{\mathrm{CU}b0}$, and $V_{\mathrm{CL}b0}$ are the initial voltages of the equivalent SMs. As illustrated in (15)–(17), to maintain the capacitor voltage balance of the FB-WSC and HB-WSC, the integral terms, which represent the accumulated energy of the WSC, must be zero over a fundamental period.

Taking phase a for analysis (similar results can be obtained for phase c). According to Fig. 3(a), the accumulated energy $W_{\mathrm{FB}a}$ of the FB-WSC over a fundamental period can be calculated as

$$\begin{aligned} W_{\mathrm{FB}a} &= \int_{\alpha_a/\omega}^{(\pi+\alpha_a)/\omega} ({}^1\!/_2 v_{\mathrm{PN}} - V_m \sin(\omega t)) I_m \sin(\omega t + \varphi) \mathrm{d}t \\ &+ \int_{(\pi+\alpha_a)/\omega}^{(2\pi+\alpha_a)/\omega} (-{}^1\!/_2 v_{\mathrm{PN}} - V_m \sin(\omega t)) I_m \sin(\omega t + \varphi) \mathrm{d}t \\ &= \frac{I_m \ (2\, V_{\mathrm{PN}} \ \cos(\alpha_a + \varphi) - \pi\, V_m \ \cos(\varphi))}{\omega}. \end{aligned} \tag{18}$$

To ensure $W_{\mathrm{FB}\,a} = 0$, the lagging phase angle of the switching signal $S_{\mathrm{U}\,a}$ under different operation conditions needs to be

$$\alpha_a = \begin{cases} -\arccos({}^1\!/_4 \pi M \cos\varphi) - \varphi, \varphi \in [-{}^1\!/_2\pi, 0] \\ \arccos({}^1\!/_4 \pi M \cos\varphi) - \varphi, \varphi \in [0, {}^1\!/_2\pi] \end{cases} \tag{19}$$

where $M = 2V_m/V_{\mathrm{PN}}$ is defined as the modulation index of the converter and $M \in [01]$. Equation (19) is defined as the energy balance condition of the hybrid phase leg. Fig. 4 illustrates the relationship among M, φ, and α_a. It can be found that varying modulation indices M and power factor angles φ require different α_a (the turned-ON angle of the $S_{\mathrm{U}\,a}$) to be set to maintain the total energy balance of the hybrid phase leg.

For phase b, the accumulated energy of the upper HB-WSC over a fundamental period can be calculated as

$$\begin{aligned} W_{\mathrm{HBU}} &= \int_{\alpha_a/\omega}^{(2\pi+\alpha_a)/\omega} v_{\mathrm{HBU}} i_{\mathrm{U}b} \mathrm{d}t \\ &= \frac{2\pi}{\omega} \left(\frac{i_{\mathrm{DC}} v_{\mathrm{PN}}}{2} - \frac{3 V_m I_m \cos\varphi}{4} \right). \end{aligned} \tag{20}$$

By substituting (13) into (20), it can be proved that E_{HBU} is always equal to 0, regardless of the values of M and φ. Similarly, for the lower HB-WSC, the accumulated energy is

$$W_{\mathrm{HBL}} = \int_{\alpha_a/\omega}^{(2\pi+\alpha_a)/\omega} v_{\mathrm{HBL}} i_{\mathrm{L}b} \mathrm{d}t$$

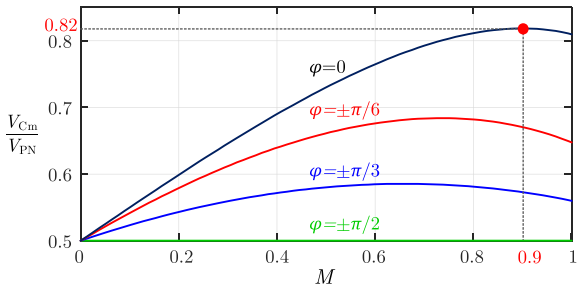

Fig. 5. Relationship among $V_{\mathrm{Cm}}/V_{\mathrm{PN}}$, φ, and M.

$$= \frac{2\pi}{\omega}\left(\frac{i_{\mathrm{DC}}v_{\mathrm{PN}}}{2} - \frac{3V_m I_m \cos\varphi}{4}\right) = 0. \tag{21}$$

This implies that the energy of the HB-WSC in AHPL-MMC is automatically balanced when the energy of the other two hybrid phase legs is balanced.

III. Parameter Design of the AHPL-MMC

A. Number of SMs

For the hybrid phase leg of phase a, it can be seen from Fig. 3(a) that under varying lagging angle α_a, the maximum output voltage V_{Cm} of the FB-WSC differs and can be determined by

$$V_{\mathrm{Cm}} = {}^1\!/_2 V_{\mathrm{PN}} + V_m \left|\sin\alpha_a\right|. \tag{22}$$

Substituting (19) into (22), we can obtain (23) shown at the bottom of this page.

The relationship among $V_{\mathrm{Cm}}/V_{\mathrm{PN}}$, φ, and M is drawn in Fig. 5. As M decreases, $V_{\mathrm{Cm}}/V_{\mathrm{PN}}$ initially increases and then decreases, reaching a maximum value of approximately 0.82 when M is around 0.9 and $\varphi = 0$. Therefore, to generate this maximum output voltage under all operation conditions, the total capacitor voltage of all cascaded FBSMs in FB-WSC should be larger than $0.82V_{\mathrm{PN}}$.

In addition, to block the fault current in case of pole-to-pole dc short-circuit fault, each FB-WSC needs to withstand the ac line voltage, as shown in Fig. 6. Therefore, the total capacitor voltage of the cascaded FBSMs should be larger than $\sqrt{3}V_m$.

Considering the above-mentioned two requirements, the SM number in each FB-WSC can be determined by

$$N_{\mathrm{FBSM}} = \max\left\{\frac{0.82V_{\mathrm{PN}}}{V_{\mathrm{CN}}M_{\mathrm{WSC}}}, \frac{\sqrt{3}MV_{\mathrm{PN}}}{2V_{\mathrm{CN}}}\right\} \tag{24}$$

where V_{CN} is the nominal voltage of the SM capacitor. M_{WSC} is the modulation index of the WSC and $M_{\mathrm{WSC}} \in [01]$.

For the traditional phase leg of phase b, the maximum output voltage of the upper or lower HBSMs is V_{PN}, so the SM number in each HB-WSC is

$$N_{\mathrm{HBSM}} = V_{\mathrm{PN}}/V_{\mathrm{CN}}. \tag{25}$$

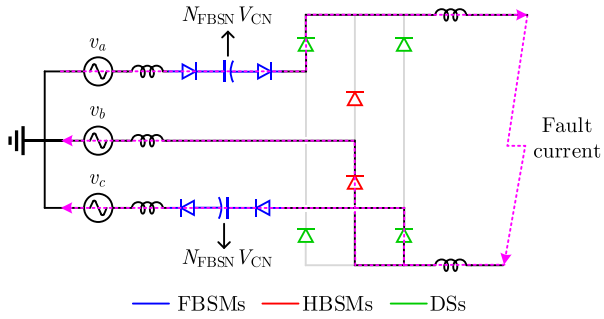

Fig. 6. Equivalent circuit of the AHPL-MMC under pole-to-pole DC short-circuit fault ($v_a > v_b$, $v_a > v_c$).

Each DS in the hybrid phase leg needs to withstand V_{PN} when turned OFF. Assuming that the DS uses the same type of switch as SMs, the number of switches in each DS is

$$N_{\mathrm{DS}} = V_{\mathrm{PN}}/V_{\mathrm{CN}}. \tag{26}$$

Thus, the total number of switches used in AHPL-MMC is

$$N_{\mathrm{SW}} = 8\left(N_{\mathrm{FBSM}} + N_{\mathrm{HBSM}}\right). \tag{27}$$

For the traditional HB-MMC, the SM number in each HB-WSC is also selected as (25), and the total number of switches is $12N_{\mathrm{HBSM}}$.

B. Filter Inductance

The requirement for the ac side filter inductor L_f in both the HB-MMC and AHPL-MMC is small, as their output voltages exhibit low harmonic content. Consequently, the ac side filter inductor for the AHPL-MMC can be designed to be identical to that of the HB-MMC, specifically at 0.02 p.u. [25], which is

$$L_f = 0.02 \times \frac{3V_m^2}{2\omega S_{\mathrm{base}}} \tag{28}$$

where S_{base} is the apparent power of the converter.

The bridge arm inductors L_{arm} in the HB-MMC serve two primary functions: they help suppress circulating currents and limit the rising rate of fault current under dc faults. The latter function is predominant, and the inductors can be sized between 0.1 and 0.3 p.u. [27]. In the proposed AHPL-MMC, there is no circulating current between phases, therefore, the bridge arm inductor is utilized solely to limit the rising rate of the fault current. Fig. 7 illustrates the equivalent discharging circuit of the HB-MMC and AHPL-MMC at the instant of dc pole-to-pole fault occurrence. Assuming that the capacitor voltage remains constant at this time, and the total output voltage of the upper and lower HB-WSCs is equal to V_{PN}. It can be observed that three sets of equivalent common-mode voltage sources of the HB-MMC discharge through the bridge arm inductor, resulting in a fault current rise rate that is three times greater than that of the AHPL-MMC. Consequently, for the same fault current

$$\frac{V_{\mathrm{Cm}}}{V_{\mathrm{PN}}} = \begin{cases} {}^1\!/_2 + {}^1\!/_2 M\left|\sin\left[-\arccos\left({}^1\!/_4\pi M\cos\varphi\right) - \varphi\right]\right|, & \varphi \in \left[-{}^1\!/_2\pi, 0\right] \\ {}^1\!/_2 + {}^1\!/_2 M\left|\sin\left[\arccos\left({}^1\!/_4\pi M\cos\varphi\right) - \varphi\right]\right|, & \varphi \in \left[0, {}^1\!/_2\pi\right] \end{cases} \tag{23}$$

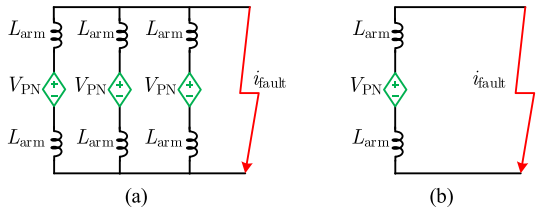

Fig. 7. Equivalent discharging circuit of the (a) HB-MMC and (b) AHPL-MMC at the instant of DC pole-to-pole fault occurrence.

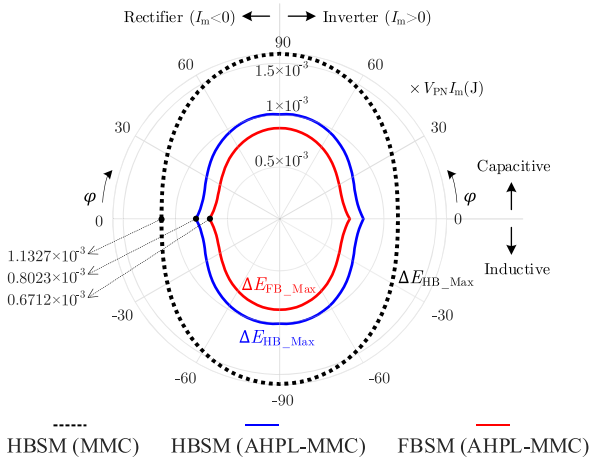

Fig. 8. Maximum energy fluctuation of the AHPL-MMC and traditional MMC.

rise rate, the bridge arm inductance of the AHPL-MMC is only one-third that of the HB-MMC, which is

$$L_{\text{arm}} = \frac{1}{3}L_{\text{arm}}^{\text{HB-MMC}} = (0.1-0.3)\times\frac{V_m^2}{2\omega S_{\text{base}}}. \tag{29}$$

C. SM Capacitance

The SM capacitance is designed according to the maximum energy fluctuation, i.e., $\Delta E_{\text{FB\_Max}}$ and $\Delta E_{\text{HB\_Max}}$, of the cascaded SMs [21], which can be expressed as

$$C_{\text{FBSM}} = \frac{\Delta E_{\text{FB\_Max}}}{2\varepsilon N_{\text{FBSM}} V_{\text{CN}}^2}, C_{\text{HBSM}} = \frac{\Delta E_{\text{HB\_Max}}}{2\varepsilon N_{\text{HBSM}} V_{\text{CN}}^2} \tag{30}$$

where ε is the peak-to-average voltage ripple factor. Since E_{FB} and E_{HB} are piecewise functions, as shown in Fig. 3. The numerical integration method is applied to find the maximum $E_{\max}$ and minimum E_{Min} values of E_{FB} and E_{HB}, respectively. Fig. 8 illustrates the measured maximum energy fluctuation of FB-WSC and HB-WSC under various power factor angles and rectifier/inverter modes when $M = 0.9$. This figure also includes the maximum energy fluctuation of the cascaded HBSMs in traditional MMC for comparison [28]. As can be seen in Fig. 8, At the rated point ($\varphi = 0$), the $\Delta E_{\text{FB\_Max}}$ of FB-WSC in AHPL-MMC is measured at $0.6712e^{-3}V_{\text{PN}}I_m$(J), while the $\Delta E_{\text{HB\_Max}}$ of HB-WSC is measured at $0.8023e^{-3}V_{\text{PN}}I_m$(J). In comparison, the $\Delta E_{\text{HB\_Max}}$ of HB-WSC in traditional HB-MMC is measured at $1.1327e^{-3}V_{\text{PN}}I_m$(J). A smaller maximum energy fluctuation can lead to smaller SM capacitance. Therefore, the SM capacitance of the AHPL-MMC can be reduced.

TABLE II
MAIN PARAMETERS OF A MMC SYSTEM

Parameters	Symbol	Value
DC source voltage	V_{DC} or V_{PN}	200 kV
The inner resistor of the DC source	R_{DC}	0.5 Ω
AC voltage magnitude	V_{m}	90 kV
AC current magnitude	I_{m}	1 kA
Apparent power	S_{base}	135Mvar
Angular frequency	ω	100π rad/s
Nominal SM capacitor voltage	V_{CN}	1.6 kV

TABLE III
PARAMETER COMPARISON FOR HB-MMC, H-MMC, AND AHPL-MMC

Parameters	HB-MMC	H-MMC	AHPL-MMC
Number of SMs in WSC, N_{FBSM} or N_{HBSM}	125	125	N_{FBSM}:114 N_{HBSM}:125
Number of switches in DS, N_{DS}	None	None	125
Total number of switches, N_{SW}	1500	2250	1912
AC side filter inductance, L_{f}	5.73mH	5.73mH	5.73mH
Bridge arm inductance, L_{arm}	50mH	50mH	17mH
SM capacitance, C_{FBSM} or C_{HBSM}	7.1mF	7.1mF	C_{FBSM}: 4.6mF C_{HBSM}: 5mF
DC circuit breaker	Yes	No	No

D. Parameter Comparison

Table II presents the main parameters of a MMC system. For the purpose of parameter calculation, we select the values $M = M_{\text{SM}} = 0.9$, $\varphi = 0$, and $\varepsilon = 5\%$ as examples. Based on (24)–(30), we can derive the component parameters for the HB-MMC, the hybrid MMC (H-MMC) incorporating 50% FBSMs [29], and the AHPL-MMC, which are detailed in Table III.

In comparison to traditional HB-MMC, the proposed AHPL-MMC demonstrates a 36.27% reduction in the total number of SMs, a 56.83% decrease in the total energy storage requirements of SM capacitors, and an 88.67% reduction in the total inductance of the bridge arm. Although the total number of switches increases by 27.47%, it provides dc fault-blocking capability. In comparison to the H-MMC, which also does not require a dc circuit breaker, the total number of switches decreases by 15%. These attributes will contribute to improvements in both the cost and volume of the converter.

IV. PERFORMANCE COMPARISON

A. Current Stress

For the traditional HB-MMC, taking the upper bridge arm of phase a as an example, the RMS current i_{U} of the bridge arm over the fundamental cycle can be calculated as

$$I_U = \sqrt{\frac{1}{T}\int_0^T \left[\frac{I_{\text{DC}}}{3} + \frac{I_m}{2}\sin(\omega t + \varphi)\right]^2 \text{d}t}$$

$$= \frac{I_m\sqrt{(M\cos\varphi)^2+2}}{4}. \tag{31}$$

For the proposed AHPL-MMC, the current flowing through the FB-WSC in phases a or c is equal to the ac current, and the RMS current is $I_{\mathrm{FB}} = \sqrt{2}I_m/2$. According to the current expression of the upper DS in phase a, the RMS current I_{DS} can be calculated as

$$I_{\mathrm{DS}} = \sqrt{\frac{1}{T}\int_{\alpha_a}^{\pi+\alpha_a} i_{\mathrm{U}a}^2 \mathrm{d}t} = \frac{I_m}{2}. \tag{32}$$

According to the current expression of the upper bridge arm in phase b, the RMS current I_{HB} can be calculated as

$$I_{\mathrm{HB}} = \sqrt{\frac{1}{T}\int_0^T i_{\mathrm{U}b}^2 \mathrm{d}t} = \frac{I_m\sqrt{240-144\sqrt{3}/\pi+\left(18\sqrt{3}\pi-108\right)(M\cos\varphi)^2}}{24}. \tag{33}$$

By substituting $M = 0.9$ and $\varphi = 0$ into (31)–(33), we can find that the current stress of the FBSM, DS, and HBSM in the AHPL-MMC is increased by 68.7%, 19.3%, and 22.8%, respectively, compared to the HBSM in the HB-MMC. This increase in current stress is likely to result in a higher cost for the switches and SM capacitors.

B. Power Loss of Switches

According to the simplified power loss calculation method for MMCs [21], [28], it is assumed that the IGBT and its antiparallel diode exhibit the same turn-ON voltage drop, denoted as V_F. By neglecting the switching power loss due to the relatively low switching frequency, the conduction power loss can be assessed based on the number of switches within the conduction path, the absolute current flowing through them, and the turn-ON voltage drop.

For each FBSM in phases a or c, there are always two switches conducting, regardless of the current direction and the states of the FBSM. The power loss of the FB-WSC can be calculated as

$$P_{\text{FB-WSC}} = 2N_{\mathrm{FBSM}}V_F \times \frac{1}{T}\int_0^{2\pi/\omega} |I_m\sin(\omega t+\varphi)|\,\mathrm{d}t = \frac{4N_{\mathrm{FBSM}}V_F I_m}{\pi}. \tag{34}$$

The upper and lower DSs are alternatively conducting, the total power loss can be calculated as

$$P_{\mathrm{DS}} = \underbrace{N_{\mathrm{DS}}V_f \times \frac{1}{T}\int_{\alpha_a/\omega}^{(\pi+\alpha_a)/\omega} |I_m\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{upperDSs}} + \underbrace{N_{\mathrm{DS}}V_f \times \frac{1}{T}\int_{(\pi+\alpha_a)/\omega}^{(2\pi+\alpha_a)/\omega} |I_m\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{lowerDSs}}$$

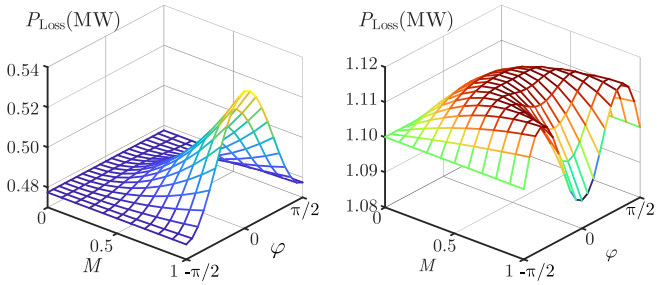

Fig. 9. Conduction power loss of (a) traditional HB-MMC and (b) AHPL-MMC.

$$= \frac{2N_{\mathrm{DS}}V_f I_m}{\pi}. \tag{35}$$

For each HBSM in phase b, one of the two switches is always conducting, regardless of the current direction and the states of the HBSM. Taking the upper HB-WSC as an example, its power loss can be calculated as

$$P_{\text{HB-WSC}} = N_{\mathrm{HBSM}}V_F \times \frac{1}{T}\int_0^{2\pi/\omega} |i_{\mathrm{U}b}|\,dt \approx \frac{N_{\mathrm{HBSM}}V_F I_m}{4\pi} \begin{bmatrix} 3\sqrt{16-9M^2(\cos\varphi)^2} - \sqrt{3}\sqrt{16-M^2\pi^2(\cos\varphi)^2} \\ +9M\cos(\varphi)\arcsin(3/4 M\cos\varphi) \\ +9M\arccos(1/4\pi M\cos\varphi)\cos\varphi - 4\pi M\cos\varphi \end{bmatrix}. \tag{36}$$

Therefore, the total power loss of the three-phase legs in AHPL-MMC can be expressed as

$$P_{\mathrm{Loss}} = 2\left(P_{\text{FB-WSC}} + P_{\mathrm{DS}} + P_{\text{HB-WSC}}\right). \tag{37}$$

For traditional HB-MMC, the power loss of each bridge arm is the same. Taking the upper bridge arm in phase a as an example, the power loss can be calculated as

$$P_{\text{HB-WSC}}^{\text{HB-MMC}} = N_{\mathrm{HBSM}}V_F \times \frac{1}{T}\int_0^{2\pi/\omega} \left|\frac{I_{\mathrm{DC}}}{3} + \frac{1}{2}I_m\sin(\omega t+\varphi)\right| dt = \frac{N_{\mathrm{HBSM}}V_F I_m}{2\pi} \begin{bmatrix} 2\sqrt{1-(1/2 M\cos\varphi)^2} + \\ M\cos\varphi\arcsin(1/2 M\cos\varphi) \end{bmatrix}. \tag{38}$$

Therefore, the total power loss of the HB-MMC is

$$P_{\mathrm{Loss}}^{\text{HB-MMC}} = 6P_{\text{HB-MMC}}^{\text{HB-WSC}}. \tag{39}$$

For the H-MMC utilizing 50% FBSMs, the power loss is 1.5 times greater than that of the HB-MMC. Based on the system parameters and assuming V_{F} is 2V, the power losses of the HB-MMC and the AHPL-MMC can be calculated under various power factor angles and modulation indices, as illustrated in Fig. 9. At the rated operating point ($M = 0.9$ and $\varphi = 0$), the conduction loss of the HB-MMC is 0.527 MW, while the conduction loss of AHPL-MMC is 1.098 MW, which is approximately 2.08 times greater. The primary reason for the increased conduction loss in AHPL-MMC is that both phases a and c utilize FBSMs

and DSs. This configuration results in a longer flow path for the ac currents, leading to higher power losses. However, in comparison to the H-MMC with blocking capability, the power loss of the AHPL-MMC is increased by only 38.9%.

C. Cost and Volume

Accurately calculating the cost and volume of new MMC topologies is difficult due to the significant variations in the size and cost of essential components, which are greatly influenced by different types, parameters, and manufacturers. Currently, approximate estimation methods are mainly used. For instance, in [30] and [31], the authors select specific types of IGBT switches and SM capacitors to calculate the actual costs and volumes of various MMC topologies, based on their sale prices and data sheets. In [32] and [33], the authors calculate the per unit values of volume and cost for the new topologies, based on the proportional relationship of component consumption. This article also employs the per-unit method. Since the SM capacitance and the switch current stress in the proposed AHPL-MMC differ from those in the HB-MMC, a correction coefficient related to the RMS current is introduced.

The cost and volume of SM capacitors are influenced by factors such as capacitance, the number of SMs, and the RMS current. It can be approximated that the cost and volume of SM capacitors in the AHPL-MMC are $K_{\rm cap}$ times greater than those in the HB-MMC. The $K_{\rm cap}$ is given by

$$K_{\rm cap}=\frac{2N_{\rm FBSM}C_{\rm FBSM}I_{\rm FB}+2N_{\rm HBSM}C_{\rm HBSM}I_{\rm HB}}{6N_{\rm HBSM}^{\rm HB\text{-}MMC}C_{\rm HBSM}^{\rm HB\text{-}MMC}I_U}. \tag{40}$$

The cost of switches is influenced by both the number of switches and their RMS current, while the volume is directly related to the number of switches. It can be approximated that the cost of the switches in the AHPL-MMC is $K_{\rm sw1}$ times that of the HB-MMC, and its volume is $K_{\rm sw2}$ times greater. The $K_{\rm sw1}$ and $K_{\rm sw2}$ are given by

$$K_{\rm sw1}=\frac{4N_{\rm DS}I_{\rm DS}+8N_{\rm FBSM}I_{\rm FB}+4N_{\rm HBSM}I_{\rm HB}}{6N_{\rm HBSM}^{\rm HB\text{-}MMC}I_U} \tag{41}$$

$$K_{\rm sw2}=\frac{4N_{\rm DS}+8N_{\rm FBSM}+4N_{\rm HBSM}}{6N_{\rm HBSM}^{\rm HB\text{-}MMC}}. \tag{42}$$

The cost and volume of the bridge arm inductor are influenced by the inductance value, the number of inductors, and the RMS current. It can be approximated that the cost and volume of the bridge arm inductor in AHPL-MMC are $K_{\rm ba}$ times greater than those in HB-MMC. The $K_{\rm ba}$ is given by

$$K_{\rm ba}=\frac{2L_{\rm arm}I_{\rm DC}}{6L_{\rm arm}^{\rm HB\text{-}MMC}I_U}. \tag{43}$$

The cost and volume of the valve's cooling system are directly related to the power loss of the switches. It can be estimated that the cost and volume of the cooling system for the AHPL-MMC are 1.5 times greater than those of the HB-MMC. Given that the AHPL-MMC possesses dc fault-blocking capability, there is no requirement for a dc circuit breaker, resulting in zero associated costs and volume. Aside from these distinctions, the costs and volumes of the dc smoothing reactors, ac transformers (including ac filters), and other equipment (such as switching equipment, starting resistors, etc.) for both AHPL-MMC and HB-MMC are similar.

TABLE IV
PER-UNIT COST AND VOLUME COMPARISON OF THE HB-MMC, H-MMC, AND AHPL-MMC

Items	HB-MMC		H-MMC		AHPL-MMC	
	Cost	Volume	Cost	Volume	Cost	Volume
Capacitor in valve	0.15	0.27	0.15	0.27	0.093	0.168
Switch in valve	0.21	0.12	0.315	0.18	0.384	0.152
Cooling system	0.02	0.07	0.03	0.105	0.03	0.105
Bridge arm inductor	0.06	0.17	0.06	0.17	0.011	0.031
Smoothing reactors	0.04	0.05	0.04	0.05	0.04	0.05
DC breaker	0.30	0.03	0	0	0	0
AC transformer & filter	0.06	0.09	0.06	0.09	0.06	0.09
Others	0.16	0.20	0.16	0.20	0.16	0.2
TOTAL	1.00	1.00	0.815	1.065	0.778	0.796

In contrast to the HB-MMC, the H-MMC exhibits differences in the number of switches and associated power losses. Furthermore, dc circuit breakers are not necessary. The cost and volume of the remaining components align with those of the HB-MMC.

Substituting the rated system parameters into (40)–(43), we can obtain $K_{\rm cap}=0.621$, $K_{\rm sw1}=0.183$, $K_{\rm sw2}=1.27$, and $K_{\rm ba}=0.184$. Columns 2 and 3 of Table IV present the cost and volume proportions of each key component in a typical HB-MMC [32], [34], while columns 4, 5 and 6, 7 display the calculated per-unit value of cost and volume for the H-MMC and the proposed AHPL-MMC, respectively. In comparison to the HB-MMC, the AHPL-MMC exhibits an increase in both the cost of switches and the volume of the cooling system. However, there is a notable reduction in the cost and volume of the SM capacitor and bridge arm inductor. Consequently, the overall cost of the AHPL-MMC can be reduced by 22.2%, while its volume can be decreased by 20.4%. When compared to the H-MMC, the proposed AHPL-MMC demonstrates a cost reduction of 4.54% and a volume reduction of 25.26%.

V. CONTROL STRATEGY

The overall control structure of the AHPL-MMC is illustrated in Fig. 10(a), which mainly contains five parts. The typical ac current inner-loop control (in dq frame) is applied to calculate the three-phase modulation signal v_a^*,v_b^*, and v_c^*. The modeling and design of this loop is mature, and thus will not be discussed in this article. The closed-loop energy balancing of phases a and c is applied to generate the lagging phase angles α_a and α_c. The closed-loop energy balancing of phase b is applied to generate the dc current reference, which is subsequently tracked by an inner dc current loop, ultimately obtaining the reference common-mode voltage $v_{\rm PN}^*$. A more detailed discussion on the design and modeling of these loops will follow. The modulator is responsible for generating the switching signals for both the SMs and DSs. The detailed modulation scheme is presented in Fig. 10(b). The reference output voltage of each FB-WSC and HB-WSC, namely $v_{\rm HBU}^*$, $v_{\rm HBL}^*$, $v_{{\rm FB}a}^*$, and $v_{{\rm FB}c}^*$, can be calculated based on (6) and (11), respectively. According to (2), the driving pulse of the DS can be generated by utilizing the α_a, α_c, and the

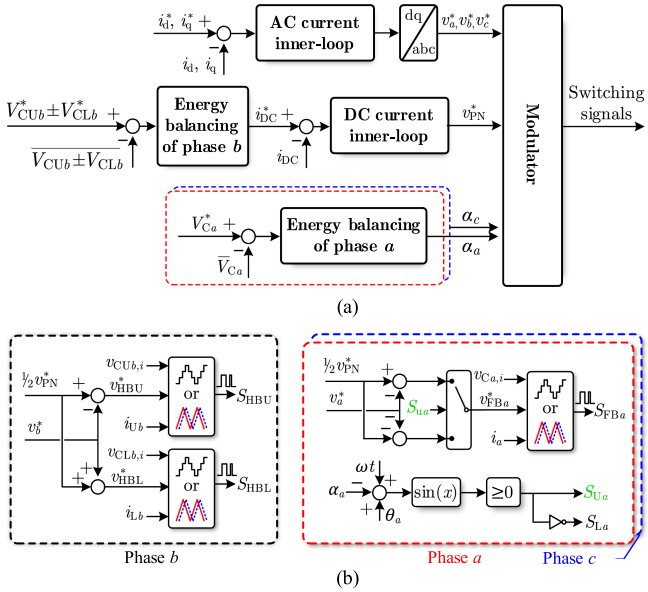

Fig. 10. Control strategies of the AHPL-MMC. (a) Overall structure. (b) Detail of the modulator block.

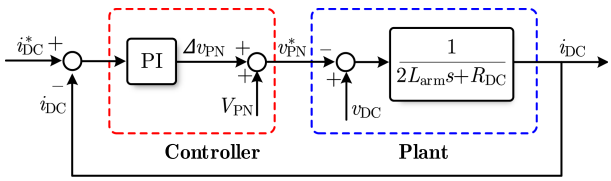

Fig. 11. Control strategy of the DC current.

synchronization signal ωt that is calculated by the phase-locked-loop of the ac voltage.

To achieve individual capacitor voltage balancing in each FB-WSC and HB-WSC, different low-level modulation and control methods can be applied depending on the number of SMs. For example, the nearest level modulation (NLM) with capacitor voltage sorting method [17] can be used for a large number of SMs, while the carrier-phase-shift pulsewidth modulation (CPS-PWM) with modulation signal compensation method [21], [35] can be used for a small number of SMs.

A. DC Current Inner Loop

From (8), by controlling the common-mode voltages of the upper and lower HB-WSCs, the dc current can be effectively adjusted. Fig. 11 shows the control strategy of the dc current, where a typical proportional-integral (PI) controller is utilized. The open-loop transfer function $G_{\text{open}}(s)$ can be expressed as

$$G_{\text{open}}(s) = -\frac{k_p s + k_i}{s} \times \frac{1}{2L_{\text{arm}} s + R_{\text{DC}}}. \tag{44}$$

Applying the pole-zero cancellation method, we can obtain

$$\frac{k_p}{k_i} = \frac{R_{\text{DC}}}{2L_{\text{arm}}}, \omega_c = \frac{-k_p}{2L_{\text{arm}}} \Rightarrow k_p = -2L_{\text{arm}}\omega_c, k_i = -\frac{4L_{\text{arm}}^2 \omega_c}{R_{\text{DC}}} \tag{45}$$

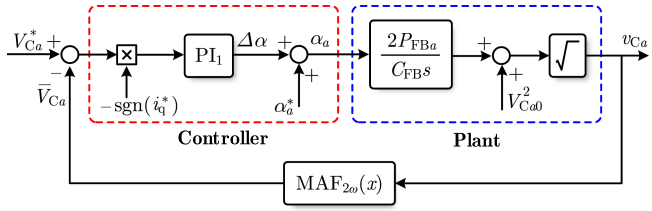

Fig. 12. Energy balance control strategy of the hybrid phase leg in phase a.

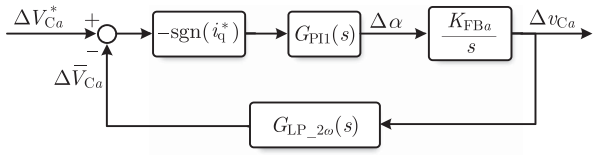

Fig. 13. Small-signal model for energy balance control of the hybrid phase leg in phase a.

where ω_c is the crossover angular frequency, which is selected as 1000π rad/s in this paper. Substituting $L_{\text{arm}} = 17e^{-3}$H and $R_{\text{DC}} = 0.5\ \Omega$ into (45), we can obtain $k_p = -106.8$ and $k_i = -1570.1$. The stability of the dc current control loop is evident, as it maintains a phase angle margin of 90° across the entire frequency spectrum.

B. Energy Balancing of Phases a and c

This article employs an averaging method over the fundamental period to analyze the energy-to-total-capacitor-voltage characteristics of the phase leg in phase a. Based on the accumulated energy $W_{\text{FB}a}$, the average power $P_{\text{FB}a}$ can be expressed as

$$P_{\text{FB}a} = \frac{W_{\text{FB}a}}{T} = \frac{I_m V_{\text{PN}}}{\pi} \cos(\alpha_a + \varphi) - \frac{V_m \cos(\varphi)}{2}. \tag{46}$$

Using average power to replace instantaneous power, then (15) can be rewritten as

$$\bar{V}_{\text{C}a} = \sqrt{\frac{2}{C_{\text{FB}}} \int P_{\text{FB}a} \mathrm{d}t + V_{\text{C}a0}^2}. \tag{47}$$

Fig. 12 illustrates the energy balance control strategy of the hybrid phase leg in phase a. To enhance the response speed and stability of the energy balance control during sudden changes in the power factor angle φ, the theoretical steady-state value of the lagging phase angle α_a^* is implemented as feedforward, which is calculated by (19) with $\varphi^* = \arctan(i_{\text{q}}^*/i_{\text{d}}^*)$ as the input.

Since the practical total capacitor voltage $v_{\text{C}a}$ contains low-frequency pulsation dominated by the second harmonic, the moving average filter (MAF) with a time window of $T_0 = \pi/\omega$ can be used to extract the dc component $\bar{V}_{\text{C}a}$ and feed it back to the controller input.

Applying the linearization method to Fig. 12, the small signal model shown in Fig. 13 can be obtained. The first-order low-pass filter $G_{\text{LP\_2}\omega}(s)$ is used to approximately replace the $\text{MAF}_{2\omega}(x)$ block, which is given by

$$G_{\text{LP\_2}\omega}(s) = \frac{0.3 \times 2\omega}{s + 0.3 \times 2\omega}. \tag{48}$$

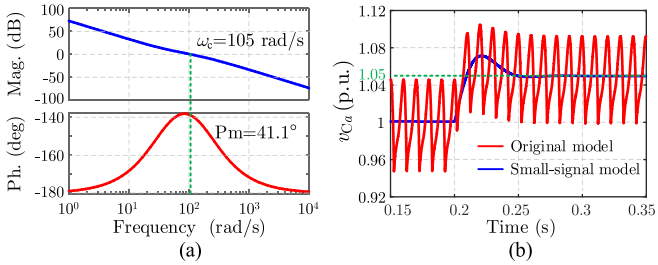

Fig. 14. Test results of energy balance control of the hybrid phase leg in phase *a*. (a) Open-loop Bode diagram of the small signal model. (b) Step response comparison.

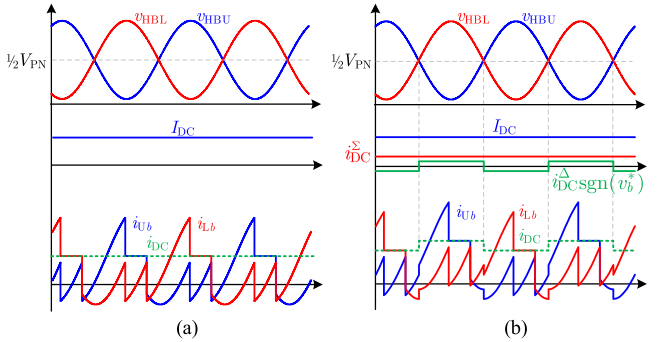

Fig. 15. Schematic diagram of the current injection method. (a) Before the current injection. (b) After the current injection.

$K_{\mathrm{FB}a}$ represents the proportional coefficient of the Plant after linearization, which is given by

$$K_{\mathrm{FB}a} = \frac{-2I_m V_{\mathrm{PN}} \sin(\alpha_a^* + \varphi^*)}{\pi C_{\mathrm{FB}}} \times \frac{1}{2V_{\mathrm{C}a0}}. \tag{49}$$

It can be observed from (49) that the polarity of $K_{\mathrm{FB}a}$ is influenced by the sign of I_m and the sign of $\sin(\alpha_a^* + \varphi^*)$. According to the relationship between φ and α depicted in Fig. 4, it is evident that the signs of α_a^* and φ^* are identical, and their absolute values both lie within the range of $[0, \pi/2]$. It can be inferred that if $\varphi^* > 0$, then $\sin(\alpha_a^* + \varphi^*) > 0$; otherwise, $\sin(\alpha_a^* + \varphi^*) < 0$. Furthermore, φ^* is associated with the active and reactive current references in the *dq* frame, namely i_{d}^* and i_{q}^*, and the sign of I_m corresponds to the sign of the active current reference i_d^*. Thus, upon simplification, it can be concluded that the polarity of $K_{\mathrm{FB}a}$ ultimately depends solely on the sign of i_q^*. Specifically, when $i_q^* > 0$, $K_{\mathrm{FB}a}$ is less than 0, and when $i_q^* < 0$, $K_{\mathrm{FB}a}$ is greater than 0. Given the variable polarity characteristics of $K_{\mathrm{FB}a}$, a proportional item with a value of $-\mathrm{sgn}(i_q^*)$ should be series into the forward channel of the control block shown in Figs. 12 and 13, ensuring that the feedback control remains negative.

Taking $i_q^* > 0$ as an example for analysis, according to Fig. 13, the open-loop transfer function $G_{\mathrm{open1}}(s)$ can be expressed as

$$G_{\mathrm{open1}}(s) = \frac{k_{p1}s + k_{i1}}{s} \times \frac{I_m V_{\mathrm{PN}} \sin(\alpha_a^* + \varphi^*)}{\pi V_{\mathrm{C}a0} C_{\mathrm{FB}} s} \times \frac{0.3 \times 2\omega}{s + 0.3 \times 2\omega} \tag{50}$$

where k_{p1} and k_{i1} represent the proportional and integral constants, respectively. Utilizing the tuning method for a typical type-II system [36] and assuming the bandwidth h is equal to 5, the PI controller parameters can be calculated as

$$k_{\mathrm{p1}} = \frac{1}{3} \times \frac{1.08\omega\pi V_{\mathrm{C}a0} C_{\mathrm{FB}}}{I_m V_{\mathrm{PN}} \sin(\alpha_a^* + \varphi^*)}, k_{i1} = \frac{\omega}{25} \times \frac{1.08\omega\pi V_{\mathrm{C}a0} C_{\mathrm{FB}}}{I_m V_{\mathrm{PN}} \sin(\alpha_a^* + \varphi^*)}. \tag{51}$$

Substituting the system parameters $V_{\mathrm{C}a0} = 182.222\mathrm{kV}$ ($N_{\mathrm{FBSM}} \times V_{\mathrm{CN}}$), $C_{\mathrm{FB}} = 4.043e^{-5}\mathrm{F}$, $\alpha_a^* = 0.78565$ rad, and $\varphi^* = 1e^{-4}$rad into (51), we can obtain $k_{\mathrm{p1}} = 1.850e^{-5}$and $k_{i1} = 6.975e^{-4}$. The open-loop Bode is presented in Fig. 14(a). The crossover angular frequency is 105 rad/s, and the phase angle margin is 41.1°, indicating that the system is stable. Fig. 14(b) presents the test results of the total capacitor voltages of the FB-WSC in phase *a*, with the reference stepping from 1 p.u. to 1.05 p.u. at $t = 0.2$ s. Two models, the original model and the small signal model, exhibit similar trends during the transient state.

C. Energy Balancing of Phase b

Equations (20) and (21) demonstrate that, under ideal conditions, the energy of the phase leg in phase *b* is inherently balanced. However, this proof does not account for system losses and parameter deviations. Consequently, in practical applications, it remains essential to implement a closed-loop controller to sustain the dynamic energy balance of the phase leg in phase *b*. From (20) and (21), it is evident that the total capacitor voltage of the HB-WSC is influenced by the parameters v_{PN}, i_{DC}, V_m, and I_m. Theoretically, the energy balance can be achieved by adjusting any of these four variables. In this study, i_{DC} is chosen as the control variable.

Assuming the dc current is controlled to be

$$i_{\mathrm{DC}} = I_{\mathrm{DC}} + i_{\mathrm{DC}}^{\sum} + i_{\mathrm{DC}}^{\Delta}\mathrm{sgn}(v_b^*) \tag{52}$$

where $i_{\mathrm{DC}}^{\sum}$ and $i_{\mathrm{DC}}^{\Delta}\mathrm{sgn}(v_b^*)$ are newly injected current components. I_{DC} is the original dc current calculated according to the power conservation (13). Fig. 15 illustrates the current waveforms of the branch current of the upper and lower bridge arm in phase *b*, namely $i_{\mathrm{U}b}$ and $i_{\mathrm{L}b}$, before and after the current injection.

After the current injection, the accumulated energy of the upper and lower HB-WSCs over a fundamental period can be recalculated as

$$W_{\mathrm{HBU}} = \int_{\alpha_a/\omega}^{(2\pi+\alpha_a)/\omega} v_{\mathrm{HBU}} i_{\mathrm{U}b} \mathrm{d}t = \frac{2\pi}{\omega}\left[\frac{\left(I_{\mathrm{DC}} + i_{\mathrm{DC}}^{\sum}\right) v_{\mathrm{PN}}}{2} - \frac{3V_m I_m \cos\varphi}{4} - \frac{2i_{\mathrm{DC}}^{\Delta} V_m}{\pi}\right] \tag{53}$$

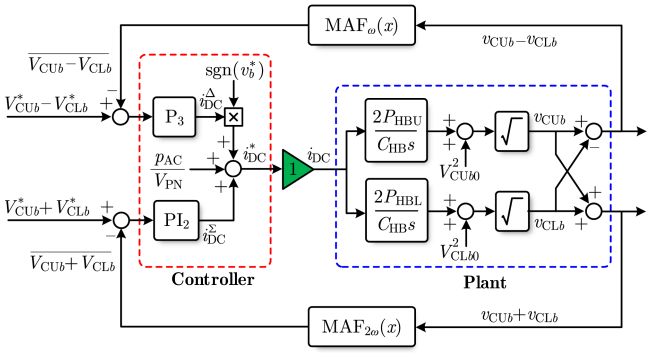

Fig. 16. Energy balance control strategy of upper and lower bridge arms in phase b.

$$W_{\mathrm{HBL}} = \int_{\alpha_a/\omega}^{(2\pi+\alpha_a)/\omega} v_{\mathrm{HBL}} i_{\mathrm{L}b} \mathrm{d}t = \frac{2\pi}{\omega}\left[\frac{\left(I_{\mathrm{DC}} + i^{\Sigma}_{\mathrm{DC}}\right) v_{\mathrm{PN}}}{2} - \frac{3V_m I_m \cos\varphi}{4} + \frac{2i^{\Delta}_{\mathrm{DC}} V_m}{\pi}\right]. \tag{54}$$

Thus, we can obtain

$$W_{\mathrm{HBU}} + W_{\mathrm{HBL}} = 2\pi i^{\Sigma}_{\mathrm{DC}} v_{\mathrm{PN}}/\omega \tag{55}$$

$$W_{\mathrm{HBU}} - W_{\mathrm{HBL}} = -8 i^{\Delta}_{\mathrm{DC}} V_m/\omega. \tag{56}$$

It can be observed from (55) and (56) that the total energy of the upper and lower bridge arms of phase b is solely dependent on the current component i^{Σ}_{DC}, while the differential energy between the upper and lower bridge arms is solely related to the current component $i^{\Delta}_{\mathrm{DC}}\mathrm{sgn}(v_b^*)$. Consequently, i^{Σ}_{DC} can be utilized to regulate the total energy balance of the upper and lower bridge arms, whereas $i^{\Delta}_{\mathrm{DC}}\mathrm{sgn}(v_b^*)$ can be employed to manage the energy balance difference between these arms.

Similar to phase a, we apply an averaging method over the fundamental period to model the energy-to-total-capacitor-voltage characteristics of the bridge arms in phase b. By utilizing average power instead of instantaneous power, the total capacitor voltages $v_{\mathrm{CU}b}$ and $v_{\mathrm{CL}b}$ of the HB-WSC, as described by (16) and (17), can be rewritten as

$$\bar{V}_{\mathrm{CU}b} = \sqrt{\frac{2}{C_{\mathrm{HB}}}\int \frac{W_{\mathrm{HBU}}}{T}\mathrm{d}t + V^2_{\mathrm{CU}b0}} \tag{57}$$

$$\bar{V}_{\mathrm{CL}b} = \sqrt{\frac{2}{C_{\mathrm{HB}}}\int \frac{W_{\mathrm{HBL}}}{T}\mathrm{d}t + V^2_{\mathrm{CL}b0}}. \tag{58}$$

Fig. 16 shows the energy balance control strategy of the upper and lower bridge arms in phase b. The $v_{\mathrm{CU}b}+v_{\mathrm{CL}b}$ primarily comprises the second harmonic, so an MAF with a time window of $T_0 = \pi/\omega$ is used to extract the dc component $\overline{V_{\mathrm{CU}b}+V_{\mathrm{CL}b}}$. Conversely, $v_{\mathrm{CU}b}-v_{\mathrm{CL}b}$ predominantly contains the fundamental frequency component, so an MAF with a time window of $T_0 = 2\pi/\omega$ to extract the dc component $\overline{V_{\mathrm{CU}b}-V_{\mathrm{CL}b}}$. As can be seen

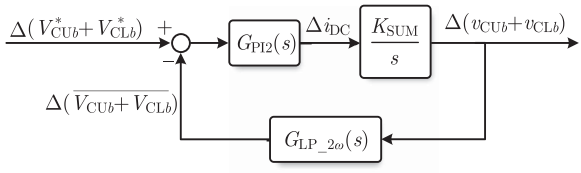

Fig. 17. Small signal model of the total energy balance of the upper and lower bridge arms in phase b.

from Fig. 16, the dc current reference value consists of three parts.

1) The output of the total energy balance control (PI$_2$) of the upper and lower bridge arms, namely i^{Σ}_{DC}.
2) The output of the differential energy balance control (P_3) of the upper and lower bridge arms, namely $i^{\Delta}_{\mathrm{DC}}\mathrm{sgn}(v_b^*)$.
3) The feedforward term, which is calculated by $p_{\mathrm{AC}}/V_{\mathrm{PN}}$. At steady state, $p_{\mathrm{AC}}/V_{\mathrm{PN}} = I_{\mathrm{DC}}$.

It should be noted that the bandwidth of the dc current inner loop (see Fig. 11) is significantly larger than that of the bridge arm energy balance control. Therefore, it can be assumed that the actual i_{DC} is always equal to its reference value i^*_{DC}, so a unit proportional link (indicated by the green triangle) is used to replace the dc current inner loop in Fig. 16.

Since the control effects of i^{Σ}_{DC} and $i^{\Delta}_{\mathrm{DC}}\mathrm{sgn}(v_b^*)$ are decoupled from each other, the total energy balance loop and differential energy balance loop, as shown in Fig. 16, can be linearized independently, allowing for the design of the controller parameters. By assuming $i^{\Delta}_{\mathrm{DC}} = 0$ and substituting this value into (57)–(58) and Fig. 16, a small signal model for the total energy balance path can be derived after linearization, as depicted in Fig. 17. Similarly, the low-pass filter $G_{\mathrm{LP\_2}\omega}(s)$ is utilized in place of the moving average filter MAF$_{2\omega}(x)$. K_{SUM} represents the proportional coefficient of the linearized Plant, which can be calculated as

$$K_{\mathrm{SUM}} = \frac{V_{\mathrm{PN}}}{2C_{\mathrm{HB}}}\left(\frac{1}{V_{\mathrm{CU}b0}} + \frac{1}{V_{\mathrm{CL}b0}}\right) = \frac{V_{\mathrm{PN}}}{V_{\mathrm{C}b0}C_{\mathrm{HB}}}. \tag{59}$$

According to Fig. 17, the open-loop transfer function $G_{\mathrm{open2}}(s)$ can be expressed as

$$G_{\mathrm{open2}}(s) = \frac{k_{p2}s + k_{i2}}{s} \times \frac{V_{\mathrm{PN}}}{V_{\mathrm{C}b0}C_{\mathrm{HB}}s} \times \frac{0.3\times 2\omega}{s + 0.3\times 2\omega} \tag{60}$$

where k_{p2} and k_{i2} represent the proportional and integral constants, respectively. Utilizing the tuning method for a typical type-II system [36], the proportional and integral constants can be calculated as

$$k_{p2} = \frac{1}{3}\times\frac{1.08\omega V_{\mathrm{C}b0}C_{\mathrm{HB}}}{V_{\mathrm{PN}}}, k_{i2} = \frac{\omega}{25}\times\frac{1.08\omega V_{\mathrm{C}b0}C_{\mathrm{HB}}}{V_{\mathrm{PN}}}. \tag{61}$$

Substituting the system parameters $V_{\mathrm{C}b0} = 200$ kV ($N_{\mathrm{HBSM}}\times V_{\mathrm{CN}}$) and $C_{\mathrm{HB}} = 4.012e^{-5}$F into (61), we can obtain $k_{\mathrm{p2}} = 4.537e^{-3}$and $k_{i2} = 0.171$. The open-loop Bode diagram is presented in Fig. 18(a). The crossover angular frequency is 105 rad/s, and the phase angle margin is 41.1°, indicating that the system is stable. Fig. 18(b) presents the simulation results of $v_{\mathrm{CU}b}+v_{\mathrm{CL}b}$, with its reference stepping from 1 to 1.05 p.u.

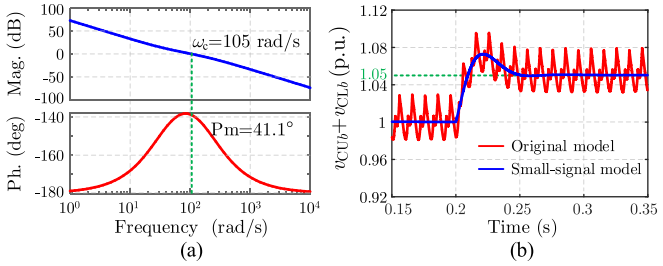

Fig. 18. Test results of total energy balance control of upper and lower bridge arm in phase *b*. (a) Open-loop Bode diagram of the small signal model. (b) Step response comparison.

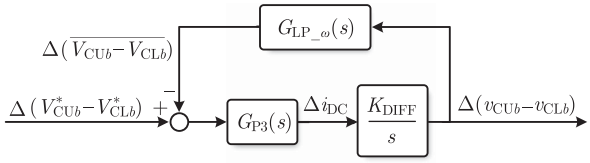

Fig. 19. Small signal model of the differential energy balance of the upper and lower bridge arms in phase *b*.

at $t = 0.2$ s. It is evident that the original model and the small signal model have similar trends of response.

By assuming $i_{\mathrm{DC}}^{\Sigma} = 0$ and substituting this value into (57)–(58) and Fig. 16, a small signal model for the differential energy balance path can be derived after linearization, as depicted in Fig. 19. Similarly, the low-pass filter $G_{\mathrm{LP\_}\omega}(s)$ is utilized in place of the Moving average filter $\mathrm{MAF}_{\omega}(x)$, which is given by

$$G_{\mathrm{LP\_}\omega}(s) = \frac{0.3 \times \omega}{s + 0.3 \times \omega}. \tag{62}$$

K_{DIFF} represents the proportional coefficient of the linearized Plant, which is

$$K_{\mathrm{DIFF}} = \frac{-2V_m}{\pi C_{\mathrm{HB}} V_{\mathrm{CUb0}}} - \frac{2V_m}{\pi C_{\mathrm{HB}} V_{\mathrm{CLb0}}} = \frac{-4V_m}{\pi C_{\mathrm{HB}} V_{\mathrm{Cb0}}}. \tag{63}$$

According to Fig. 19, the open-loop transfer function $G_{\mathrm{open3}}(s)$ can be expressed as

$$G_{\mathrm{open3}}(s) = k_{p3} \times \frac{-4V_m}{\pi C_{\mathrm{HB}} V_{\mathrm{Cb0}} s} \times \frac{0.3 \times \omega}{s + 0.3 \times \omega} \tag{64}$$

where k_{p3} represents the proportional constants of the P_3 controller. Utilizing the tuning method for a typical type-I system [36] and assuming the damping ratio ξ is 0.707, the proportional constants can be calculated as

$$k_{p3} = -\frac{0.3\omega\pi C_{\mathrm{HB}} V_{\mathrm{Cb0}}}{8V_m}. \tag{65}$$

Substituting the system parameters $V_{\mathrm{Cb0}} = 200$ kV and $C_{\mathrm{HB}} = 4.012\ e^{-5}$F into (65), we can obtain $k_{\mathrm{p3}} = -3.299e^{-3}$. The open-loop Bode diagram of Fig. 19 is presented in Fig. 20(a). The crossover angular frequency is 42.9 rad/s, and the phase angle margin is 65.5°, indicating that the system is stable. Fig. 20(b) presents the simulation results of $v_{\mathrm{CU}b} - v_{\mathrm{CL}b}$, with its reference stepping from 0 to 0.05 p.u. at $t = 0.2$ s. The original model and the small signal model also have similar results. These test results validate the correctness and effectiveness of

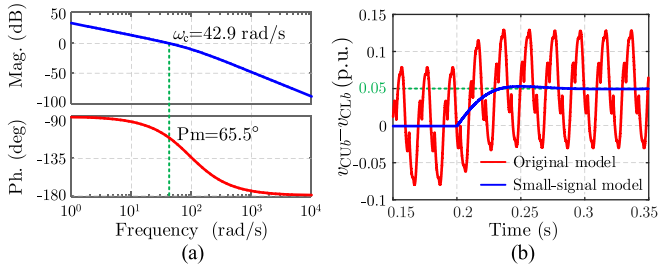

Fig. 20. Test results of differential energy balance control of upper and lower bridge arm in phase *b*. (a) Open-loop Bode diagram of the small signal model. (b) Step response comparison.

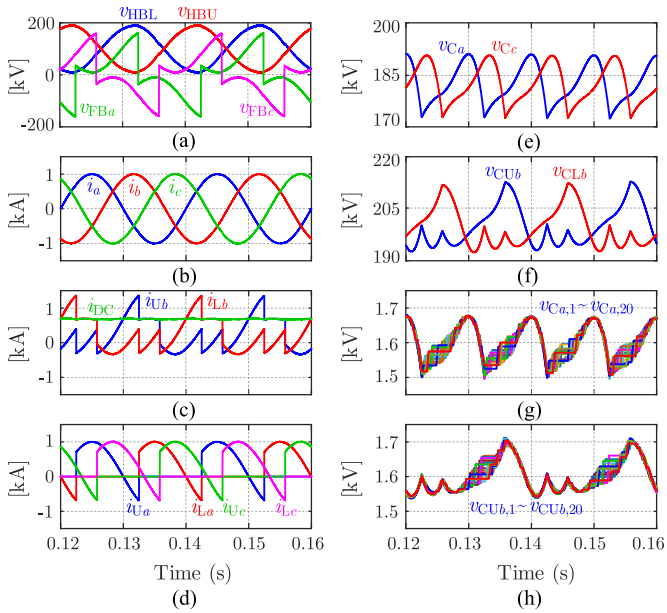

Fig. 21. Steady-state simulation results of AHPL-MMC. (a) Branch voltages of the FB-WSCs and HB-WSCs. (b) Three-phase AC currents. (c) DC current and branch current of bridge arm in phases *b*. (d) Branch current of bridge arm in phases *a* and *c*. (e) Total capacitor voltage of FB-WSC in phases *a* and *c*. (f) Total capacitor voltage of upper and lower HB-WSCs in phase *b*. (g) Part of capacitor voltages of FBSMs in phase *a*. (h) Part of capacitor voltages of upper HBSMs in phase *b*.

the small signal model, the parameter design method, and the control strategy.

VI. Simulation and Experimental Verification

A. Simulation Results

To better illustrate the principle of the proposed topology and control method, simulation cases were performed for the AHPL-MMC. The main circuit parameters are listed in Tables II and III. Since hundreds of SMs are applied, the NLM with capacitor voltage sorting method is applied for low-level capacitor voltage balancing control in the simulation.

Fig. 21 illustrates the steady-state simulation results of the AHPL-MMC operating at unity power factor. As can be seen in Fig. 21(a)–(d), the ac currents exhibit nearly pure sine wave characteristics, while the branch voltages and currents of the FB-WSC and HB-WSC closely align with the theoretical values

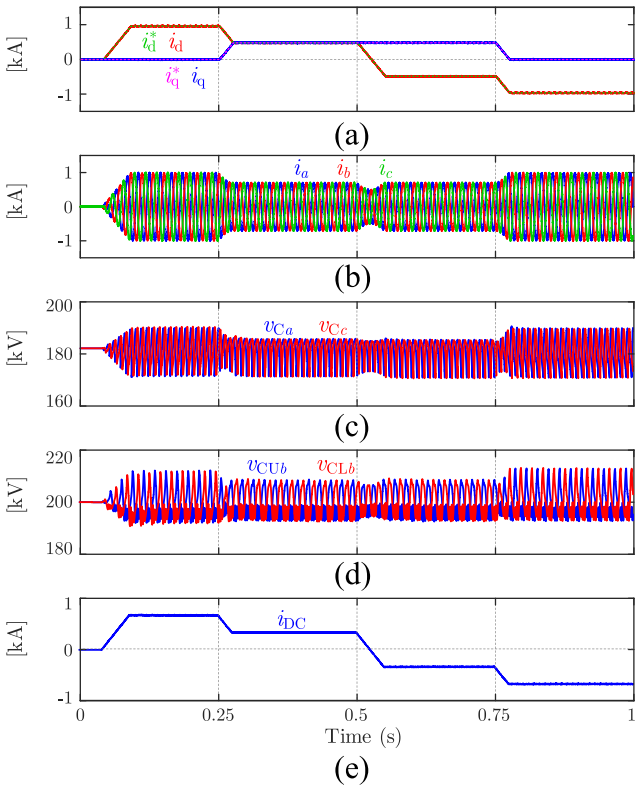

Fig. 22. Dynamic response to the change in active and reactive current. (a) Active and reactive current. (b) Three-phase AC currents. (c) Total capacitor voltage of FB-WSCs in phases a and c. (d) Total capacitor voltage of upper and lower FB-WSCs in phase b. (e) DC current.

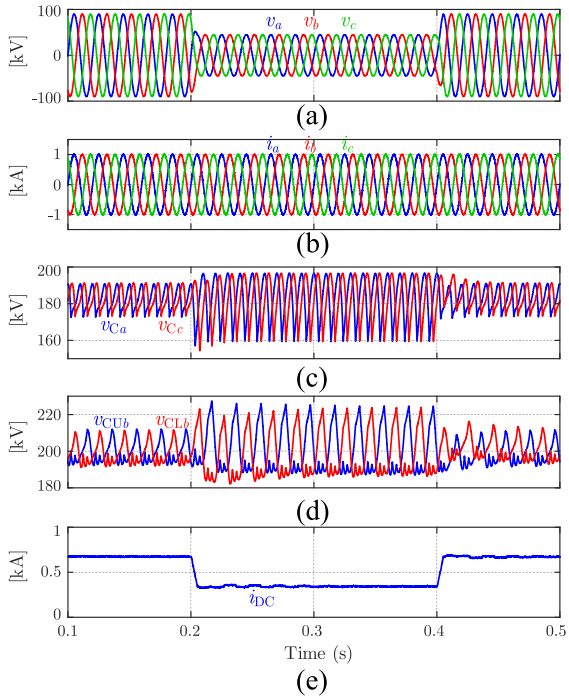

Fig. 23. Simulation results under symmetrical AC voltage sags. (a) Three-phase AC voltages. (b) Three-phase AC currents. (c) Total capacitor voltage of FBSMs in phases a and c. (d) Total capacitor voltage of upper and lower HBSMs in phase b. (e) DC current.

depicted in Fig. 3. In Fig. 21(e) and (f), the total capacitor voltages of the FB-WSC and HB-WSC are approximately 182.22 and 200 kV, respectively. Their peak-to-average voltage ripple are 9.05 kV and 9.95 kV, respectively, which closely match the design specification of 5%. Fig. 21(d) and (e) shows the voltages of the partial SM capacitors in phase a and in the upper bridge arm of phase b. The capacitor voltage sorting control ensures that the voltage of each SM capacitor fluctuates slightly around its nominal value of 1.6 kV.

The simulation results of the AHPL-MMC when changing the reference of the active and reactive ac current ($i^*{}_d$ and $i^*{}_q$) are shown in Fig. 22. It can be observed in Fig. 22(c) and (d) that the total capacitor voltages of the FB-WSCs and HB-WSCs respectively remain close to their nominal values. The transient time is small and the balancing performance is satisfactory, confirming the effectiveness of the proposed bridge arm energy balancing method. Besides, the dc current varies along with the active current and always exhibits a small current ripple, as shown in Fig. 22(e).

Fig. 23 illustrates the simulation results of the AHPL-MMC under symmetrical ac voltage sags. The ac voltages drop to 50% at $t = 0.2$ s and return to normal at $t = 0.4$ s. The active and reactive current references remain constant during this period. Fig. 23(b)–(d) demonstrates the smooth transients of the ac currents, and the maintenance of nominal values for the total capacitor voltage of the FB-WSCs and HB-WSCs, with a response time of less than 0.1 s. In Fig. 23(e), the dc current is reduced by approximately 50% during the sag period, while still maintaining minimal current ripple.

Fig. 24 presents the simulation results of the AHPL-MMC under a pole-to-pole dc fault. The dc voltage drops to 0 kV at $t = 0.3$ s and subsequently recovers to 200 kV at $t = 0.35$ s. When the converter detects that the fault current exceeds the allowable limit or that the total capacitor voltages of each WSC deviate from their normal operational range, all driven signals are blocked. It is observed from Fig. 24(d) that the fault current rapidly decreases to zero after blocking. Once the fault is cleared, the converter can be restored to its rated operating status.

B. Experimental Results

To further verify the functionality of the proposed topology, a scaled-down experimental prototype was constructed, as illustrated in Fig. 25. The dc voltage is 100 V, while the rated ac peak voltage stands at 45 V. The converter operates in inverter mode with a load resistance of 20 Ω connected on the ac side. Each FB-WSC and HB-WSC comprises two series SMs with nominal capacitor voltages of 50 V and 46 V, respectively. The capacitance of all SM capacitors is 1.8 mF. Both the ac and dc filtering inductors have a value of 3 mH. Due to the reduced number of SMs used, the CPS-PWM with modulation signal compensation is employed for low-level capacitor voltage balancing control. The switching frequency is set at 10 kHz and the control period is set at 100 μs. The part numbers of

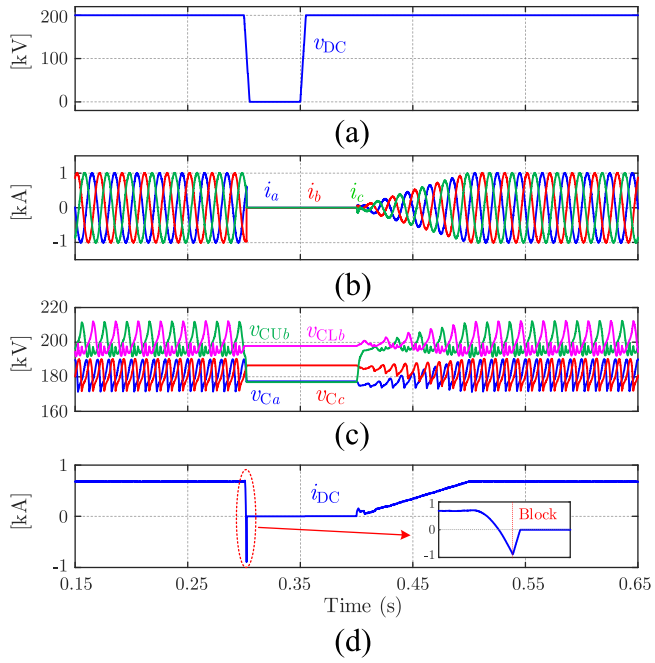

Fig. 24. Simulation results under a pole-to-pole DC fault. (a) DC voltage. (b) Three-phase AC currents. (c) Total capacitor voltages of each WSC. (d) DC current.

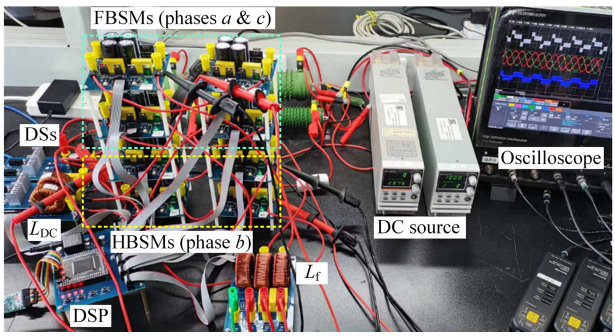

Fig. 25. Experimental prototype of the AHPL-MMC.

TABLE V
KEY COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Components	Description
MOSFETs of SMs,	IRFB4229, 300V/38 mΩ
Diver Chip of SMs	IR2184, 20V/2.3A
MOSFETs of DSs,	NVHL080N120SC1, 1200V/110 mΩ
Diver Chip of DSs	IVCR1401DR, 35V/4A
Capacitor of SMs	RL2D471, 470μF/200V×4
Filter inductor	77438A7, 3mH/8A
Digital signal processor (DSP)	TMS320F28379D

the components used in the experiment prototype are listed in Table V.

Fig. 26 shows the steady-state experimental results obtained from the AHPL-MMC prototype. In Fig. 26(a), the FFT analysis of the measured three-phase ac currents indicates an average total harmonic distortion of 1.68%, which agrees with the operation standards. The measured high-frequency current ripple in the dc current is 30.7%, while a relatively small low-frequency

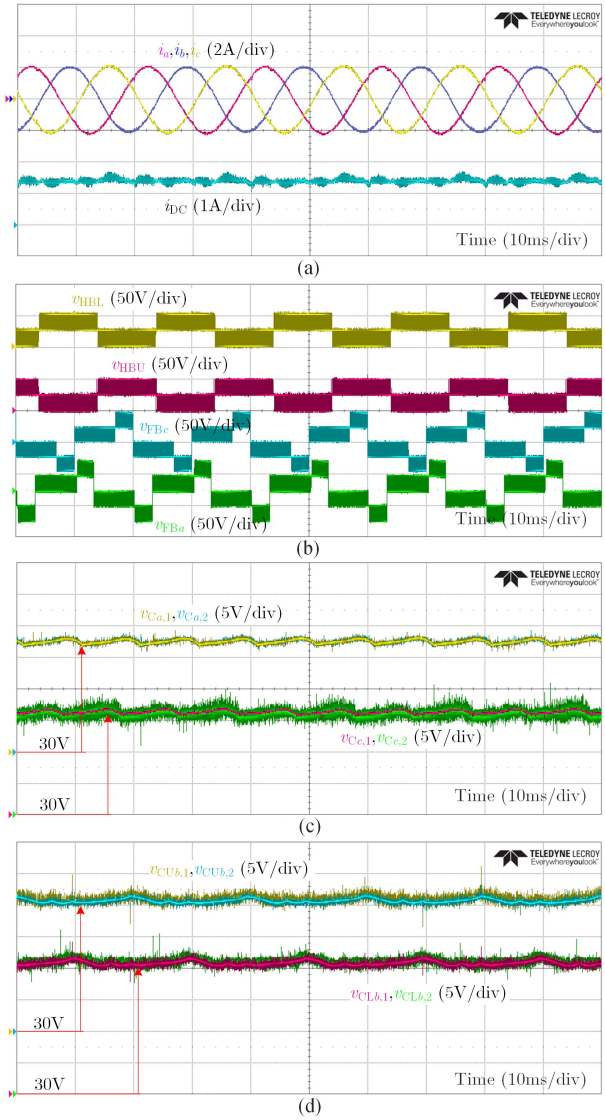

Fig. 26. Steady-state experimental results of AHPL-MMC. (a) AC currents and DC current. (b) Output voltages of the FB-WSCs and HB-WSCs. (c) Capacitor voltages of FB-WSCs in phases a and c. (d) Capacitor voltages of upper and lower HB-WSCs in phase b.

ripple can be found in the dc current. As can be seen in Fig. 26(b), the FB-WSC demonstrates five-level staircase waves, whereas the HB-WSC exhibits three-level staircase waves, depending on the SM number and type. Fig. 26(c) and (d) demonstrates the balanced capacitor voltage of each SM, closely aligning with its nominal value. The fluctuation pattern is akin to the total capacitor voltage observed in the simulation.

Fig. 27 presents the transient experimental results of the AHPL-MMC, illustrating the response when the active current reference suddenly changes from 1 to 0.5 p.u., while the reactive current reference is maintained at 0. In Fig. 27(a), the transient response of the dc current, ac current of phase a, and ac voltage of phase a is rapid, with no evident distortion or spikes. It is observed in Fig. 27(b) and (c) that the capacitor voltages of the FB-WSC and HB-WSC always remain balanced with small overshoot and response time. These simulation and experimental

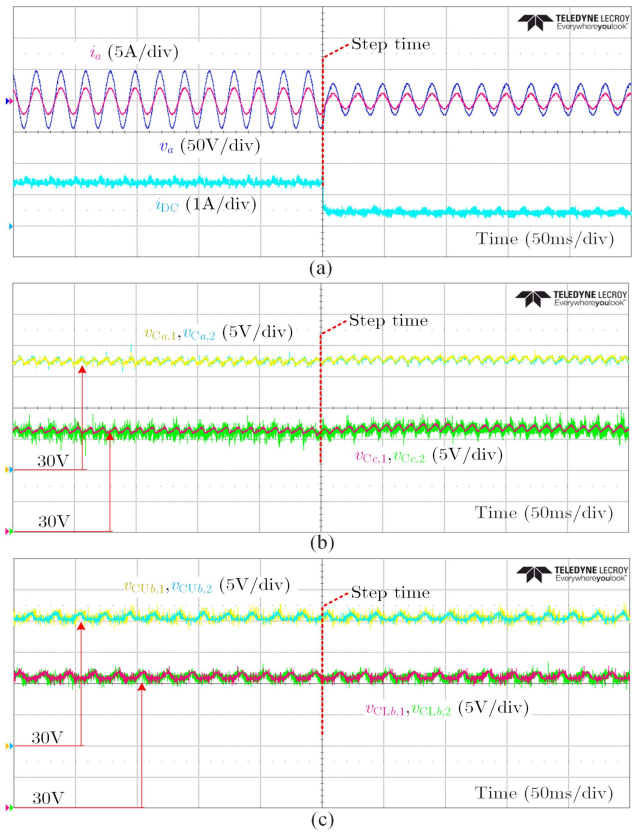

Fig. 27. Step response of AHPL-MMC. (a) AC voltage/current of phase *a* and DC current. (b) Capacitor voltages of FBSMs in phases *a* and *c*. (c) Capacitor voltages of upper and lower HBSMs in phase *b*.

results validate the effectiveness of the proposed topology and control method.

VII. Conclusion

This article introduces a new AHPL-MCC topology based on an innovative asymmetric hybrid phase leg configuration. Comprehensive analysis of the operation, parameter design, performance comparisons, and control strategies of the new converter are provided. Based on the results, the following conclusions can be made.

1) The AHPL-MMC demonstrates enhanced performance in terms of both cost and volume, primarily attributable to the substantial reduction in passive components.
2) The AHPL-MMC retains the advantages of the HB-MMC, providing a modulation index that ranges from 0 to 1, a tiny dc current ripple, the capability to operate in four quadrants, and the elimination of additional dc supporting capacitors or nonstandard ac transformers.
3) The proposed control strategy facilitates the stable operation of the AHPL-MMC, enabling it to effectively ride through both ac and dc faults.

The advantages of the proposed AHPL-MMC make it a promising topology suite for applications such as offshore wind power transmission and city center substations, where space is limited.

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