A Structure-Reconfigurable Isolated Bidirectional DC–DC Converter for Wide Voltage Gain Range Applications

Xianbin Qi, *Member, IEEE*, Cheng Yuan, Mingzhu Fang, *Member, IEEE*, Helong Li, *Senior Member, IEEE*, Zhiqing Yang, *Member, IEEE*, Shuang Zhao, *Senior Member, IEEE*, and Lijian Ding, *Member, IEEE*

***Abstract*—In this article, a structure-reconfigurable isolated bidirectional dc–dc converter is proposed. This converter can be configured into four operation structures with different voltage gains, which is suitable for wide voltage gain range applications. Through unified phase-shift modulation, the bidirectional power transfer of different operation structures is able to be regulated, which has a simple parameter design and is easy to implement. In addition, the energy stored in the leakage inductance is absorbed and utilized with the operating state of the converter, thereby avoiding the voltage spikes caused by the leakage inductance. Also, the proposed converter achieves soft-switching operation of the switches, decreases the turns ratio of the transformer, and the power components (e.g., transformers, power switches, inductors, etc.) are partially enabled in different operation structures, thus implementing high conversion efficiency. The topology structure, operating principles, and design considerations are described in more depth, and an experimental prototype with 40–200 V on the low-voltage side and 400 V on the high-voltage side is established. The theoretical analysis and experimental results fully verify the correctness and effectiveness of the proposed converter.**

***Index Terms*—Bidirectional dc–dc converter, phase-shift control, reconfigurable structure, wide voltage gain range.**

I. Introduction

TO ENSURE efficient and stable operation, the energy storage system with energy buffering capability has become an integral component of power systems such as electric vehicles, renewable power systems, and uninterruptable power supplies [1], [2]. As seen in Fig. 1, to connect the energy storage device with the dc bus, the isolated bidirectional dc–dc converter is necessary. Nevertheless, since the voltage of energy storage devices (e.g., supercapacitors and batteries) varies over a wide range based on the state of charge, this requires the converter to have the capability of wide voltage gain [3], [4].

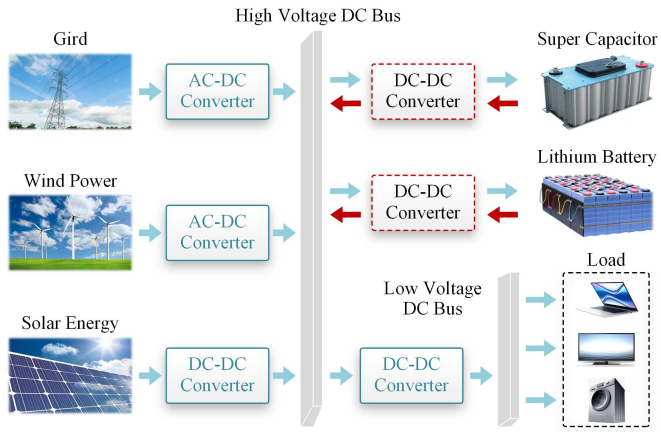

Fig. 1. Configuration of power system with energy storage devices.

To achieve a wide voltage gain range, a series of topologies have been widely studied and improved, including frequency-modulated converters, phase-shift modulated converters, and pulsewidth modulated converters. For frequency-modulated converters, the *LLC* resonant converter is of great interest due to its superior soft-switching performance [5]. But when the voltage gain is large, its operating frequency is far from the resonant frequency, which may cause large circulating currents to significantly increase losses. Also, the *LLC* converter has a narrow gain range during reverse operation and lacks boost capability, so it cannot be directly used in bidirectional power transmission applications [6]. To address this limitation, some multielement resonant converters such as *CLLC* and *CLLLC* converter have been proposed to improve the *LLC* converter [7], [8]. However, due to the large number of resonant elements, the design of the resonant tank will be complex, and the reliability and efficiency of the converter will be affected. In addition,

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Xianbin Qi, Helong Li, Zhiqing Yang, Shuang Zhao, and Lijian Ding are with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China, and also with the Institute of Energy, Hefei Comprehensive National Science Center, Hefei 230031, China (e-mail: xianbin_qi@hfut.edu.cn; helong.li@hfut.edu.cn; zhiqing.yang@hfut.edu.cn; shuang.zhao@hfut.edu.cn; ljding@hfut.edu.cn).

Cheng Yuan and Mingzhu Fang are with the Power Electronics and Electrical Drives Research Center, Harbin Institute of Technology (Shenzhen), Shenzhen 518055, China (e-mail: 21b953014@stu.hit.edu.cn; fangmingzhu@stu.hit.edu.cn).

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another widely used topology for realizing bidirectional power transmission is the dual-active-bridge (DAB) converter, whose control strategy consists of pulsewidth modulation and phase-shift modulation. The pulsewidth modulation strategy is easy to implement, but it restricts the dynamic performance and voltage regulation range of this converter [9]. The phase-shift modulation strategy allows zero-voltage switching (ZVS) for all switches, but it has drawbacks such as limited ZVS range and large backflow power [10]. To address these issues, several improvements for topology and modulation strategy have been proposed to improve the performance for wide voltage range applications [11], [12]. But the resulting complex structure and parameter design limit their reliability and practicality.

Another approach to achieving a wide voltage gain range is to cascade multiple converters. A half-bridge cascaded DAB converter with partial switch sharing is presented in [13]. Combined with the multiobjective optimal control, this converter obtains good soft-switching characteristics and low reactive backflow loss. In [14], an interleaved boost-integrated *LLC* resonant converter is introduced. Through the integration of the full-bridge *LLC* converter and the two-phase interleaved boost converter, the voltage gain range is extended and fixed frequency operation of the *LLC* converter is achieved. Besides, an integrated cascade converter is presented in [15], which is a combination of a DAB converter and a buck-boost converter. However, it is important to note that the power in these converters is processed through multiple stages, which greatly damages the conversion efficiency and also reduces the responsiveness of the converter to load variations.

Connecting multiple converter modules to constitute series-parallel power systems is also an effective technique to extend the voltage gain range [16], [17]. By adjusting the number of converters and the form of series-parallel connection between ports, flexible adjustment of input/output voltages, currents, and powers can be realized. Usually, the output voltage can be increased under the series connection structure, while the output current can be increased under the parallel connection structure [18], [19]. However, when the required voltage gain range is wide, a large number of converter modules are required to be configured, which leads to large volume and cost. At the same time, the voltage and current sharing control is indispensable to guarantee the balance of voltage, current, and power between these converter modules, which leads to complex control and low reliability of the entire system [20].

Further, to extend the voltage gain range more efficiently, many studies have been conducted on structure reconfigurable technology. A series of structure reconfigurable converters for wide voltage gain range applications are proposed in [21], [22], [23], and [24], but the structure and design parameters limit these converters to unidirectional operation. For bidirectional power transfer, a converter combining the three-level full-bridge and the *CLLLC* resonant tank is given in [25], which introduces four working modes to achieve a wide voltage gain range. A reconfigurable gain circuit for an *LCLC* resonant converter is introduced in [26], which can achieve different voltage gains by configuring the secondary side as an active voltage doubling circuit or a full bridge circuit. Moreover, the resonant tank of the converter proposed in [27] can be controlled to operate in both the *LLC* and *LLCC* modes, thereby achieving wide voltage gain during bidirectional power transfer. However, these converters suffer from a number of drawbacks that limit their practicality and reliability, which are summarized as follows.

1) The switching of multiple structures complicates the design of control strategies and resonant elements.
2) Additional power switches need to be configured for structural reconfiguration.
3) Bidirectional power conversion and high conversion efficiency over a wide voltage range cannot be achieved for some converters.

Considering the above-mentioned problems, the motivation of this article is to propose a more efficient and simpler converter for wide voltage gain range applications. From this, a structure-reconfigurable isolated bidirectional dc–dc converter is proposed. Close observation indicates that this converter has the following significant advantages.

1) The proposed converter can be configured into different operation structures during the bidirectional operation, which greatly extends the voltage gain range.
2) The different operation structures of the converter can be controlled by a unified phase-shift control strategy, which has a simple parameter design and is easy to implement.
3) The power components are partially enabled in different operation structures, and the small turns ratio transformer and ZVS operation reduces transformer and switching losses, so the converter can maintain high conversion efficiency.
4) The transformer leakage inductance is utilized as part of the ac-link inductor of the converter, which allows the voltage spikes caused by the leakage inductance to be avoided.

The rest of this article is organized as follows. In Section II, the topology structure and operating principle of the proposed structure-reconfigurable converter are introduced. In Section III, the characteristics and design considerations are described. In Section IV, the experimental and comparative results are given. Finally, Section V concludes this article.

II. Proposed Converter and Operating Principles

A. Topology of the Structure-Reconfigurable Converter

The proposed structure-reconfigurable isolated bidirectional dc–dc converter and its derivation process are shown in Fig. 2. Among them, V_{LV} is the low-voltage side for connecting energy storage devices such as supercapacitors or batteries, while V_{HV} is the high-voltage side for connecting dc bus. The inductors L_{S1} and L_{S2} are ac-link inductors composed of transformer leakage inductance and external series inductance, and T_1 and T_2 are high-frequency transformers with a turn ratio of 1: n. From the derivation process shown in Fig. 2, it can be seen that the low-voltage side of the converter consists of two full-bridge circuits sharing switches S_{p3}, S_{p4}, and S_{p5}, and the midpoint of each two switches is connected to the primary sides of the dual transformers T_1 and T_2. Besides, the derivation process shows that the high voltage side consists of two half-bridge circuits

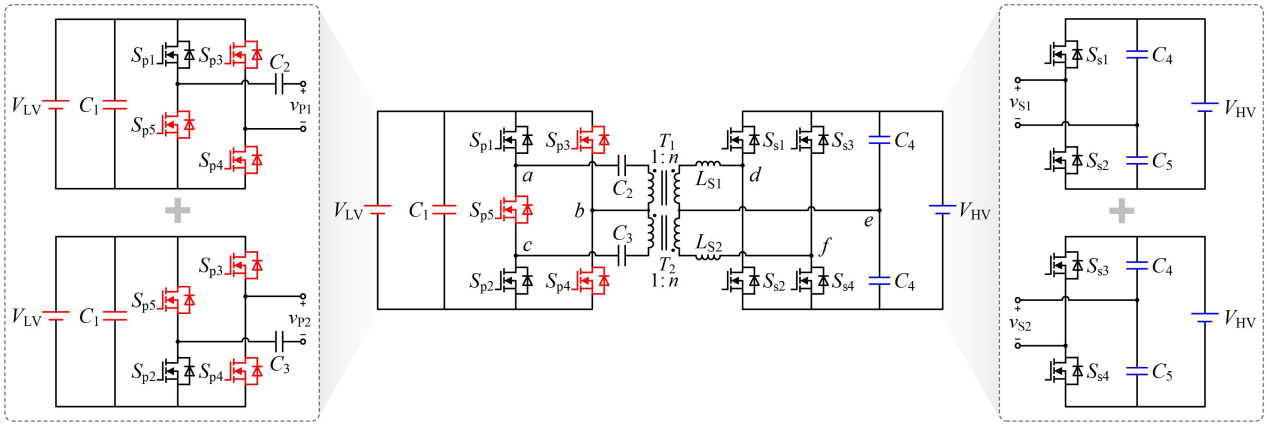


Fig. 2. Proposed structure-reconfigurable isolated bidirectional converter and its derivation process for high-voltage and low-voltage sides.

connected in parallel, and the midpoint of each bridge arm is connected to the secondary sides of the transformers.

By configuring the active switches in ON or OFF states, the low-voltage and high-voltage sides of the converter can be reconfigured into different structures. The constructed structures and the corresponding switching states are shown in Table I. As seen, the low-voltage side contains four structures, whose detailed descriptions are given as follows.

1) *Structure and State I:* S_{p1} is kept ON, S_{p2} and S_{p5} are kept OFF, while S_{p3} and S_{p4} are driven complementary. The input voltage v_{ab} of T_1 is a square wave varying between 0 and V_{LV}, and the input voltage v_{bc} of T_2 remains zero.
2) *Structure and State II:* S_{p2} is kept ON, S_{p1} and S_{p5} are kept OFF, while S_{p3} and S_{p4} are driven complementary. The input voltage v_{ab} of T_1 remains zero, and the input voltage v_{bc} of T_2 is a square wave varying between 0 and V_{LV}.
3) *Structure and State III:* S_{p1} and S_{p2} are kept ON, S_{p5} is kept OFF, while S_{p3} and S_{p4} are driven complementary. The input voltages v_{ab} and v_{bc} of the dual transformers T_1 and T_2 are both square waves varying between 0 and V_{LV}.
4) *Structure and State IV:* S_{p5} is kept ON, while S_{p1}, S_{p4} and S_{p2}, S_{p3} are driven complementary. The input voltages v_{ab} and v_{bc} of the dual transformers T_1 and T_2 are both square waves varying between -V_{LV} and V_{LV}.

Moreover, it can be seen from Table I that the high-voltage side contains three structures, and their detailed analysis and description are given as follows.

1) *Structure and State I:* S_{s3} and S_{s4} are kept OFF, while S_{s1} and S_{s2} are driven complementary. The output voltage v_{de} of T_1 is a square wave varying between -V_{C5} and V_{C4}, and the output voltage v_{ef} of T_2 remains zero.
2) *Structure and State II:* S_{s1} and S_{s2} are kept OFF, while S_{s3} and S_{s4} are driven complementary. The output voltage v_{de} of T_1 remains zero, and the output voltage v_{ef} of T_2 is a square wave varying between -V_{C4} and V_{C5}.
3) *Structure and State III:* S_{s1} and S_{s2}, S_{s3} and S_{s4} are driven complementary. The output voltage v_{de} of T_1 is a square wave varying between -V_{C5} and V_{C4}, and the output voltage v_{ef} of T_2 is a square wave varying between -V_{C4} and V_{C5}.

Based on the configurable structures of the low-voltage and high-voltage sides in Table I, the four operation structures of the proposed converter can be derived and presented in Fig. 3. Since the input and output voltages of the dual transformers T_1 and T_2 are different, these operation structures can obtain different voltage gains, which can be divided into low-voltage gain (LVG) structure, medium-voltage gain (MVG) structure and high-voltage gain (HVG) structure. During the bidirectional power transfer process, flexible switching between multiple operation structures can be realized by reasonably configuring the ON or OFF states of the active switches, thereby effectively expanding the voltage gain range of the converter.

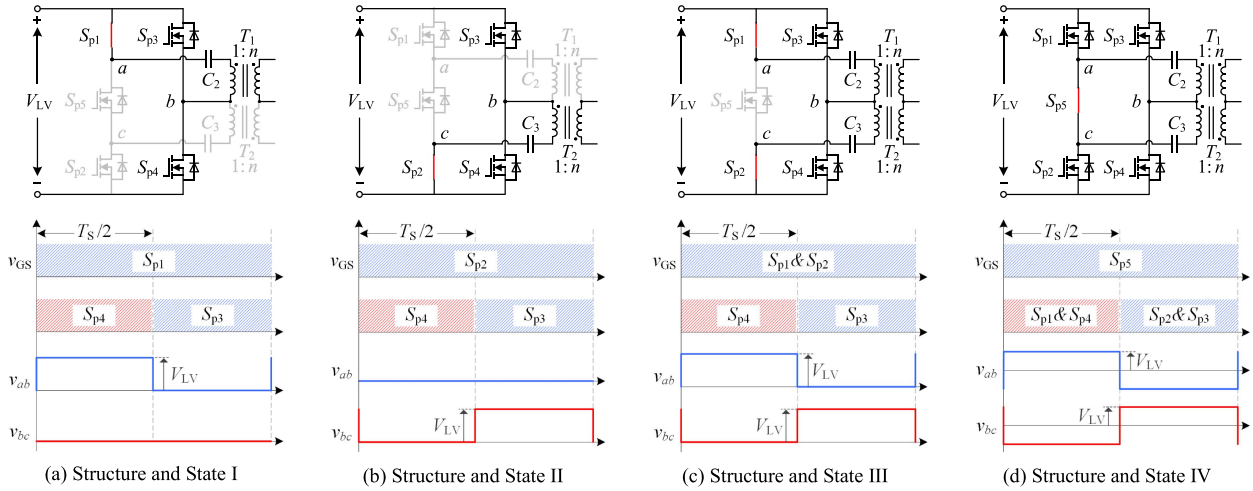
Combined with Table I and Fig. 3, it can be seen that the voltage waveforms of the transformers in the four operation structures are all square waves. Thus, a phase-shift modulation strategy can be imposed to uniformly achieve the bidirectional power transfer of different operation structures. To simplify the length of the article, the most representative HVG structure is taken as an example for detailed derivation and analysis in the following. Accordingly, based on the same principle, the LVG and MVG structures can be analyzed, and the corresponding performance characteristics can be concluded.

B. Operating Principle in Boost Mode

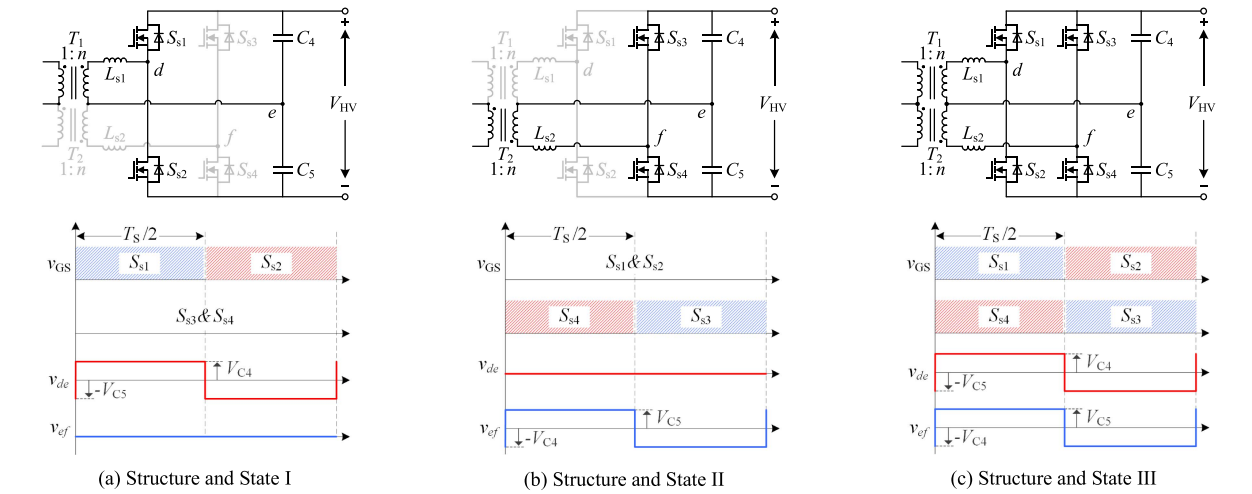
The switching sequence diagrams of the HVG structure in boost mode is presented in Fig. 4, and there are six switching states in one switching period T_S. The phase-shift duty cycle D_P between the low-voltage side and high-voltage side is greater than zero. The switch S_{p5} is always ON, and the other switches have a constant duty cycle of 0.5. Besides, the current-flow paths of the converter are drawn in Fig. 5. Due to the fact that the operating states are symmetrical in every half switching cycle, only the first three states are plotted, and the last three states can be drawn according to the same principle.

TABLE I
CONFIGURABLE STRUCTURES AND SWITCHING STATES OF LOW-VOLTAGE AND HIGH-VOLTAGE SIDES OF THE PROPOSED CONVERTER

Configurable Structures and Switching States of the Low-Voltage Side



Configurable Structures and Switching States of the High-Voltage Side



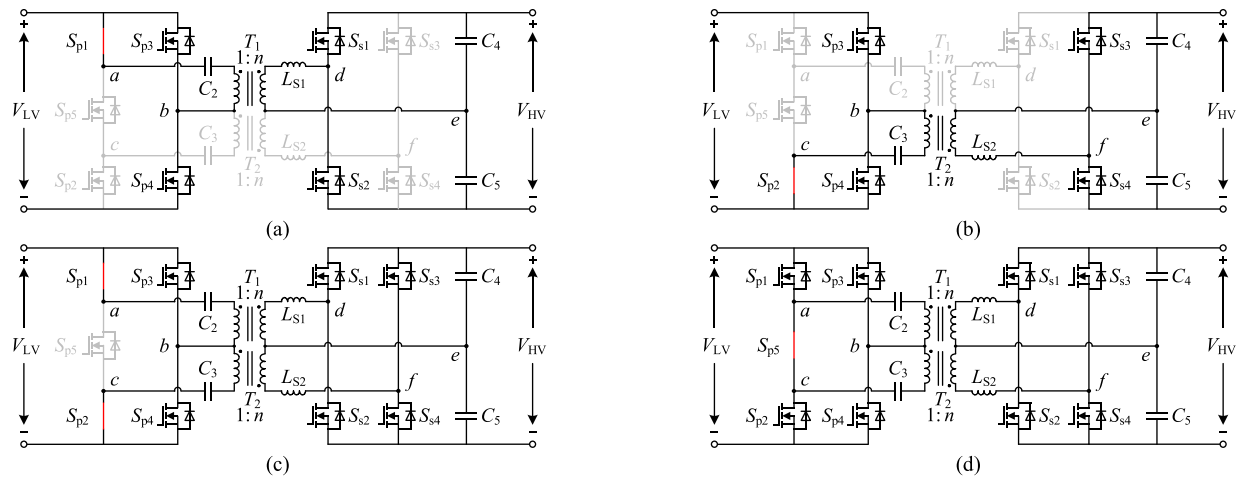


Fig. 3. Four operation structures of the proposed converter. (a) LVG structure_1. (b) LVG structure_2. (c) MVG structure. (d) HVG structure.

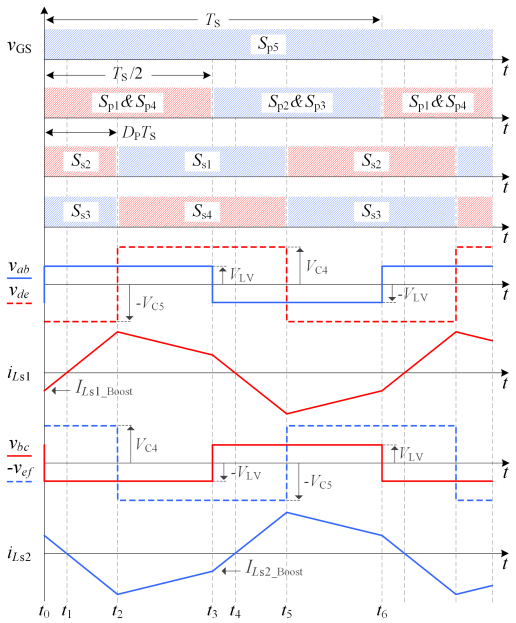


Fig. 4. Switching sequence diagrams of the HVG structure in boost mode.

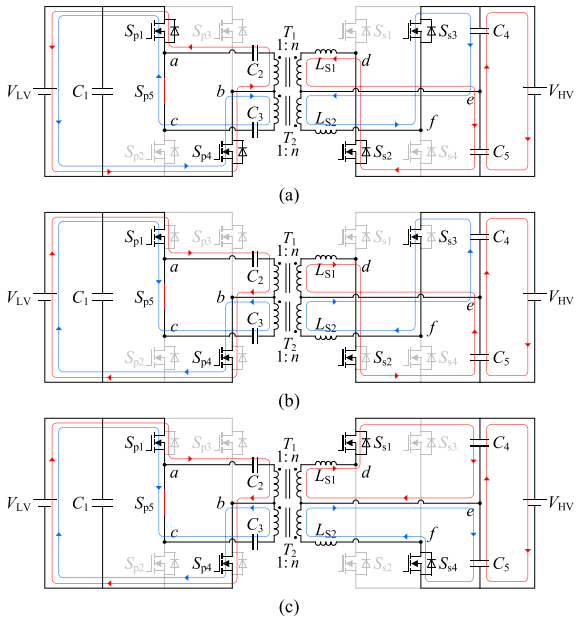


Fig. 5. Current-flow paths of the HVG structure in boost mode. (a) State 1 [t_0–t_1]. (b) State 2 [t_1–t_2]. (c) State 3 [t_2–t_3].

Based on the switching sequence diagrams in Fig. 4 and the current-flow paths in Fig. 5, the volt-second balance relations of L_{S1} and L_{S2}, as well as the voltage relation between V_{C4}, V_{C5}, and V_{HV}, can be respectively written by

$$\begin{cases} (nV_{LV}-V_{C4})\left(\frac{T_S}{2}-D_P T_S\right)-(nV_{LV}-V_{C5})\left(\frac{T_S}{2}-D_P T_S\right) \\ =(nV_{LV}+V_{C4})D_P T_S-(nV_{LV}+V_{C5})D_P T_S \\ V_{C4}+V_{C5}=V_{HV} \end{cases}. \tag{1}$$

By simplifying (1), the voltage relationship of the HVG structure in boost mode can be obtained by

$$V_{C4}=V_{C5}=V_{HV}/2. \tag{2}$$

Assuming that I_{Ls1_Boost} is the initial current on the inductor L_{S1}. Combining (2) and the operating principles shown in Fig. 4 and Fig. 5, the current flowing through L_{S1} during a switching cycle can be derived as follows:

$$i_{Ls1}=\begin{cases} I_{Ls1\_Boost}+\frac{2nV_{LV}+V_{HV}}{2L_{S1}}t & (t_0\le t<t_2) \\ I_{Ls1\_Boost}+\frac{D_P V_{HV} T_S}{L_{S1}}+\frac{2nV_{LV}-V_{HV}}{2L_{S1}}t & (t_2\le t<t_3) \\ I_{Ls1\_Boost}+\frac{nV_{LV}+D_P V_{HV}}{L_{S1}}T_S-\frac{2nV_{LV}+V_{HV}}{2L_{S1}}t & (t_3\le t<t_5) \\ I_{Ls1\_Boost}-\frac{2nV_{LV}-V_{HV}}{2L_{S1}}(t-T_S) & (t_5\le t<t_6) \end{cases}. \tag{3}$$

Similarly, assuming that I_{Ls2_Boost} is the initial current on the inductor L_{S2}. Based on the same principle, the current i_{Ls2} in a switching cycle can be expressed as

$$i_{Ls2}=\begin{cases} I_{Ls2\_Boost}+\frac{nV_{LV}+D_P V_{HV}}{L_{S2}}T_S \\ \quad -\frac{2nV_{LV}+V_{HV}}{4L_{S2}}(2t+T_S) & (t_0\le t<t_2) \\ I_{Ls2\_Boost}-\frac{2nV_{LV}-V_{HV}}{4L_{S2}}(2t-T_S) & (t_2\le t<t_3) \\ I_{Ls2\_Boost}+\frac{2nV_{LV}+V_{HV}}{4L_{S2}}(2t-T_S) & (t_3\le t<t_5) \\ I_{Ls2\_Boost}+\frac{D_P V_{HV} T_S}{L_{S2}} \\ \quad +\frac{2nV_{LV}-V_{HV}}{4L_{S2}}(2t-T_S) & (t_5\le t<t_6) \end{cases}. \tag{4}$$

Combining (3), (4) and the ampere-second balance relations of capacitors C_4 and C_5, the initial values of i_{Ls1} and i_{Ls2} in boost mode can be calculated as

$$\begin{cases} I_{Ls1\_Boost}=\frac{(V_{HV}-2nV_{LV}-4D_P V_{HV})T_S}{8L_{S1}} \\ I_{Ls2\_Boost}=\frac{(V_{HV}-2nV_{LV}-4D_P V_{HV})T_S}{8L_{S2}} \end{cases}. \tag{5}$$

By integrating the voltage and current of v_{ab} port during a switching cycle, the power transferred to the high-voltage side through transformer T_1 can be obtained

$$\begin{aligned} P_{Boost\_ab}&=\frac{1}{T_S/2}\int_{t_0}^{t_3} n v_{ab} i_{Ls1}(t)dt \\ &=\frac{nV_{LV}V_{HV}T_S D_P(1-2D_P)}{2L_{S1}}. \end{aligned} \tag{6}$$

Likewise, by integrating the voltage and current of v_{bc} port during a switching cycle, the power transferred to the high-voltage side through transformer T_2 can be derived as

$$\begin{aligned} P_{Boost\_bc}&=\frac{1}{T_S/2}\int_{t_3}^{t_6} n v_{bc} i_{Ls2}(t)dt \\ &=\frac{nV_{LV}V_{HV}T_S D_P(1-2D_P)}{2L_{S2}}. \end{aligned} \tag{7}$$

TABLE II
COMPONENTS AND PARAMETERS OF THE PROTOTYPE

Parameters	Values
Low-voltage side V_{LV}	40–200 V
High-voltage side V_{HV}	400 V
Rated Power P_{rated}	500 W
Switching frequency f_S	100 kHz
Transformer T_1 and T_2	PQ40/20-PC95, Turns ratio: 1:2 Leakage inductance: L_s=5.41 μH Magnetizing inductance: L_m=74.1 μH
Capacitors C_1	470 μF, multilayer ceramic capacitor
Capacitors C_2 and C_3	30 μF, film capacitor
Capacitors C_4 and C_5	470 μF, aluminum electrolytic capacitor
Inductors L_{S1} and L_{S2}	68 μH, CSBL2212-680M, R_{DS}=26.3 mΩ
MOSFETs S_{p1}-S_{p5}	IRF250P224, 250 V/128 A, R_{DS_on}=9 mΩ
MOSFETs S_{s1}-S_{s4}	C3M0025065D, 650 V/97 A, R_{DS_on}=25 mΩ

According to (6) and (7), the transmitted power of the HVG structure in boost mode can be represented as

$$P_{\text{Boost}} = P_{\text{Boost}\_ab} + P_{\text{Boost}\_bc} = \frac{nV_{\text{LV}}V_{\text{HV}}T_{\text{S}}D_{\text{P}}(1-2D_{\text{P}})(L_{\text{S1}}+L_{\text{S2}})}{2L_{\text{S1}}L_{\text{S2}}}. \quad (8)$$

Assuming that R_{HV} is the equivalent load on the high-voltage side, the transmitted power can also be obtained as $V_{\text{HV}}{}^2/R_{\text{HV}}$. Combined with (8), the voltage gain of the HVG structure in boost mode can be obtained

$$G_{\text{Boost\_HVG}} = \frac{V_{\text{HV}}}{V_{\text{LV}}} = \frac{nT_{\text{S}}R_{\text{HV}}D_{\text{P}}(1-2D_{\text{P}})(L_{\text{S1}}+L_{\text{S2}})}{2L_{\text{S1}}L_{\text{S2}}}. \quad (9)$$

For the convenience of visually comparing the voltage gains of different operation structures, the boost gain of HVG structure with fixed transmitted power and output voltage can be derived from (8) and (9), which can be expressed as

$$G_{\text{Boost\_HVG}} = \frac{nV_{\text{HV}}{}^2T_{\text{S}}D_{\text{P}}(1-2D_{\text{P}})(L_{\text{S1}}+L_{\text{S2}})}{2P_{\text{Boost}}L_{\text{S1}}L_{\text{S2}}}. \quad (10)$$

Based on the same principle as the HVG structure, the boost gain of the MVG and LVG structures can be calculated as

$$\begin{cases} G_{\text{Boost\_MVG}} = \frac{nV_{\text{HV}}{}^2T_{\text{S}}D_{\text{P}}(1-2D_{\text{P}})(L_{\text{S1}}+L_{\text{S2}})}{4P_{\text{Boost}}L_{\text{S1}}L_{\text{S2}}} \\ G_{\text{Boost\_LVG}} = \frac{nV_{\text{HV}}{}^2T_{\text{S}}D_{\text{P}}(1-2D_{\text{P}})(L_{\text{S1}}+L_{\text{S2}})}{8P_{\text{Boost}}L_{\text{S1}}L_{\text{S2}}} \end{cases}. \quad (11)$$

By substituting the parameters in Table II into (10) and (11), the voltage gain curves of LVG, MVG, and HVG structures in boost mode can be plotted in Fig. 6. It can be seen that by controlling the converter into different operation structures, its voltage gain range can be effectively extended. Besides, based on the abovementioned operating principle, the energy stored in the leakage inductance is absorbed and utilized with the operating state of the converter, which can avoid voltage spikes caused by leakage inductance and reduce the voltage stress of power components. Meanwhile, the power components (e.g., power switches, transformers, inductors, etc.) are partially enabled in different operation structures, so the converter can maintain high conversion efficiency over a wide voltage range.

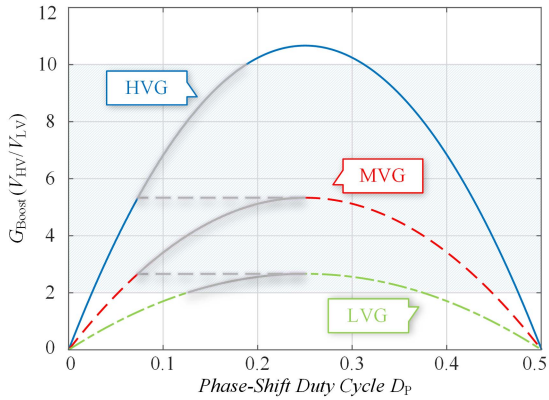


Fig. 6. Voltage gain curves of the proposed converter in boost mode.

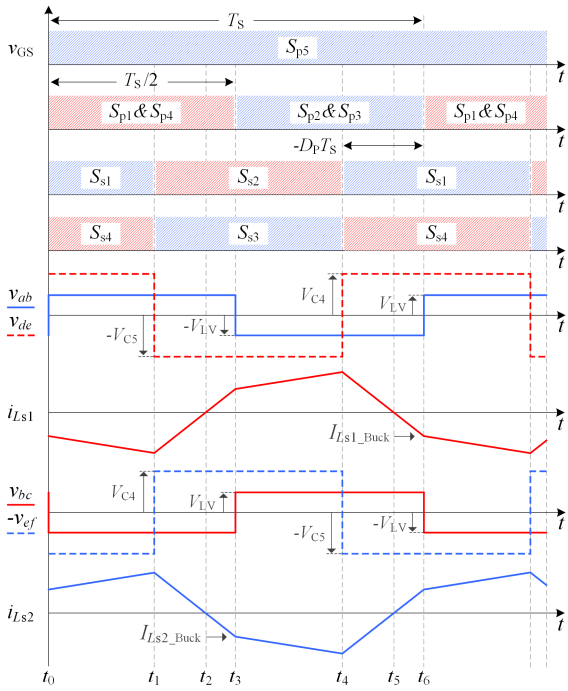


Fig. 7. Switching sequence diagrams of the HVG structure in buck mode.

C. Operating Principle in Buck Mode

The switching sequence diagrams of the HVG structure in buck mode is shown in Fig. 7, and there are also six switching states in one switching period. Similar to the boost mode, the switch S_{p5} remains ON, and the other switches have a constant duty cycle of 0.5. However, the difference is that the phase-shift duty cycle D_P between the low-voltage and high-voltage sides is less than zero. The current-flow paths of the HVG structure in buck mode are shown in Fig. 8, where only the first three

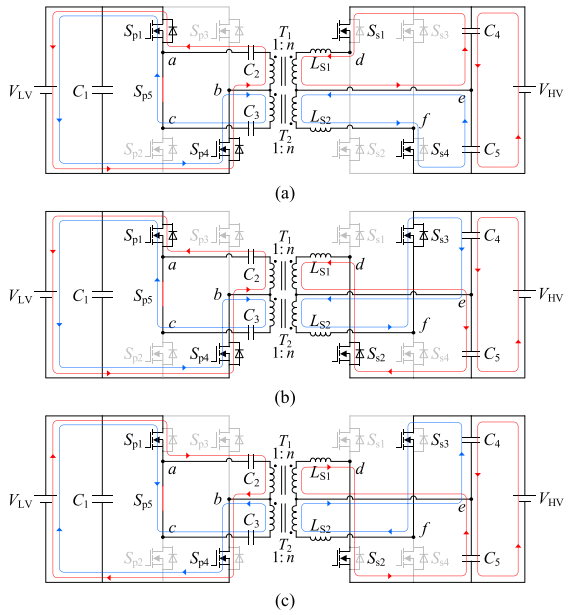


Fig. 8. Current-flow paths of the HVG structure in buck mode. (a) State 1 [t_0–t_1]. (b) State 2 [t_1–t_2]. (c) State 3 [t_2–t_3].

states are plotted, and the other three states can be drawn based on the same principle. In addition, to maintain uniformity of the derivation, the positive direction of each voltage and current is set to be identical to that of the boost mode.

According to the switching sequence diagrams in Fig. 7 and the current-flow paths in Fig. 8, the voltage relation between V_{C4}, V_{C5}, and V_{HV}, as well as the volt-second balance relations of L_{S1} and L_{S2}, can be respectively represented as

$$\begin{cases} (V_{C4}-nV_{LV})\left(\frac{T_S}{2}+D_PT_S\right)-(V_{C5}-nV_{LV})\left(\frac{T_S}{2}+D_PT_S\right) \\ \qquad =(V_{C4}+nV_{LV})D_PT_S-(V_{C5}+nV_{LV})D_PT_S \\ V_{C4}+V_{C5}=V_{HV} \end{cases}. \tag{12}$$

By simplifying (12), the voltage relationship of the HVG structure in buck mode can be derived as

$$V_{C4}=V_{C5}=V_{HV}/2. \tag{13}$$

Assuming that I_{Ls1_Buck} is the initial current on L_{S1}. Combining (13) and the operating principles illustrated in Fig. 7 and Fig. 8, the current i_{Ls1} in a switching cycle can be expressed as

$$i_{Ls1}=\begin{cases} I_{Ls1\_Buck}-\frac{V_{HV}-2nV_{LV}}{2L_{S1}}t & (t_0\le t<t_2) \\ I_{Ls1\_Buck}-\frac{1+2D_P}{2L_{S1}}V_{HV}T_S & \\ \quad +\frac{V_{HV}+2nV_{LV}}{2L_{S1}}t & (t_2\le t<t_3) \\ I_{Ls1\_Buck}-\frac{D_PV_{HV}T_S}{L_{S1}} & \\ \quad +\frac{V_{HV}-2nV_{LV}}{2L_{S1}}(t-T_S) & (t_3\le t<t_5) \\ I_{Ls1\_Buck}-\frac{V_{HV}+2nV_{LV}}{2L_{S1}}(t-T_S) & (t_5\le t<t_6) \end{cases}. \tag{14}$$

Similarly, assuming that I_{Ls2_Buck} is the initial current on L_{S2}, the current i_{Ls2} in a switching cycle can be derived as

$$i_{Ls2}=\begin{cases} I_{Ls2\_Buck}-\frac{D_PV_{HV}T_S}{L_{S2}} & \\ \quad +\frac{V_{HV}-2nV_{LV}}{4L_{S2}}(2t-T_S) & (t_0\le t<t_2) \\ I_{Ls2\_Buck}-\frac{V_{HV}+2nV_{LV}}{4L_{S2}}(2t-T_S) & (t_2\le t<t_3) \\ I_{Ls2\_Buck}-\frac{V_{HV}-2nV_{LV}}{4L_{S2}}(2t-T_S) & (t_3\le t<t_5) \\ I_{Ls2\_Buck}-\frac{1+2D_P}{2L_{S1}}V_{HV}T_S & \\ \quad +\frac{V_{HV}+2nV_{LV}}{4L_{S2}}(2t-T_S) & (t_5\le t<t_6) \end{cases}. \tag{15}$$

Subsequently, by combining (14) and (15) with the ampere-second balance relations of C_4 and C_5, the initial values of i_{Ls1} and i_{Ls2} in buck mode can be solved as

$$\begin{cases} I_{Ls1\_Buck}=\frac{(V_{HV}-2nV_{LV}+4D_PV_{HV})T_S}{8L_{S1}} \\ I_{Ls2\_Buck}=\frac{(V_{HV}-2nV_{LV}+4D_PV_{HV})T_S}{8L_{S2}} \end{cases}. \tag{16}$$

Similar to the boost mode, by integrating the voltage and current of v_{ab} port and v_{bc} port during a switching cycle, the power transferred to the high-voltage side through transformers T_1 and T_2 in buck mode can be represented as

$$\begin{cases} P_{Buck\_ab}=\frac{1}{T_S/2}\int_{t_0}^{t_3}nv_{ab}i_{Ls1}(t)dt=\frac{nV_{LV}V_{HV}T_SD_P(1+2D_P)}{2L_{S1}} \\ P_{Buck\_bc}=\frac{1}{T_S/2}\int_{t_3}^{t_6}nv_{bc}i_{Ls2}(t)dt=\frac{nV_{LV}V_{HV}T_SD_P(1+2D_P)}{2L_{S2}} \end{cases}. \tag{17}$$

Based on this, the transmitted power of the HVG structure in buck mode can be obtained

$$\begin{aligned} P_{Buck}&=P_{Buck\_ab}+P_{Buck\_bc} \\ &=\frac{nV_{LV}V_{HV}T_SD_P(1+2D_P)(L_{S1}+L_{S2})}{2L_{S1}L_{S2}}. \end{aligned} \tag{18}$$

Since the positive direction of each voltage and current is set to be identical to that of the boost mode, and the energy is transferred from the high-voltage side to the low-voltage side. Therefore, the transmitted power of the HVG structure in buck mode obtained in (17) and (18) is negative.

Assuming that R_{LV} is the equivalent load on the low-voltage side, the transmitted power can also be expressed as $-V_{LV}{}^2/R_{LV}$. By combining with (18), the voltage gain of the HVG structure in buck mode can be calculated as

$$G_{Buck\_HVG}=\frac{V_{LV}}{V_{HV}}=-\frac{nT_SR_{LV}D_P(1+2D_P)(L_{S1}+L_{S2})}{2L_{S1}L_{S2}}. \tag{19}$$

To visually compare the voltage gains of different operation structures, the buck gain of the HVG structure with fixed input voltage and transmitted power can be derived from (18) and (19), which can be derived as

$$G_{Buck\_HVG}=\frac{2P_{Buck}L_{S1}L_{S2}}{nV_{HV}{}^2T_SD_P(1+2D_P)(L_{S1}+L_{S2})}. \tag{20}$$

Subsequently, according to the same derivation principles, the buck gain of the MVG structure and the LVG structure can be represented as follows:

$$\begin{cases} G_{Buck\_MVG}=\frac{4P_{Buck}L_{S1}L_{S2}}{nV_{HV}{}^2T_SD_P(1+2D_P)(L_{S1}+L_{S2})} \\ G_{Buck\_LVG}=\frac{8P_{Buck}L_{S1}L_{S2}}{nV_{HV}{}^2T_SD_P(1+2D_P)(L_{S1}+L_{S2})} \end{cases}. \tag{21}$$

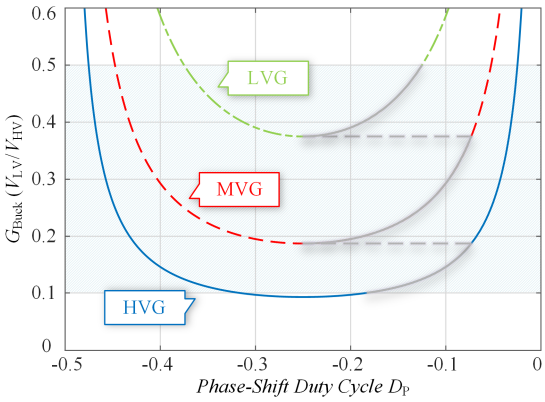


Fig. 9. Voltage gain curves of the proposed converter in buck mode.

By substituting the parameters in Table II into (20) and (21), the buck gain curves of LVG, MVG and HVG structures can be drawn in Fig. 9. As can be seen, by controlling the converter into different operation structures, its buck gain range can be extended. Furthermore, the power components in buck mode are partially enabled in different operation structures, which facilitates the proposed converter to maintain high conversion efficiency over a wide voltage range.

III. Characteristics and Design Considerations

A. Parameter Design

Based on the above-mentioned operating principle and for the convenience of parameter calculation, the values of L_{S1} and L_{S2} are set to be identical. By simplifying the (10) and (11) of the boost mode, it follows that L_{S1} and L_{S2} first increase and then decrease as D_P increases. To enable the converter to operate properly under different operation structures, the value of the inductors should be less than the maximum value within its optional range, which can be represented as

$$L_{S1} = L_{S2} < \frac{n{V_{HV}}^2 T_S D_P (1 - 2D_P)}{P_{Boost} G_{Boost\_HVG}}. \tag{22}$$

Furthermore, it is also important to ensure that the converter operates properly in buck mode. By simplifying the (20) and (21) of the buck mode, the value range of L_{S1} and L_{S2} can also be obtained as follows:

$$L_{S1} = L_{S2} < \frac{n{V_{HV}}^2 T_S D_P (1 + 2D_P) G_{Buck\_HVG}}{P_{Buck}}. \tag{23}$$

Combining (22), (23) and the actual parameters in Table II, when the turns ratio of the transformers is taken as 1:2 and the leakage inductance L_s of the transformer is 5.41 μH, the ac-link inductors L_{S1} and L_{S2} can be selected as 68 μH.

B. Switching Principle Between Operation Structures

During normal operation, the unified phase-shift modulation strategy is adopted to achieve bidirectional power transfer of the converter. However, theoretically, discontinuities may exist during transitions between LVG, MVG, and HVG, which may generate significant voltage and current fluctuations. Hence, to achieve a smooth transition, a soft scheme is adopted to smooth the switching between different operation structures, which is identical to the scheme applied in [28] and [29].

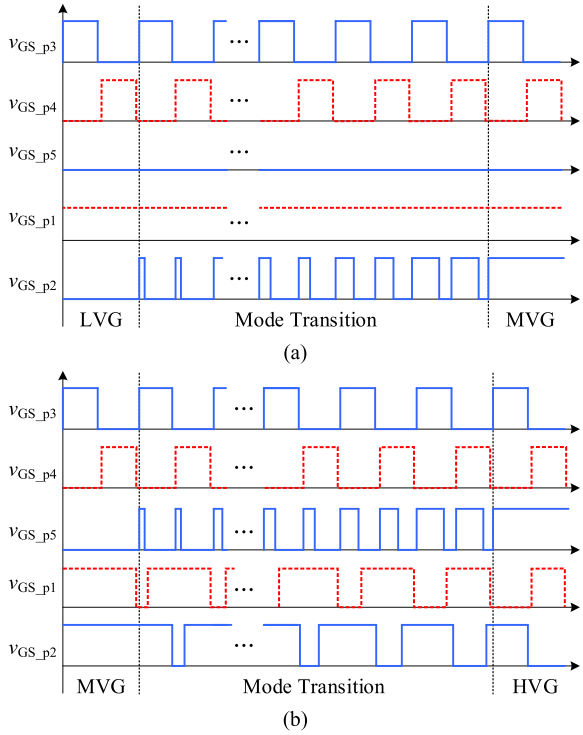


Fig. 10. Switching sequence diagrams of the converter during the transition. (a) From LVG to MVG. (b) From MVG to HVG.

Specifically, Fig. 10 shows the switching sequences during the transition from LVG to MVG and from MVG to HVG. As shown, the implementation principle is to gradually change the duty cycle of the corresponding switches, whereby smooth and continuous transitions can be achieved. Following the same principle, the switching sequences from HVG to MVG and from MVG to LVG can be implemented in reverse.

C. ZVS Analysis

From the operating principles presented in Section II, it can be seen that the proposed converter operates similarly in boost mode and buck mode. For this reason, the following takes the HVG structure in boost mode as an example for detailed ZVS analysis to save space. The ZVS conditions and ranges for the buck mode and the other operation structures can be concluded based on the same derivation principles. In addition, it should be noted that there is a dead time between switches of the same bridge arm to prevent shoot-through, which shall be considered during the ZVS analysis. However, for simplicity, it is assumed that the inductor currents during this time are constant and equal to the value at the initial of the dead time.

1) ZVS of Low-Voltage Side: As shown in Figs. 4 and 5, after S_{p1} and S_{p4} are turned OFF at t_3, the ZVS realization condition of S_{p2} and S_{p3} is that the currents i_{LS1} and i_{LS2} flow through their body diodes during the dead time. In the same way, this is

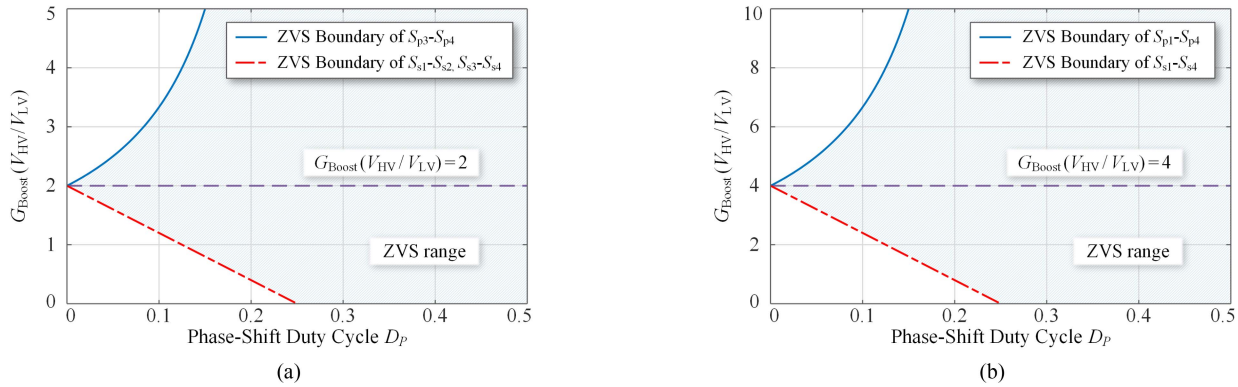


Fig. 11. ZVS range in boost mode. (a) ZVS range of LVG structure and MVG structure. (b) ZVS range of HVG structure.

also the ZVS realization condition for S_{p1} and S_{p4} after S_{p2} and S_{p3} are turned OFF at t_6, which can be written by

$$n(I_{Ls1\_Boost} + I_{Ls2\_Boost}) < 0. \tag{24}$$

By substituting (5) into (24), the ZVS condition of S_{p1}–S_{p4} in boost mode can be further derived as

$$\frac{nT_S(V_{HV} - 2nV_{LV} - 4D_P V_{HV})}{4L_{S1}} < 0. \tag{25}$$

2) ZVS of High-Voltage Side: After S_{s2} and S_{s3} are turned OFF at t_2, the ZVS realization condition of S_{s1} is that the current i_{LS1} flow through its body diode during the dead time, and the ZVS realization condition of S_{s4} is that the current i_{LS2} flow through its body diode during the dead time. Besides, these are also the ZVS realization conditions for S_{s2} and S_{s3} after S_{s1} and S_{s4} are turned OFF at t_5, which can be represented as

$$\begin{cases} I_{Ls1\_Boost} + \frac{(2nV_{LV}+V_{HV})D_P T_S}{2L_{S1}} > 0 \\ I_{Ls2\_Boost} + \frac{(2nV_{LV}+V_{HV})D_P T_S}{2L_{S2}} > 0 \end{cases}. \tag{26}$$

Since L_{S1} and L_{S2} are set to be equal, by combining (5) and (26), the ZVS condition of S_{s1}–S_{s4} in boost can be given by

$$\frac{(V_{HV} - 2nV_{LV} + 8nD_P V_{LV})T_S}{8L_{S1}} > 0. \tag{27}$$

By simplifying (25) and (27), the ZVS conditions of the HVG structure in boost mode can be derived as

$$\begin{cases} D_P > \frac{(V_{HV}/V_{LV})-2n}{4(V_{HV}/V_{LV})} \\ D_P > \frac{2n-(V_{HV}/V_{LV})}{8n} \end{cases}. \tag{28}$$

Based on the same principles, the ZVS conditions of the MVG and LVG structures in boost mode can be calculated as

$$\begin{cases} D_P > \frac{(V_{HV}/V_{LV})-n}{4(V_{HV}/V_{LV})} \\ D_P > \frac{n-(V_{HV}/V_{LV})}{4n} \end{cases}. \tag{29}$$

The ZVS boundary curves of the proposed converter in boost mode can be plotted in Fig. 11 based on (28) and (29). As can be seen, the high-voltage side switches can realize ZVS over the full load range when the boost gain is greater than two times for the LVG and MVG structures, or greater than four times for the HVG structure. As for the low-voltage side switches, when the converter is operated in the right-half region of D_P (i.e., 0.25–0.5), all of the switches can realize ZVS in the full load range. And when the converter is operated in the left-half region of D_P (i.e., 0–0.25), the ZVS range of HVG structure at high voltage gain is wider than that of LVG and MVG structures, which ensures the ZVS realization of the converter over a wide voltage range. Considering that the loop current is small when the converter is operated in the left-half region, the operating region is set in this region to keep high efficiency, the specific operation trajectory is shown in Fig. 6.

Based on the same derivation principles, the ZVS conditions in buck mode can be concluded, and the ZVS boundary curves can be drawn in Fig. 12. It is seen that when the buck gain is greater than four times (i.e., $G_{Buck}<0.25$) for the HVG structure, or greater than two times (i.e., $G_{Buck}<0.5$) for the LVG and MVG structures, the high-voltage side switches can realize ZVS over the full load range. For the low-voltage side switches, when the converter is operated in the left-half region of D_P (i.e., -0.5 to -0.25), all of the switches can realize ZVS in the full load range. When the converter is operated in the right-half region of D_P (i.e., -0.25 to 0), the ZVS range of the HVG structure at high buck gain is wider than that of LVG and MVG structures. This shows that the ZVS range can be extended by controlling the converter into different operation structures. Considering that the loop current is small when the converter is operated in the right-half region. Thus, as shown in the operation trajectory in Fig. 9, the operation region in buck mode is set in the right-half region to maintain high conversion efficiency.

IV. Experimental Verification

To validate the theoretical analysis and performance of the proposed structure-reconfigurable bidirectional dc–dc converter, an experimental prototype is established. Further, a couple of experiments are carried out for the steady-state characteristics, dynamic-state characteristics and conversion efficiency, and the obtained results are analyzed and demonstrated in this section. The picture of the experimental platform is shown in Fig. 13, and the utilized components are presented in Table II. Besides, the employed digital controller is TMS320F28335. The rated power of the converter is designed to be 500 W.

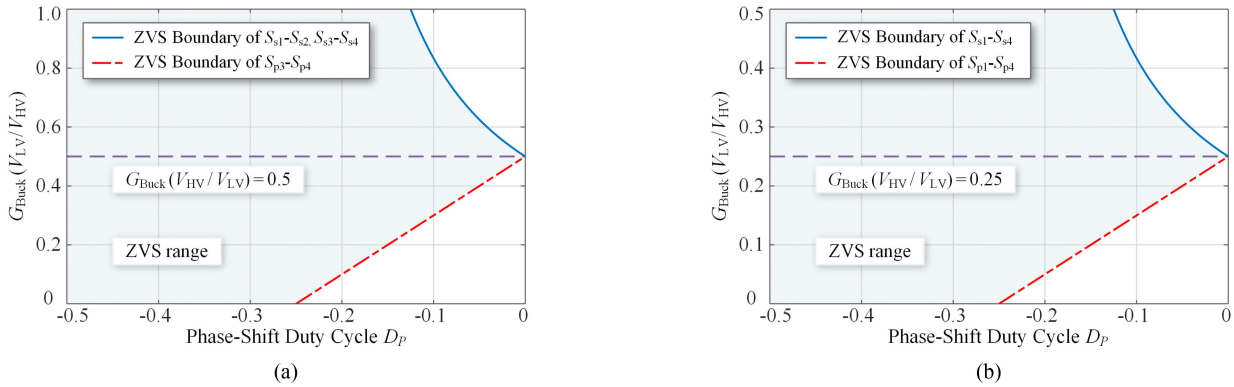


Fig. 12. ZVS range in buck mode. (a) ZVS range of LVG structure and MVG structure. (b) ZVS range of HVG structure.

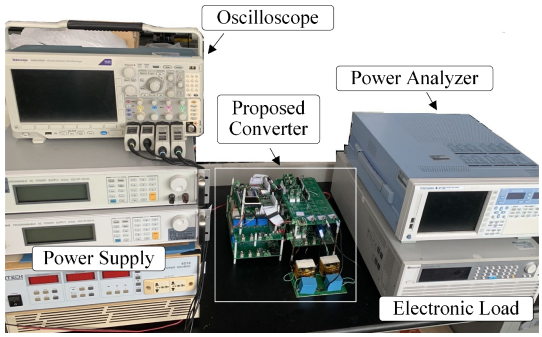


Fig. 13. Photograph of the experimental platform.

The switching frequency is designed to be a constant 100 kHz. The low-voltage side voltage is designed to be 40–200 V, while the high-voltage side voltage is designed to be 400 V.

A. Experimental Waveforms

The steady-state waveforms when the proposed converter is operated in boost mode under LVG, MVG, and HVG structures are presented in Figs 14 –16. Wherein, the converter operates at rated power, the input voltage V_{LV} is 200 V in LVG structure, 80 V in MVG structure, and 40 V in HVG structure. In addition, it should be noted that the verification of the LVG structure is exemplified by the structure shown in Fig. 3(a).

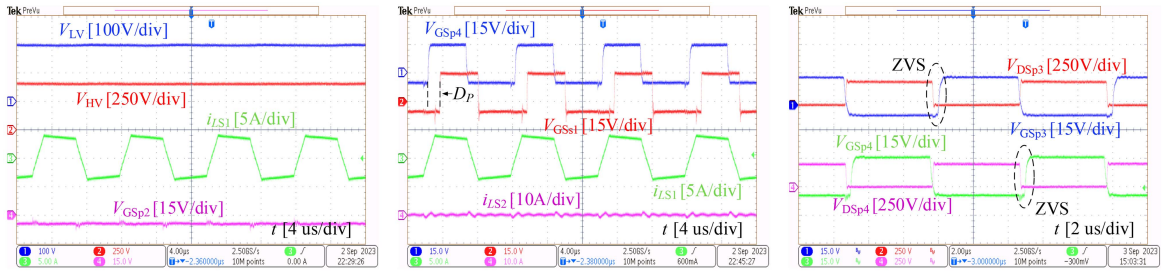
From the experimental waveforms in Figs. 14(a), 15(a), and 16(a), it can be seen that the proposed converter can be controlled into different operation structures to boost input voltages of 40, 80, and 200 V to an output voltage of 400 V, which verifies its capability of wide voltage gain range. Also, the phase-shift duty cycle D_P and the currents on the ac-link inductors are displayed in Figs. 14(b), 15(b), and 16(b). As can be seen, the switch gate drive signals as well as the currents i_{LS1} and i_{LS2} are consistent with the theoretical settings in Table I and Fig. 6, and the voltage spikes caused by leakage inductance are avoided, which validates the effectiveness and correctness of the theoretical derivation in Section II. Since the high-voltage side switches in boost mode can realize ZVS over the full load range, Figs. 14(c), 15(c), and 16(c) display the ZVS waveforms of S_{p1}/S_{p3} and S_{p4} (i.e., the low-voltage side switches) for different operation structures, respectively, which adequately confirms the validity of the ZVS analysis.

Similarly, the steady-state waveforms when the converter is operated in buck mode under LVG, MVG, and HVG structures are given in Figs 17 –19. Among them, the converter operates at rated power, the output voltage V_{LV} is 40 V in HVG structure, 80 V in MVG structure, and 200 V in LVG structure. As can be seen in Figs. 17(a), 18(a), and 19(a), the proposed converter can be controlled into different operation structures to step down an input voltage of 400 V to output voltages of 200, 80, and 40 V, which confirms its wide buck gain range. Besides, the gate drive signals of the switches and the currents on the ac-link inductors are presented in Figs. 17(b), 18(b), and 19(b). Obviously, the phase-shift duty cycle D_P and the currents i_{LS1} and i_{LS2} agree with the theoretical settings in Table I and Fig. 9, which verifies the effectiveness of the theoretical derivation of the buck mode. Moreover, since the experiments in boost mode provide the ZVS waveforms of the low-voltage side switches. To ensure the completeness of the experiments, Figs. 17(c), 18(c), and 19(c) show the ZVS waveforms of S_{s1} and S_{s2}/S_{s4} (i.e., the high-voltage side switches), which fully verify the effectiveness of the ZVS analysis.

As illustrated in Figs. 6 and 9, the critical voltage gains exist between the LVG structure and MVG structure, as well as between the MVG structure and HVG structure. Therefore, the transition of the operation structure at these critical voltage gains is supposed to be verified experimentally. Based on this, the dynamic transition waveforms at rated power in boost mode are given in Fig. 20, and the dynamic transition waveforms at rated power in buck mode are given in Fig. 21. As can be seen, the fluctuations of output voltage are minimal, which indicates that smooth transitions between adjacent operation structures are achieved. At the same time, the gate drive signal V_{GSp2} and the currents i_{LS1} and i_{LS2} are in agreement with the theoretical analysis in Section II, which further verifies the feasibility and correctness of the proposed converter.

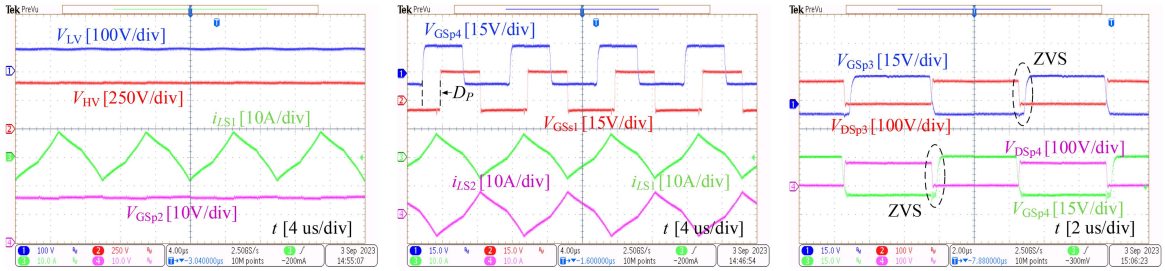
B. Efficiency and Loss Analysis

The curves of the measured conversion efficiency at full load, 50% load, and 20% load are shown in Figs. 22 –24. As seen, the



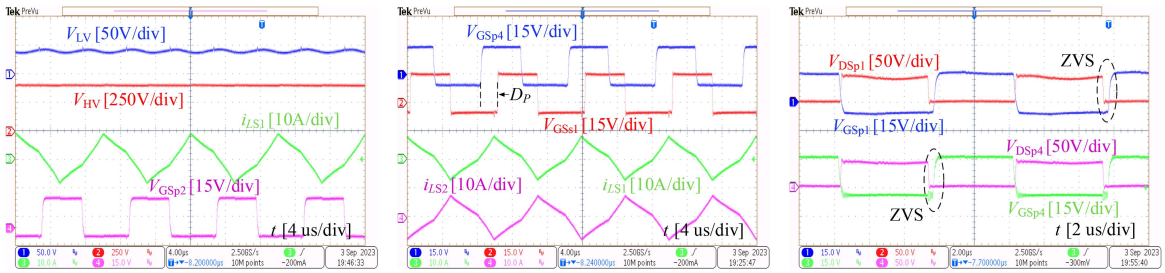
(a) (b) (c)

Fig. 14. Steady waveforms of LVG structure in boost mode ($V_{\mathrm{LV}} = 200$ V). (a) V_{LV}, V_{HV}, i_{LS1} and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1} and i_{LS2}. (c) ZVS waveforms of S_{p3} and S_{p4}.



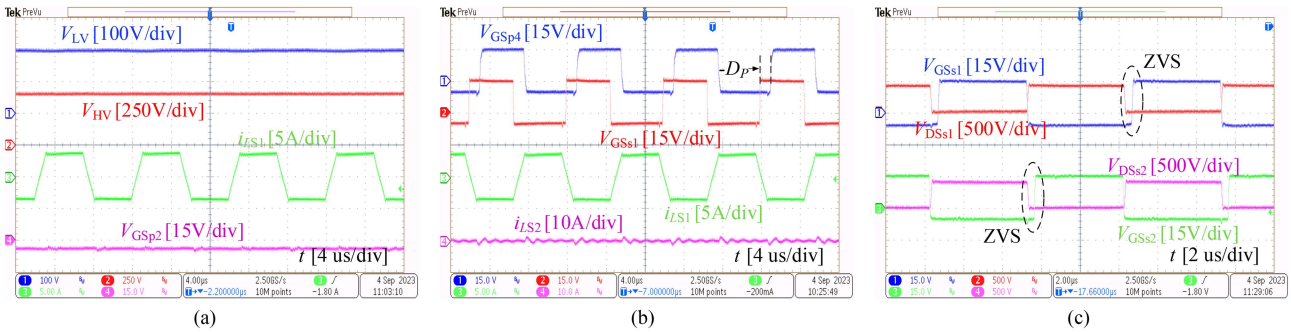
(a) (b) (c)

Fig. 15. Steady waveforms of MVG structure in boost mode ($V_{\mathrm{LV}} = 80$ V). (a) V_{LV}, V_{HV}, i_{LS1} and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1} and i_{LS2}. (c) ZVS waveforms of S_{p3} and S_{p4}.



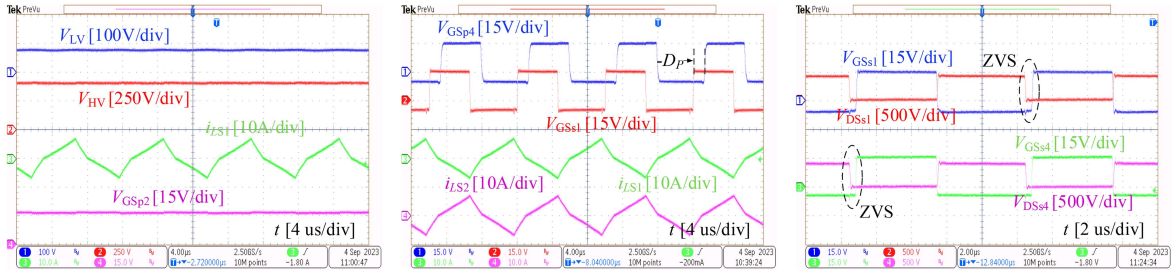
(a) (b) (c)

Fig. 16. Steady waveforms of HVG structure in boost mode ($V_{\mathrm{LV}} = 40$ V). (a) V_{LV}, V_{HV}, i_{LS1}, and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1}, and i_{LS2}. (c) ZVS waveforms of S_{p1} and S_{p4}.



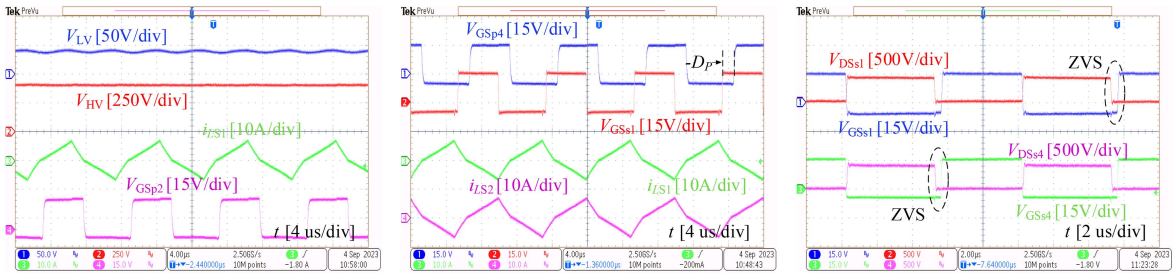
(a) (b) (c)

Fig. 17. Steady waveforms of LVG structure in buck mode ($V_{\mathrm{LV}} = 200$ V). (a) V_{LV}, V_{HV}, i_{LS1}, and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1}, and i_{LS2}. (c) ZVS waveforms of S_{s1} and S_{s2}.



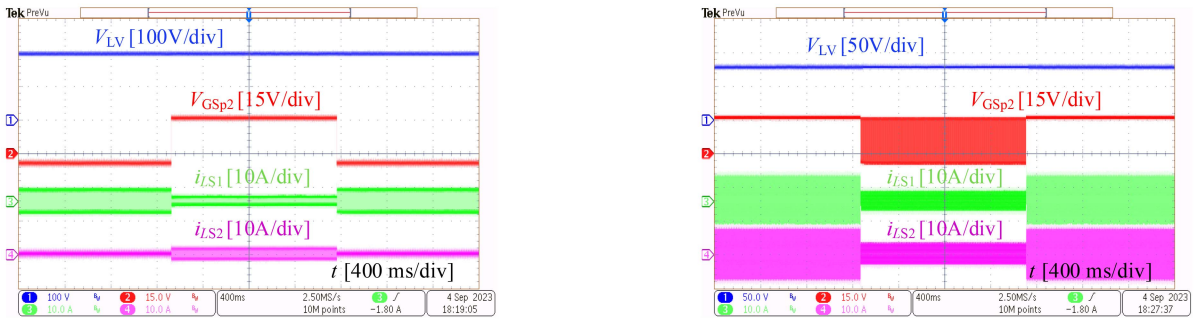
(a) (b) (c)

Fig. 18. Steady waveforms of MVG structure in buck mode ($V_{\mathrm{LV}} = 80$ V). (a) V_{LV}, V_{HV}, i_{LS1}, and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1}, and i_{LS2}. (c) ZVS waveforms of S_{s1} and S_{s4}.



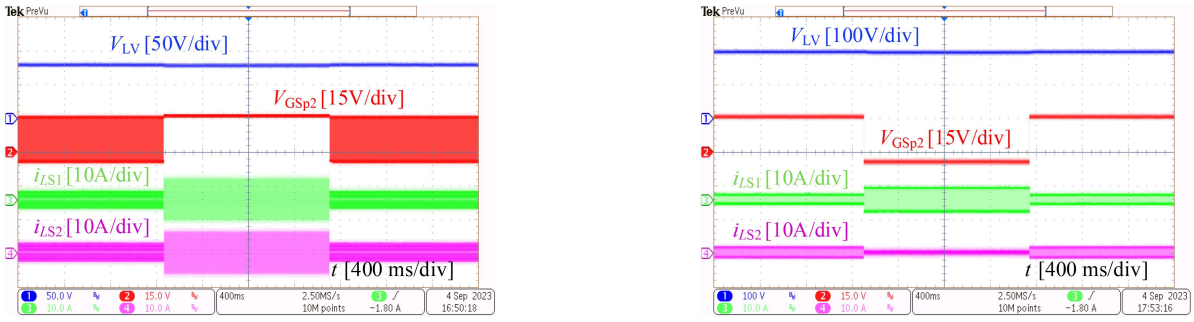
(a) (b) (c)

Fig. 19. Steady waveforms of HVG structure in buck mode ($V_{\mathrm{LV}} = 40$ V). (a) V_{LV}, V_{HV}, i_{LS1}, and V_{GSp2}. (b) V_{GSp4}, V_{GSs1}, i_{LS1}, and i_{LS2}. (c) ZVS waveforms of S_{s1} and S_{s4}.



(a) (b)

Fig. 20. Dynamic transition waveforms between different operation structures in boost mode. (a) From LVG to MVG to LVG. (b) From MVG to HVG to MVG.



(a) (b)

Fig. 21. Dynamic transition waveforms between different operation structures in buck mode. (a) From HVG to MVG to HVG. (b) From MVG to LVG to MVG.

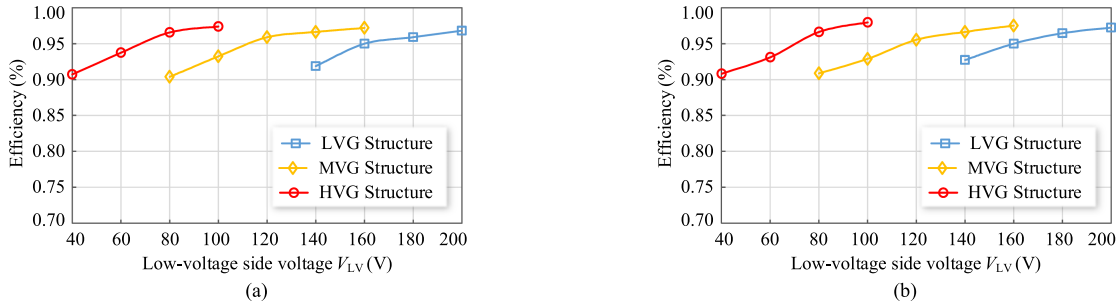


Fig. 22. Measured conversion efficiency at rated load. (a) Conversion efficiency in boost mode. (b) Conversion efficiency in buck mode.

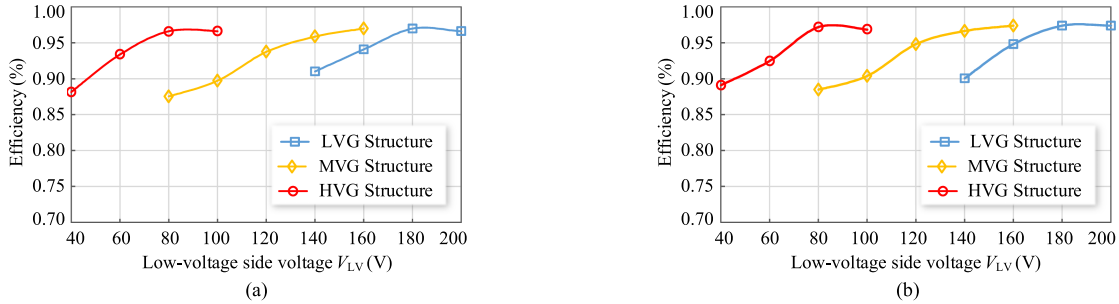


Fig. 23. Measured conversion efficiency at 50% load. (a) Conversion efficiency in boost mode. (b) Conversion efficiency in buck mode.

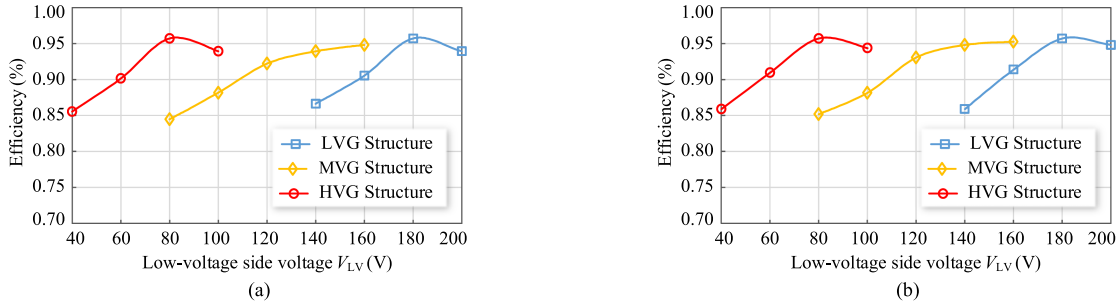


Fig. 24. Measured conversion efficiency at 20% load. (a) Conversion efficiency in boost mode. (b) Conversion efficiency in buck mode.

peak efficiency reaches 97.4% in boost mode and 97.9% in buck mode. Furthermore, combined with the loss model presented in [30], [31], and [32] and the utilized power components, the loss breakdown of the proposed converter can be derived, and the specific loss mathematical equations are presented in the Appendix. To intuitively display the differences in the losses of each component under different operation structures, the loss distribution at several typical operating conditions is plotted as an example, as shown in Figs. 25 and 26. On this basis, by analyzing and comparing the losses of various components in different operation structures, the efficiency advantages of the converter can be better demonstrated.

Combined with the above-mentioned analysis, it can be found that low transformer loss is achieved due to the use of transformers with smaller turn ratios and the avoidance of voltage spikes caused by leakage inductance. Besides, low switching loss is achieved due to the soft-switching operation of power switches. Further, the power components (e.g., transformers, inductors, and power switches) are partially enabled in different operation structures, and the converter is operated in a region where the loop current is relatively small, so that the overall losses of the converter are further reduced. Based on the efficiency test and loss analysis results of different operation structures, it can be concluded that the proposed structure-reconfigurable converter maintains high conversion efficiency within the whole operation range.

C. *Performance Comparison and Analysis*

To evaluate and highlight the performance of the proposed converter, a systematic comparison among various structure-reconfigurable converters is performed. The comparison results are presented in Table III, which focuses on component count, bidirectional power transfer capability, modulation strategy, voltage gain range, and conversion efficiency. Among them, the number of power components directly determines the size and cost of the converter, and the modulation strategy determines the complexity of parameter design and control

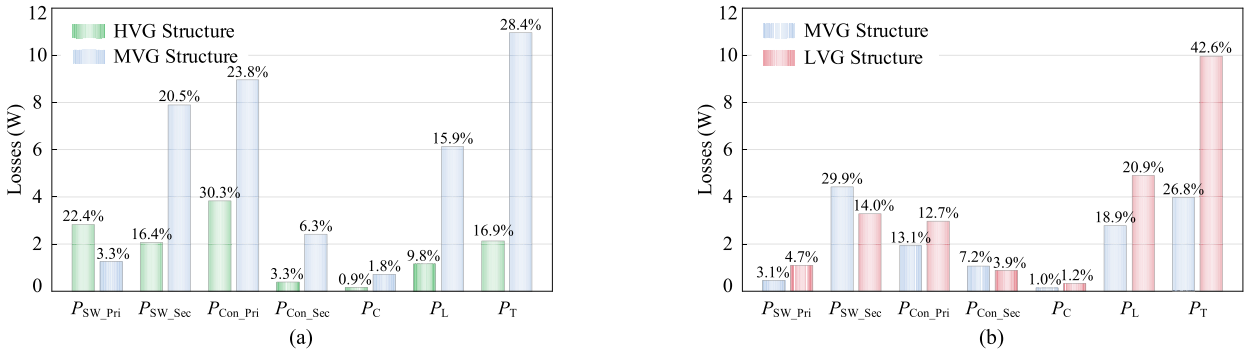


Fig. 25. Loss distribution and comparison of different operation structures in boost mode. (a) $V_{LV} = 100$ V and $P = 500$ W. (b) $V_{LV} = 160$ V and $P = 500$ W.

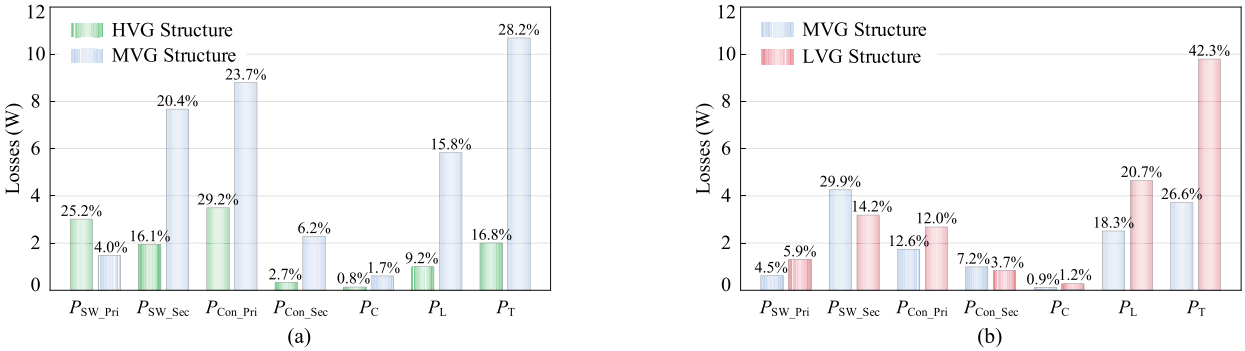


Fig. 26. Loss distribution and comparison of different operation structures in buck mode. (a) $V_{LV} = 100$ V and $P = 500$ W. (b) $V_{LV} = 160$ V and $P = 500$ W.

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH CONVENTIONAL CONVERTERS

Topology		Proposed method	Reference [21]	Reference [22]	Reference [23]	Reference [26]	Reference [27]
Number of	Switches	9	6	7	4	8	12
	Diodes	0	8	3	4	0	0
	Transformers	2	2	1	2	2	1
	Inductors	2	1	1	2	3	2
	Capacitors	5	3	4	4	4	4
Bidirectional power transfer		Yes	No	No	No	Yes	Yes
Modulation Strategy		PSM	PFM	PWM	PFM	PSM	PFM
Switching frequency		100 kHz	80–140 kHz	100 kHz	80–160 kHz	80 kHz	80–180 kHz
Transformer turns ratio_1		1:2	1:5.6	4:27	1:2	1:5	1:2.5
Transformer turns ratio_2		1:2	1:2	/	1:2	1:5	/
Low-voltage side V_{LV}		40–200 V	25–100 V	30–60 V	80–200 V	18–36 V	160–400 V
High-voltage side V_{HV}		400 V	210 V	200/400 V	400 V	250/400 V	400 V
Rated Power		500 W	250 W	500 W	1000 W	1000 W	1000 W
Peak efficiency (Boost / Buck mode)		97.4% & 97.9%	98.0% & Nil	95.4% & Nil	97.5% & Nil	96.4% & 96.2%	93.0% & Nil
Figure of merit S_{FoM}		0.737	2.308	4.245	2.626	1.986	8.172

Modulation Strategy: PWM (Pulse-width modulation), PSM (Phase-shift modulated), PFM (Pulse-frequency modulation).

system. The low-voltage/high-voltage side voltage and transformer turns ratio reflects the voltage gain range. Moreover, the bidirectional power transfer capability and conversion efficiency can be visually compared based on the metrics in Table III.

From the comparison results, it can be concluded that the proposed converter realizes bidirectional power transfer with nine power devices (i.e., switches and diodes) and seven passive devices (i.e., inductors and capacitors), which exhibits competitive cost and volume advantages. Besides, compared with the frequency-modulated strategy used in [21], [23], and [27], the proposed converter employs a fixed-frequency phase-shift modulation strategy to uniformly achieve bidirectional control of different operation structures, which has a simple parameter design and is easy to implement.

In addition, it can be observed that the proposed converter achieves a 2–10 times voltage gain when the turns ratio of the transformers is 1:2. This means that the converter can achieve the same voltage gain conditions with the minimum transformer turns ratio, featuring a smaller core volume and fewer winding turns compared to other converters, thus exhibiting advantages in transformer size and converter compactness. Moreover, as can be seen in Figs. 22–24, the proposed converter can maintain high conversion efficiency over the whole operation range, with peak efficiencies of 97.4% and 97.9% in boost mode and buck mode, respectively. Combined with Table III, it is evident that the efficiency of the proposed converter is higher than most existing wide voltage gain converters.

To make the performance comparison of different converters more convenient, the "Figure of Merit (FoM)" is defined, and its calculation principle is shown in (30). Among them, T_n represents the transformer turns ratio (averaged when more than one transformer exists), N represents the number of active and passive devices, V_{HV} represents the voltage on the high-voltage side, $V_{\mathrm{LV\_min}}$ and $V_{\mathrm{LV\_max}}$ represent the minimum and maximum voltages on the low-voltage side, while η_{E} represents the peak efficiency of different converters (averaged when bidirectional transmission)

$$S_{\mathrm{FoM}} = \frac{N \times T_{\mathrm{n}} \times V_{\mathrm{LV\_min}}}{\eta_E \times V_{\mathrm{HV}} \times V_{\mathrm{LV\_max}}/V_{\mathrm{LV\_min}}} = \frac{N T_{\mathrm{n}} V_{\mathrm{LV\_min}}^2}{\eta_E V_{\mathrm{HV}} V_{\mathrm{LV\_max}}}. \tag{30}$$

In this equation, $V_{\mathrm{HV}}/(T_{\mathrm{n}} \times V_{\mathrm{LV\_min}})$ reflects the maximum voltage gain, while $V_{\mathrm{LV\_max}}/V_{\mathrm{LV\_min}}$ reflects the voltage gain width range. In addition, the performance indicators such as switching frequency and rated output power are not fixed, and only relatively suitable values are selected for verification in various literatures, which are not suitable for FoM assessment. The comparison results of FoM values for different converters based on (30) are shown in Table III. A smaller FoM indicates a better balance between voltage gain width range, conversion efficiency, and power component count, indicating that the corresponding converter has better performance advantages and is more suitable for wide voltage gain range applications. In summary, based on the above-mentioned comparative analysis results, it can be concluded that the proposed converter has significant advantages over the similar converters, which is an excellent candidate for wide voltage gain range applications.

V. Conclusion

This article presents a structure-reconfigurable isolated bidirectional converter for wide voltage gain range applications. The proposed converter can be configured into LVG structure, MVG structure, and HVG structure. These different operation structures can be uniformly controlled with a frequency-fixed phase-shift modulation strategy. Compared with conventional converters, the proposed scheme provides the widest voltage gain range, features simple parameter design, implements high conversion efficiency, and exhibits competitive cost and size advantages, which is promising in practical applications. The operating principles and key characteristics, i.e., the topology structure, voltage gain, power flow, parameter design, and ZVS analysis, are detailed. A 500-W experimental prototype with peak efficiencies of 97.4% and 97.9% is built and tested. The experimental and comparative results validate the theoretical derivation and analysis, and demonstrate the superiority and feasibility of the proposed converter.

APPENDIX

1) The switching loss (P_{SW}) include turn-ON and turn-OFF transient losses, parasitic output capacitor loss, gate charge loss, and body diode reverse-recovery loss, which can be given as

$$\begin{aligned} P_{\mathrm{SW}} = {} & \sigma_1 \times (0.5 f_S V_{\mathrm{DS}} I_{\mathrm{on}} t_{\mathrm{on}}) + \sigma_2 \times (0.5 f_S V_{\mathrm{DS}} I_{\mathrm{off}} t_{\mathrm{off}}) \\ & + \sigma_3 \times (f_S Q_{rr} V_{rr}) + 0.5 f_S C_{\mathrm{oss}} V_{\mathrm{DS}}^2 + f_S Q_g V_g. \end{aligned} \tag{31}$$

In (31), V_{DS} is the drain-source voltage, I_{on} is the current in the turn-ON transient (t_{on}), I_{off} is the current in the turn-OFF transient (t_{off}), C_{oss} is the parasitic output capacitor, Q_{rr} is the reverse recovery charge, V_{rr} is the reverse recovery voltage, Q_g is the total gate charge, and V_{g} is the total gate voltage. Further, depending on the soft-switching realization of the switch, the variables σ_1, σ_2, and σ_3 can be taken as 1 or 0.

2) The conduction loss (P_{CON}) consists of the loss of the MOSFET during the conduction period ($P_{\mathrm{CON,\ Mos}}$) and the loss of its body diode during the dead time ($P_{\mathrm{CON,\ Diode}}$). Among them, $P_{\mathrm{CON,\ Mos}}$ can be obtained by integrating the instantaneous conduction loss over a switching cycle, while $P_{\mathrm{CON,\ Diode}}$ can be obtained by performing calculation on the voltage and current of the body diode during the dead time. Based on this, the conduction loss can be calculated as

$$\begin{aligned} P_{\mathrm{CON}} &= P_{\mathrm{CON,Mos}} + P_{\mathrm{CON,Diode}} \\ &= R_{\mathrm{DSon}} I_{\mathrm{DS,rms}}^2 + V_{\mathrm{Diode}} I_{\mathrm{Diode,rms}}. \end{aligned} \tag{32}$$

In (32), $I_{\mathrm{DS,\ rms}}$ is the root-mean-square (RMS) value of the drain current over a switching cycle, and $I_{\mathrm{Diode,\ rms}}$ is the RMS value of the diode current. R_{DSon} is the on-state resistance of MOSFET, and V_{Diode} is the forward voltage of the body diode, which can be obtained from the datasheet.

3) The inductor loss (P_L) is composed of winding loss ($P_{L,\,\mathrm{Wdg}}$) and core loss ($P_{L,\,\mathrm{Core}}$). Here, $P_{L,\,\mathrm{Wdg}}$ can be obtained by performing calculation on the dc resistance of the winding and the RMS current flowing through the inductor, while $P_{L,\,\mathrm{Core}}$ can be obtained from the empirical formula provided by core manufacturer. From this, the calculation methods of inductor loss can be expressed as

$$\begin{aligned} P_L &= P_{L,\mathrm{Wdg}} + P_{L,\mathrm{Core}} \\ &= I_{L,\mathrm{rms}}^2 R_{L,\mathrm{DC}} + C_m f^{\alpha} B^{\beta} V_{\mathrm{core},L}. \end{aligned} \tag{33}$$

In (33), C_m, α, and β reflect the effect of frequency on core loss, and these values can be obtained from empirical data provided by the core manufacturer. In addition, $V_{\mathrm{core},L}$ is the core volume, and B is the ac flux density.

4) The capacitor loss (P_C) is caused by the equivalent series resistance (ESR), and can be calculated by multiplying $R_{C,\,\mathrm{ESR}}$ with the current RMS value, which can be expressed as

$$P_C = I_{C,\mathrm{rms}}^2 R_{C,\mathrm{ESR}}. \tag{34}$$

5) The transformer loss (P_{T}) includes winding loss ($P_{\mathrm{T},\,\mathrm{Wdg}}$) and core loss ($P_{\mathrm{T},\,\mathrm{Core}}$), which can be calculated separately as (35). The winding loss includes primary winding loss ($P_{\mathrm{Tp},\,\mathrm{Wdg}}$) and secondary winding loss ($P_{\mathrm{Ts},\,\mathrm{Wdg}}$), and the copper loss can be calculated by using the improved Steinmetz equation

$$\begin{cases} P_{T,\mathrm{Wdg}} = P_{\mathrm{Tp,Wdg}} + P_{\mathrm{Ts,Wdg}} \\ \qquad\qquad = I_{\mathrm{Tp,rms}}^2 R_{\mathrm{Tp}} + I_{\mathrm{Ts,rms}}^2 R_{\mathrm{Ts}} \\ P_{T,\mathrm{Core}} = 4^{\alpha} k f_s^{\alpha} B_{\mathrm{pk}}^{\beta} V_{\mathrm{core},T} \end{cases}. \tag{35}$$

Accordingly, the transformer loss can be expressed as (#16). $I_{\mathrm{Tp,rms}}$ and $I_{\mathrm{Ts,rms}}$ are the RMS values of the current through the primary and secondary of the transformer, R_{Tp} and R_{Ts} are the dc resistances of the primary and secondary windings of the transformer. Moreover, $V_{\mathrm{core,T}}$ is the core volume, B_{pk} is half of the peak ac flux density, and the parameters k, α, and β are determined by the selected core material

$$P_T = P_{T,\mathrm{Wdg}} + P_{T,\mathrm{Core}}. \tag{36}$$

In combination with (31)–(36), the theoretical efficiency η_E of the converter can be calculated as

$$\eta_E = 1 - \frac{P_{\mathrm{LOSS}}}{P_{\mathrm{IN}}} = \frac{P_O}{P_O + P_{\mathrm{SW}} + P_{\mathrm{CON}} + P_L + P_C + P_T}. \tag{37}$$

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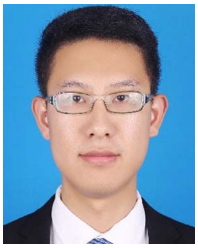
Xianbin Qi (Member, IEEE) received the B.S. degree from China University of Petroleum, Qingdao, China, in 2017, and the M.S. and Ph.D. degrees from Harbin Institute of Technology, Shenzhen, China, in 2019 and 2024, respectively, all in electrical engineering.

From 2022 to 2023, he was a Visiting Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He joined the Hefei University of Technology in 2024. He is currently an Associate Professor with the School of Electrical Engineering and Automation, Hefei University of Technology. His current research interests include battery equalization, bidirectional power conversion, and pulsed power supply systems.



Cheng Yuan was born in Qingdao, China, in 1995. He received the B.S. and M.S. degrees in electrical engineering from the College of New Energy, China University of Petroleum, Qingdao, China, in 2018 and 2021, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Harbin Institute of Technology, Shenzhen, China.

His research interests include power electronics, control of electrical drives, and electrolytic capacitorless ac motor drives.

Mingzhu Fang (Member, IEEE) received the B.S. degree from North China University of Technology, Beijing, China, in 2017, and the M.S. and Ph.D. degrees from Harbin Institute of Technology, Shenzhen, China, in 2019 and 2024, respectively, all in electrical engineering.

Since 2024, she has been with the Deep Space Exploration Laboratory, Hefei, China. Her current research interests include power electronics, dynamic modeling, and aerospace power technology.

Helong Li (Senior Member, IEEE) received the B.S. and M.S. degrees from Harbin Institute of Technology, Harbin, China, in 2010 and 2012, respectively, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2015, all in electrical engineering.

From 2016 to 2019, he worked with Dynex Semiconductor Ltd., as Senior and Principal R&D Engineer in power semiconductor packaging. From 2019 to 2021, he worked with CREE Europe GmbH in the field of SiC automotive applications. Since 2021, he has been with Hefei University of Technology, Hefei, China, as a Professor, focusing on power semiconductor packaging and power electronics applications. He participated in the definition of automotive standard AQG324 for SiC power modules.

Dr. Li serves as a Guest EiC for IEEE OPEN JOURNAL OF POWER ELECTRONICS.

Zhiqing Yang (Member, IEEE) received the B.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2013, and the M.S. and Dr.-Ing. degrees in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2017 and 2021, respectively.

From April to September 2016, he was a Research Intern with Advanced Technology R&D Center, Mitsubishi Electric, Amagasaki, Japan. From 2017 to 2021, he was a Research Associate with the Institute for Power Generation and Storage System, RWTH Aachen University, Aachen, Germany. Since 2022, he has been with Hefei University of Technology, Hefei, China, as an Associate Professor. His research interests include power electronic systems in renewable generations and electric vehicles and pulsed power supply systems.

Shuang Zhao (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in electrical engineering from the University of Arkansas, Fayetteville, AR, USA, in 2019.

In 2018, he was an intern with ABB US Corporate Research Center, Raleigh, NC, USA. In 2019, he joined Infineon Technologies, El Segundo, CA, USA, where he was a Sr. Application Engineer for ATV. Since 2022, he has been with Hefei University of Technology, Hefei, China, as an Associate Professor. His research interests include wide bandgap device application, gate driver, vehicle electrification, and distributed generation.

Dr. Zhao serves as a Guest Co-EiC for IEEE OPEN JOURNAL OF POWER ELECTRONICS, a Guest Editor for IET POWER ELECTRONICS AND MDPI ELECTRONICS.

Lijian Ding (Member, IEEE) received the B.S. and M.S. degrees in electrical materials and insulation technology from the Harbin Institute of Electrical Engineering, Harbin, China, in 1992 and 1995, respectively, and the Ph.D. degree in theory and new technology of electrical engineering from the North China Electric Power University, Beijing, China, in 2000.

He is currently a Professor with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China. He also leads the Institute of Energy, Hefei Comprehensive National Science Center. His research interests include high-voltage technology and fault identification, electromagnetic compatibility and reliability of wide bandgap power semiconductors, and power electronic systems.