A Soft-Switching High Step-Down Regulated DC–DC Converter: Topology Construction and Control Method

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***Abstract*—Resonant switched-capacitor converters have been widely studied and applied with the ability of high efficiency and power density, which well meets the requirements of data center power supply systems. However, due to its operation in DC transformer (DCX) mode, it does not have the ability to regulate voltage, which limits its application in certain situations and makes it difficult to meet the continuously increasing demand for data center applications. This article proposes a soft-switching high voltage step-down ratio hybrid switched-capacitor converter with voltage regulation capability and their corresponding phase-shift voltage regulation method. The voltage regulation principle and soft switching characteristics are analyzed in detail through mathematical derivation. In order to verify the theoretical analysis, an experimental prototype is built. The prototype can achieve 12 V output voltage under 40–60 V input voltage and the power density achieves 1987 W/in^3 with 98.4% peak efficiency.**

***Index Terms*—Hybrid switched-capacitor converter, phase-shift control, voltage regulation, zero-voltage switching.**

I. Introduction

THE rapid development of technologies such as cloud computing and Big Data has brought increasing pressure to data centers [1], [2], [3], [4], [5], [6]. Therefore, continuously improving the efficiency and power density of data center power supply systems under the difficult conditions of low voltage and high current output is a valuable research topic and also a current research hotspot [7]. In order to solve the significant conduction loss caused by high current output, the 48 V bus architecture has been gradually proposed and widely applied [6], [8], [9], [10]. To power the low-voltage devices in the system (e.g., CPU, GPU, memory, and so on) with high efficiency and power density, a two-stage architecture is usually adopted, including an unregulated 48-to-12-V Intermediate bus converters (IBC) as the first stage and a multiphase buck converter as the second stage [10].

However, in addition to supplying power to low-voltage loads such as CPUs and GPUs, the data center power supply system often also needs to supply power to some 12 V high-voltage loads, such as CPU fans, hard disk drives, and batteries [11]. In the 48 V bus power supply system, there is no direct power supply condition for it. Even if a two-stage power supply is selected and the midpoint voltage is 12 V, due to the lack of voltage regulation capability of the front-end converter, once the bus voltage fluctuates, the corresponding 12 V voltage will also fluctuate, thereby affecting the normal operation of the load. In this case, it is often necessary to design a separate power supply for these high-voltage loads, which is very detrimental to the overall efficiency and power density improvement of the data center power supply system. Based on the above reasons, the focus of this article is on the topology structure and control method of the first-stage IBC, with the aim of improving efficiency and power density.

Due to the absence of magnetic components in the circuit, high power density can be achieved, making the switched-capacitor converter a high-quality choice for IBC converters in the data center power supply system. However, the problems such as hard charging and transition voltage spikes make it difficult to achieve high working efficiency, which is a significant disadvantage. The introduction of resonant inductor in the capacitor charging and discharging circuit can solve this problem and achieve efficient and high-density power conversion [12]. Therefore, resonant switched-capacitor (RSC) converters have been gradually studied in recent years [11], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. Among them, it can be seen that existing research on single-stage RSC converters can be divided into the following categories based on the voltage step-down ratio: 2:1, 3:1, 4:1, 6:1, and 8:1 [16], [17], [18], [19], [21], [22], [23]. These converters all have the following characteristics:

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they operate in open-loop mode, have a fixed voltage step-down ratio, and therefore, do not have the ability to regulate the output voltage. Therefore, this article will propose a family of hybrid switched-capacitor (HSC) converters with voltage regulation capabilities and analyze their voltage regulation principles in detail to meet the application requirements of data center power supply systems.

With the increasing research and application of RSC converters, corresponding voltage regulation methods and control strategies have also developed rapidly [11], [24], [25], [26], [27], [28], [29], [30], [31], [32]. Ge et al. [11] proposed a pulse width modulation (PWM) control method for a cascaded 4:1 cascaded RSC converter, which can achieve a stable output of 12 V in the input range of 48–60 V and reduce the capacitance of the decoupling capacitor by merging switch nodes. However, it cannot provide a voltage step-down ratio higher than 0.25.

Zhu and Maksimović [24] proposed a family of transformerless stacked active bridge converters with continuous voltage regulation capabilities. The working state of such converters can be divided according to the switching frequency to the resonant frequency ratio $k = f_{sw}/f_r$. The first mode is when the converter operates in a resonant state, where $k \approx 1$. This means that the converter does not have the ability to regulate voltage and can only achieve a fixed voltage step-down ratio, which means it operates in DC transformer (DCX) mode. At this time, this type of converter can be called an RSC converter. The other mode operates above resonance ($k > 1$), which leads to near-trapezoidal inductor current waveforms and DAB-like regulation capability, and the converter can be referred to as a HSC converter.

The above control method is used for the switched-capacitor-based resonant converter in [25]. In this method, we can adjust the magnitude of the resonant current by adjusting the phase-shift angle, thereby achieving the adjustment of the output voltage. Thus, the voltage conversion ratio can be regulated not only lower but also higher than the nominal value, and the converter can achieve zero voltage switching (ZVS), which greatly improves the efficiency of the converter. Setiadi and Fujita [26] combined the phase-shift control method with the frequency control method proposed in [27], proposing a new symmetrical control method that expands the input voltage and load range that can achieve ZVS in phase-shift control method, enabling it to still achieve ZVS under wide input range and light load conditions. Setiadi and Fujita [29] proposed an asymmetric control method, which adjusts the duty cycle of the devices based on the symmetric control method in [26]. This can expand the ZVS range while reducing the switching frequency, thereby reducing frequency related losses such as driving losses and switching losses, and further increasing work efficiency.

For above mentioned problem, this article proposes a family of regulated HSC converters and provides a detailed analysis of the voltage regulation principle. The rest of this article is organized as follows. Section II proposes a family of high step-down ratio HSC converters based on modular cells. In Section III, a phase-shift control method corresponding to the topology is proposed, and its working mode is analyzed in detail. In Section IV, a detailed analysis is conducted on the implementation conditions

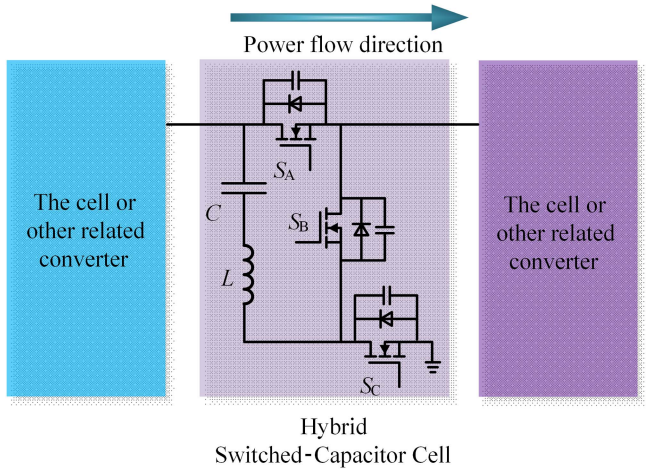

Fig. 1. High voltage step-down ratio DC–DC converter circuit architecture based on proposed hybrid switched-capacitor cells.

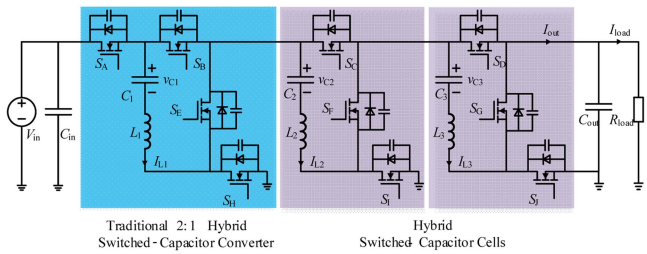

Fig. 2. Proposed 4:1 hybrid switched-capacitor converter.

of its soft switching, and based on this, the resonant parameters in the proposed converter are designed. Section V gives the experimental results of the regulated HSC converter. Finally, Section VI concludes this article.

II. High Step-Down DC–DC Converter Based on Switched-Capacitor Cells

This article proposes a family of high voltage step-down ratio dc–dc converters based on HSC cells, and the circuit architecture is shown in Fig. 1.

As shown in Fig. 1, the input and output sides of this HSC cell can be connected to other HSC converters of the same type to form different circuit structures. In this article, a 2:1 HSC converter is chosen to be connected to the input side of the HSC cell, while on the output side, depending on the number of HSC cells used, the converter can achieve different sizes of nominal voltage step-down ratios. The 3:1 RSC converter proposed in [23] is exactly the form of using only one HSC cell as previous mention architecture. In order to further analyze the working characteristics of this family of converters and meet the application requirements of the 12 V load, this article will take the 4:1 voltage step-down ratio HSC converter as an example for detailed analysis.

The topology structure of the proposed 4:1 HSC converter is shown in Fig. 2. In order to provide the proposed converter with a certain voltage regulation capability, the following analysis in this article will focus on the working state where the resonant

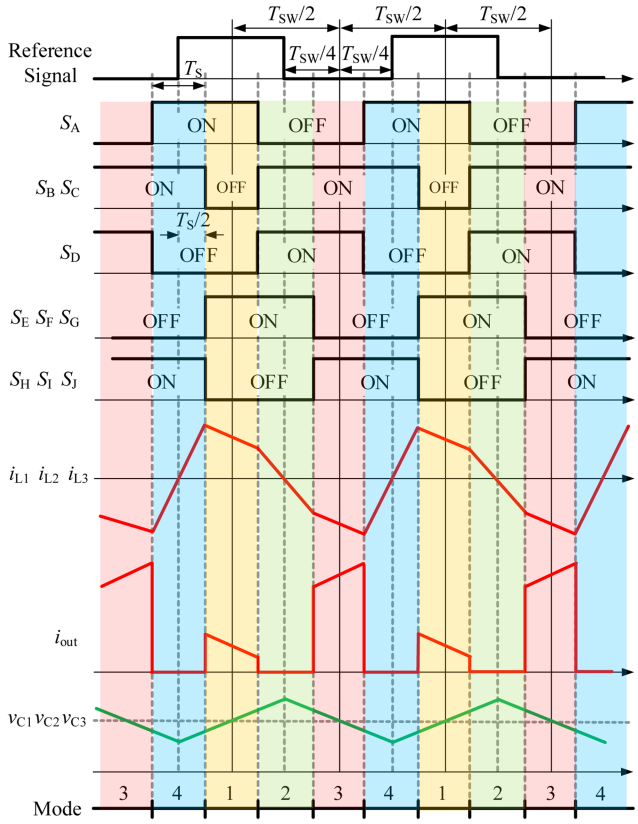

Fig. 3. MOSFETs action timing and key voltage and current waveforms.

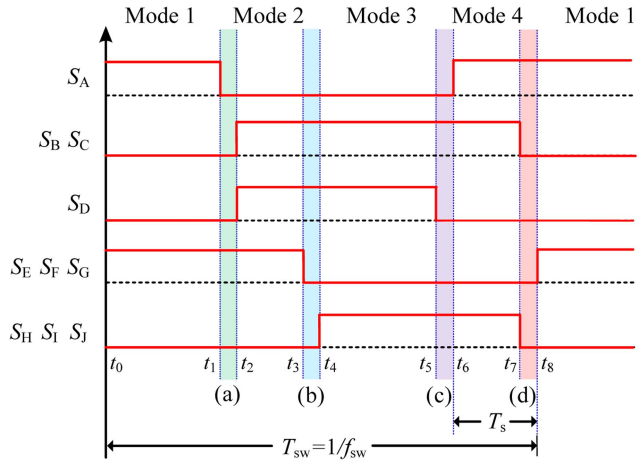

Fig. 4. Driving signal waveforms of each MOSFET.

frequency ratio $k = f_{sw}/f_r > 1$. Taking into account factors such as the voltage regulation capability and working efficiency of the converter, this article ultimately chooses k = 2.

III. Working Mode Analysis and Controller Design

A. Working Mode Analysis Under Phase-Shift Control

For the proposed HSC converter, this article chooses to use phase-shift control method to regulate the output voltage. Under this control method, the driving waveforms of each MOSFET in the 4:1 HSC converter, as well as the waveforms of each inductor current and capacitor voltage, are shown in Fig. 3. The waveforms in this figure correspond to the situation when the converter operates at the nominal voltage step-down ratio, i.e., M = 0.25. M is defined as the voltage step-down ratio of the converter, and its expression is

$$M = V_{\text{out}}/V_{\text{in}}. \tag{1}$$

From Fig. 3, it can be seen that the proposed 4:1 HSC converter has four main operating modes within a complete switching period, and the equivalent circuit of each mode is shown in Fig. 5. Under the proposed phase-shift control strategy, if the angle corresponding to a complete switching period is defined as 360°, then the angle corresponding to mode 2 or mode 4 is the phase-shift angle, and its time length is represented by T_S. In addition, there are four transition states between these four main working modes: state a-state d, as shown in Fig. 4.

In Fig. 3, in order to facilitate the generation of control and driving signals, a reference signal with a frequency equal to the switching frequency of the MOSFET and a duty cycle of 50% is set in this article. All MOSFET driving signals can be obtained by phase shifting the reference signal and changing the duty cycle of the reference signal. In this converter, all MOSFETs except S_B and S_C conduct at a fixed duty cycle of 50%. However, the duty cycle of S_B and S_C will vary with the change of phase-shift angle to ensure a smooth energy transfer path during the duration of Mode 4 and guarantee average voltage 0 in inductors and average current 0 in capacitors. The expression for the duty cycle of S_B and S_C is shown in

$$D_{B,C} = 0.5 + T_S/T_{SW}. \tag{2}$$

In this converter, the transmission and transformation of electrical energy mainly rely on the resonance between the inductors and capacitors. Its resonant frequency is shown in

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{3L_1 \cdot C_1/3}} = \frac{1}{2\pi\sqrt{L_1 C_1}}. \tag{3}$$

It should be noted that there are three sets of *LC* resonant tanks in the converter, and in a certain operating state, the three resonant tanks will be directly connected in series. To ensure that the resonant frequency does not change, the inductance and capacitance values in the three resonant tanks should correspond equally. In order to achieve phase-shift control, the switching frequency f_{SW} should be set at a higher frequency than the resonant frequency of the series resonant circuit f_r. Under this circumstance, the resonant tanks in the circuit have inductive impedance characteristics, therefore, the resonant currents of the resonant tanks can be adjusted by adjusting the magnitude of the phase-shift angle.

Due to the different voltages applied to the inductor in four different modes, the inductor current waveforms are divided into four segments within one switching period. It should be noted that when the switching frequency of the MOSFETs is much higher than the resonant frequency, each segment of the inductor current waveforms will approach straight lines.

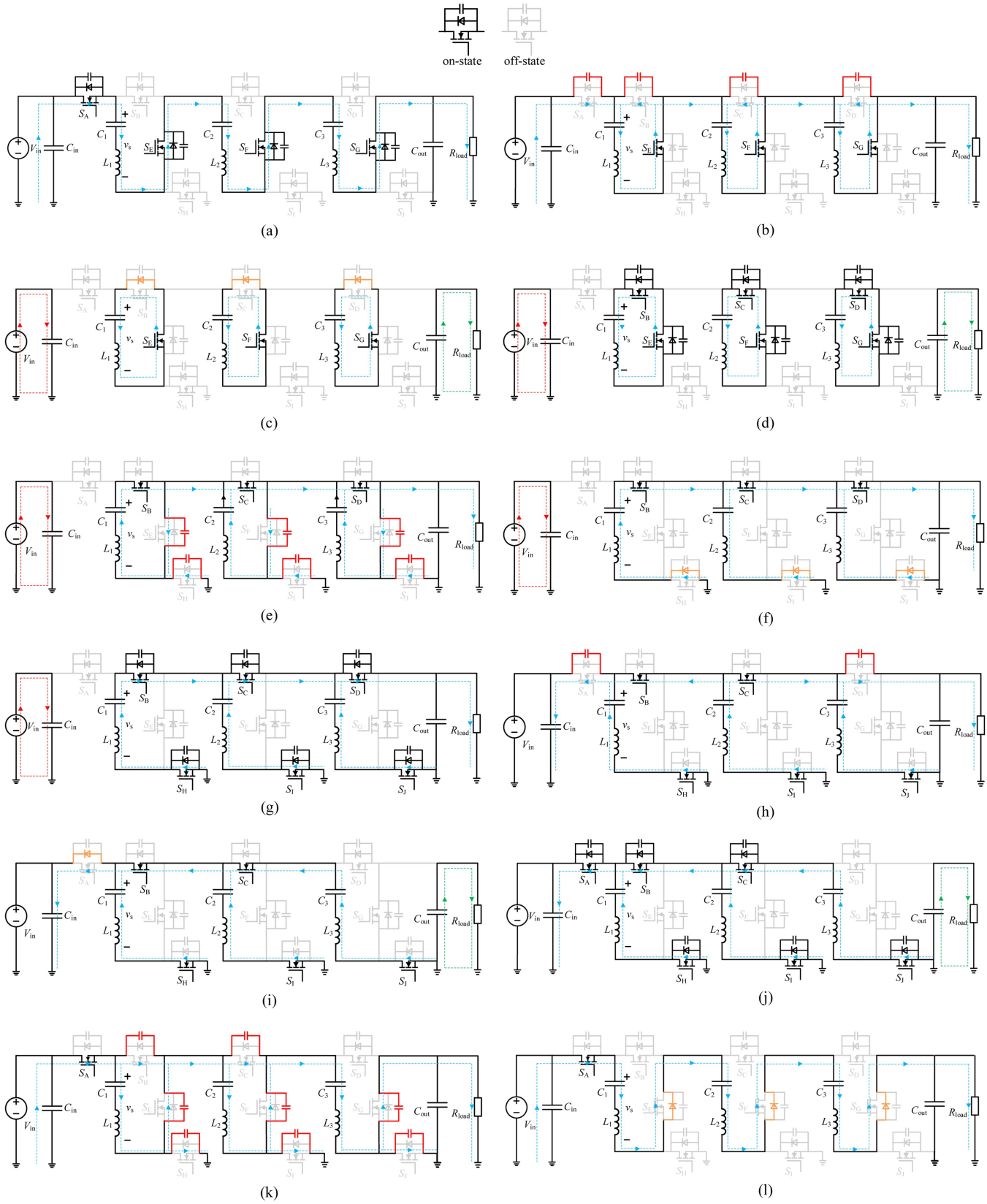

Fig. 5. Equivalent circuit of the converter in each mode within a complete switching period under phase-shift control strategy. (a) Mode 1. (b) The first phase of the transition state a. (c) The second phase of the transition state a. (d) Mode 2. (e) The first phase of the transition state b. (f) The second phase of the transition state b. (g) Mode 3. (h) The first phase of the transition state c. (i) The second phase of the transition state c. (j) Mode 4. (k) The first phase of the transition state d. (l) The second phase of the transition state d.

However, in practical design, considering the impact of high switching frequency on the efficiency of the converter, a very high switching frequency will not be chosen. Taking into account factors such as the voltage regulation capability and working efficiency of the converter, this article ultimately chooses $k = f_{sw}/f_r = 2$. Therefore, in the experiment, the waveform of the inductor currents may exhibit bending, especially in the segments corresponding to mode 1 and mode 3. Since the output current $i_{\rm out}$ is the current obtained by series parallel connection and rectification of resonant currents i_{L1}, i_{L2}, and i_{L3}, the average value of $i_{\rm out}$ is proportional to the amplitude of the resonant currents. Therefore, phase-shift control can achieve adjustment of the output current size. Synchronously adjusting the phase-shift angle when the load changes can also achieve regulated voltage output.

To prevent the occurrence of direct short circuits, a dead time is often added to the driving signal during the state transition process of the converter. If the dead time can be reasonably designed, the converter can achieve ZVS turn-ON of all MOSFETs in the phase-shift control mode, greatly increasing the efficiency of the converter. Next, this article will provide a detailed introduction to the principle of utilizing dead time to achieve ZVS for all MOSFETs through detailed modal analysis.

Fig. 4 shows the detailed driving signal waveforms of each MOSFET in the proposed 4:1 HSC converter under phase-shift control. In order to achieve ZVS for all MOSFETs, this article fully utilizes the dead time between driving signals and adds four transition states on the basis of the original four working modes. The equivalent circuit diagram of these four working modes will be shown in Fig. 5 together with the original four working modes. In these four transition states, the parasitic output capacitors and the body diodes of the MOSFETs are fully utilized.

Taking the transition process from Mode 1 to Mode 2 and Mode 2 to Mode 3 as an example. Before t_1, the converter work in Mode 1, S_A, S_E, S_F, and S_G keep on state, while other MOSFETs stand in OFF state. At t_1, S_A is turned OFF, the converter starts working in State a. The inductor currents commutate from S_A to the parasitic output capacitors of S_B, S_C, and S_D, and charge and discharge them. The voltage across S_A gradually increases, and ZVS can be achieved after this turn-OFF transition. After the parasitic output capacitors are fully discharged, their body diodes start to conduct, and State a enters the second stage. This state will continue until the t_2 moment when S_B, S_C, and S_D conduct with ZVS. Next, the converter starts working in Mode 2. At time t_3, with the shutdown of S_E, S_F, and S_G, the converter operates in another transitional state - State b. At this point, the resonant currents in the circuit flow in the direction shown in Fig. 5(e), charging and discharging the parasitic output capacitors of the MOSFETs in the converter, creating conditions for S_H, S_I, and S_J to achieve ZVS. After the charge exchange process is completed, State b enters the second stage, and the resonant currents flow through the body diodes of S_H, S_I, and S_J. When the turn-ON signals of these three MOSFETs arrive, the currents commutate from the body diode to these three MOSFETs, and the converter officially enters Mode 3. Another transitional process of the converter, which is the state transition process from Mode 3 to Mode 1, can achieve ZVS of the MOSFETs based on similar principles.

From the abovementioned analysis, it can be seen that under the proposed control method, all MOSFETs in the converter can achieve ZVS, which significantly reduces the switching losses generated by the converter during operation, thereby greatly improving the working efficiency. In addition, the good ZVS characteristics allow to choose MOSFETs with lower on state resistance and a relatively large output capacitance, further improving the efficiency.

B. Stress Analysis of Switching Devices

Due to the fact that the operation of the converter proposed in this article relies on the resonance of inductors and capacitors in the circuit, we need to conduct a detailed analysis of the stress borne by the switching devices during the operation of the converter, in order to provide guidance for prototype design.

First, we conducted a detailed analysis of the four working modes during the operation of the converter, and obtained the voltage stress of each MOSFET in the converter. Among them, the stress borne by S_A and S_D is $V_{\rm in} - V_{\rm out}$, the stress borne by S_B and S_C is $(V_{\rm in} - V_{\rm out})/3$, and the stress borne by S_G and S_J is $V_{\rm out}$. In addition, due to the introduction of two new operating modes, namely Mode 2 and Mode 4, in the voltage regulation method proposed in this article, some MOSFETs in the converter will experience increased voltage stress. Therefore, special attention should be paid when selecting components. Among them, S_E and S_F will bear a stress of $V_{\rm in}$, S_H will bear a stress of $(2V_{\rm in} + V_{\rm out})/3$, and S_I will bear a stress of $(V_{\rm in} + 2V_{\rm out})/3$.

Next, we will analyze and calculate the current stress of each component in the converter proposed in this article. The current stresses of the MOSFETs can be derived based on the working mode of the converter and the magnitude of the inductor currents. It should be noted that in this section, each segment of the inductor current waveform is approximately treated as a straight segment. After calculation, when $M > 0.25$, the maximum value of inductor current $I_{\rm Lmax} = I_{\rm LM1}$, while when $M < 0.25$, $I_{\rm Lmax} = I_{\rm LM2}$. The expressions for $I_{\rm LM1}$ and $I_{\rm LM2}$ are shown in

$$I_{LM1} = \frac{T_S' \left(\frac{V_{\rm in}-8V_{\rm out}}{3} - 4V_{C1}\right) + 6T_S\left(V_{\rm in} - V_{C1}\right)}{4L_1} - \frac{T_{sw} I_{\rm out}}{2T_S'} \tag{4}$$

$$I_{LM2} = \frac{T_{sw} I_{\rm out}}{2T_S'} - \frac{T_S' \left(\frac{V_{\rm in}-8V_{\rm out}}{3} - 4V_{C1}\right) + 2T_S\left(V_{\rm in} - V_{C1}\right)}{4L_1}. \tag{5}$$

After obtaining the maximum value of the inductor currents, we can determine the current stress that each MOSFET needs to bear based on its connection relationship with the inductors. Among them, the current stress that S_A and S_D need to bear is $3I_{\rm Lmax}$, the current stress that S_B and S_C need to bear is $2I_{\rm Lmax}$, and the current stress that other devices need to bear is $I_{\rm Lmax}$.

TABLE I
COMPARISON OF STRESS BETWEEN THREE TOPOLOGIES

		Cascaded 4:1 RSC	S-P 4:1 RSC	Novel 4:1 HSC (this work)	
Operation mode		Open loop	Open loop	Open loop	Phase-shift control
Voltage stress	V_o	S_E-S_H	S_C, S_D, S_G, S_I, S_J	S_B-S_G, S_J	S_B, S_C, S_G, S_J
	$2V_o$	S_A-S_D	S_B, S_F	S_I	S_I
	$3V_o$		S_A, S_E, S_H	S_A, S_H	S_A, S_D, S_H
	$4V_o$				S_E, S_F
Current stress	I_{Lmax}	S_A-S_D	S_A-S_J	S_A, S_B, S_E-S_J	S_E-S_J
	$2I_{Lmax}$	S_E-S_H		S_C	S_B, S_C
	$3I_{Lmax}$			S_D	S_A, S_D

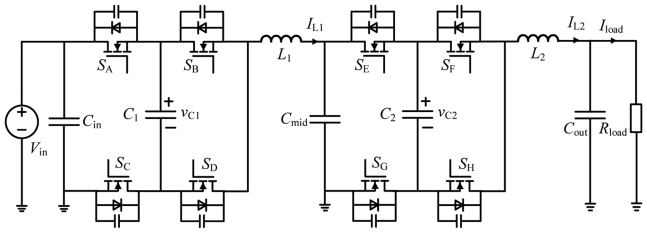

Fig. 6. Cascaded 4:1 resonant switched-capacitor converter.

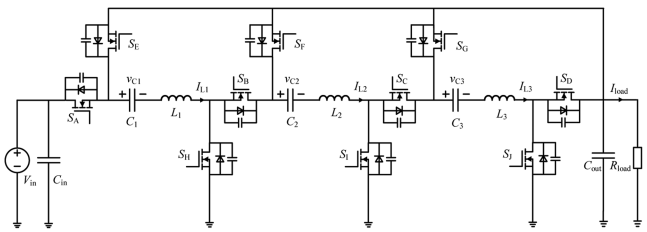

Fig. 7. Series-parallel 4:1 resonant switched-capacitor converter.

Next, this article compares the component stress of the proposed converter with two other hybrid (resonant) switched-capacitor converters that can achieve a 4:1 voltage step-down ratio under full load operating conditions. The topology structures of the two converters are shown in Figs. 6 and 7, respectively. The stress of the components in the two converters is shown in Table I.

According to Table I, when operating in open-loop unregulated mode, although the total current stress of the converter proposed in this article is greater than that of Series-parallel 4:1 SCC, its voltage stress is significantly smaller. Overall, the total stress of the three converters is not significantly different. In addition, the two-stage structure of the Cascaded 4:1 RSC converter has a significant disadvantage in terms of power density. The biggest advantage of the converter proposed in this article is that it can adjust the output voltage through phase-shift control, which Series-parallel 4:1 RSC and Cascaded 4:1 RSC cannot achieve. However, when the converter operates in phase-shift voltage regulation mode, the voltage and current stress that the device needs to bear both increase significantly. That is to say, the converter can regulate the output voltage at the cost of increasing stress, which should be particularly noted in practical applications.

C. Mathematical Derivation of the Relationship Between the Average Output Current and the Phase-Shift Angle

In order to facilitate the design of the phase-shift controller in the following section, this article will derive the mathematical relationship between the average output current of the converter and the phase-shift angle under stable operating conditions.

The following assumptions are made to derive the mathematical relationships: The input voltage and output voltage of the converter are constant; The parasitic parameters such as parasitic resistance and inductance of all components in the converter are ignored; The switching characteristics of MOSFETs are ideal, i.e., without considering their rising and falling times, so the driving signal does not require deadtime.

In addition, it should be noted that when the voltage step-down ratio of the converter deviates from the nominal value, the slope of the inductor current waveform in each section will change, but its overall trend remains unchanged. Moreover, since the voltage step-down ratio deviating from the nominal value only operates within a small range of bus voltage fluctuations in the application background of this article, it can be assumed that its slope remains unchanged and the inductor current waveform is symmetrical in this analysis.

From Figs. 2 and 3, it can be seen that the 4:1 HSC converter contains three sets of *LC* resonant tanks, whose parameters and the operating state are exactly the same, and the output current is obtained by combining the three resonant currents in series or parallel under different operating modes. Therefore, this article only provides a detailed analysis and calculation of one group of resonant tanks.

The voltage applied to the resonant tank v_s has different values under different operating modes, and its expression is shown in (6).

It should be noted that since the three *LC* resonant tanks in the circuit are directly connected in series in Mode 1, the voltage applied to a single resonant tank is not a constant value, but will have a certain amplitude of oscillation. But the impact of this oscillation on the working state of the resonant tank can be ignored. Therefore, in this article, the average value is chosen as the voltage added to the resonant tank in Mode 1

$$v_s = \begin{cases} V_{\text{in}} & \text{Mode 4} \\ (V_{\text{in}} - V_{\text{out}})/3 & \text{Mode 1} \\ 0 & \text{Mode 2} \\ V_{\text{out}} & \text{Mode 3.} \end{cases} \tag{6}$$

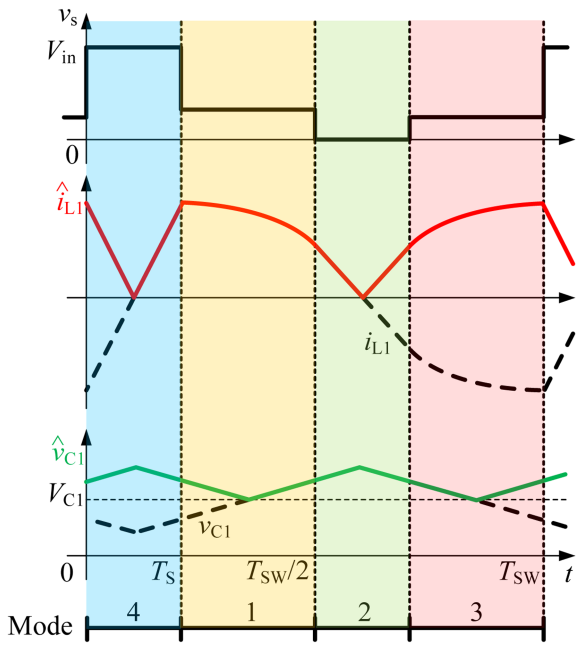

Fig. 8. Key waveform of the resonant tank.

In this case, the key waveform of the resonant tank is shown in Fig. 8. In Fig. 8, for the convenience of subsequent derivation, the two state variables were transformed as

$$\hat{i}_{L1}(t) = |i_{L1}(t)| \tag{7}$$

$$\hat{v}_{C1}(t) = V_{C1} + |v_{C1}(t) - V_{C1}|\,. \tag{8}$$

In the above equation, V_{C1} is the average value of the resonant capacitor voltage. To solve this parameter, it is first necessary to obtain the expression of the resonant capacitor voltage v_{C1} within one switching cycle.

First, set a starting time T_0, where the initial values of the state variables are I_{L10} and V_{C10}, respectively. From a transient analysis of the circuit, the following expressions for the resonant capacitor voltage and resonant current can be derived:

$$i_{L1}(t) = \frac{v_s - V_{C10}}{\omega_r L_1}\sin\omega_r(t-T_0) + I_{L10}\cos\omega_r(t-T_0) \tag{9}$$

$$v_{C1}(t) = V_{C10} + \omega_r^2 L_1 \int_{T_0}^{t} i_{L1}(t)dt$$

$$= (V_{C10} - V_s)\cos\omega_r(t-T_0) + Z_1 I_{L10}\sin\omega_r(t-T_0) + V_s \tag{10}$$

where ω_r is the angular resonant frequency, which can be expressed as

$$\omega_r = \frac{1}{\sqrt{L_1 C_1}}. \tag{11}$$

From (10), it can be seen that the expression of the resonant capacitor voltage consists of three terms, among which the first two terms containing the trigonometric function determine the amplitude of its voltage fluctuation, while the third term determines the steady-state value of the voltage. Therefore, the average value of the resonant capacitor voltage within one switching period is equal to the average value of the resonant tank voltage.

As shown in Fig. 3, the duration of Modes 2 and 4 within a switching period is T_S, and the duration of Modes 1 and 3 is $T_{SW}/2 - T_S$. Therefore, the expression for V_{C1} is

$$V_{C1} = \frac{[(V_{in}-V_{out})/3 \bullet (T_{SW}/2-T_S) + V_{out} \bullet (T_{SW}/2-T_S) + V_{in} \bullet T_S]}{T_{SW}}$$

$$= \frac{T_{SW}(V_{in}+2V_{out}) + 4T_S(V_{in}-V_{out})}{6T_{SW}}. \tag{12}$$

Next, this article will analyze the four working modes separately to derive their average output current.

1) Mode 4 ($0 < t < T_S$): In this mode, $T_0 = 0$, $v_s = V_{in}$, $I_{L10} = -\hat{i}_{L1}(0)$, and $V_{C10} = 2V_{C1} - \hat{v}_{C1}(0)$, the expressions for the two state variables at the end of this mode are as follows:

$$\hat{i}_{L1}(T_S) = \frac{V_{in} - [2V_{C1} - \hat{v}_{C1}(0)]}{\omega_r L_1}\sin\omega_r T_S - \hat{i}_{L1}(0)\cos\omega_r T_S \tag{13}$$

$$\hat{v}_{C1}(T_S) = [2V_{C1} - \hat{v}_{C1}(0)] + \omega_r^2 L_1 \int_0^{T_S} i_{L1}(t)dt \tag{14}$$

where

$$i_{L1}(t) = \frac{V_{in} - [2V_{C1} - \hat{v}_{C1}(0)]}{\omega_r L_1}\sin\omega_r t - \hat{i}_{L1}(0)\cos\omega_r t. \tag{15}$$

2) Mode 1 ($T_S < t < T_{SW}/2$): In this mode, $T_0 = T_S$, $v_s = (V_{in} - V_{out})/3$, $I_{L10} = \hat{i}_{L1}(T_S)$, and $V_{C10} = 2V_{C1} - \hat{v}_{C1}(T_S)$, the expressions for the two state variables at the end of this mode are as follows:

$$\hat{i}_{L1}(T_{SW}/2) = \frac{(V_{in} - V_{out})/3 - [2V_{C1} - \hat{v}_{C1}(T_S)]}{\omega_r L_1} \sin\omega_r\left(\frac{T_{SW}}{2} - T_s\right) + \hat{i}_{L1}(T_S)\cos\omega_r\left(\frac{T_{SW}}{2} - T_s\right) \tag{16}$$

$$\hat{v}_{C1}(T_{SW}/2) = [2V_{C1} - \hat{v}_{C1}(T_S)] + \omega_r^2 L_1 \int_{T_S}^{T_{SW}/2} i_{L1}(t)dt \tag{17}$$

where

$$i_{L1}(t) = \frac{(V_{in} - V_{out})/3 - [2V_{C1} - \hat{v}_{C1}(T_S)]}{\omega_r L_1}\sin\omega_r(t - T_S) + \hat{i}_{L1}(T_S)\cos\omega_r(t - T_S)\,. \tag{18}$$

According to (18), the average output current under these two modes can be obtained as follows:

$$I_{out1} = \frac{\int_{T_S}^{T_{SW}/2} i_{L1}(t)\,dt}{T_{SW}/2}. \tag{19}$$

3) Mode 2 ($T_{SW}/2 < t < T_{SW}/2 + T_S$): In this mode, $T_0 = T_{SW}/2$, $v_s = 0$, $I_{L10} = \hat{i}_{L1}(T_{SW}/2)$, and $V_{C10} = \hat{v}_{C1}(T_{SW}/2)$, the expressions for the two state variables at the

end of this mode are as follows:

$$\hat{i}_{L1}(T_{SW}/2+T_S) = -\frac{\hat{v}_{C1}(T_{SW}/2)}{\omega_r L_1}\sin\omega_r T_s + \hat{i}_{L1}(T_{SW}/2)\cos\omega_r T_s \quad (20)$$

$$\hat{v}_{C1}(T_{SW}/2+T_S) = \hat{v}_{C1}(T_{SW}/2) + \omega_r^2 L_1 \int_{T_{SW}/2}^{T_{SW}/2+T_S} i_{L1}(t)dt \quad (21)$$

where

$$i_{L1}(t) = -\frac{\hat{v}_{C1}(T_{SW}/2)}{\omega_r L_1}\sin\omega_r\left(t-\frac{T_{SW}}{2}\right) + \hat{i}_{L1}(T_{SW}/2)\cos\omega_r\left(t-\frac{T_{SW}}{2}\right). \quad (22)$$

4) Mode 3 ($T_{SW}/2+T_S < t < T_{SW}$): In this mode, $T_0 = T_{SW}+T_S$, $v_s = V_{\text{out}}$, $I_{L10} = -\hat{i}_{L1}(T_{SW}/2+T_S)$, and $V_{C10} = \hat{v}_{C1}(T_{SW}/2+T_S)$, according to the periodicity of the state variables, their values at the end of this mode are exactly equal to the initial values of mode 4, and their expressions are as follows:

$$\hat{i}_{L1}(0) = \hat{i}_{L1}(T_{SW}) = \frac{V_{\text{out}}-\hat{v}_{C1}(T_S+\frac{T_{SW}}{2})}{\omega_r L_1}\sin\omega_r\left(\frac{T_{SW}}{2}-T_s\right) - \hat{i}_{L1}\left(T_S+\frac{T_{SW}}{2}\right)\cos\omega_r\left(\frac{T_{SW}}{2}-T_s\right) \quad (23)$$

$$\hat{v}_{C1}(0) = \hat{v}_{C1}(T_{SW}) = \hat{v}_{C1}\left(T_S+\frac{T_{SW}}{2}\right) + \omega_r^2 L_1\int_{T_{SW}/2+T_S}^{T_{SW}} i_{L1}(t)dt \quad (24)$$

where

$$i_{L1}(t) = \frac{V_{\text{out}}-\hat{v}_{C1}(T_S+\frac{T_{SW}}{2})}{\omega_r L_1}\sin\omega_r\left[t-\left(T_S+\frac{T_{SW}}{2}\right)\right] - \hat{i}_{L1}\left(T_S+\frac{T_{SW}}{2}\right)\cos\omega_r\left[t-\left(T_S+\frac{T_{SW}}{2}\right)\right]. \quad (25)$$

Due to the parallel output of three resonant tanks in Mode 3, the average output current at this time should be three times the average current of each resonant tank, as shown in (26). The expression for $i_{L1}(t)$ is shown in (25)

$$I_{\text{out2}} = 3\times\frac{\int_{T_{SW}/2+T_S}^{T_{SW}} i_{L1}(t)\,dt}{T_{SW}/2}. \quad (26)$$

Due to the complexity of the derivation process, the derivation process and intermediate results are not presented here, only the final result is provided. The key steps of the derivation process can be found in the Appendix. It can be obtained that the average output current of the circuit throughout the entire switching period can be obtained as

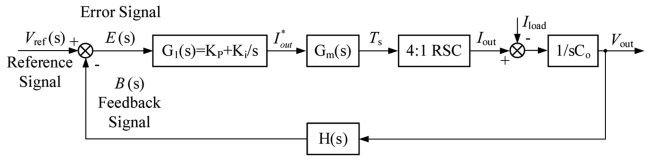

Fig. 9. Block diagram of the output voltage controller.

$$I_{\text{out}} = \frac{4A\omega_r L_1\sin(\omega_r T_S')+\left[8V_{C1}-4B-\frac{4}{3}(V_{\text{in}}-V_{\text{out}})\right]\cos(\omega_r T_S')}{T_{SW}\omega_r^2 L_1} \quad (27)$$

where

$$T_S' = \frac{T_{SW}}{2}-T_S. \quad (28)$$

In (27), for the convenience of expression and calculation, intermediate variables A and B are defined, and their expressions are shown in

$$A = \frac{[V_{\text{in}}(1+\omega_r L_1)-2V_{C1}]\sin(\omega_r T_S)}{2\omega_r L_1(1+\cos\omega_r T_S)} \quad (29)$$

$$B = \frac{[2V_{C1}-(1+Z_1)V_{\text{in}}]\sin^2\omega_r T_S}{2(1+\cos\omega_r T_S)^2} + \frac{[2V_{C1}-V_{\text{in}}]\cos\omega_r T_S+V_{\text{in}}}{1+\cos\omega_r T_S} \quad (30)$$

where Z1 is the characteristic impedance of the *LC* resonant tank, which can be expressed as

$$Z_1 = \sqrt{\frac{L_1}{C_1}}. \quad (31)$$

When the load is light, achieving the same voltage conversion ratio requires a smaller phase-shift angle. When the angle is small enough, the simplified formula shown in (32) can be used for calculation and controller design

$$I_{\text{out}} = \frac{\left[8V_{C1}-4\frac{[2V_{C1}-V_{\text{in}}]\cos\omega_r T_S+V_{\text{in}}}{1+\cos\omega_r T_S}-\frac{4}{3}(V_{\text{in}}-V_{\text{out}})\right]\cos(\omega_r T_S')}{T_{SW}\omega_r^2 L_1}. \quad (32)$$

D. Closed Loop Controller Design

Based on the theoretical derivation in the previous text, this article obtains the transfer function of the proposed 4:1 HSC converter, which can be used for the design of a closed-loop controller. The block diagram of the output voltage controller for the proposed 4:1 HSC converter is shown in Fig. 9.

Adopting traditional proportional integral (PI) control for closed-loop control of HSC converter. In Fig. 9, K_p is a proportional gain, K_i is an integral gain, $G_m(s)$ is the transfer function of the phase shift controller, whose expression is shown in (33),

and H(s) is the transfer function of the feedback voltage divider network

$$G_m(s) = \frac{T_S}{I^*_{\text{out}}}. \tag{33}$$

The reference of the averaged output current is given as follows:

$$I^*_{\text{out}}(s) = G_1(s)E(s) = \left(K_p + \frac{K_i}{s}\right)\left[V_{ref}(s) - B(s)\right]. \tag{34}$$

The feedback control proposed in this article achieves precise voltage regulation, despite the input voltage fluctuations and voltage drops in switching devices in the system, and does not require any current sensors.

IV. Analysis of the Requirements for the ZVS Operation

Based on the analysis of the ZVS principle in the previous section, we can draw the following conclusion: the most critical factors determining whether the MOSFETs can achieve ZVS are the magnitude and direction of the resonant inductor currents. If the resonant inductor currents are very small during the state transition process, the converter will not be able to fully charge and discharge the parasitic output capacitors of the MOSFETs. At this point, the energy stored in the parasitic output capacitors of the MOSFETs that has not been released will be consumed on the MOSFETs during the conduction process, causing significant switching losses.

Taking State a in Fig. 5(b), as an example, the parasitic output capacitor of S_B is discharged by the inductor current i_{L1}, and its voltage decreases during the first phase of State a. Assuming that the capacitance of the parasitic capacitors of all MOSFETs are much smaller than that of the resonant capacitors. At this point, the parasitic capacitor C_s will resonate with the resonant inductor L_1. The expression for the resonant current is shown in

$$i_{rs}(t) = I_{a0}\cos\omega_{rs}t \tag{35}$$

where I_{a0} is the initial value of the inductor current in State a. ω_{rs} is the angular resonant frequency, which can be expressed as

$$\omega_{rs} = \frac{1}{\sqrt{2C_sL_1}}. \tag{36}$$

The parasitic capacitor voltage can be calculated using the following equation:

$$v_{ss}(t) = \frac{V_{\text{in}}}{4} - \frac{1}{2C_s}\int_0^{\tau} i_{rs}(\tau)d\tau. \tag{37}$$

The expression for parasitic capacitor voltage can be obtained by combining (35) and (37)

$$v_{ss}(t) = \frac{V_{\text{in}}}{4} - I_{a0}\sqrt{\frac{L_1}{2C_s}}\sin\omega_{rs}t. \tag{38}$$

During the state transition process, if the current is sufficient to completely discharge the parasitic capacitor of the MOSFET, its voltage should be reduced to 0. But when the resonant inductor current is too small to fully discharge it, the capacitor voltage will reach its minimum value at $t = \pi/2\omega_{rs}$. Therefore, the length of the dead time should be set to: $t_{\text{dead}} = \pi/2\omega_{rs}$, to ensure the minimum switching losses. From this, the condition required to achieve ZVS can also be obtained

$$I_{a0} \geq V_{\text{in}}\sqrt{\frac{C_s}{8L_1}}. \tag{39}$$

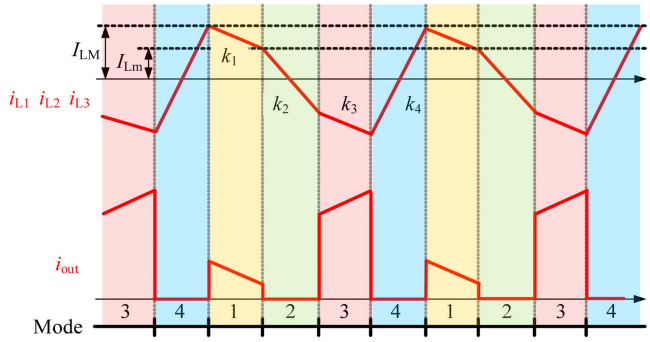

Fig. 10. Detailed drawings of resonant currents and output current.

Fig. 10 shows the detailed waveforms of the resonant currents and the output current. It is still assumed that the switching frequency is sufficiently high, and each waveform segment is approximately straight. Since the resonant capacitor voltage v_{Cr} is equal to V_{C1} on average, V_{C1} and $V_{\text{in}} - V_{C1}$ are applied to the inductors in modes 2 and 4, respectively. Therefore, the slope of current variation in modes 2 and 4 are shown as

$$k_2 = -\frac{V_{C1}}{L_1} \tag{40}$$

$$k_4 = \frac{V_{\text{in}} - V_{C1}}{L_1}. \tag{41}$$

Similarly, the slopes of the resonant currents in modes 1 and 3 can be obtained

$$k_1 = \frac{(V_{\text{in}} - V_{\text{out}})/3 - V_{C1}}{L_1} \tag{42}$$

$$k_3 = \frac{V_{\text{out}} - V_{C1}}{L_1}. \tag{43}$$

From the abovementioned expression, it can be seen that the size of the resonant inductance directly determines the slope of the resonant current in each mode. The smaller the resonant inductors, the greater the slopes of the resonant currents, and at the same time, the larger I_{LM}, the smaller I_{Lm}. Therefore, the requirement for ZVS operation in (39) can be represented by

$$I_{Lm} \geq V_{\text{in}}\sqrt{\frac{C_s}{8L_1}}. \tag{44}$$

In the design process of the converter, the sizes of the resonant inductors should be reasonably designed to meet (44) within the maximum possible scope of work. After considering the voltage regulation capability of the converter, the range of soft switching implementation, and the power density of the converter, this article chooses a resonant inductance of 470 nH.

According to (44), under the input condition of 40 V, 48 V, and 60 V, the minimum I_{Lm} required to achieve ZVS of all MOSFETs

TABLE II
PARAMETERS OF MAIN COMPONENTS

Component	Manufacture and Part number	Value/Parameter
80V MOSFET	Infineon, IQE050N08NM5CG	80V, 5.0mΩ Profile: 3.3*3.3*1.1(mm)
40V MOSFET	Infineon, IQE013N04LM6CG	40V, 1.35mΩ Profile: 3.3*3.3*1.1(mm)
Resonant capacitor C_1, C_2, C_3,	Murata, GRM21BZ71H475KE15L SAMSUNG, CL21B105KBFNNNE	4.7μF*, 50V, X7R, 0805×6 1μF*, 50V, X7R, 0805×9
Resonant inductor L_1, L_2, L_3,	Coilcraft, XGL6030-471MEC	470nH, ±20%
Gate driver	Linear Technology, LTC4440ES6-5	80V
Bootstrap diode	Infineon, BAT6402VH6327XTSA1	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

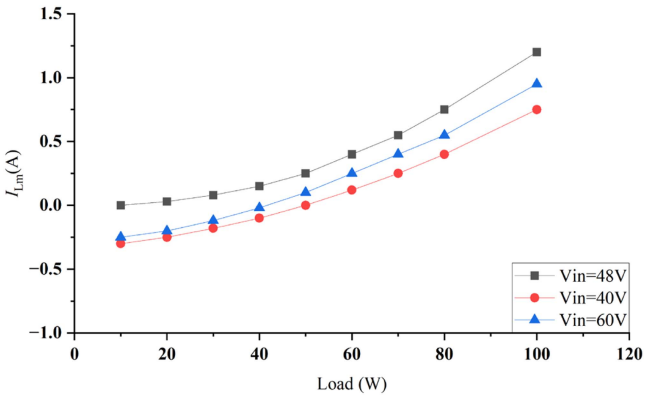

Fig. 11. Variation curve of I_{Lm} with load.

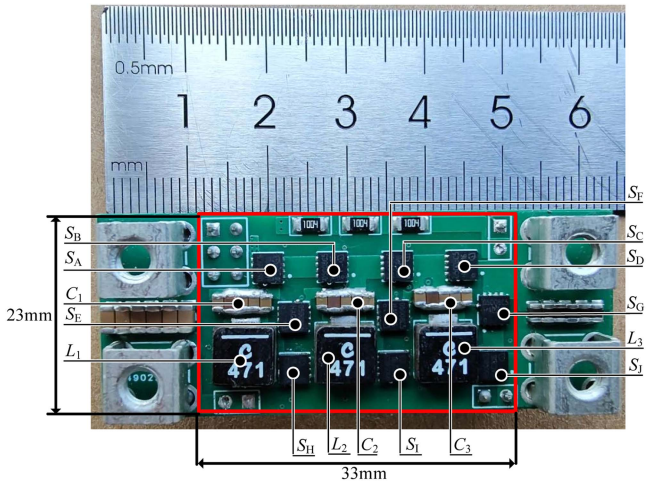

Fig. 12. Picture of the designed prototype.

are 0.358 A, 0.429 A and 0.536 A, separately. After theoretical calculation and simulation verification, the curves of I_{Lm} values with load variation under three input conditions during light load operation are shown in Fig. 11.

According to the curve in Fig. 11, Under the rated input condition of 48 V, the minimum load value that can achieve ZVS for all MOSFETs in the converter is about 56 W. Under the input conditions of maximum 60 V/minimum 40 V, the minimum load values are 76 W/72 W, respectively. Using the same method, the minimum load value that the converter can achieve soft switching of all MOSFETs at any point within the full range of input voltage can be estimated.

V. EXPERIMENTAL RESULTS

To verify the above design and analysis, a 4-to-1 regulated HSC converter prototype is built in the laboratory. Taking into account the voltage regulation capability, working efficiency, and power density of the converter, the resonant frequency of the resonant tanks in the converter is set to 100 kHz, and the switching frequency of the switching devices is set to 200 kHz. Moreover, the flying capacitors and resonant inductors are carefully selected to achieve good soft switching and voltage regulation characters. A full component list of the prototype is provided in Table II.

The picture of the prototype is shown in Fig. 12. This article placed a ruler next to the prototype to more clearly evaluate the size of the converter. A six-layer printed circuit board (PCB) board with 2 oz. copper for each layer is designed to increase the current carrying capacity and reduce the trace resistance. The main circuit section, including the MOSFETs, flying capacitors, and resonant inductors, are placed on the top layer of the PCB. The driver circuit, including the driver chips, bootstrap diodes, and bootstrap capacitors, are placed on the back of the PCB. The gate drive power is provided by the cascaded bootstrap method in [32]. Due to the fact that the novel 4:1 HSC converter proposed in this article has three grounded switching devices, all 10 switching devices in the circuit will be divided into three groups based on their connection relationship with the three grounded devices, and will be bootstrapped separately. Among them, S_A, S_B, S_E, S_H are a group; S_C, S_F, S_I are the second group; S_D, S_G, and S_J are the third group. The driving circuit of the first group of MOSFETs is shown in Fig. 13, and the driving principles of the other two groups of MOSFETs are the same. Through this design, the converter proposed in this article achieves high power density of 1987 W/in^3.

Fig. 14 shows the experimental waveforms of output voltage, resonant capacitor voltage, and resonant inductor current at rated input voltage and maximum/minimum input voltage under a full-load (300 W) condition when the voltage reference is 12 V. In addition, in Fig. 14, in order to make the experimental waveform

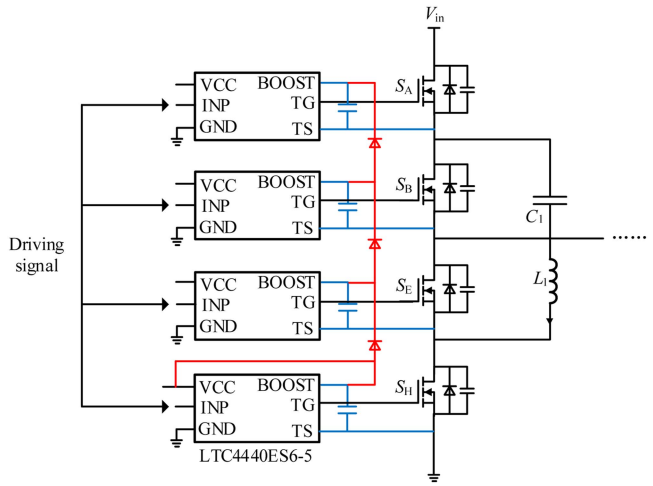

Fig. 13. Schematic diagram of cascaded bootstrap drive circuit.

more clearly reflect the working state of the converter, this article labeled four different states within a complete switching period.

As shown in Fig. 14, the proposed converter can achieve a stable output of 12 V within the input voltage range of 40–60 V, and the ripple of the output voltage is extremely small. The magnitude and waveform of the resonant capacitor voltage and the resonant inductor current are consistent with the theoretical analysis. Among them, when the voltage step-down ratio deviates from the nominal value, the waveform of the resonant inductor current will undergo distortion, but it does not affect the voltage regulation effect of the converter when the voltage step-down ratio deviation is not significant.

Figs. 15, 16, and 17 show the voltage waveforms at the drain source terminals of the proposed converter's MOSFET, as well as its driving voltage waveform, and the corresponding inductor current waveform throughout the entire ZVS process under phase-shift control mode under different input voltage conditions. From the figure, it can be seen that within the input voltage range of 40–60 V, the voltage between MOSFET's drain-source electrodes has dropped to 0 before the MOSFET conduction signal arrives, achieving good ZVS turn-ON, hence, the switching losses are greatly reduced.

It should be noted that, according to theoretical analysis, the output voltage of the proposed converter is positively correlated with the phase-shift angle and load current. Based on the experimental results, it can be known that according to the proposed phase-shift control method, the converter can achieve 12 V stable output under conditions of 40–60 V input and full load 300 W output at a phase-shift angle not exceeding 42°.

Figs. 18 and 19, respectively, show the waveform of the output voltage when the input voltage and load current suddenly change. In Fig. 18, the input voltage is continuously and rapidly adjusted in the order of 60 V-48 V-40 V-48 V-60 V. Under the control strategy proposed in this article, the output voltage remains stable at 12 V, with only minimal fluctuations at the switching point. In Fig. 19, rapid and repeated switching of the load between 50 W and 100 W, the output voltage also remains stable, demonstrating the rationality of the controller design.

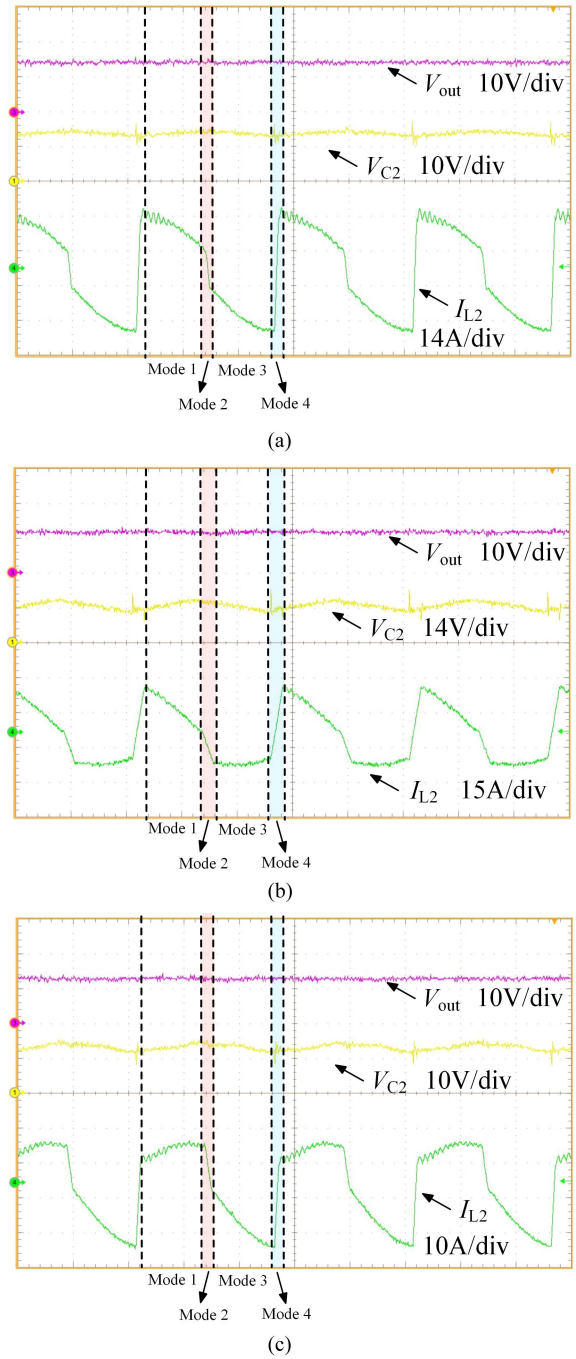

Fig. 14. Key waveforms under phase-shift control of the proposed converter. (a) $V_{in} = 48$ V. (b) $V_{in} = 40$ V. (c) $V_{in} = 60$ V.

According to the proposed control method, the converter can achieve a 12 V stable output and included almost no error within the entire scope of work, with high voltage regulation accuracy. This meets the requirements of application scenarios and design metrics. As a comparison, traditional RSC converters without voltage feedback and closed-loop control exhibit poor voltage regulation performance over a wide load range. The phase-shift control method proposed for this topology can eliminate steady-state errors due to its integral gain component in the voltage feedback loop.

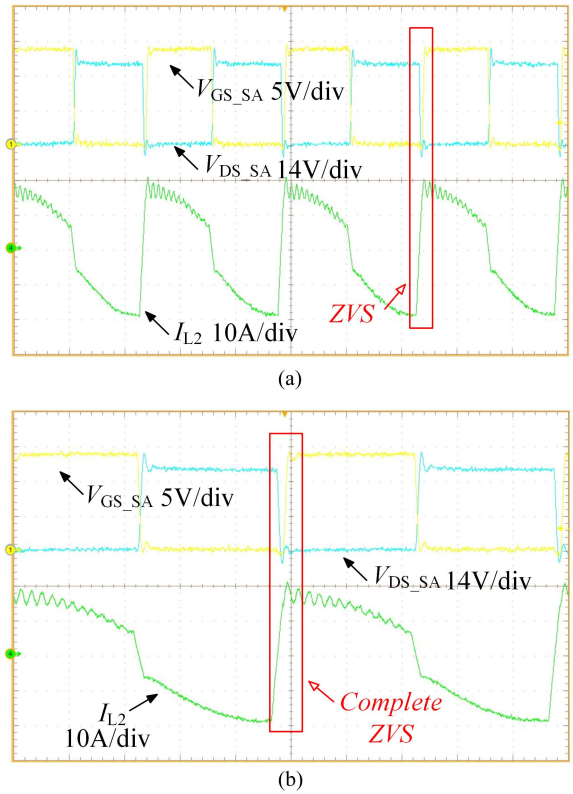

Fig. 15. Key waveforms for the converter to implement ZVS under 48 V input conditions. (a) Overall waveform image. (b) Partial enlarged detail image.

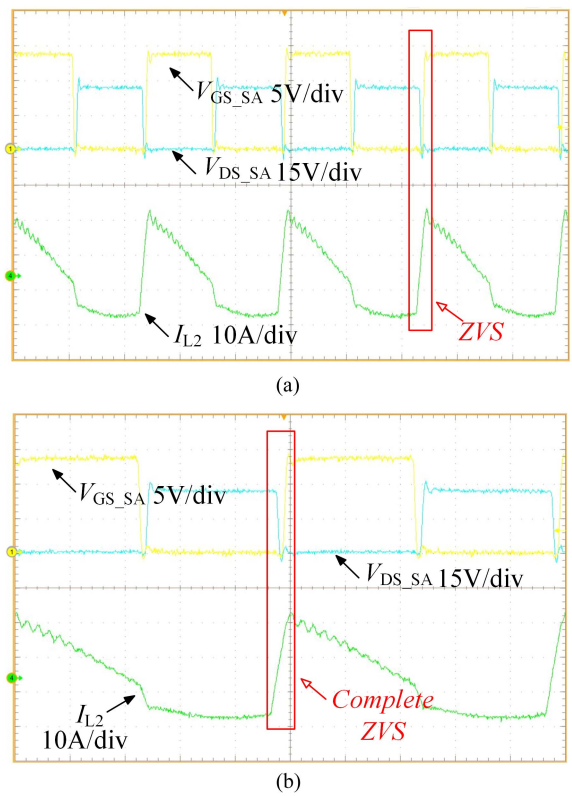

Fig. 16. Key waveforms for the converter to implement ZVS under 40 V input conditions. (a) Overall waveform image. (b) Partial enlarged detail image.

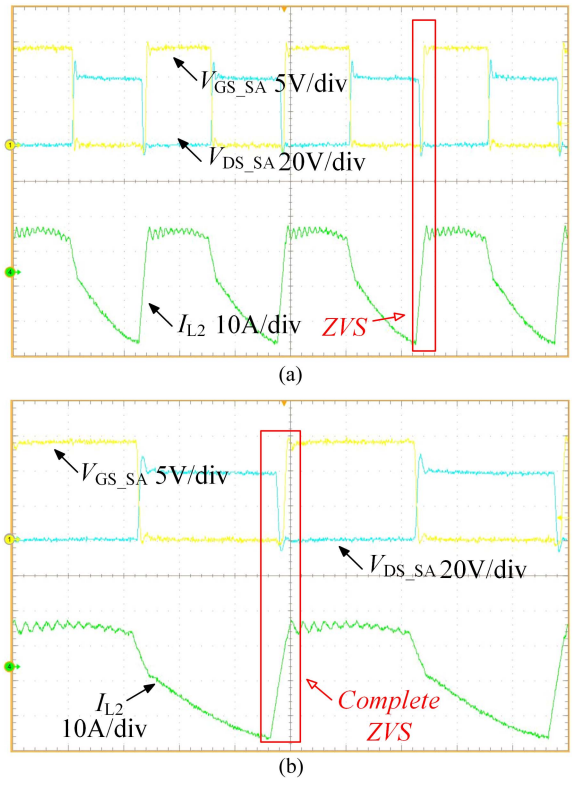

Fig. 17. Key waveforms for the converter to implement ZVS under 60 V input conditions. (a) Overall waveform image. (b) Partial enlarged detail image.

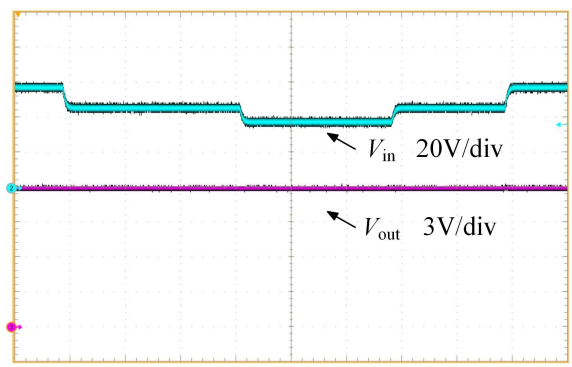

Fig. 18. Output voltage waveform when there is a sudden change in input voltage.

Fig. 20(a) shows the efficiency curves of the proposed converter under different input voltages. The efficiency curve trend in the three curves is similar. As can be seen from the figure, under light load conditions, a part of MOSFETs in the converter cannot achieve ZVS, resulting in significant switching losses and low efficiency. As the load gradually increases, the converter enters the ZVS working state, which can achieve high efficiency. It is worth noting that when the converter deviates from the nominal voltage step-down ratio, the load range that can achieve full ZVS will be reduced. Therefore, compared to 48 V input, the light load efficiency under 40 V and 60 V input

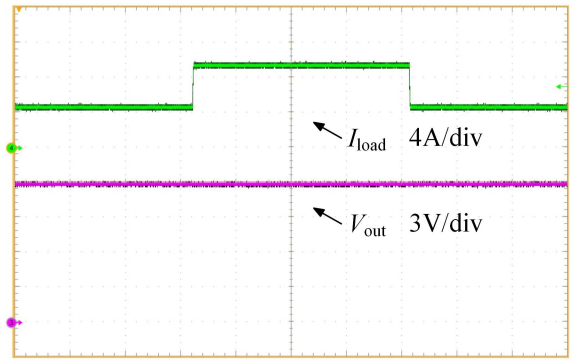

Fig. 19 Output voltage waveform when there is a sudden change in load current.

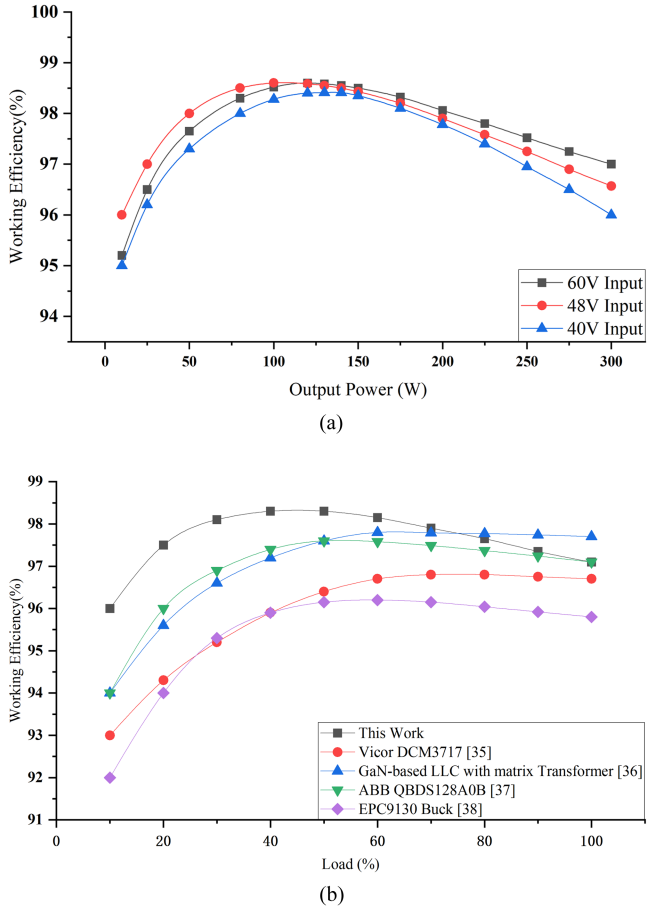

Fig. 20. Efficiency curve of the converter. (a) The variation curve of efficiency with output power under different input voltages. (b) Comparison of efficiency between the proposed converter and other related converters.

conditions is slightly lower. But when the load is heavy, due to the lower input current at 60 V input, the corresponding on-state loss of the MOSFETs is also lower, and the overall efficiency is slightly higher than the working state of 48 V input. But overall, the efficiency is still at a relatively high level. According to Fig. 20(a), the peak efficiency of the converter reaches 98.4%, and the full-load efficiency of the converter reaches 97.1%.

Based on the experimental results, the article conducted a detailed analysis of the losses of the converter. The analysis focuses on two situations: namely peak efficiency and full load. First, the losses of each part at the peak efficiency can be calculated and analyzed. According to the experimental results, the peak efficiency occurs at an output power of around 100 W. Based on the resonance between inductor and capacitor in the circuit, the converter can achieve good soft switching. At this point, the turn-ON losses of MOSFETs are zero. Therefore, the losses of the converter mainly include the following parts: conduction loss of MOSFETs, driving loss of MOSFETs, conduction loss caused by the ESR of flying capacitors, inductor loss, and other losses. The "other losses" mainly include MOSFET turn OFF losses, losses caused by parasitic parameters such as conduction losses of printed circuit boards, all of which are difficult to accurately quantify. This article analyzes and estimates them through simulation and experiments.

Among them, the conduction loss of the MOSFETs can be calculated according to the following formula:

$$P_{\text{on}} = \sum_{n} I_{\text{rms}\_n}^2 R_{DS(\text{on})\_n} \tag{45}$$

where I_{rms} is the effective value of the current flowing through the MOSFETs, and $R_{DS(\text{ON})}$ is the ON-resistance of the MOSFET. The $R_{DS(\text{ON})}$ of the MOSFETs in the test prototype are 5 mΩ and 1.35 mΩ. Therefore, the conduction loss is 0.405 W when output power is 100 W. The losses caused by the ESR of flying capacitors can also be calculated using (45). According to calculations, the losses under 100 W output conditions is approximately 0.1 W.

The driving loss of MOSFET is only related to its characteristics and switching frequency, and is not related to the output power. It can be calculated by the following formula:

$$P_{\text{drive}} = \sum_{n} Q_{g\_n} U_g f_{sw}. \tag{46}$$

Among them, Q_g is the gate charge of the MOSFET, according to the datasheet, the gate charge of the MOSFETs in two-stage converters are $Q_{g1} = 41$ nC, $Q_{g2} = 35$ nC. U_g is the driving voltage, and f_{sw} is the operating frequency of the MOSFETs. The drive loss is a fixed value 0.35 W.

The finished inductor model used in this article is XGL6030-471MEC. The losses on inductors mainly include magnetic core losses and dc and ac conduction losses. This article analyzes and calculates the losses on the inductors based on the information in the inductor datasheet and experimental results. It can be obtained that the total inductor loss is 0.375 W when the output power is 100 W.

With simulations, the other loss can be estimated as 0.39 W.

The pie chart of the losses is shown in Fig. 21.

With the same method under full load condition, the losses can be calculated as follows: MOSFET driving loss 0.35 W, MOSFET conduction loss 3.645 W, inductor conduction loss 3.317 W, flying capacitor ESR loss 0.9 W, and other loss 0.738 W.

Similarly, the corresponding loss proportion as a pie chart can be shown in Fig. 22.

TABLE III
PERFORMANCE OF THE PROPOSED CONVERTER AND OTHER RELATED CONVERTERS

Topology	Range of input voltage	Output Current (A)	System Efficiency	Power Density (W/in3)
Vicor DCM3717 [35]	40-60V	62.5	Full-load: 96.7% Peak: 96.8%	2613
GaN-based LLC with matrix Transformer [36]	40-60V	83.3	Full-load: 97.7% Peak: 97.8%	677
ABB QBDS128A0B [37]	48-60V	128.3	Full-load: 97.1% Peak: 97.6%	810
EPC9130 Buck [38]	36-60V	60	Full-load: 95.8% Peak: 96.2%	1000
this work	40-60V	25	Full-load: 97.1% Peak: 98.4%	1987

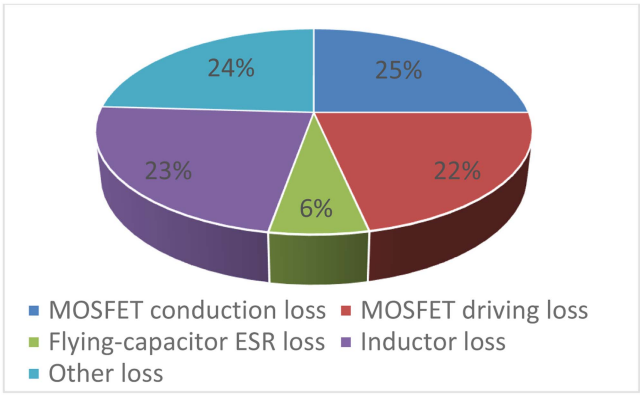

Fig. 21. Figure of the proportion of losses in each part at 100 W.

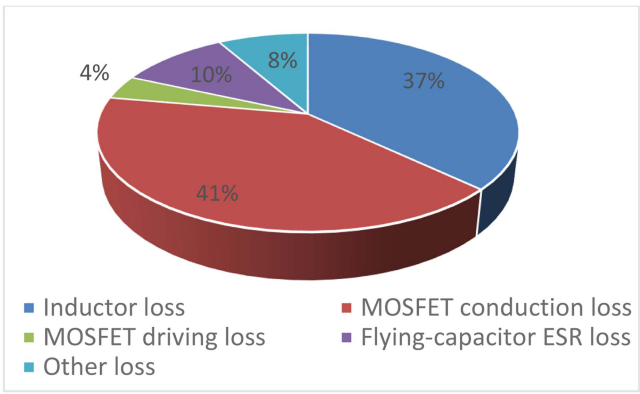

Fig. 22. Figure of the proportion of losses in each part at 300 W.

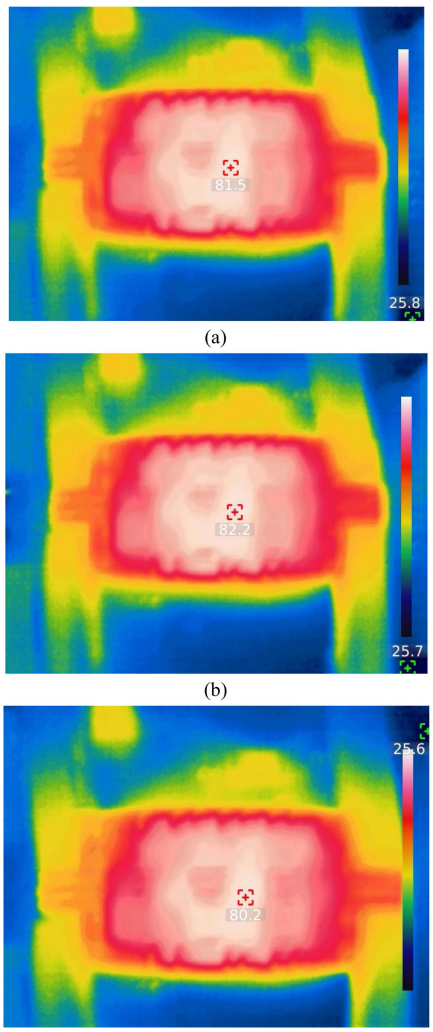

Fig. 23. Thermal imaging diagram of the proposed converter at full load. (a) $V_{\rm in} = 48$ V. (b) $V_{\rm in} = 40$ V. (c) $V_{\rm in} = 60$ V.

From the figure, it can be seen that at the peak efficiency point, the proportion of various losses is similar. However, as the output power continues to increase, the MOSFET driving loss does not change, while other losses are significantly increasing, especially the conduction loss of MOSFETs, which is also the main factor restricting the further improvement of converter efficiency.

Compare the technical indicators of the proposed converter with that of other state-of-the-art regulated 48-to-12-V IBC, the results are shown in Table III, and the comparison of efficiency curves is shown in Fig. 20(b). From the table and the figure, the converter proposed in this article and the converter proposed by Vicor in [34] both have good comprehensive performance. Although the converter proposed in this article has slightly lower power density compared to the converter in [34], its working efficiency has significant advantages, especially in light load

operation, which makes it highly advantageous in practical application scenarios of data center power supply systems. In terms of power density, the proposed converter does have significant room and potential for improvement. For example, in the future, we will adopt driver and device integration methods and design our own inductors to further improve the power density of the converter.

Due to the proposed converter achieving ZVS for all devices, the converter has achieved high working efficiency, greatly simplifying the heat dissipation design. As seen from Fig. 23, under rated 48 V input conditions, the maximum operating temperature of the converter at full load is 81.5°C. Due to the deviation of the voltage step-down ratio from the nominal value, the working efficiency slightly decreases, and the full load working temperature also slightly increases at 40/60 V input, reaching 82.2°C and 80.2°C, respectively. The temperature of the converter is relatively low throughout the entire operating range, which has sufficient thermal margin for the on-board power devices. The conduction path is evenly distributed throughout the entire converter, with sufficient heat dissipation area.

VI. Conclusion

This article proposes a family of RSC converters with voltage regulation capability and the corresponding regulation methods. By properly utilizing the deadtime of the driving signals, the converter can achieve zero voltage turn-ON within a certain load range. Next, this article proposes a phase-shift control method, and analyzes its voltage regulation principle in detail, deducing its mathematical relationship. Then, this article analyzes and calculates the load range that the converter can achieve ZVS for all MOSFETs, and based on this, designs the resonant tank parameters. The experimental results of the 300 W prototype verify the rationality of theoretical analysis and control method, and all active devices can operate under well soft switching conditions. The system efficiency can be 98.4% and the system power density can achieve 1987 W/in^3.

Appendix
Specific Derivation Process of Average Output Current

In Section B of Chapter III, this article provides a detailed analysis of the four different operating modes of the proposed converter within one switching period, and derives the expression of its state variables. In this appendix, this article will provide the specific process of deriving the average output current of the converter based on this result.

From Fig. 3, it can be clearly seen that the average output current is determined by the inductor current values in Mode 1 and Mode 3 stages. Except for the initial and final values, the current values during the duration of Mode 2 and Mode 4 have no effect on the average output current value. Therefore, when deriving the average output current value, this article approximates the inductor current waveforms in modes 2 and 4 as linear segments, with slopes, as shown in (40) and (41). According to this assumption, the resonant capacitor voltages can be considered constant during the duration of modes 2 and 4, and it does not affect the final calculation of the average output current. Based on the abovementioned assumptions, it can be concluded that

$$\hat{v}_{C1}(T_S) = \hat{v}_{C1}(0) \tag{47}$$

$$\hat{v}_{C1}\left(T_S + \frac{T_{sw}}{2}\right) = \hat{v}_{C1}\left(\frac{T_{sw}}{2}\right). \tag{48}$$

By combining the above two equations with (17) and (24), a system of equations about $\hat{v}_{C1}(0)$ and $\hat{v}_{C1}(\frac{T_{sw}}{2})$ can be obtained, as shown in (49) and (50). According to (49) and (50), the expressions for $\hat{v}_{C1}(0)$ and $\hat{v}_{C1}(\frac{T_{sw}}{2})$ can be further obtained

$$\hat{v}_{C1}(0) = \hat{v}_{C1}\left(\frac{T_{sw}}{2}\right) + \left[V_{\text{out}} - \hat{v}_{C1}\left(\frac{T_{sw}}{2}\right)\right][1-\cos\omega_r T_S'] - \omega_r L_1 \hat{i}_{L1}\left(T_S + \frac{T_{sw}}{2}\right)\sin\omega_r T_S' \tag{49}$$

$$\hat{v}_{C1}\left(\frac{T_{sw}}{2}\right) = 2V_{C1} - \hat{v}_{C1}(0) + \omega_r L_1 \hat{i}_{L1}(T_S)\sin\omega_r T_S' + [(V_{\text{in}} - V_{\text{out}})/3 - 2V_{C1} + \hat{v}_{C1}(0)][1-\cos\omega_r T_S']. \tag{50}$$

Based on the abovementioned results, we can obtain the expression of the average output current of the converter more conveniently. First, calculate the average output current during the first half switching period (Mode 1 and Mode 4). By substituting (18) into (19), it can be calculated that

$$I_{\text{out1}} = \frac{[(V_{\text{in}} - V_{\text{out}})/3 - (2V_{C1} - \hat{v}_{C1}(T_S))](1-\cos\omega_r T_s')}{T_{sw}\omega_r^2 L_1/2} + \frac{\hat{i}_{L1}(T_S)\sin\omega_r T_s'}{T_{sw}\omega_r/2}. \tag{51}$$

Similarly, when calculating the average output current in the second half of the switching period (Mode 2 and Mode 3). By substituting (25) into (26), it can be calculated that

$$I_{\text{out2}} = 3\frac{\left[V_{\text{out}} - \hat{v}_{C1}\left(\frac{T_{sw}}{2}\right)\right](1-\cos\omega_r T_s')}{T_{sw}\omega_r^2 L_1/2} - 3\frac{\hat{i}_{L1}\left(T_S + \frac{T_{sw}}{2}\right)\sin\omega_r T_s'}{T_{sw}\omega_r/2}. \tag{52}$$

Based on the relationship between the inductor currents in each mode and the average output current of the converter during a complete switching cycle, it can be obtained that

$$I_{\text{out}} = \frac{I_{\text{out1}} + I_{\text{out2}}}{2}. \tag{53}$$

By substituting (51) and (52) into (53), the average output current of the converter during a complete switching cycle can be calculated, as shown in

$$I_{\text{out}} = \frac{4A\omega_r L_1 \sin(\omega_r T_S') + \left[8V_{C1} - 4B - \frac{4}{3}(V_{\text{in}} - V_{\text{out}})\right]\cos(\omega_r T_S')}{T_{SW}\omega_r^2 L_1} \tag{54}$$

where

$$T_S' = \frac{T_{SW}}{2} - T_S. \tag{55}$$

In (54), for the convenience of expression and calculation, intermediate variables A and B are defined, and their expressions are shown in

$$A = \frac{[V_{\text{in}}(1+\omega_r L_1) - 2V_{C1}]\sin(\omega_r T_S)}{2\omega_r L_1(1+\cos\omega_r T_S)} \tag{56}$$

$$B = \frac{[2V_{C1} - (1+Z_1)V_{\text{in}}]\sin^2\omega_r T_S}{2(1+\cos\omega_r T_S)^2} + \frac{[2V_{C1} - V_{\text{in}}]\cos\omega_r T_S + V_{\text{in}}}{1+\cos\omega_r T_S} \tag{57}$$

where Z_1 is the characteristic impedance of the *LC* resonant tank, which can be expressed as

$$Z_1 = \sqrt{\frac{L_1}{C_1}}. \tag{58}$$

When the load is light, achieving the same voltage conversion ratio requires a smaller phase-shift angle. When the angle is small enough, the simplified formula shown in (59) can be used for calculation and controller design

$$I_{\text{out}} = \frac{\left[8V_{C1} - 4\frac{[2V_{C1}-V_{\text{in}}]\cos\omega_r T_S + V_{\text{in}}}{1+\cos\omega_r T_S} - \frac{4}{3}(V_{\text{in}} - V_{\text{out}})\right]\cos(\omega_r T_S')}{T_{SW}\omega_r^2 L_1}. \tag{59}$$

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