A Robust Adjustable Speed Drive to Operate in Polluted Grid Conditions With Improved Line Current Harmonics

Seshadri Gopalan, *Member, IEEE*, Krishna Vasudevan, *Senior Member, IEEE*, and Dinesh Kumar, *Senior Member, IEEE*

***Abstract*—With an increase in the abnormalities in the supply voltage, it is required that the Adjustable Speed Drive (ASD) connected to the grid be immune to those disturbances. Based on the field Power Quality (PQ) data study, distortion in the supply voltage is found to be the dominant disturbance followed by unbalance. It is found that these disturbances mainly affect the lifetime of dc bus capacitor and in critical cases, it may lead to a failure. In order to save the ASD from such grid disturbances, a compensation module is introduced in this article. While reducing the stress on the capacitor, this module also mitigates the harmonics in the source current of ASD. The proposed module can be a retrofit to the existing commercial ASD and can be used where the supply voltage quality is poor. The proposed topology is analyzed by simulations and validated by the test setup created in the lab.**

***Index Terms*—Capacitor heating factor (CHF), distortion, power quality (PQ), unbalance.**

I. Introduction

ADJUSTABLE speed drives (ASDs) are broadly used in both industrial and commercial applications due to their effective and flexible means of achieving motion control. It is identified that the dc bus capacitor is one of the reliability–critical components in the ASDs and most affected by ageing effect [1], [2]. Increasing penetration of renewable energy and nonlinear loads in the distribution system lead to increase the level of abnormalities in the grid voltage [3], [4]. In order to understand the quality of supply voltage in the Indian grid, power quality (PQ) meters were deployed at different industrial sites [5]. From the recorded data, the dominating PQ events and their range were observed, and are used for this study. A brief overview of PQ disturbances observed is given in Section II. Based on this field data study, distortion and unbalance in the supply voltage are found to be the dominant disturbances. Therefore, their effect on ASD is of interest. There are only a few works reported that analyze the effect of harmonics (distortion) in supply voltage on the front end of an ASD [6], [7], [8], [9]. Carbone [7] and Mansoor et al. [8] discussed the effect of background supply voltage distortion on dc bus voltage and THD_i of the source current, respectively. The severity of the impact of supply voltage harmonics and unbalance on the dc bus capacitor is discussed in [6], [9], and [10]. It shows that the presence of unbalance and/or harmonics beyond a certain limit in the supply voltage can cause the dc bus capacitor ripple current to cross its critical value resulting in possible damage to the capacitor. It is identified from the study [9] that though the distortion level in the supply voltage is lesser than the standard limit as per IEC-61800- 3 [11] (12% limit), the dc bus capacitor of the ASD may get damaged based on the individual harmonics magnitude and its angle. Hence, it is important to safeguard the ASD under polluted grid conditions. There are a few possible generic solutions such as modified dynamic voltage restorer (MDVR) [12] and active front-end rectifier (AFR) [13], which can also safeguard the dc bus capacitor under abnormal supply voltage conditions. While considering the cost and the number of extra components the MDVR and AFR are however, not satisfying solutions. The cost of an active front-end ASD is more than double the cost of an equivalent diode bridge front-end ASD. To the best of authors' knowledge no direct attempt at addressing the impact of PQ disturbances on the capacitor is reported in literature. A cost-effective solution is required that will make the ASD dc link components immune to supply voltage distortion and unbalance. Gopalan et al. [14] proposed a cost-effective solution to suppress the effect of even ordered harmonics on the dc bus capacitor for an ASD with a thyristor bridge front end. However, the problem still exists for an ASD with a diode bridge front end. Wang et al. [15] proposed a series voltage compensator (SVC) in order to support a reduced capacitance at the dc link. Due to this reduction in the capacitance, there will be an increase in the ripple in the dc link. The SVC that is introduced between the dc link capacitor and the inverter helps to achieve a ripple free voltage at the inverter input terminals. Though the inverter input voltage has become ripple-free, the ripple present in the dc link capacitor is still not

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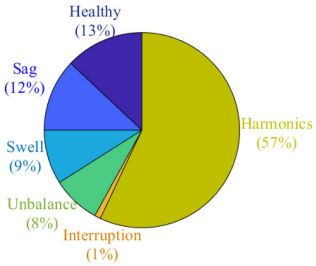

Fig. 1. Occurrences of different PQ events in industrial sites.

addressed in [15]. In the case of grid disturbances, the capacitor may face an increased stress.

In order to address this issue, an add-on low power electronic circuitry is proposed in [16]. This will act as a compensator for the ripple in the dc side of the ASD and reduce stress on the capacitor. Also, a ripple-free voltage at the inverter input terminals is achieved. This compensator is named as grid disturbance compensation module (GDCM). This requires a diode bridge, a dc bus capacitor, an H-bridge, and a transformer. The power rating of this module depends on the extent of compensation required for the dc bus voltage of the ASD. Based on the worst-case disturbance observed in the field study, the module is designed and it is identified that the power level of the module is only about $1/7^{\text{th}}$ of the power level of the main ASD. The proposed module can be a retrofit to the commercial ASD and used where the PQ is poor. The proposed GDCM will reduce the ripple current in the dc bus capacitor and thereby increase the useful life of the capacitor. It also decreases the THD_i of the source current to 33% irrespective of the disturbance (unbalance and harmonics) present in the supply voltage and drive loading conditions. As a result of the proposed GDCM, the inductor current becomes free from low frequency ripple content which in turn reduces the thermal stress on the inductor in the ASD. As an extension of [16], this article presents a design oriented analyses of the proposed GDCM. An extensive validation study is also presented under different grid impedance and disturbance conditions. Further, a 7.5 kW test setup is built in the laboratory and the GDCM is validated under different grid disturbance cases.

The rest of this article is organized as follows. Section II presents an overview of PQ disturbances observed in the Indian grid scenario. Section III presents the ASD topology taken for the study along with the indices to quantify performance. Section IV presents an overview of the effect of dominant PQ disturbances on the dc bus capacitor. Section V describes the proposed GDCM along with its design, and validation under different disturbances and grid impedance conditions. It also presents the experimental validation of the proposed GDCM. Finally, Section VI concludes this article.

II. Overview of PQ Disturbances in Indian Grid

PQ meters were deployed [5] at six different industrial sites in India that include casting and spinning industries. The data are recorded for more than two years and Fig. 1 shows the consolidated occurrences of different types of PQ disturbances (crossing

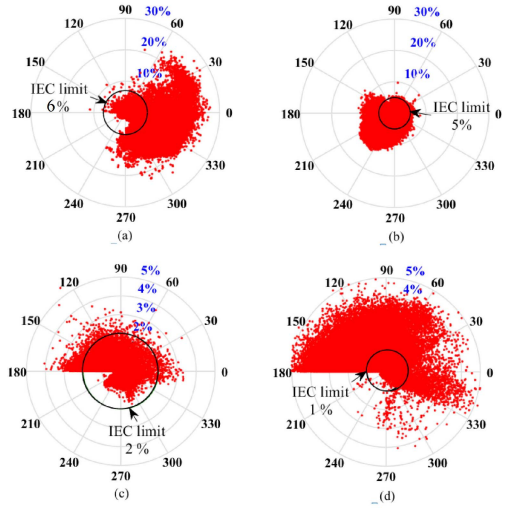

Fig. 2. Magnitude and angle of harmonics in the supply voltage (a) 5^{th}, (b) 7^{th}, (c) 2^{nd}, and (d) 4^{th}.

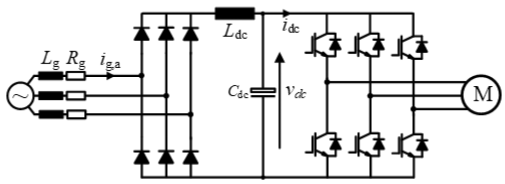

Fig. 3. ASD configuration with diode bridge front end.

respective IEC limits) recorded in the sites as a percentage of the total number of disturbances recorded. It can be seen that 57% of the disturbances recorded correspond to distortion crossing limits prescribed by IEC 61000-2-4 [17].

Further, the polar distribution of recorded values of lower-order harmonics (2^{nd}, 4^{th}, 5^{th}, and 7^{th}) are shown in Fig. 2. The lower-order harmonics are more critical with respect to the capacitor ripple current than the higher-order harmonics [6]. Fig. 2 shows that there are many instances where the magnitude of harmonics is crossing its corresponding IEC standard limit. It is also identified from the previous study [6] that the capacitor ripple current may cross its critical limit even when the magnitude of harmonics are less than their IEC standard limit based on the angle of harmonics. The next class of disturbances in the order of occurrences are sags and swells. However, symmetrical sag/swell in the supply voltage will not much alter the ripple current in the capacitor [10]. These PQ disturbances will just alter the average value of the dc bus voltage. Unbalance in the supply voltage is the next dominant disturbance and its worst-case value observed in the site is 7%. Hence the focus in this article is given to distortion (harmonics) and unbalance in the supply voltage. These practical values are used for the simulation analysis.

III. ASD Topology and Impact Assessment Parameters

A 7.5 kW ASD feeding an induction motor is the system considered for the study as shown in Fig. 3 and its parameters are given in Table I. It is shown in [9] that the effect of supply

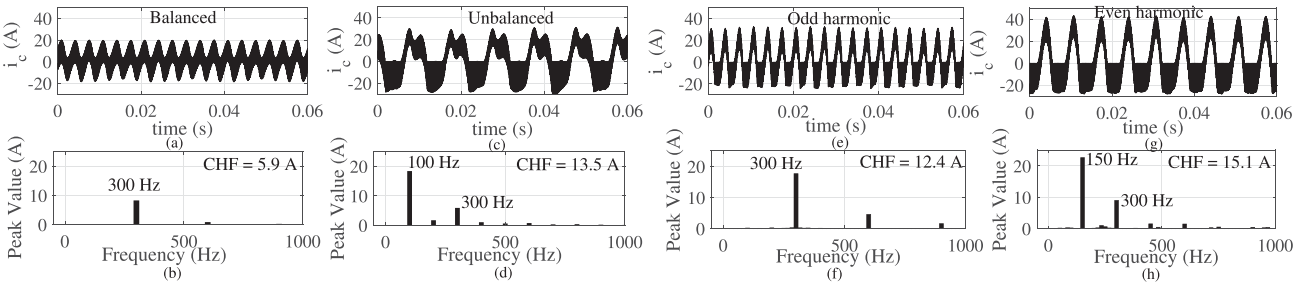

Fig. 4. Capacitor current - Instantaneous waveform and FFT under: (a) and (b) balanced, (c) and (d) 7% unbalanced, (e) and (f) 5^{th} harmonic of 12% at 180°, (g) and (h) 2^{nd} harmonic of 2% at 0° in the supply voltage.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
Source voltage and frequency	400 V (L-L), 50 Hz
Grid impedance - L_g, R_g, R_{SCE}	50 µH, 5.8 $m\Omega$, 1000
DC choke inductance L_{dc}	2.5 mH
DC bus capacitance C_{dc}	500 µF
Inverter switching frequency	5 kHz
Induction Motor Drive	7.5 kW, 400 V, 50 Hz

voltage distortion on the dc bus capacitor is more with a stiff grid than with a weak grid. Hence, the grid impedance considered is with an R_{SCE} of 1000 (stiff grid), to study the worst case. For the simulation studies, the dc bus capacitor is modeled using its parameter values taken from the datasheet [19]. In order to model the actual saturable inductor, the *B–H* characteristic of the dc choke is measured in the lab and used in the simulations.

As discussed, the main focus of this study is the impact of supply voltage disturbances on the dc bus capacitor. In order to assess the stress on the capacitor, it is necessary to include the heating created by all the frequency components present in the capacitor current. A term called " Capacitor Heating Factor" (CHF) (1), is introduced in [18], to assess this. In (1), I_n is the RMS value of current at a particular frequency " n" and M_{f_n} is the ripple current multiplication factor (or frequency multipliers) that can be obtained from the datasheet of the capacitor [19]. Frequencies up to 6 kHz are chosen for the computation since the inverter switching frequency is 5 kHz. As per the datasheet, the maximum CHF value of this dc bus capacitor is 11 A at an ambient temperature of 55 °C. The CHF is mainly contributed by the low-frequency components (< 1 kHz) due to higher equivalent series resistance (ESR) and low M_{f_n} in the low-frequency range [9], [20]

$$\text{CHF} = \sqrt{\sum_{n=1}^{\infty} \frac{I_n^2}{M_{f_n}^2}}. \tag{1}$$

As can be seen from the simulation studies presented in Section V, the abnormalities in the supply voltage result in an increase of distortion in the current drawn by the ASD. Hence the THD_i, defined in (2), along with the CHF are used in this study to quantify the performance of the system proposed

$$\text{THD}_i = \frac{\sqrt{\sum_{n=2}^{40} I_n^2}}{I_1} \times 100\%. \tag{2}$$

IV. Overview of Effects of Dominating PQ Events on Capacitor

A detailed study on the effects of distortion and unbalance in the supply voltage are given in [9]. This section gives an overview of the impact of these dominant disturbances on the capacitor current. Fig. 4(a) and (b) shows the waveform of the capacitor current and its FFT, respectively, when the supply voltage to the ASD is balanced and undistorted, for the purpose of comparison.

A. Effect Under an Unbalance Case

A 7% unbalance (calculated using sequence component definition in IEC 61000-2-4 [17]), being the extreme case observed in field, is introduced in the supply voltage and the capacitor current response is shown in Fig. 4(c) and (d). It can be seen that the capacitor current has a dominant 100 Hz component while the magnitude of 300 Hz component is not appreciably altered in comparison to the balanced case [cf. Fig. 4(b) and (d)]. Due to this dominant 100 Hz component, the net CHF has increased to 13.5 A. From several simulation runs, it has been found that a 5% unbalance will result in a CHF of 11 A, which is the critical level for the capacitor used at an ambient temperature of 55°C [10].

B. Effect Under an Odd Ordered Harmonic

It is seen from the recorded data that the magnitude of 5^{th} and 7^{th} harmonics are observed up to 20% and their angles are spread over the entire 360° (cf. Fig. 2). It is identified from the previous study [9] that 180° is a critical harmonic angle for the 5^{th} ordered harmonic concerning its effect on the CHF. Hence, 20% 5^{th} harmonic at an angle of 180° is introduced in the supply voltage and the capacitor current for this case is shown in Fig. 4(e) and (f). The odd ordered harmonics increase the amplitude of the six times the supply frequency component (300 Hz for a 50 Hz supply) [9]. This is also evident by comparing Fig. 4(b) and (f). The resultant CHF for this case is 12.4 A. It is also found from the studies that the angle of harmonic strongly influences the CHF response [9].

C. Effect Under an Even Ordered Harmonic

Even ordered harmonics in the supply voltage create asymmetry between the positive and negative half cycles of the supply

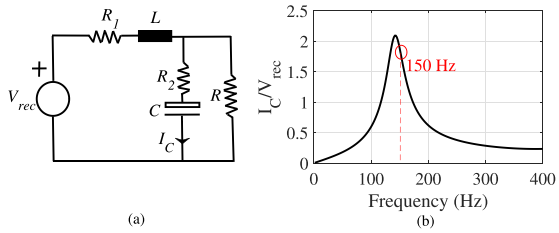

Fig. 5. (a) Simplified DC bus network. (b) Frequency response of capacitor current.

voltage. It has been found that this results in triple the supply frequency component (150 Hz for 50 Hz supply) in the dc bus [14]. It is found from the previous study [6] that 0° harmonic angle is critical for 2nd ordered harmonic concerning its effect on the CHF. Also, the level of 2nd harmonic observed in the field is around 4%. Hence, 4% 2nd harmonic at an angle of 0° is introduced in the supply voltage. The resultant capacitor current and its FFT are shown in Fig. 4(g) and (h). It can be seen from Fig. 4(h) that while the value of 300 Hz component is nearly same as in Fig. 4(b) a dominant 150 Hz component is present in this case. Due to this, the net CHF value increased to 15.1 A. This shows the importance of even ordered harmonics on the capacitor current. To understand the reason for such high value of 150 Hz component in the capacitor current, the dc network of the ASD is modeled as shown in Fig. 5(a). The input to the circuit shown is V_{rec}, which is the voltage measured at the output of the diode bridge (before dc choke). The resistance associated with the dc choke is represented as R_1. The ESR of the capacitor is modeled as $R_{2\omega}$ as it is frequency-dependent and the values are taken from datasheet [19]. The ASD load is modeled as resistive (R). The capacitor current (RMS value — I_C) is a function of the magnitude and frequency of diode bridge output voltage and is given in (3). The frequency response of I_C/V_{rec} is shown in Fig. 5(b). It can be seen from Fig. 5(b) that the 150 Hz component is present near the resonant peak and the presence of a small value of V_{rec} at 150 Hz will result in a large value in the capacitor current. Due to the constraints in placing the resonant peak during the design [14] this amplification is difficult to eliminate by proper sizing of dc bus components.

$$\frac{I_C}{V_{\text{rec}}} = \frac{-j\omega C\left(\omega C R R_{2\omega} - jR\right)}{d\left(\omega\right)} \tag{3}$$

where $d(\omega) = \omega C(RR_1 + R_1R_{2\omega} + RR_{2\omega}) + \omega L + j(\omega^2 LC(R + R_{2\omega}) - R_1 - R)$.

V. Proposed GDCM

It is clear from the previous section that the supply voltage distortion and unbalance are critical to the dc bus capacitor. To operate the ASD under such polluted grid conditions, an add-on circuit named GDCM is proposed as shown in Fig. 6. It consists of a diode bridge, a bus capacitor, an H-bridge, and a transformer.

The waveform of the rectified voltage (v_{rec}) for an unbalance case of 7% is shown in Fig. 7(a). It is seen to contain both dc and ac components. While the dc component is only desirable in v_{rec}, the ac ripple is normally unavoidable. The amplitude

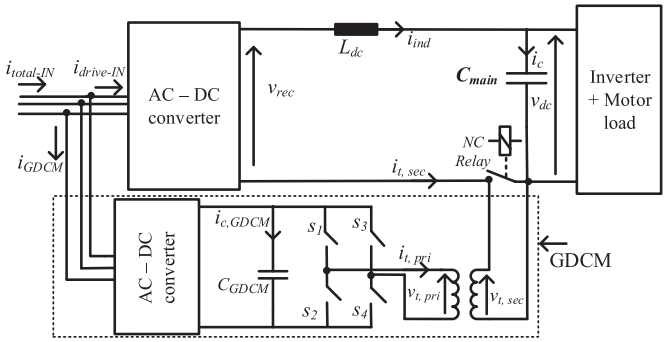

Fig. 6. Proposed GDCM topology.

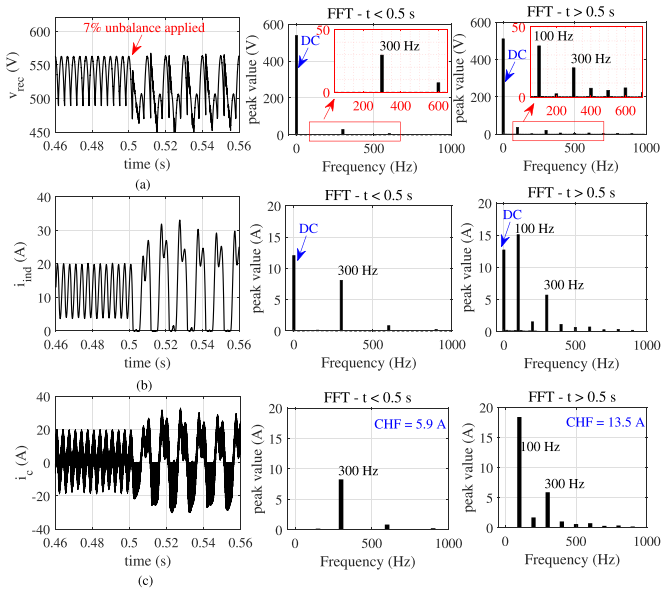

Fig. 7. Response to a 7% unbalance in supply voltage (a) rectified voltage (v_{rec}), (b) inductor current (i_{ind}), and (c) capacitor current (i_c).

and frequency of ac ripple depend on the level and type of disturbance in the ASD input. As a response to this ac ripple voltage, the ripple in the inductor current and capacitor current can be observed as shown in Fig. 7(b) and (c), respectively. Increase in this ripple current reduces the life of the capacitor and may cause damage if it crosses its critical limit. The proposed module delivers a controlled ac voltage that nullifies the effect of voltage ripple across the diode bridge of the main ASD.

A. Control Loop

As mentioned in Section I, the control will be turned ON whenever required based on the estimation of CHF using the measured v_{rec}, as shown in Fig. 8.

$$G_{\text{LPF}}(s) = \frac{3944}{s^2 + 88.8s + 3944}. \tag{4}$$

The CHF estimation procedure is as follows. The ripple part of the v_{rec} ($v_{\text{rec\_ripple}}$) is extracted by eliminating the average value which is found by using a low pass filter (LPF) with a cut off frequency of 10 Hz. The transfer function of the filter $[G_{\text{LPF}}(s)]$ is given in (4). The magnitudes (mag_{f_i}) of interested

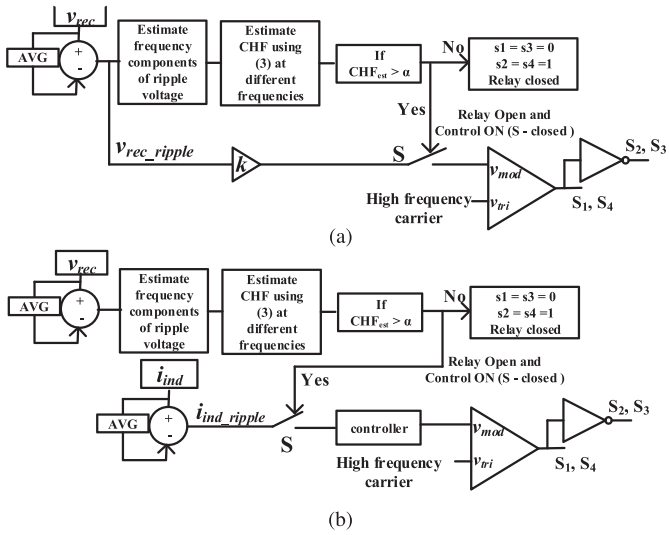

Fig. 8. Control methods of GDCM. (a) Method I and (b) Method II.

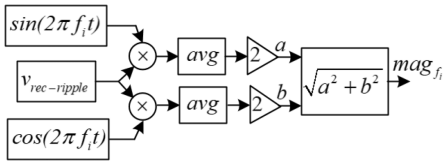

Fig. 9. Extraction of magnitudes of interested frequency (f_i) components from $v_{\text{rec}-\text{ripple}}$.

frequency components (dominant low frequency and switching frequency) present in $v_{\text{rec\_ripple}}$ are found using the approach given in Fig. 9. Using the I_c/V_{rec} values at different frequencies calculated using (3), the capacitor current magnitude (I_c) at different frequencies and hence the CHF value can be estimated. If this estimated CHF (CHF_{est}) is more than a critical value (α) then the control is turned ON, as shown in Fig. 8. This critical limit can be fixed based on the value of maximum allowable ripple current obtained from the datasheet of the capacitor. For the capacitor used in this study, $\alpha = 11\ \ A$.

The aim of this GDCM is to suppress the effects of PQ disturbances on the capacitor and reduce the CHF. This is achieved by suppressing the effects of $v_{\text{rec\_ripple}}$. This can be done by two methods. Method I is an open loop control where the $v_{\text{rec\_ripple}}$ is extracted and injected out of phase by the GDCM. In order to do this, $v_{\text{rec\_ripple}}$ is scaled down to ± 1 V (peak value of the carrier signal) by a scaling factor 'k', as shown in Fig. 8(a). The value of k is decided based on the peak value of the $v_{\text{rec\_ripple}}$ under the worst case disturbance. From the simulation studies based on the field data, the peak value of worst case $v_{\text{rec\_ripple}}$ is 120 V. Hence the k value is chosen as 0.008, in order to scale down the ripple to ± 1 V. This scaled ripple is used as the modulating signal (v_{mod}) and compared with a 10 kHz carrier signal to generate the pulses for the H-bridge. In this way, the magnitude of the low frequency ripple in the i_c can be suppressed.

Suppression of the effect of $v_{\text{rec\_ripple}}$ is also possible by measuring the current through the inductor. This is referred to as Method II. The ac component of the inductor current ($i_{\text{ind}-\text{ripple}}$) acts as the measure of error between the $v_{\text{rec\_ripple}}$ and v_{sec}. Hence, instead of measuring the v_{sec} and finding the error, the scaled error ($i_{\text{ind}-\text{ripple}}$) itself is measured. The $i_{\text{ind}-\text{ripple}}$ is extracted from the measured i_{ind} by filtering the dc component and processed through a controller. The output of the controller is compared with the carrier signal for pulse generation, as shown in Fig. 8(b).

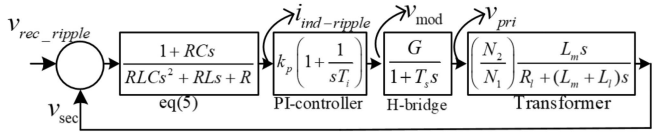

Fig. 10. Control loop of Method II.

TABLE II
GDCM CONTROL LOOP PARAMETERS

Parameter		Value
Controller	k_p - Proportional constant	0.45
	T_i - Integral time constant	800 μs
Inverter	G - Gain ($V_{\text{dc}-\text{GDCM}}/2$)	270
	T_s - Switching delay time	50 μs
Transformer	N_2/N_1 - Transformation ratio	1/5
	L_m - Magnetizing inductance	60 mH
	L_l - Leakage inductance referred to primary	0.62 mH
	R_l - Winding resistance referred to primary	4 Ω

TABLE III
CLOSED LOOP TRANSFER FUNCTION COEFFICIENTS

	Value
a_1	$T_i\,(T_s + RC)$
a_2	$T_i + RC$
b_1	$RLCT_iT_s\,(L_m + L_l)$
b_2	$RLCT_i\,\{R_lT_s + (L_m + L_l)\} + (L_m + L_l)\,(L + RT_i)\,T_sT_i$
b_3	$R_lRLCT_i + (L_m + L_l)\,(L + RT_s)\,T_i + R_lT_sT_iL + k_pGL_mRCT_i$
b_4	$k_pGL_m\,(1 + RC) + RR_lT_sT_i + T_i\,\{(L_m + L_l)\,R + LR_l\}$
b_5	$k_pGL_m + RR_lT_i$

The control loop for this method II is given in Fig. 10 and the parameter values are given in Table II. As mentioned, the ac component of inductor current ($i_{\text{ind}-\text{ripple}}$) is a representation of the error between $v_{\text{rec\_ripple}}$ and v_{sec}. The value of $i_{\text{ind}-\text{ripple}}$ for a given ripple voltage in the dc side is calculated using the expression (5), which is derived based on the simplified dc network shown in Fig. 5(a). The resistances associated with the choke and capacitor are neglected for this transfer function, for the sake of simplicity. This $i_{\text{ind}-\text{ripple}}$ is input to the PI controller as shown in Fig. 10. Due to the oscillatory nature of $i_{\text{ind}-\text{ripple}}$, the error ($i_{\text{ind}-\text{ripple}}$) may not be completely zero. However, its magnitude can be reduced as low as possible to 1% of its value prior to the control action. Since the ripple frequency to be compensated is in the range of 300 Hz, the bandwidth of the closed loop transfer function is kept higher. Hence, the controller parameters (k_p, T_i) are chosen such that the error is 1% and bandwidth is around 2 kHz. The closed loop transfer function of the control loop is given in (6) and the coefficients are given in Table III. The frequency domain response of this loop is given in Fig. 11. It can be seen that the bandwidth is 2.1 kHz. The transformer parameters used in this control loop are measured

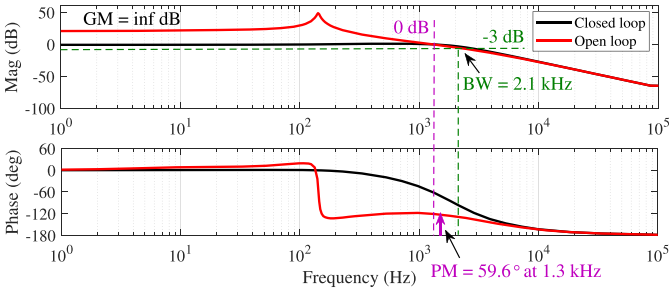

Fig. 11. Bode plot of control loop.

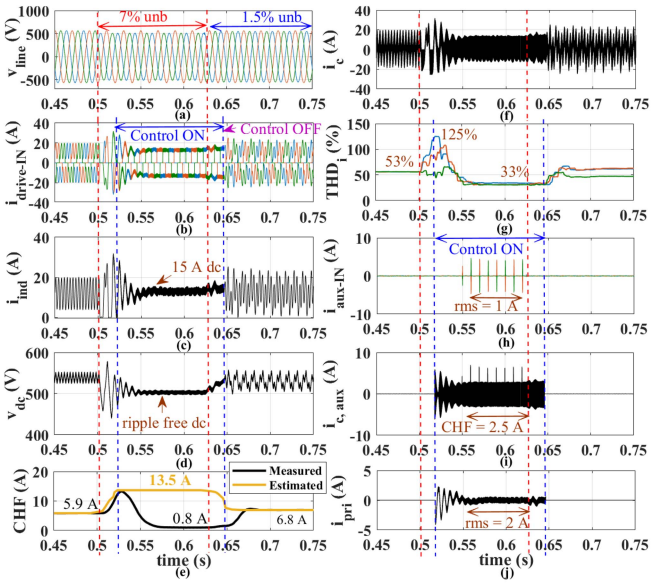

Fig. 12. Simulated response of the proposed ASD+GDCM under a supply voltage unbalance of 7%: (a) input line voltage, (b) drive input current, (c) inductor current, (d) DC bus voltage, (e) measured and estimated value of CHF, (f) capacitor current, (g) THD_i of the ASD input, (h) input current to the GDCM, (i) GDCM capacitor current, and (j) transformer primary current.

from the built unit and its design is given in the next section

$$\frac{i_{\text{ind-ripple}}}{v_{\text{rec\_ripp}} - v_{\text{sec}}} = \frac{1 + RCs}{RLCs^2 + RLs + R} \tag{5}$$

$$\frac{v_{\text{rec\_ripp}}}{v_{\text{sec}}} = \frac{k_p G L_m \left\{a_1 s^2 + a_2 s + 1\right\}}{b_1 s^4 + b_2 s^3 + b_3 s^2 + b_4 s + b_5}. \tag{6}$$

A sample validation of the proposed control under an unbalanced supply voltage is shown as a simulation study in Fig. 12. A 7% unbalance is introduced in the supply voltage at $t = 0.5$ s. When the estimated CHF (CHF_{est}) crosses the preset limit of 11 A, the control is turned ON. At $t = 0.65$ s, the unbalance in the supply voltage is reduced to 1.5%. As a result, the CHF_{est} reduces below 11 A and hence the control is turned OFF. Thus, the operation of the GDCM is controlled by the value of CHF_{est}. The simulated waveform shows the reduction of input current THD_i from 125% (in the worst phase) to 33% as shown in Fig. 12(g). The CHF reduction from 13.5 to 0.8 A is shown in Fig. 12(e). Thus, the GDCM reduces the stress on the dc bus capacitor. Also, a ripple-free (low frequency) inductor current and dc bus voltage are observed as shown in Fig. 12(c) and (d),

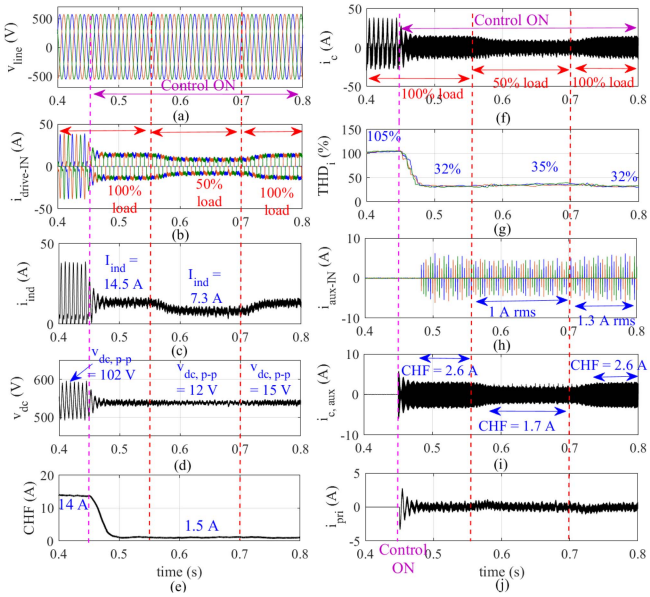

Fig. 13. Simulated response of the proposed ASD+GDCM with a supply voltage having 2% of 2^{nd} harmonic under different load conditions: (a) input line voltage, (b) drive input current, (c) inductor current, (d) dc bus voltage, (e) measured value of CHF, (f) capacitor current, (g) THD_i of the ASD input, (h) input current to the GDCM, (i) GDCM capacitor current, and (j) transformer primary current.

respectively, when the GDCM control is ON. The voltage and current signals of the GDCM are also shown in Fig. 12. It can be seen that the current input to the GDCM is 1 A RMS ($\approx 9\%$ of the ASD rated current) with a peak value less than 5 A. Also, the CHF of the capacitor in the GDCM is only 2.5 A. The current through the primary side of the transformer is 2 A RMS. This shows that the required rating of the GDCM is much lesser than that of the main ASD. It can be observed from Fig. 12(e) that during transition period, the CHF_{est} is comparatively faster than the actual CHF, which is calculated based on the measured capacitor current. This is due to the reason that the estimation is directly based on the measured v_{rec}. In a way, it is advantageous as the control will take action little faster (before the current actually reaches its critical limit). However, in the steady state, they are equal, when the control is OFF. In the case of PQ disturbances, there will be a considerable $v_{\text{rec\_ripple}}$ and hence the CHF_{est}.

Once the CHF_{est} crosses its preset limit, the GDCM control is turned ON and the actual CHF in the capacitor current reduces. So, until the disturbance is present, the estimated value will be high while the actual value will be low. Hence, the estimated value will not be equal to the actual value when the control is ON.

The performance of GDCM is also evaluated under light load conditions. For instance, a simulated case is shown in the Fig. 13, where the supply voltage is added with 2% of 2^{nd} ordered harmonic at 0°. The impact of this distorted supply voltage on all the signals can be seen from $t = 0.4$–0.45 s. Notably, the THD_i of input current is increased to 105% [see Fig. 13(g)], dc bus voltage ripple is around 102 V [see Fig. 13(e)], and CHF of capacitor current is 14 A. When the control is turned ON at 0.45 s, the values of all the forementioned parameters reduced

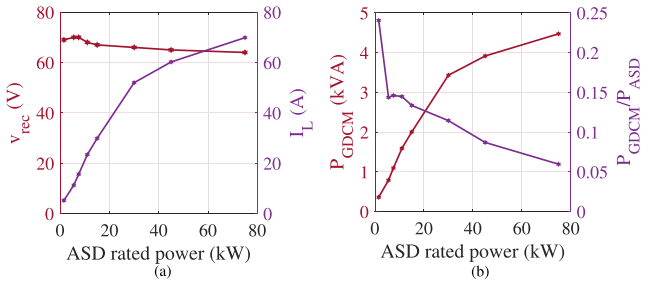

Fig. 14. GDCM ratings for different power rated ASDs. (a) Voltage and current ratings. (b) Power rating of GDCM and its ratio with respect to ASD rated power.

– 32 % THD_i, 15 V dc bus ripple, and 1.5 A CHF. To verify the performance of the GDCM under light load conditions, the load on the drive is reduced from full load to half load at 0.55 s. During this low load condition also, the control maintains the same quasi-square shape of the input current which validates the performance of GDCM, as can be seen from the Fig. 13(b). It is also worth to note that the impact of grid disturbances on the dc bus capacitor are less severe under light load conditions compared to the full load condition [9].

B. Power Circuit Design of GDCM

The power rating of compensation module depends on the level of disturbance that GDCM has to support. Based on the field data – 7% of unbalance, 20% of odd harmonic distortion, and 4% of even order harmonic distortion are the worst-case boundary values [9]. It is found from the simulation studies that the maximum magnitude of ripple voltage (RMS) that correspond to the above disturbance condition is: 25 V at 100 Hz, 50 V at 300 Hz, and 10 V at 150 Hz. Hence, the worst case ripple voltage that needs to be compensated by this GDCM for these worst-case disturbances is calculated as 58 V (RMS). With a safety factor of 1.2, the voltage rating of GDCM is set as 70 V. The current response for a given ripple voltage (v_{rec}) can be calculated from (7), which is derived using the dc network as in Fig. 5(a). Using (7), the net RMS value of the current rating is calculated as 15 A. Hence, the rating of the GDCM is $70 \times 15 \approx 1.1$ kVA, which is approximately $1/7^{\text{th}}$ the rating of the ASD.

$$\frac{I_L}{V_{\text{rec}}} = \frac{\omega C\left(R_{2\omega} - R\right) - j\left(1 + RR_{2\omega}\omega^2 C^2\right)}{d\left(\omega\right)}. \tag{7}$$

Further, the following exercise is carried out to understand the power rating of GDCM for different power rated ASDs. For this, ASDs of different power ratings from 1.5 to 75 kW are considered. It is found from the simulation studies that the worst case ripple voltage is nearly same (around 65–70 V) for all the ASDs of different rated power. Using (7), the RMS value of the current (I_L) is calculated for each power level and plotted as shown in Fig. 14(a). The ratio of power rating of the GDCM (P_{GDCM}) to the ASD rated power (P_{ASD}) is shown in Fig. 14(b). It can be seen that this power ratio is decreasing with increase in the ASD power rating. Hence, GDCM is more advantageous with high power ASDs than with low power ASDs.

The transformation ratio (N_2/N_1) of the transformer is decided based on the worst-case peak value of the ripple voltage ($v_{\text{rec\_ripp-peak}}$) to be compensated and the dc bus voltage of GDCM ($V_{\text{DC-GDCM}}$). The worst-case value of $v_{\text{rec\_ripp-peak}}$ that is observed from the simulation studies is 90 V. The value of $V_{\text{DC-GDCM}}$ depends on the supply voltage. It is likely that sag may also occur along with other PQ disturbances in the supply voltage. Most of the ASDs may trip in under voltage fault due to the sag when the residual supply voltage is in the range of 70%−80% based on their internal settings. For the selected ASD, the under voltage trip level is set at 80% of its rated voltage. Hence, the GDCM may be required to support up to this sag level. The dc voltage of GDCM at 80% supply voltage is $0.8 \times 400 \times 1.35 = 432$ V. In order to ensure the GDCM control not entering in to the over modulation, the required transformation ratio is calculated using (8) as 0.208 ($\approx 1/5$). In (8), MI denotes the modulation index. The values of the GDCM components are given in Table IV. In the worst-case ripple condition, the CHF value of the capacitor (C_{GDCM}) is observed to be 2.5 A [cf. Fig. 12(i)] and hence a 5 A rated current capacitor is sufficient in the GDCM. Similarly, the maximum current through the IGBTs is 4 A and hence a 10 A rated current device is sufficient. Diode bridge rectifier is used to support the dc voltage at GDCM. Though there is no real power support given by the GDCM to the main ASD, the use of diode bridge has two major advantages. One is to supply the losses for the GDCM and the other one is on the reduction in the required capacitance at the dc link. The losses in the transformer and the H-bridge can be supported by this diode bridge in the GDCM. Since the diode bridge can charge the capacitor (six times in a power cycle), the required capacitance for a reasonable ripple (3%) in the dc bus of GDCM is very less. In the present circuit, two 460 μF (in series for a dc bus of 800 V) capacitors are used. In order to maintain the same dc bus ripple (around 3%) without the diode bridge, the required capacitance will be around 3300 μF (around 7 times more than the previous value). Further, the value of this capacitance is more than the capacitance used in the main ASD. Moreover, the cost of this bulky capacitor is much higher than the extra diode bridge used. Hence, considering the cost and space, using the diode bridge seems to be a better method than a bulky capacitor. The design of the transformer is discussed as follows:

TABLE IV
GDCM PARAMETERS

Parameter	Diode	Capacitor	IGBTs	Transformer
Value	800 V, 5 A	800 V, 230 µF	800 V, 10 A	1.1 kVA , 5:1

$$V_{\text{DC-GDCM}} \times MI \times \frac{N_2}{N_1} = v_{\text{rec\_ripp-peak}}. \tag{8}$$

Design of transformer: As mentioned, the transformer is rated for 1.1 kVA with a turns ratio of 1/5. On the secondary side, the transformer has to carry dc current and hence a dc flux in the core as well. Hence the transformer needs to be designed with care to avoid saturation. An amorphous core (with EE geometry) is used in the present design. The primary and secondary turns are calculated to be 450 and 90, respectively, to have the peak value of ac flux density under a worst-case

TABLE V
GDCM LOSSES

Parameter	Diode bridge	Capacitor	IGBTs	Transformer
Losses	10.4 W	5 W	13.1 W	46.3 W

disturbance to be 0.35 T. To avoid saturation, an air gap of 3 mm is provided in the core to restrict the dc flux density to be 0.55 T, calculated using (9), [21]. In (9), N_s represents the secondary turns, I_{dc} is the average value of the choke current under full load condition which is 15 A, l_g is the air gap (in cm), MPL is the Magnetic Path Length of the core which is 41 cm, and μ_m is the permeability of the magnetic material which is found as 3000 by experimental measurements in the lab. On the whole, the peak value of flux density ($B_{\text{dc}} + B_{\text{AC,peak}} = 0.55\ T + 0.35\ T$) is restricted to be lesser than 1T.

$$B_{\text{dc}} = \frac{0.4\pi N_s I_{\text{dc}}}{l_g + \frac{\text{MPL}}{\mu_m}} \times 10^{-4}\ T. \tag{9}$$

C. Efficiency of GDCM

The losses of GDCM power components are tabulated in Table V. Total losses in GDCM circuit is 74.8 W (10.4 + 5 + 13.1 + 46.3). The efficiency of GDCM circuit alone is 93.2%.

Loss calculation considering the total ASD unit along with GDCM circuit: The efficiency of the ASD will drop when the supply voltage is polluted with disturbances such as unbalance and harmonics. The calculated efficiency of the drive (only ASD) when the supply voltage is 7% unbalanced (worst-case) is 92% where the loss is 600 W. This is due to the reason that the power components (input rectifier, dc chokes, dc capacitors) will face extra ripple current. When the GDCM is active, the current drawn will be a quasi-square and the rms value reduces compared to the case with disturbance. The efficiency of ASD in this case is 95% (more than the value under its normal operating conditions, as the choke and capacitor losses reduced). The loss under this case is 300 W. Also, an extra loss of 74.8 W (as mentioned) will be there in the GDCM circuit. Hence, the efficiency of the total unit (ASD+GDCM) (when the GDCM circuit is operating) will be 95% (7500 – (300+74.8) / 7500). It can be noted that the due to GDCM the efficiency of the overall system (ASD+GDCM) increased from 92% to 95%.

D. Validation of Proposed GDCM

The proposed GDCM is validated for a large set of combinations of unbalance and harmonics in the supply voltage considering the variation in grid impedance conditions. The system is also validated by the test setup created in the lab.

1) Validation Under a Large Set of Data: For this validation, the set of input voltage combinations are taken based on the field data, as follows. The even ordered harmonics (2nd and 4th) are varied from 0 to 4% in steps of 2% along with its angle variation from 0° to 180° in steps of 60°. Also, the odd ordered harmonics (5th and 7th) are varied from 0 to 20% in steps of 10% along with the harmonic angle variation from 0° to 360° in steps of 60°. Altogether, 46 656 combinations are obtained. Along with these combinations, the unbalance of magnitude

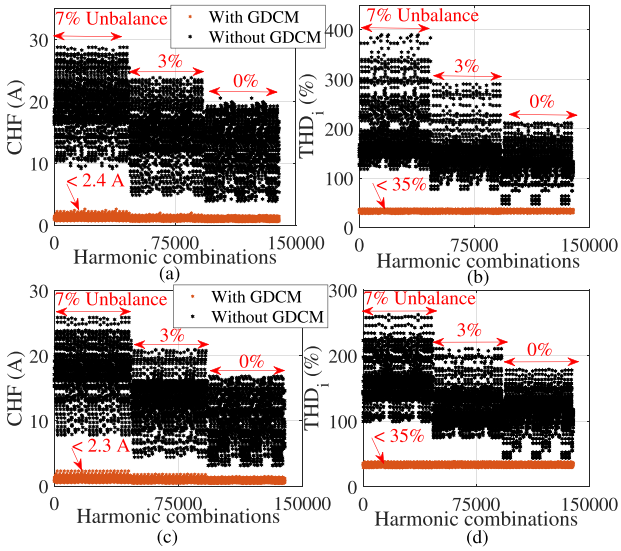

Fig. 15. Performance evaluation of proposed control for a large set of disturbances under different grid impedances: $R_{\text{SCE}} = 1000$ – (a) CHF, (b) THD_i; and $R_{\text{SCE}} = 100$ – (c) CHF, and (d) THD_i.

0%, 3%, and 7%, is also introduced simultaneously in the supply voltage. On the whole, 139 968 different combinations of supply voltages are obtained. All these different voltage sets are applied to the ASD and simulated with the proposed GDCM through automated scripts. In order to verify the efficiency of the proposed compensator under all the disturbance conditions, control is kept always ON irrespective of estimated CHF value. The resultant CHF and THD_i values for all the combinations are shown in Fig. 15(a) and (b), respectively. It can be seen that the maximum CHF value for all the cases is lesser than 2.5 A. This proves the validity of the proposed compensation technique under a wide range of disturbance conditions. Also, the THD_i values are less than 35% for all the cases irrespective of the disturbances.

2) Validation Under a Weak Grid Condition: In the previous section, the validation of the proposed GDCM is studied under a stiff grid ($R_{\text{SCE}} = 1000$) condition. In order to validate the proposed control under a comparatively weak grid condition, the grid impedance value is altered such that the R_{SCE} value is 100. This grid impedance is considered based on the Single Line Diagram of an industrial site. Under this grid impedance condition, the different combinations of supply voltage used in the previous section are applied to the ASD and simulated. The CHF and THD_i responses under all the disturbance conditions, with and without GDCM, are shown in Fig. 15(c) and (d), respectively. It is evident from these plots that the GDCM works satisfactorily under a weak grid condition also.

3) Hardware Validation: The proposed GDCM is validated using the test setup created in the lab as shown in Fig. 16. The ASD taken is a Danfoss VLT FC302 7.5 kW drive. The developed compensation module along with the designed transformer is also shown in Fig. 16. A TMS320F28335 DSP controller is used for the implementation of the control algorithm. The MX22.5-3Pi programmable power supply from Ametek is used for introducing the different unbalance and harmonics at

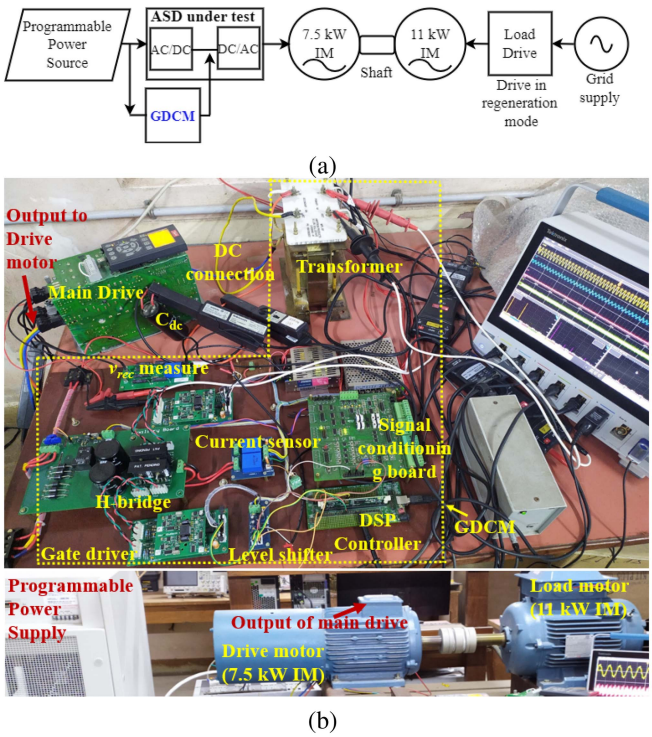

Fig. 16. Hardware test Setup. (a) Block diagram. (b) actual pictures.

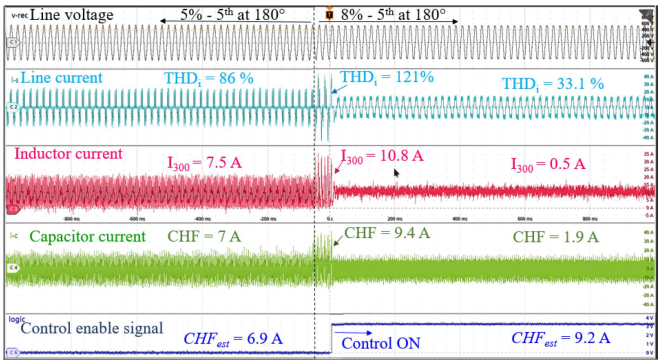

Fig. 17. Validation of GDCM under a odd harmonic case – 5^{th} harmonic magnitude variation from 5% to 10% at 180°.

required magnitude and angle. The CHF limit in order to turn ON the compensation is set as 9 A (conservatively, instead of 11 A) for the validation purpose.

Supply voltage with odd harmonic (5^{th}) is shown for a sample validation case. As mentioned, 180° is a critical harmonic angle for 5^{th} harmonic. Hence, 5% 5^{th} harmonic at 180° is applied to the supply voltage and the response of the ASD for this supply condition is shown in Fig. 17. It shows the line voltage, line current, inductor current, capacitor current, and control enable signal. The CHF value is estimated as 6.9 A while the actual CHF is measured as 7 A. The magnitude of 5^{th} harmonic is increased to 8% and the increase in the line, inductor, and capacitor currents can be noted in Fig. 17. As the estimated value (9.2 A) of CHF crosses its limit, the control is turned ON. Subsequent to initiation of control, the CHF and THD_i values reduce to 1.9 A and 33.1%, respectively, as seen from the plot. The CHF_{est} is still 9.2A as the 5^{th} harmonic is still present in the supply voltage.

The validation study is also carried out for different harmonic and unbalance cases and Fig. 18 shows two cases – one case where the supply voltage is with even ordered harmonics and other case with unbalance. A 1.4% 2^{nd} harmonic at 0° (critical angle for 2^{nd} harmonic [14]) is applied to the supply voltage and the response line, inductor and capacitor currents are shown in Fig. 18(a). The CHF and THD_i values are calculated as 9.2 A and 118%, respectively. For the same input voltage condition, the response currents with GDCM is shown in Fig. 18(b). It can be seen that the CHF and THD_i values reduced to 2.1 A and 32.2%, respectively.

The supply voltage is introduced with 5% of unbalance and the response line, inductor and capacitor currents are shown in Fig. 18(c). The CHF and THD_i values are calculated as 9.8 A and 127%, respectively. For the same input voltage condition, the response currents with GDCM is shown in Fig. 18(d). It can be seen that the CHF and THD_i values reduced to 2.2 A and 32.6%, respectively.

VI. Advantages of GDCM – Technology Comparison

As mentioned in Section I, there is no direct solution reported to reduce the stress on the dc link capacitor in the presence of PQ disturbances. However, some of the solutions available to reduce the input harmonic current and use of active capacitors, may also reduce the stress on the capacitor. Hence such techniques are considered for the comparison study. For this study, the existing techniques such as MDVR, SVC, and AFR are considered. A modified DVR [12] can be used to filter out the disturbances in the supply voltage and provide a balanced sinusoidal supply to the ASD. While this seems to be a workable solution, the additional components and their ratings are comparatively higher. The topology of MDVR is shown along with its parameter values in Fig. 19(a). It requires seven voltage sensors and thee current sensors for its operation. The size of the filter inductance (L_f) and dc bus capacitor (C_{MDVR}) used in the MDVR is comparable to the corresponding ASD main dc link parameters. The next existing solution is SVC [15] and its topology is shown in Fig. 19(b). It requires a single phase inverter with an *LC* filter connected between the dc bus voltage and the inverter. It requires three sensors for its operation. The comparison of the performance of the techniques and their ratings (current and voltage) are better understood using simulations. Hence, a sample case with the supply voltage having 10% 5^{th} harmonic at 0° and 2% 2^{nd} harmonic at 0° is considered for the study. This distorted supply voltage is input to the ASD with different techniques mentioned (MDVR, SVC, and GDCM) and simulated separately (one technique at a time). The simulation results are plotted as shown in Fig. 20. The responses of the existing techniques to this distorted supply voltage are compared with GDCM as follows.

1) ASD Input Current: Due to this distorted supply voltage, the THD_i of input current drawn by ASD+SVC is 81% as seen from Fig. 20(c). The MDVR, on the other hand, cancels the harmonics in the line side due to its voltage introduced as shown by v_{dvr} [see Fig. 20(b)] and the ASD terminal voltage (v_t) is

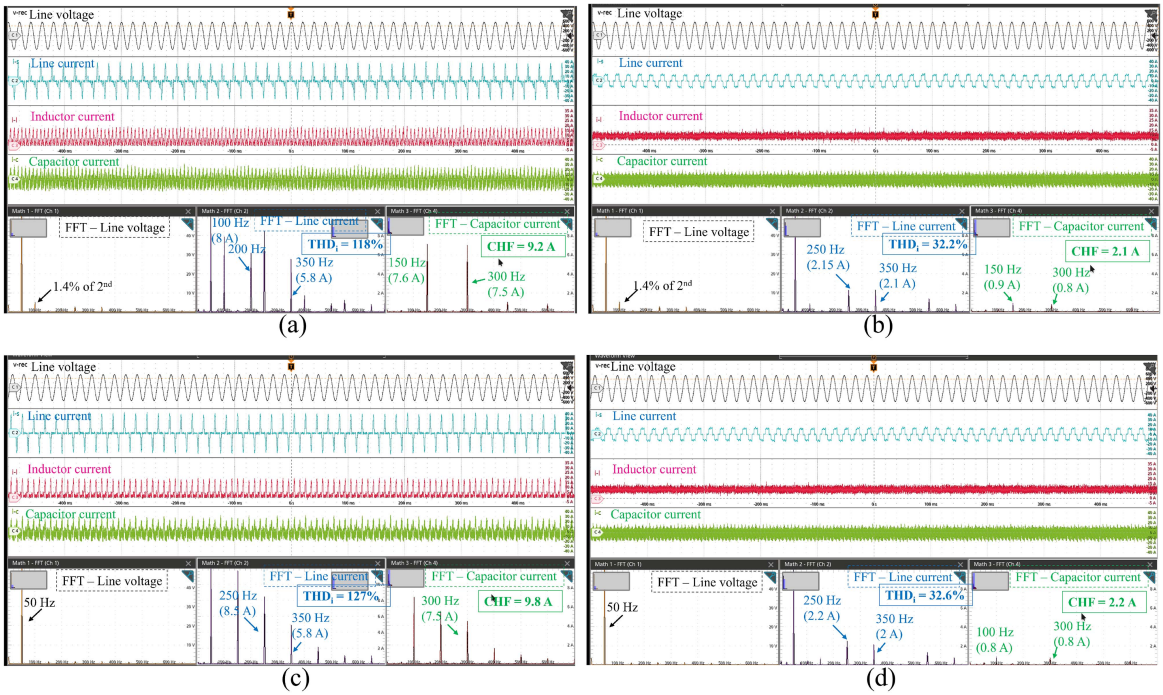

Fig. 18. Validation of GDCM under – even ordered harmonic of 1.4% 2nd at 0° - (a) without control and (b) with control; 5% unbalance - (c) without control and (d) with control.

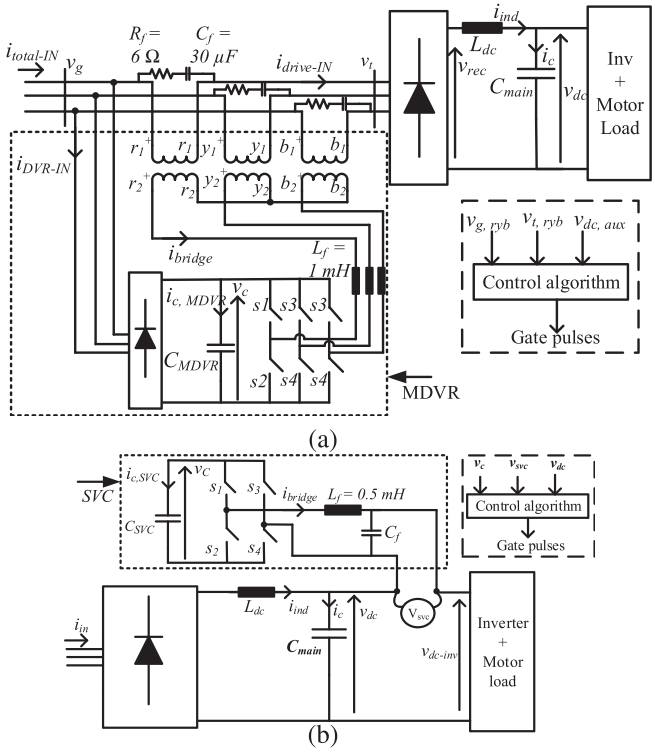

Fig. 19. Topology of (a) Modified DVR (MDVR) [12] and (b) SVC [15].

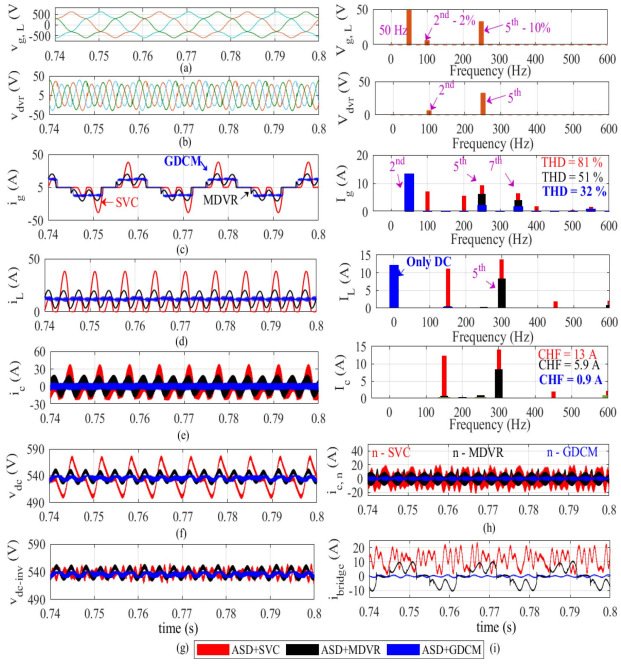

Fig. 20. Comparison of the proposed GDCM with MDVR and SVC: (a) input line voltage and its FFT, (b) voltage output from MDVR and its FFT, (c) source current and its FFT, (d) inductor current and its FFT, (e) capacitor current and its FFT, (f) dc bus voltage, (g) voltage input to the inverter, (h) capacitor current in additional unit, and (i) current through the bridge in additional unit.

free from the distortion. The THD_i of the drive input current reduces to 51% due to the filtering of 2nd and 5th harmonics in the supply voltage and only the ASD characteristic harmonics are present as seen from Fig. 20(c). The GDCM, however, reduces this THD_i to 32% due to the quasi-square shape of the current.

2) Ripple in DC Link Inductor and Capacitor Currents of ASD: Inductor (and capacitor) current is dominated with by 150

TABLE VI
COMPARISON OF GDCM WITH MDVR [12], AFR [13], AND SVC [15]

Parameter	MDVR [12]	AFR [13]	SVC [15]	GDCM (proposed)
Compensation	source side	source side	DC bus side	DC bus side
Main aim	Balanced sinusoidal voltage at load	THD_i of source current $< 5\%$	DC link Capacitance reduction	Capacitor stress reduction
DC choke and capacitor stress	Medium - 300 Hz ripple is still present	Less - only switching frequency components	More - ripple is still present	Less - only switching frequency components
Retrofit option	Yes - feasible	No	Yes - feasible	Yes - feasible
Running condition	Whenever required	Always	Whenever required	Whenever required
Additional components	High - 1 bridge rectifier, 1 DC bus capacitor, 1 VSC (6 switches), 3 LCR filters, 3 transformers	High - 3 filter inductors, 6 high current switches	Less - 1 bridge rectifier, 1 DC bus capacitor, 1 H-bridge	Less - 1 bridge rectifier, 1 DC bus capacitor, 1 H-bridge, 1 transformer
Control requirement	complex - dq control	complex - vector or direct power control	simple - no complex math calculations	simple - no complex math calculations
Sensing requirement	grid voltages (3), load voltages (3), and load currents (3)	grid voltages (3), load voltages (3), and grid currents (3)	DC capacitor voltage (1) and voltage across SVC (1)	rectified voltage (1) or inductor current (1)

and 300 Hz components in the ASD+SVC due to the presence of even and odd ordered harmonics respectively, as shown in Fig. 20(d) and (e), respectively. It can be seen that the 150 Hz component is absent in the inductor and capacitor currents in ASD+MDVR topology as shown in Fig. 20(d) and (e), respectively. This is due to the removal of even ordered harmonics at the ASD terminal by the MDVR. However, a 300 Hz ripple still appears due to the six pulse rectification, whereas this 300 Hz ripple is also filtered out in ASD+GDCM. This provides a low frequency ripple-free flat inductor current, capacitor current, and dc bus voltage.

3) DC Bus Voltage to the Load: Due to the compensation by SVC, the dc voltage applied at the inverter input terminal is free from low frequency components as shown in Fig. 20(g). The impact of SVC can be observed by comparing the dc bus voltage and inverter input voltage as shown in Fig. 20(f) and (g) respectively. For the other two techniques (ASD+MDVR and ASD+GDCM), the inverter input voltage is same as the dc bus voltage. ASD+MDVR topology will still have low frequency ripple in the $v_{\mathrm{dc-inv}}$ and the magnitude of ripple is based on the *LC* design value, usually less than 5%. While $v_{\mathrm{dc-inv}}$ in other two topologies (ASD+GDCM and ASD+SVC) will have only a negligible magnitude of low frequency ripple, as can be seen from Fig. 20(g).

4) Capacitor Ripple Current in Additional Circuit: All additional circuits (MDVR, SVC, and GDCM) have a capacitor in its their dc link. This capacitor is named as C_{MDVR}, C_{SVC}, and C_{GDCM}, as shown in Figs. 19(a), (b), and 6, respectively. The RMS values of the capacitor current in the additional circuit C_n (where n is MDVR or SVC or GDCM) is 12.5 A with SVC, 6 A with MDVR, and 3.2 A with GDCM. From this, it can be inferred that the capacitor ripple current in additional circuit is comparatively high with SVC and MDVR, than with GDCM as shown in Fig. 20(h). Hence a higher current rating capacitor is required for SVC and MDVR, compared to GDCM.

An AFR could be another option that reduces the THD_i of the source current to lesser than 5% but the cost is nearly 2 to 3 times the cost of a normal diode bridge front-end ASD. Thus GDCM is better than SVC, MDVR, and AFR in terms of control, performance, quantity, and rating of extra components. A detailed comparison is given in Table VI. This shows the advantage of GDCM over the other methods.

VII. CONCLUSION

While the PQ of the industrial grid is poor due to the dominance of distortion and unbalance, its effect on the dc bus capacitor is alarming. Also, it is seen that the CHF value may cross its critical reference value for some cases, where the distortion level is even lesser than the corresponding IEC standard limit. Hence the dominance of distortion and unbalance in the supply voltage is critical to the dc bus capacitor. In order to operate the ASD under such polluted grid conditions, an additional circuit (GDCM) that could be retrofitted to the main ASD is proposed. It is seen that the power level of the proposed module is much lesser than that of the main ASD. The proposed GDCM improves the line current harmonics and it is expected to improve the lifetime of the dc bus capacitor.

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