A Parallel Input and Versatile Output Dual Active Bridge Converter

Sohaib Qazi, *Graduate Student Member, IEEE*, Prasanth Venugopal, *Senior Member, IEEE*, Alan J. Watson, *Senior Member, IEEE*, Patrick Wheeler, *Fellow, IEEE*, and Thiago Batista Soeiro, *Senior Member, IEEE*

***Abstract*—Due to their easy scalability to high power, simple control mechanism, and effective semiconductor and transformer utilization, H-bridge-derived isolated dc/dc converters have taken a central stage in various power electronics applications such as fast charging stations, dc microgrids, and renewable energy integration. Among the bidirectional variants, the dual active bridge (DAB) converter stands out as a common choice due to its direct power flow control mechanism, inherent soft switching realization, symmetric and modular structure, etc. However, the conventional version of the topology exhibits a significant reduction in efficiency when subjected to wide ranges in voltage gain and output power. This limitation can potentially hinder its application in public dc chargers, where different charging profiles and vehicle voltage classes are frequently expected. This article proposes a new versatile topology derived from the DAB converter that caters to the requirement of a wide output voltage range and improves the efficiency characteristics while mitigating the current and/or voltage stresses on the semiconductor devices. Furthermore, a suitable modulation strategy is developed that optimizes the soft switching action of the converter in accordance with the load demand. The converter operation is explained and validated through a steady-state model, simulations and an 11 kW experimental prototype.**

***Index Terms*—Dual active bridge (DAB), fast charging, isolated dc-dc converter, modulation, power converter.**

I. Introduction

THE emissions arising from port activities, shipping, and inland waterways have largely gone unnoticed and unaddressed amidst the ever-increasing global freight and mobility operations [1]. Within the port environment, terrestrial and waterborne transport not only contribute to the global greenhouse gas emissions, but also cause the formation of several pollutants that are hazardous to the natural ecosystem in the port vicinity [2]. Therefore, quite recently, the greening up of ports and inland waterways has been identified as a key milestone in enhancing environmental sustainability within the transportation sector and as a result, efforts are being undertaken to help achieve that goal [3]. There has been a push toward greening up of the vessels and operating equipment within major harbour areas, much of which can take place through electrification [4], [5].

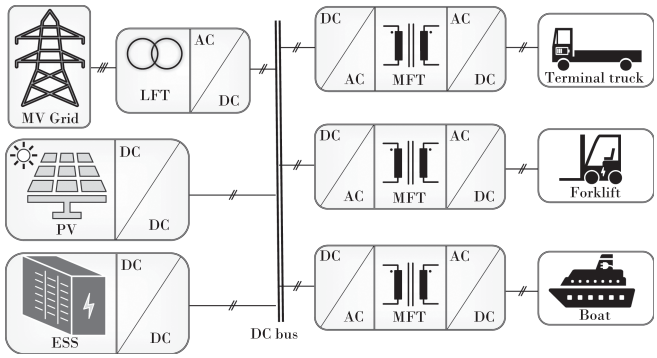

Fig. 1. Onshore DC charging infrastructure employing solar power and energy storage system.

One of the challenges in accelerating the process of electrification in port areas is the deployment of sufficient charging stations required for various onshore applications. Fig. 1 shows a typical onshore charging station framework wherein the isolated dc/dc converters employ medium frequency transformers (MFTs). Each converter may comprise of multiple building blocks connected in parallel each equipped with an MFT or alternatively employ only one MFT connected to a single high-power ac/dc module on each side. The former approach enables the use of discrete devices, easy scalability, and flexibility while the latter reduces the parts count, component cost, and can result in a simpler design. These converters are tasked with handling the power drawn from the fixed-voltage shore dc bus and appropriately match the voltage/current with the vehicle requirements. In addition to water-borne transport such as boats and water taxis, various terrestrial vehicles operate within the shore environment such as trucks, automated guided vehicles,

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Sohaib Qazi is with the Power Electronics Group, University of Twente, 7500 AE Enschede, The Netherlands, and also with the Power Electronics, Machines and Control Research Institute, University of Nottingham, NG7 2RD Nottingham, U.K. (e-mail: sohaib.qazi@utwente.nl).

Prasanth Venugopal and Thiago Batista Soeiro are with the Power Electronics Group, University of Twente, 7500 AE Enschede, The Netherlands (e-mail: prasanth.venugopal@utwente.nl; t.batistasoeiro@utwente.nl).

Alan J. Watson and Patrick Wheeler are with the Power Electronics, Machines and Control Research Institute, University of Nottingham, NG7 2RD Nottingham, U.K. (e-mail: alan.watson@nottingham.ac.uk; pat.wheeler@nottingham.ac.uk).

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terminal tractors, reach stackers, forklifts, etc. Depending on the powertrain of the vehicle, the output voltage requirement for the back-end onshore converter can be quite wide. Furthermore, the battery and powertrain bus voltages have been going up recently to increase the charging power and reduce the charging times without excessively incrementing the cable copper. As a result, many manufacturers are already offering commercial units that can facilitate multifunctional charging and operate at a $1\,\mathrm{kVdc}$ output, such as Kempower Satellite V1/V2, Heliox Ultrafast FC, ChargePoint Express Plus, Blink Hypercharger, etc. [6], [7], [8], [9]. In order to increase the return on investment and make these solutions future-proof, manufacturers are incentivised to go further and develop solutions up to a $1.5\,\mathrm{kV}$ output which is the maximum dc voltage covered under the IEC 62196-1:2022 combined charging system (CCS) standard for the conductive charging inlets and connectors as well as the latest ChaoJi GB/T standards [10], [11]. However, conventionally used converter topologies such as the full-bridge-derived isolated dc/dc converters exhibit efficiency characteristics that can severely deteriorate from the optimum under changes in output voltage and/or power. For example, in the case of conventional *LLC* resonant converters, for a given load, the converter exhibits a deteriorating efficiency with a reduction in voltage. Consequently, for a charging unit designed for a wide output voltage range, the majority of vehicles (which are presently lower voltage class) would suffer from low-efficiency charging if conventional topologies are employed. Moreover, higher output voltage necessitates the use of semiconductor devices with increased blocking voltage capability in the back end which may increase cost, reduce reliability, and compromise the efficiency due to higher semiconductor losses. Therefore, the development of an across-the-board efficient charging infrastructure can be challenging for manufacturers. Since the variation in battery voltages naturally came up with the adoption of different EVs and battery types, the development of wide-output voltage charging converters for increased efficiency has been extensively explored in the literature. Furthermore, both unidirectional and bidirectional topologies have been investigated recently wherein innovations primarily comprise topological modifications [12], [13], [14], enhancements in modulation and control [15], [16], [17], [18], employing hybrid semiconductor architectures [19], [20], [21], [22], use of multistage converters [23], [24], etc. The dual active bridge (DAB) converter and its variants have particularly received a lot of attention due to its flexibility, simple control, easy-to-scale modular structure along with inherent bidirectionality, which enables vehicle-to-grid (V2G) power transfer. The V2G resource is particularly attractive for vehicles with large energy storage onboard that can provide a spinning reserve, aid in peak load levelling, and enhance the grid stability [25], [26]. However, the existing literature pertaining to vehicle charging with DAB is directed at output voltages in the range 0–1000 V [27], [28], [29]. Therein, the use of low-frequency auxiliary switches to aid in voltage or current doubling is often carried out using mechanical or solid-state switches. This configuration effectively results in two near-identical peak efficiencies in different operating modes and enables low-voltage high-current and high-voltage low-current power delivery. Such an approach has been carried out in conventional DABs [27], phase-shift full-bridge converters [30] asymmetrical three-phase dc–dc converters [31], etc. However, widening the voltage range of such systems results in extending the operating regions in each mode quite significantly ($750\,\mathrm{V}$ in each mode assuming a symmetrical threshold). As a consequence, the operating efficiencies are compromised for the wide output range in the individual modes.

This article introduces a novel parallel-input and versatile-output DAB (PIVODAB) converter topology, as shown in Fig. 2(a). The converter is fed from a $750\,\mathrm{V}$ bus and can operate with an output voltage range of 150–$1500\,\mathrm{V}$ while maintaining high power transfer efficiency throughout the domain of operation. The versatile architecture of the topology enables reconfiguration through the transformer winding circuitry and auxiliary switches (S_5, S_6, S_7), which can collectively alleviate the voltage and current stress on the semiconductor devices while maintaining full utilization of the transformer core and winding material. This configuration gives rise to three peak efficiency points across the voltage spectrum in contrast to the single peak observed in a conventional DAB [32]. Qazi et al.[33] proposed the unidirectional circuit concept as an *LLC* converter. Although the topology therein is able to improve the efficiency characteristics of the converter, the high conduction loss due to the increased number of conducting diodes in low-voltage modes results in a much lower local peak efficiency. Second, for the same values of load current, the converter exhibits a different tank quality factor (Q) for different voltage modes. Since the voltage regulation in *LLC* converters with conventional pulse frequency modulation or dual phase/frequency control is heavily dependent on the operating Q, the low voltage modes require higher frequency/phase shift values for regulation away from the local peak efficiency point resulting in increased power losses [33]. Consequently, the light load efficiency in lower voltage modes can be lesser than in higher voltage modes. In typical constant current and constant voltage (CCCV) battery charging profiles, light-load efficiency of the power conversion interface is especially important since the beginning of the CC stage (increasing battery voltage at rated current) and the latter part of the CV stage (decreasing injected current at constant voltage) are both characteristics of a light to medium load condition. Therefore, for the DAB, the limited zero voltage switching (ZVS) range and increase in circulating current with conventional single phase shift (SPS) modulation strategies can lead to higher losses [32]. In order to tackle this, a suitable modulation strategy for the PIVODAB is implemented which further enhances the efficiency per the load demand giving rise to flatter efficiency characteristics against voltage and power.

The rest of this article is organized as follows. The converter operation and principle are described in Section II. Section III introduces the modulation strategy employed for the topology. Experimental results are presented in Section IV. Finally, Section V concludes this article.

II. Analysis of the Proposed Topology

Depending on the input bus voltage, the proposed topology can be set up either in a parallel connection [PIVODAB, shown

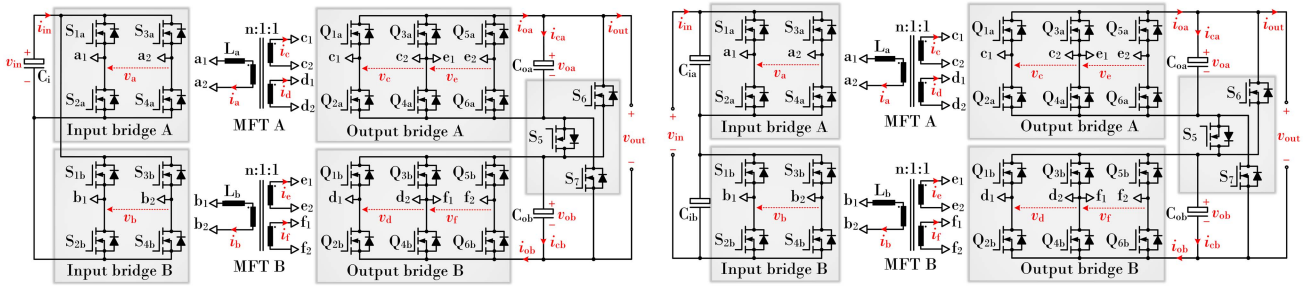

Fig. 2. Possible configurations of the proposed DAB converter topologies. (a) Parallel input versatile output (PIVODAB). (b) Series input and versatile output (SIVODAB).

in Fig. 2(a)] or in series [SIVODAB, shown in Fig. 2(b)] at the input. There is no significant difference between the two besides the current sharing in PIVODAB and the voltage sharing in SIVODAB (which changes the loss mechanisms on the input side). Therefore, this work only focuses on the former in order to analyze the proposed circuit concept. Through subsequent analysis, it will be shown that, though the converter features more than two H-bridges, it is still classified as a DAB topology since it effectively operates as multiple DABs operating in parallel.

A. Topology Schematic

Fed from a constant dc bus as shown in Fig. 2(a), the converter consists of two bridges – A (S_{1a} - S_{4a}) and B (S_{1b} - S_{4b}) connected in parallel while their ac terminals are connected to the primary windings (a_1, a_2 and b_1, b_2) of identical three-winding transformers both of which have a turns ratio $n:1:1$. The terminals of both secondary windings (c_1, c_2 and e_1, e_2) are connected to the three-phase bridge A (Q_{1a} - Q_{6a}) while both the tertiary windings (d_1, d_2 and f_1, f_2) are connected to the three-phase bridge B (Q_{1b} - Q_{6b}). The three-phase bridges employ dc side capacitors (C_{oa} and C_{ob}) and are interconnected via low-frequency auxiliary switches (S_5, S_6, S_7). Collectively, these three-phase bridges feed the positive and negative output rails.

B. Converter Operation

The versatility of the output side is realized by two independent operations. First, by manipulating the state of the backend low-frequency switches (S_5, S_6, S_7), which resemble those in a typical two-winding voltage/current doubler setup. With S_5 turned ON and S_6, S_7 turned OFF, the output bridges A and B are cascaded while with S_5 turned OFF and S_6, S_7 turned ON, the output bridges A and B are paralleled. Second, by varying the relative phase between the input bridges A and B the output bridges can be internally connected in a cascade or parallel configuration. This effect is demonstrated via Figs. 3 and 5, where the DABs are SPS-modulated.

When the input bridges A and B are synchronously modulated [see Figs. 3(a) and 5(a)], only two phases of the secondary side bridges are switched, which are modulated with a phase shift φ relative to the input bridges ($-1 < \varphi < 1$) while the central leg switches Q_{3a}, Q_{4a}, Q_{3b}, Q_{4b} are not switched. This phase shift in the secondary side switches is characteristic of a conventional DAB and governs the magnitude and direction of power transfer. During this operation, the output bridge A consists of an internal series connection through the secondary windings of transformers A and B while the output bridge B consists of an internal series connection through the tertiary windings of transformers A and B . The corresponding central leg switches remain clamped to the secondary and tertiary winding voltages, respectively,

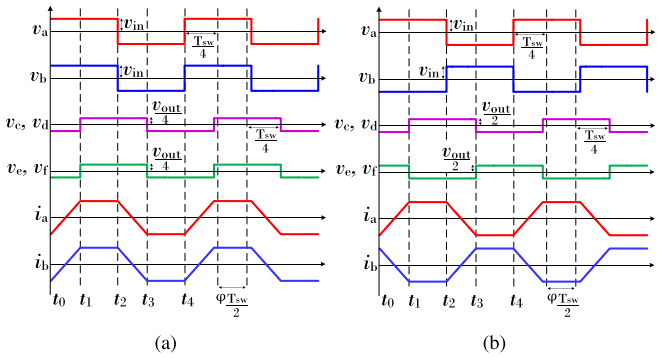

Fig. 3. Idealized operating waveforms with SPS modulation. (a) Synchronous operation [$V_o = 2 \cdot V_{in}$]. (b) Complementary operation [$V_o = V_{in}$].

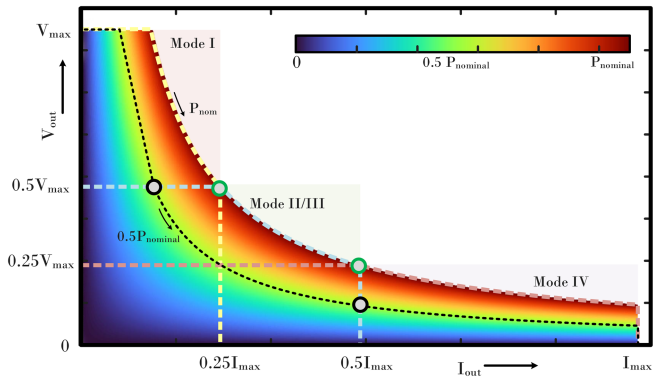

Fig. 4. Operating characteristics for the PIVODAB illustrating extension of *V/I* ranges.

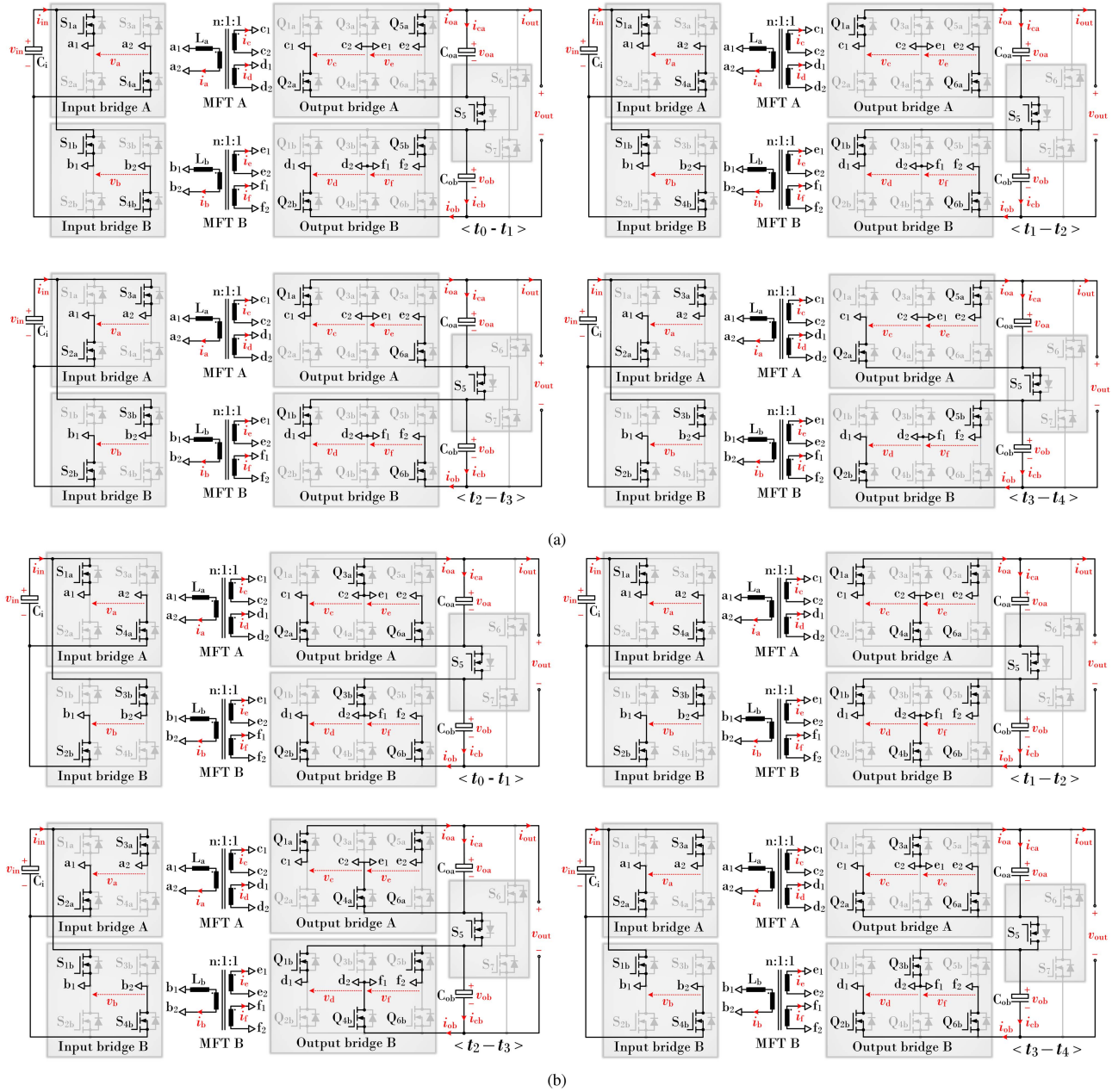

Fig. 5. Switching states of PIVODAB for an ideal switching cycle $[t_0, t_4]$ under SPS modulation (commutation intervals and dead time conduction states not shown). (a) Synchronous operation [mode I]. (b) Complementary operation [mode III]; modes II and IV (not shown) operate similar to modes I and II, respectively, albeit with the state of auxiliary switches reversed.

and therefore block a voltage equal to one-fourth of the output terminal voltage. On the other hand, the noncentral leg devices block the bridge capacitor voltages during their OFF states in each switching cycle which is one-half of the output terminal voltage. Under the complementary operation of input bridges A and B [see Figs. 3(b) and 5(b)], all three phases of the secondary side output bridges are modulated wherein the outer legs are switched simultaneously while the central leg is switched in complement for each half cycle. Again, there is a relative phase shift φ between the input and output side bridges, which governs the power transfer. During this operation, the central leg devices conduct the currents from two secondary-side windings while the noncentral leg devices each carry a single winding current. Therefore, the output bridge A consists of a parallel connection through the secondary windings of transformers A and B while the output bridge B consists of a parallel connection through the tertiary windings of transformers A and B. In both the synchronous and complementary operations, the output bridges A (Q_{1a} - Q_{6a}) and B (Q_{1b} - Q_{6b}) are always modulated identically regardless of the relative phase of input bridges. Furthermore, the state of auxiliary switches S_5, S_6, S_7 can be reversed for either operation to enable external voltage/current doubling through the output bridges. Under SPS modulation, these configurations yield a DAB converter with a varying equivalent turns ratio

TABLE I
PIVODAB OPERATING MODES

Mode	Phase ($\angle Q_{1a} - \angle Q_{1b}$)	Auxiliary Switches	Turns (n_e)
I	0 (synchronous)	$S_5 = 1$, $S_6 = S_7 = 0$	$n/4$
II	0 (synchronous)	$S_5 = 0$, $S_6 = S_7 = 1$	$n/2$
III	0.5 (complementary)	$S_5 = 1$, $S_6 = S_7 = 0$	$n/2$
IV	0.5 (complementary)	$S_5 = 0$, $S_6 = S_7 = 1$	n

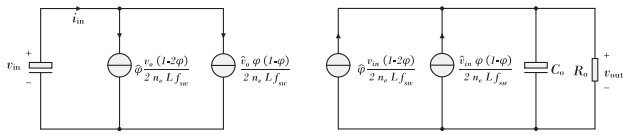

Fig. 6. First order small signal model of the PIVODAB.

obeying the well-known power transfer equation (multiplied with a factor of 2 to account for parallelly operating bridges) given as follows [34]:

$$P_{\mathrm{o}} = \frac{n_{\mathrm{e}} \cdot V_{\mathrm{in}} \cdot V_{\mathrm{o}} \cdot \varphi \cdot (1 - |\varphi|)}{f_{\mathrm{sw}} \cdot L} \quad ; \varphi \in (-1, 1) \tag{1}$$

where the effective turns ratio value, n_e, is given by Table I.

With the assumption of identical networks ($L_{\mathrm{a}} = L_{\mathrm{b}} = L$), the output power P_{o} is maximized at $\varphi = 0.5$ for given values of averaged input voltage (V_{in}), averaged output voltage (V_{o}), and switching frequency (f_{sw}). The reconfiguration summarized in Table I results in the change of the effective number of turns by a factor of up to four while ensuring full utilization of the transformer core and winding copper which in turn enables constant peak power operation at three different output voltage points. Effectively, this process enables connecting the four secondary windings in series (mode I), in parallel (mode IV), and in a series–parallel combination (mode II, III, which offer a redundancy and a voltage stress vs. power loss tradeoff) while keeping the winding currents and voltages invariant and the transformer volt–seconds uniform across all the modes. Furthermore, the power is shared evenly in the input and output bridges A and B in all operating modes by virtue of current and/or voltage sharing, alleviating the individual semiconductor stress. Following further analysis, it is shown that with a suitable modulation technique, the converter exhibits multiple peak efficiency points and offers a relatively flat efficiency characteristic with output voltage and power variations. It is pertinent to mention that the reconfiguration process described herein is static and not dynamic. Therefore, depending on the required output voltage range, the appropriate mode is selected by comparing the voltage value against preset voltage boundaries, prior to the converter start-up and switching which can easily be achieved via the vehicle communication system. The voltage versus current characteristics of the PIVODAB across various modes are shown in Fig. 4 illustrating the adaptability of the topology in operating over wide voltage and current ranges without compromising the system power capability.

The impact of various modes on the plant can be examined with the SPS-based small signal model of the PIVODAB as shown in Fig. 6 [35]. The effect of reconfiguration manifests in the model as the variable turns ratio n_e and the equivalent output capacitance C_o. The effective turns ratio scales the respective transfer functions (e.g., control-to-output, input-to-output) based on the operating mode. The reconfiguration sets up the output capacitors in series for modes I and III [$C_o = 0.5 \cdot C_{oa} = 0.5 \cdot C_{ob}$] and in parallel for modes II and IV [$C_o = 2 \cdot C_{oa} = 2 \cdot C_{ob}$], which alters the output impedance given by $R_o/(1 + sC_oR_o)$ and accordingly the frequency response. The transfer functions listed below highlight, where these reconfigurations affect the plant.

1) Phase-shift-to-input-current transfer function

$$G_{i_{\mathrm{in}}\varphi} = \frac{v_{\mathrm{out}}\,(1 - 2\varphi)}{2n_e f_{\mathrm{sw}} L}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

2) Output-voltage-to-input-current transfer function

$$G_{i_{\mathrm{in}}v_{\mathrm{out}}} = \frac{\varphi\,(1 - \varphi)}{2n_e f_{\mathrm{sw}} L}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

3) Phase-shift-to-output-current transfer function

$$G_{i_{\mathrm{out}}\varphi} = \frac{v_{\mathrm{in}}\,(1 - 2\varphi)}{2n_e f_{\mathrm{sw}} L}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

4) Input-voltage-to-output-current transfer function

$$G_{i_{\mathrm{out}}v_{\mathrm{in}}} = \frac{\varphi\,(1 - \varphi)}{2n_e f_{\mathrm{sw}} L}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

5) Input-voltage-to-output-voltage transfer function

$$G_{v_{\mathrm{out}}v_{\mathrm{in}}} = \frac{\varphi\,(1 - \varphi)}{2n_e f_{\mathrm{sw}} L} \cdot \frac{R_o}{1 + sC_oR_o}$$

$$C_o \in \{0.5C_{oa}, 2C_{oa}\}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

6) Phase-shift-to-output-voltage transfer function

$$G_{i_{\mathrm{out}}\varphi} = \frac{v_{\mathrm{in}}\,(1 - 2\varphi)}{2n_e f_{\mathrm{sw}} L} \cdot \frac{R_o}{1 + sC_oR_o}$$

$$C_o \in \{0.5C_{oa}, 2C_{oa}\}, \quad n_e \in \left\{n, \frac{n}{2}, \frac{n}{4}\right\}.$$

It can be noted from Fig. 6 that since the output voltage scales linearly with the effective turns, the input current remains invariant across modes. This is consistent with Figs. 3 and 5, wherein the magnitude of the total current injected by the dc source does not alter even though the two full bridges differ in phase in the two modes. When operated with other modulation strategies, the variation due to the changes in n_e and C_o remain consistent. With these modifications, the converter model can be assumed to behave like a conventional lossless DAB model in each mode and accordingly, the digital controller can adopt the appropriate voltage and current control scheme in coordination with the battery management system.

III. CONVERTER MODULATION

In recent years, several methods have been used to modulate the DAB topology and its variants [36]. In order to enhance efficiency, variation of switching frequency along with the equivalent duty cycles on the primary and/or secondary sides of the transformer is commonly resorted to by employing closed-form

equations or other optimization techniques such as the use of Lagrange multipliers, Karush–Kuhn–Tucker conditions, artificial intelligence, genetic algorithms, etc. [37], [38], [39], [40]. These methods are generally aimed at the reduction of current stresses and the extension of ZVS range which in turn reduce the conduction and switching losses, respectively, thereby improving the system efficiency. These mechanisms yield combinations of the enhanced phase shift (EPS), dual phase shift (DPS), and triple phase shift (TPS) modulation schemes with the latter being the most general case, where both the H-bridges are modulated to yield quasi-square waves on their respective ac terminals, allowing ZVS behavior optimization, and mitigation of circulating current [32]. Based on the duty cycle constraints, the TPS operation can be divided into 12 operating regions with varying power transfer ranges, ZVS characteristics, RMS currents, power flow direction, etc. [38]. With the increase in load demand, the duty cycle of the H-bridges is monotonically increased pushing the converter into EPS and ultimately SPS where maximum power is transferred when the two bridges operate in quadrature. The PIVODAB retains some of these well-documented features of the traditional DAB topology and they can be used to contrive a suitable modulation strategy for the proposed converter.

A. TPS in the PIVODAB

When the conventional DAB is modulated with TPS, for a nonzero time interval during every switching cycle, both the high-side switches or both the low-side switches are turned ON to yield a null voltage across the secondary ac terminals. In the PIVODAB, this effect can be replicated by a mode-dependent switching action that results in a zero voltage across both pairs of secondary and tertiary windings simultaneously. Under synchronous operation, this is achieved by the switching sequence shown in Fig. 7(a) for mode I. The modulation effectively results in a circulating current in serially connected secondary windings $c_1 - c_2$ and $e_1 - e_2$ via the high-side and low-side switches of output bridge A during intervals $t_2 - t_3$ and $t_5 - t_6$, respectively. Since the switching in the output bridges is identical, tertiary windings $d_1 - d_2$ and $f_1 - f_2$ exhibit similar behavior in the output bridge B. In complementary operation, TPS is carried out through the switching sequence shown in Fig. 7(b) for mode III. During intervals $t_2 - t_3$ and $t_5 - t_6$, a null voltage is set up across each winding via high-side and low-side devices, respectively. Furthermore, during TPS operation, both the input bridges exhibit the conventional DAB behavior under synchronous and complementary operation. The TPS operation is characterized by the equivalent duty cycles D_1 (for v_a and v_b), D_2 (for v_c, v_d, v_e and v_f) per each half cycle (T_H) of the switching period. The phase-shift between the turn ON of the corresponding primary and secondary switches is denoted by D_3 while φ represents the phase-difference between the central axis of the quasi-square waves on the primary and secondary bridges and is equal to D_3+0.5($D_2 - D_1$).

B. Optimizing the Modulation

Depending on the output voltage and power requirements, there may be infinite combinations of D_1, D_2, and D_3 that yield the required specifications for a given design (L, f_{sw}, V_{in}, n). These control variables alter the switching ON/OFF intervals of the semiconductor devices and their choice ultimately determines power flow, switching, and conduction losses in the system. Closed-form equations in literature aim to optimize the system efficiency at a designated operating point while also enabling direct online transitions in case of changes in required voltage or power [36]. In [32], the control variables are determined by the minimum switched current required for ZVS, which necessitates fulfilment of two conditions, that is, sufficient inductive energy to discharge the semiconductor capacitances and an optimum dead time for the energy exchange to take place while ensuring the correct current polarity at the time of switching to prevent hard turn-ON. The evaluation of the required inductive energy has in itself been subject to wide research as both charge-equivalent and energy-equivalent models are usually based on approximations [41], [42]. Accordingly, the charge equivalent capacitance ($C_{Q,eq}$) given by (2)–(3) is used in this work

$$C_{Q,eq}(V_{DS}) = \frac{Q_{oss}(V_{DS})}{V_{DS}} = \frac{1}{V_{DS}} \int_0^{V_{DS}} C_{oss}(v)\, dv \tag{2}$$

$$\frac{1}{2} L I_{sw}^2 \geq \left(\frac{k}{2} C_{Q,eq}(V_{DS}) + C_{par} \right) \cdot V_{blk}^2 \tag{3}$$

wherein V_{blk} is the voltage across C_i, C_{oa} or C_{ob} depending on the switching device, V_{DS} is the drain to source switch voltage, C_{oss} is curve-fitted with V_{DS} from the datasheet, I_{sw} is the inductor current at the switching instant and C_{par} comprises the parasitic capacitance of windings, PCB, etc. The first term of the right-hand side of (3) is scaled accordingly with the number of switching devices (k). This is particularly relevant to the PIVODAB as the number of switching devices on the secondary

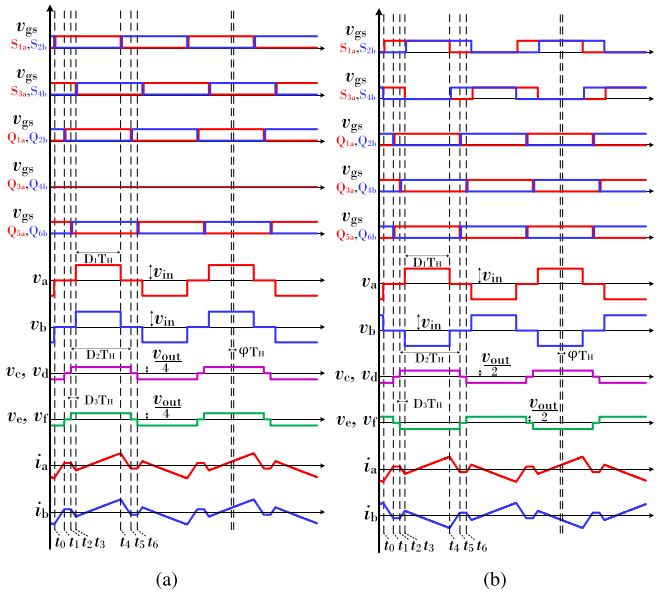

Fig. 7. Operational waveforms for TPS-modulated PIVODAB. (a) Synchronous operation [mode I; $V_o = 1.6 \cdot V_{in}$]. (b) Complementary operation [mode III; $V_o = 0.8 \cdot V_{in}$].

TABLE II
EQUIVALENT DUTY CYCLE VARIATION WITH LOAD

Modulation	Parameters
TPS	$D_1 = \frac{2M\Phi + I_\mathrm{p}}{1-M}, D_2 = \frac{D_1 + I_\mathrm{s}}{M}, D_3 = \frac{-(I_\mathrm{p} + I_\mathrm{s})}{2M}$ $P_\mathrm{o} = \frac{-M(D_1^2 - D_1D_2 - 2D_1D_3)V_\mathrm{in}^2}{2f_sL}$ $P_{\mathrm{o,\,max,T}}$ at $D_2 = 1$; go to EPS A
EPS A	$D_1 = M - I_\mathrm{s}, D_2 = 1, D_3 = \Phi - \frac{(1 - M + I_\mathrm{s})}{2}$ $P_o = \frac{-M(D_1^2 - D_1 - 2D_1D_3)V_\mathrm{in}^2}{2f_sL}$ $P_{\mathrm{o,\,max,A}}$ at $D_3 = 0$; go to EPS B
EPS B	$D_1 = 2D_3 + M - I_\mathrm{s}, D_2 = 1, \Phi = \frac{1 - M + I_\mathrm{s}}{2}$ $\zeta = \frac{I_\mathrm{s}(M+1) - M^2 + \sqrt{I_\mathrm{s}^2 + M^2(I_\mathrm{s} - M)^2}}{2M}$ $P_o = \frac{M(-D_1^2 - 2D_3^2 + D_1 + 2D_1D_3)V_\mathrm{in}^2}{2f_sL}$ $P_{\mathrm{o,\,max,B}}$ at $D_3 = \zeta$; go to EPS C
EPS C	$D_1 = \frac{M + 2\Phi - 1 + \gamma}{M}, D_2 = 1$ $D_3 = \frac{\Phi(2+2M) - 1 + \gamma}{2M}$ $\gamma = \sqrt{(2\Phi - 1 + M)^2 + M^2(2\Phi - 1)^2}$ $P_\mathrm{o} = \frac{M(-D_1^2 - 2D_3^2 + D_1 + 2D_1D_3)V_\mathrm{in}^2}{2f_sL}$ $P_{\mathrm{o,\,max,C}}$ at $D_1 = 1$; go to SPS
SPS	$D_1 = 1, D_2 = 1, D_3 = \Phi, P_\mathrm{o} = \frac{M(D_3 - D_3^2)V_\mathrm{in}^2}{2f_sL}$ $P_{\mathrm{o,\,max}}$ at $D_3 = 0.5$

side is different in synchronous and complementary modes and therefore it modifies the ZVS current requirement. Furthermore, in this work, the central leg devices are assembled using two hard paralleled devices of the same technology as the noncentral legs. Adopting such a design leads to a more symmetric switching behavior and more uniform thermal dissipation in the converter. Therefore, for the same phase shifts, the number of devices switching on the secondary side under complementary operation is twice that of the synchronous operation. In addition, the charge-equivalent capacitance will be higher for complementary operation compared to the synchronous operation for the same output power as it corresponds to a lower voltage output. However, since each device blocks only half the voltage, the net effect is that the total energy needed in complementary operation is less than the requirement for synchronous operation (at the same power output). Since mode switching is anyway static and not dynamic, this detail can be incorporated into the modulation algorithm. Alternatively, a universal setpoint can be employed based on the synchronous operation as it will ensure ZVS across all modes. As detailed in [32] and [38], the converter modulation is divided into five regions depending on the load demand, which determines the required values of D_1, D_2, and D_3. Table II summarizes the equations that yield the required duty cycle values for grid-to-vehicle (G2V) mode. Therein, M is the ratio of ac voltage amplitudes given by $M = n_eV_o/V_\mathrm{in}$,

TABLE III
SYSTEM PARAMETERS

Parameter	Value
Input voltage, V_in	750 V
Output voltage, V_out	150–1500 V
Maximum output power, $P_{\mathrm{out,max}}$	11 kW
Switching frequency, f_sw	48 kHz
Turns ratio, n	28/14/14
Series inductance (incl. L_lkg), L_a = L_b	255 μH
Output capacitance, C_oa = C_ob	20 μF

where n_e is obtained from Table I and the normalized (I_1 and I_2) and actual ZVS currents (I_p and I_s) are given as follows:

$$
\begin{aligned}
I_1 &= -\min\left(\frac{-Q_\mathrm{p}V_\mathrm{in}}{T_\mathrm{d}} - \frac{(V_\mathrm{in} + n_\mathrm{e}V_\mathrm{o})T_\mathrm{d}}{2L}, -\frac{(V_\mathrm{in} + n_\mathrm{e}V_\mathrm{o})T_\mathrm{d}}{L}\right)\\
I_\mathrm{p} &= I_1 \cdot \left(\frac{4f_\mathrm{sw}L}{V_\mathrm{in}}\right)\\
I_2 &= \max\left(\frac{Q_\mathrm{s}V_\mathrm{in}}{T_\mathrm{d}} + \frac{n_\mathrm{e}V_\mathrm{o}T_\mathrm{d}}{2L}, \frac{n_\mathrm{e}V_\mathrm{o}T_\mathrm{d}}{L}\right)\\
I_\mathrm{s} &= I_2 \cdot \left(\frac{4f_\mathrm{sw}L}{V_\mathrm{in}}\right)
\end{aligned}
\tag{4}
$$

where T_d is the deadtime while Q_p and Q_s denote the total stored charge in C_par and $C_\mathrm{Q,eq}$ for the input and output side switching MOSFETs, respectively. Under light load conditions, the algorithm exhibits an all-ZVS-based TPS modulation. With the increase in load, φ increases as well until D_2 clamps at 1 and the converter transitions to EPS A wherein only half of the primary side switches exhibit ZVS. The subsequent increase in φ leads to EPS B when D_3 becomes 0. Further increase in power comes at constant φ with increasing D_3 until it reaches its maximum value given by ζ, where the transition to an optimal current-based algorithm, EPS C, is made. Herein, as φ and D_1 are increased with load, D_1 is ultimately clamped to 1, pushing the converter into SPS. It is pertinent to mention that Table II governs a buck-type operation for the equivalent DAB model. For the design employed in this work (input/output voltages, transformer turns ratio, and mode boundaries), the algorithm suffices for G2V operation. However, for V2G or a different design, the process can be extended for boost operation using the presented analysis and other reported work [32], [38]. Corresponding to the system parameters in Table III, the variation of D_1, D_2, and D_3 with the increase in load is shown in Fig. 8 for different values of M which exhibit similar behaviour across all operating voltage modes. Furthermore, the variation in bridge voltages and primary currents for synchronous and complementary operation is illustrated through Figs. 9 and 10, respectively.

IV. RESULTS AND ANALYSIS

The operation of the PIVODAB is verified via an 11 kW SiC-based prototype shown in Fig. 11, which is consistent with the Table III parameters. The converter design is summarized in

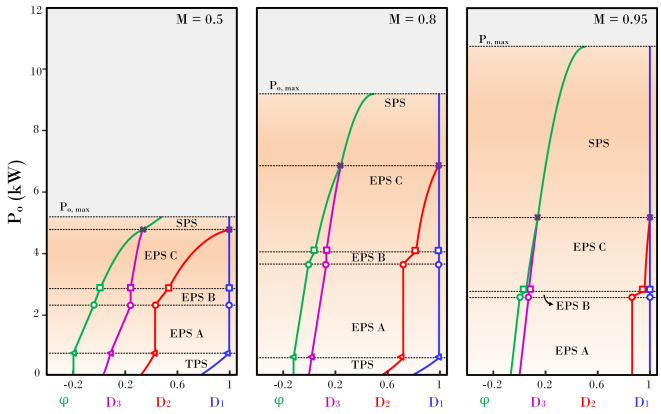

Fig. 8. Variation of duty cycles with increase in load for different values of M illustrating the monotonic characteristics.

TABLE IV
EXPERIMENTAL PROTOTYPE SUMMARY

Component	Design Selection
H-bridge MOSFETS	TO-247-3 G2 SiC
$S_1 - S_4$, $Q_1 - Q_6$	Wolfspeed C2M0080120D (2·12x)
Auxiliary switches	Monostable power relay
S_5 , S_6 , S_7	TE Connectivity T9GV5L14-5 (3x)
Output capacitors	Metallized polypropylene film
C_{oa} , C_{ob}	EPCOS/TDK B32774D8505K000 (2·4x)
DC blocking capacitors	Metallized polypropylene film
C_{dca}, C_{dcb}	EPCOS/TDK B32621A0682J000 (2·225x)
Series inductors	EE 64/10/50 [2 stacks], 480-str. AWG-41 Litz
L_a , L_b	Ferroxcube ferrite 3C95 (2·x)
Three-winding MFTs	EE 65/32/27 [2 stacks], 480-str. AWG-41 Litz
T_A , T_B	P-S-P-T intraleaved structure
	EPCOS/TDK ferrite N87 (2·x)
Control units	Texas Instruments F28379D LaunchXL (2·x)
Gate drive ICs	Broadcom ACPL-344JT (2·12x)
Relay switch	Fairchild MMBF170 (3x)
Voltage sensors	LEM DVC 1000-P (3·x)
Cooling fans	CUI Devices CFM-4020CF-095-342 (2·3x)
Thermal sinks	Ohmite C40-058-AE (2·6x)

Table IV. Since the converter transformers employ multiple secondary windings, an interleaved winding structure is employed for uniform current sharing between the secondary and tertiary windings [43]. Furthermore, bidirectional power supplies from ITECH (IT6018C-1500-40) are employed at the input and the output of the converter, which facilitates G2V and V2G operation. The voltage and current signals are measured using TA043 differential-type voltage probes from Pico Technology and N2783B current probes from Keysight, respectively. The converter efficiency is measured using Yokogawa WT500 while Keysight DSOX3024A is used for capturing real-time waveforms. The control is executed through two Texas Instruments LAUNCHXL-F28379D kits, which are optically synchronized.

The interleaved structure on the primary side and the versatile structure on the secondary side enables the use of low-voltage and current devices on either end. Specifically, for the PIVODAB design in the manuscript, the primary side devices are required to block the full dc voltage of the 750 V bus that is used at the input. Assuming a 20% safety margin, devices from the 900 V rating class can be used at the input. Though the output voltage range extends upto 1500 V, the cascaded configuration in mode I ensures a maximum voltage of 750 V across the output capacitors. Therefore, with a 20% safety margin, the same 900 V rating class can be used for the noncentral legs of the secondary side as well. The central leg devices are clamped to half the voltage of the output bus and therefore an even lower voltage class can be used. In the experimental prototype presented in the article, the already available Wolfspeed C2M0080120D devices have been used to expedite the testing process in the lab.

A. Steady-State Operation

In order to validate the performance of the proposed converter, the operation of the experimental prototype is demonstrated under varying output conditions of voltage and power. The steady-state operation of the PIVODAB at rated power is illustrated in Figs. 12 and 13 under mode I synchronous operation and mode IV complementary operation, respectively. Therein the primary side voltages and currents exhibit the in-phase behavior for synchronous operation (1500 V at 11 kW) and antiphase behavior for complementary operation (375 V at 11 kW). On the other hand, the secondary and tertiary currents for both bridges remain identical regardless of the operating mode. These characteristics are also consistent with modes II and III, where only the state of auxiliary switches changes with respect to modes I and IV, respectively. The V2G operation is demonstrated in Fig. 14(a) at a 1200 V output. Under this condition, the system is characterized by a negative phase shift angle i.e, $\varphi < 0$, indicating an averaged back power flow in accordance with (1).

Due to the inherent nature of both reconfigurations, an online smooth transition across any of the modes is not possible. The appropriate mode is chosen based on the maximum battery voltage by comparing it with the preset voltage boundary before the converter start-up and switching. This can be easily realized with the vehicle-to-charger communication link already present in the charging framework. Alternatively, a mid-cycle mode reset can be employed to maximize efficiency at the cost of a minuscule charging time. Consequently, mode switching during an operation is not illustrated. However, the effect of load change for the proposed converter is shown in Fig. 14(b). Typically, the increase/decrease of the charging current is governed by the slow battery-charging cycle. However, since the experiment is carried out using dc power supplies, a generic ramp current reference of $0.2\,\mathrm{A/sec}$ is employed. Further validation of the converter modulation is illustrated through Fig. 15(a)–(f), wherein the effect of an increase in load demand is examined. With the converter operating in mode II at 600 V, the system obeys the control law illustrated in Fig. 8 for $M = 0.8$. Under a very light load, the converter is modulated with the triple phase shift modulation [see Fig. 15(a)]. As the load is increased, the converter transitions to the various EPS modulation schemes [see Fig. 15(b)–(d)]. After D_1 is clamped to 1, the converter operates under SPS modulation

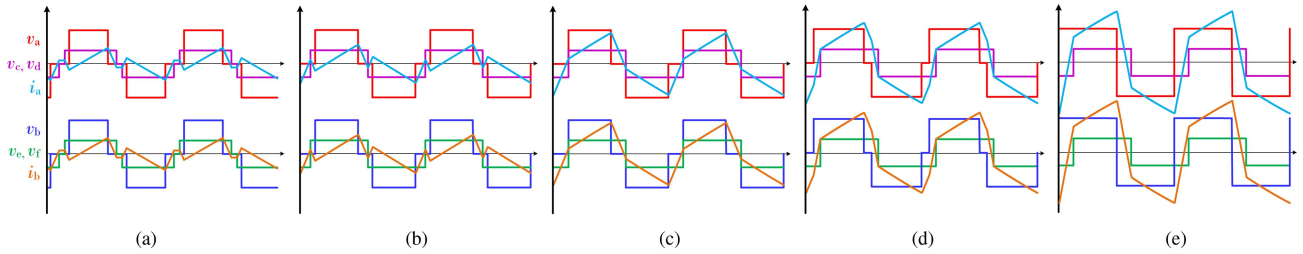

Fig. 9. Synchronous operation inductor currents and bridge voltages with an increase in load demand [$V_{out} = 1200$, mode I]. (a) 0.0708 p.u. with TPS. (b) 0.1024 p·u· with EPS A (c) 0.2935 p·u· with EPS B (d) 0.4497 p·u· with EPS C (e) 0.5879 p·u· with SPS.

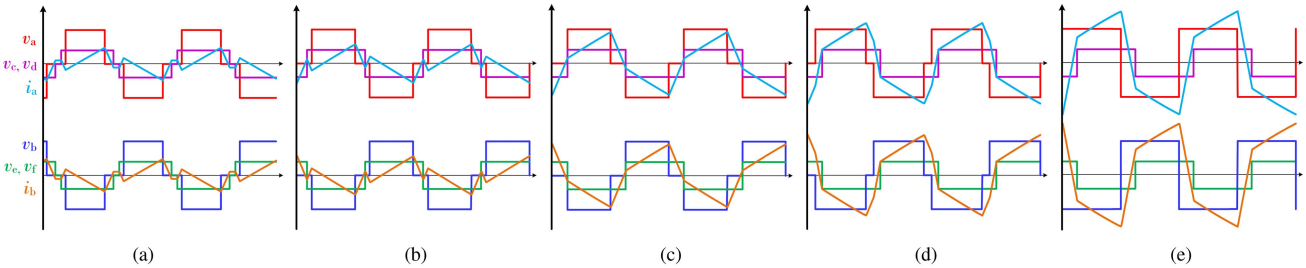

Fig. 10. Complementary operation inductor currents and bridge voltages with an increase in load demand [$V_{out} = 300$, mode IV]. (a) 0.0708 p.u. with TPS. (b) 0.1024 p·u· with EPS A. (c) 0.2935 p·u· with EPS B. (d) 0.4497 p·u· with EPS C. (e) 0.5879 p·u· with SPS.

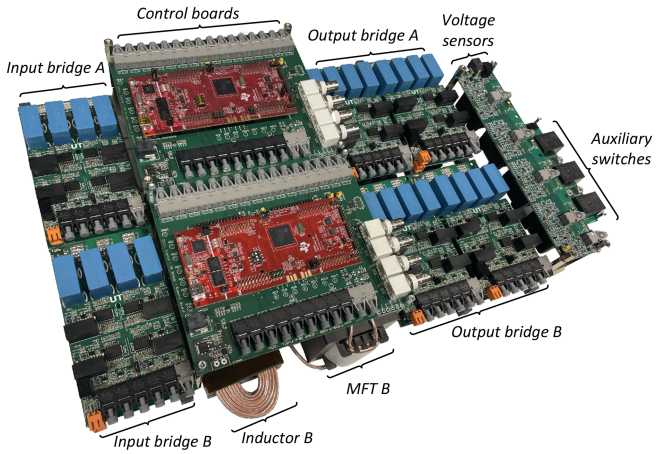

Fig. 11. Experimental prototype of SiC-based PIVODAB rated at 11 kW/ 750 V/1500 V.

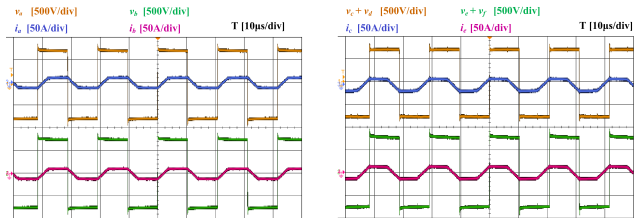

Fig. 12. Primary and secondary side waveforms under synchronous operation [mode I, $V_o = 1500$ V, SPS with $D_3 = 0.4$].

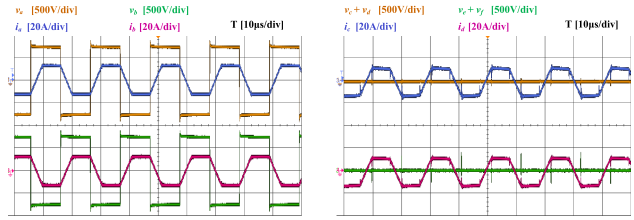

Fig. 13. Primary and secondary side waveforms under complementary operation [mode IV, $V_o = 375$ V, SPS with $D_3 = 0.4$].

[see Fig. 15(e)], beyond which the power flow is increased by the control of a single variable [$\varphi = 0.4$ in Fig. 15(f)]. While the proposed converter operates over a significantly broader range compared to other contemporary converters, it utilizes a relatively higher number of semiconductor devices, exhibits poorer output-side device utilization and uses two transformers. However, the inherent topology construction ensures three peak efficiency points, higher margin in winding isolation, voltage sharing at the output terminals, and current sharing at the input terminals, resulting in reduced peak voltage stress on the output capacitors and devices, as well as lower current stress on the input-side MOSFETs. Along with the voltage range, several other key aspects from recent research, such as the number of switching devices, efficiency, and normalized voltage stresses are compared and summarized in Table V.

B. Losses and Efficiency

A power loss breakdown and efficiency analysis of the converter is carried out to assess its performance in wide voltage and power ranges. The calculation of power losses is carried

TABLE V
COMPARATIVE ANALYSIS OF BIDIRECTIONAL WIDE OUTPUT VOLTAGE DC/DC CONVERTERS

	Reconfigurable DAB [27]	Variable Freq. DAB [37]	Three-level CLLC [44]	FB/HB CLLC [45]	Three-Phase Asymmetrical DAB [31]	This work
Control	TPS and modes	TPS with variable f_{sw}	PFM and modes	PFM, FB/HB variable V_{in}	PSM and modes	TPS and modes
Output Voltage Range	$200-1000$V	$250-950$V	$200-700$V	$200-800$V	$150-900$V	$150-1500$V
Switching Frequency	100kHz	$25-50$kHz	$31-70$kHz	$140-250$kHz	100kHz	48kHz
Required Semiconductor Devices	12	8	24	8	24	20
Auxiliary Switches	3	–	–	–	–	3
Transformers	1	1	1	2	3	2
Highest Efficiency	98.4 %	98.8 %	96.8 %	98.5%	97%	98.6%
Peak Efficiency Points	2	1	3	2	2	3
Maximum Power	10kW	11kW	3 5kW	22kW	3kW	11kW
Normalized Voltage Stress (Output)	0.5 p.u.	1 p.u.	0.5 p.u.	1 p.u.	0.33 p.u.	0.5 p.u.
Normalized Voltage Stress (Input)	1 p.u.	1 p.u.	0.5 p.u.	1 p.u.	1 p.u.	1 p.u.

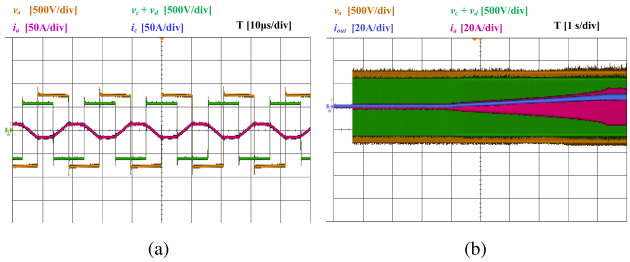

Fig. 14. Operating waveforms (a) Steady-state V2G operation [mode I, $V_o = 1200\,V$, SPS with $D_3 = -0.5$]. (b) Converter operation for a ramp-up current load at 1200 V output.

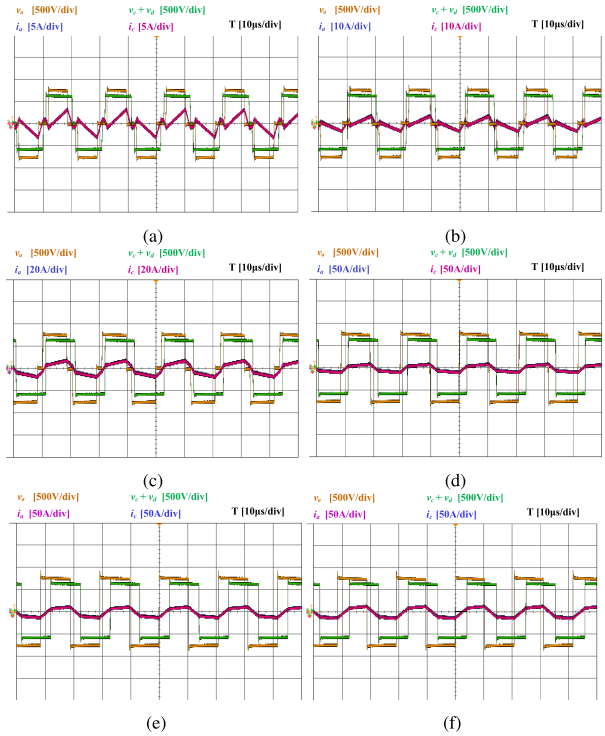

Fig. 15. Effect of increase in load demand on phase shift variation [mode II; $V_o = 600$ V]. (a) 0.8 kW (b) 1.25 kW (c) 5.35 kW (d) 6.7 kW (e) 8.3 kW (f) 8.8 kW.

out using PLECS thermal models (for the conduction and switching losses of SiC MOSFETs), improved generalized Steinmetz equation (for calculation of magnetic core losses), Dowell's equations (for calculation of winding losses) and other resistive losses (for dc blocking capacitor ESRs, dc bus capacitor ESRs, relays, etc.) [46], [47]. The losses in the other additional circuitry (such as driving and control, sensing, and cooling) are neglected and the experimentally measured efficiency matches well with the calculated values. The impact of reconfiguration and the implemented modulation strategy (IMS) on the PIVODAB efficiency is demonstrated via Fig. 16. The IMS is compared with the SPS modulation for various operating voltages across the power range, clearly revealing the efficiency enhancement in Fig. 16(a)–(c). Furthermore, the reconfiguration enables rated power transfer for the designed prototype at lower output voltages while also giving rise to flatter efficiency characteristics with power and voltage. The rated power efficiencies at 1500 V, 750 V and 375 V are 97.38%, 97.36% and 96.62%, respectively, while the peak efficiencies exceed 98% for all operating modes. The variation is expected as the number of conducting devices on the secondary side (auxiliary switches or MOSFETs) varies from mode to mode. This discrepancy can be reduced by using devices with lower $R_{DS,ON}$, if desired. A breakdown of losses for these operating points is shown in Fig. 17.

To further illustrate the effectiveness of the proposed solution, additional efficiency characteristics are plotted in Fig. 18, wherein the improved system corresponds to a solution comprising of reconfiguration capability and two peak efficiencies such as in [27]. The performance is compared for a 7.5 A

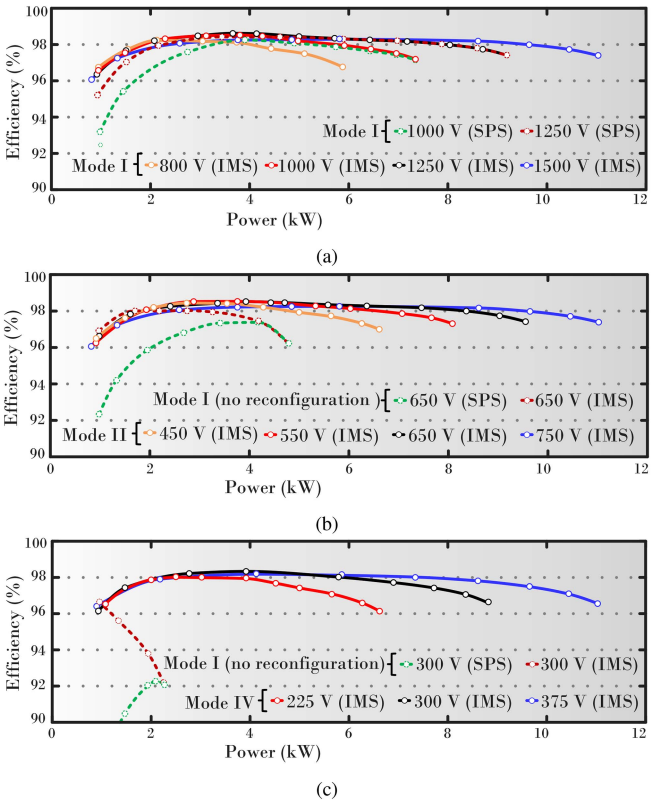

Fig. 16. Efficiency characteristics with varying P_{out} for different operation voltages illustrating the efficiency improvement with reconfiguration and modulation. (a) 750 V $< V_{\text{out}} \leq$ 1500 V (b) 375 V V $< V_{\text{out}} \leq$ 750 V. (c) 150 V $< V_{\text{out}} \leq$ 375 V.

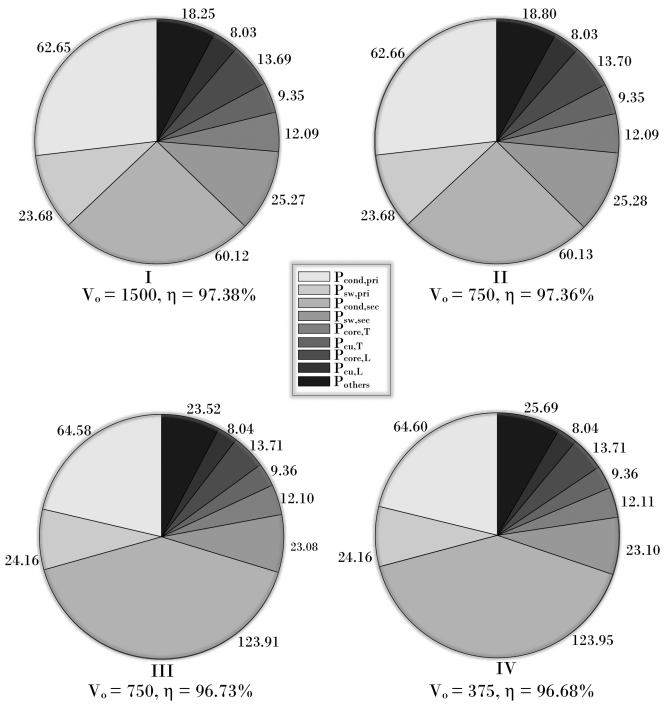

Fig. 17. Distribution of power losses (watts) and efficiencies at nominal load (11 kW) for various operating modes.

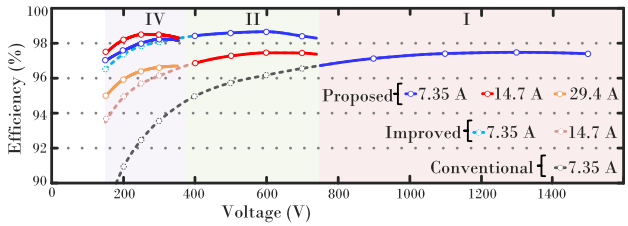

Fig. 18. Efficiency characteristics for various values of output current, I_o, over the full output voltage range.

across all three voltage ranges. The improved system corresponds to a solution comprising of single reconfiguration capability and two peak efficiencies such as in [27]. An additional comparison for a 15 A current is made against the improved system. Without any reconfiguration, the system efficiencies (greyed dotted line) decrease to much smaller values for lower voltages.

V. Conclusion

In this research, a novel parallel input and reconfigurable output-based DAB converter is proposed. The circuit concept developed is aimed at use in general-purpose charging applications where a range of wide output voltages is often required. The topology allows the usage of relatively lower voltage devices (e.g., 900 V class) at the input and the output for 1500 V charging systems while simultaneously maintaining the flexibility of low-voltage/high-current and high-voltage/low-current output without compromising the peak power capability of the output. Operating modes of the converter are identified allowing the circuitry to function as multiple DAB converters operating in parallel. Furthermore, a modulation scheme is implemented that ensures optimum duty-cycle and phase-shift calculations to reduce the power losses in the system. Consequently, over extremely wide voltage and power ranges, a flatter efficiency behavior is achieved compared to a nonreconfigurable system and/or without using the implemented modulation scheme. Such a characteristic is very beneficial for CCCV battery charging profiles, where light-load efficiency of the power conversion interface is vital due to light to medium load conditions during both the initial CC stage and the later CV stage. In order to validate the converter performance, a SiC-based 11 kW experimental prototype is tested under various operating conditions and both directions of power flow. Efficiencies exceeding 96% are obtained nearly throughout the voltage range as the power is varied from 0.1−1 p·u· with peak efficiencies exceeding 98% for all operating modes. Finally, through device thermal modeling and analytical computations, semiconductor and passive device power losses are computed which aids in identifying possible improvements in achieving an even better efficiency profile.

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Sohaib Qazi (Graduate Student Member, IEEE) received the bachelor's degree in electrical engineering and the master's degree in electrical power and energy systems from the National Institute of Technology Srinagar, Jammu and Kashmir, India, in 2018 and 2021, respectively. Since 2021, he has been working toward the Ph.D. under the Marie Skłodowska-Curie Actions ETUT project for a joint doctoral degree with Power Electronics Group, University of Twente, Enschede, The Netherlands, and with the Power Electronics, Machines and Control Research Institute, University of Nottingham, Nottingham, U.K.

Prasanth Venugopal (Senior Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from Amrita Vishwa Vidyapeetham University (silver medal), Coimbatore, India, in 2010, the M.Sc. degree (cum laude) in electrical engineering, and the Ph.D. degree in magnetic energy transfer inroads from the Delft University of Technology, Delft, The Netherlands, in 2012 and 2016, respectively.

From 2016 to 2018, he was with the Qualcomm Halo, Munich, Germany, as a Senior Electrical Engineer in the field of power electronic systems and applications. In 2019, he joined TDK Europe Gmbh, Munich, Germany, as a Technical Specialist for xEV applications. Since 2020, he has been an Assistant Professor with the Power Electronics Group, University of Twente, Enschede, The Netherlands. His research interests include battery electronics, artificial intelligence in predictive maintenance and condition monitoring of power electronics systems and wireless power transfer.

Dr. Venugopal has previously served as an Associate Editor for IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION.

Alan J. Watson (Senior Member, IEEE) received the M.Eng. (Hons.) degree in electronic engineering and the Ph.D. degree in power electronics from the University of Nottingham, Nottingham, U.K., in 2004 and 2008, respectively.

In 2009, he joined the Power Electronics, Machines and Control Research Group, University of Nottingham, as a Research Fellow. Since 2009, he has been involved in various projects in high-power electronics including resonant converters, high-voltage power supplies, and multilevel converters for grid-connected applications such as HVDC and flexible ac transmission systems. In 2012, he was promoted to a Senior Research Fellow before becoming an Assistant Professor of high-power electronics, in 2013. Since 2022, he has been an Associate Professor of high-power electronics. His current research interests include the development and control of advanced high-power conversion topologies for industrial applications, grid-connected converters, and HVDC transmission.

Patrick Wheeler (Fellow, IEEE) received the B.Eng. (Hons.) degree in electrical engineering from the University of Bristol, U.K., in 1990, and the Ph.D. degree in electrical engineering for his work on matrix converters from the University of Bristol, Bristol, U.K., in 1994.

In 1993, he moved to the University of Nottingham and worked as a Research Assistant with the Department of Electrical and Electronic Engineering. In 1996, he became a Lecturer with the Power Electronics, Machines and Control Research Group, University of Nottingham, Nottingham, U.K. Since January 2008, he has been a Full Professor with the same research group. He is currently the Global Engagement Director for the Faculty of Engineering, the Head of the Power Electronics, Machines and Control Research Institute, and the Director of the University of Nottingham's Institute of Aerospace Technology. He was the Head of the Department of Electrical and Electronic Engineering, University of Nottingham from 2015 to 2018. He has authored or co-authored more than 1000 academic publications in leading international conferences and journals.

Dr. Wheeler is a member of the IEEE PELS AdCom and is currently IEEE PELS Vice-President for Technical Operations.

Thiago Batista Soeiro (Senior Member, IEEE) received the B.S. (Hons.) and M.S. degrees from the Federal University of Santa Catarina, Florianopolis, Brazil, in 2004 and 2007, respectively, and the Ph.D. degree from the Swiss Federal Institute of Technology, Zurich, Switzerland, in 2012, all in electrical engineering.

He was a Visiting Scholar with the Power Electronics and Energy Research Group, Concordia University, Montreal, QC, Canada, and with the Center for Power Electronics Systems, Blacksburg, VA, USA, respectively. From 2012 to 2013, he was a Researcher with the Power Electronics Institute, Federal University of Santa Catarina. From 2013 to 2018, he was a Senior Scientist with the Corporate Research Center, ABB Switzerland Ltd., Baden-Dattwil, Switzerland. From 2018 to 2022, he was an Associate Professor with the DC Systems, Energy Conversion and Storage Group, Delft University of Technology, Delft, The Netherlands. From January to October 2022, he was with the Power Management and Distribution Section (TEC-EPM) for the European Space Research and Technology Centre, Noordwijk, The Netherlands. Since October 2022, he has been a Full Professor in power electronics with the Power Electronics Group, University of Twente, Enschede, The Netherlands. His research interests include advanced high-power converters and dc system integration.

Dr. Soeiro is a recipient of the 2013 IEEE Industrial Electronics Society Best Conference Paper Award and the Best Paper Awards in the following IEEE conferences: International Conference on Power Electronics (ECCE Asia 2011), the International Conference on Industrial Technology (ICIT 2013), the Conference on Power Electronics and Applications EPE'15 (ECCE Europe 2015), and the International Conference on Power Electronics and Motion Control 2020 and 2022 (PEMC 2020 and 2022).