A Novel Simplified Time Domain Analysis-Based Synchronous Rectification Strategy for *LLC* Converter Featuring Real-Time Full-Range Operation

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***Abstract*—Model-based synchronous rectification (SR) approach for LLC converters offers significant advantages, such as low cost, high scalability, and elimination of additional losses, as no high-frequency signal sampling is required. However, the performance of model-based SR approach heavily depends on the accuracy of the underlying model. Moreover, given that the LLC converters operate in various modes, each necessitating a different model, it is crucial to identify the operating mode to apply the appropriate model. An inaccurate model or failure to recognize the operation mode may lead to degraded SR performance and even risk of system instability. In this article, a novel model-based SR strategy via simplified time domain analysis is proposed, which is integrated with both SR timing online algorithm and operation mode online recognition algorithm. Unlike the existing model-based SR strategies, all the results are calculated online in the proposed SR strategy without relying on fitting curves, and the proposed SR strategy is available under all typical LLC converter operating mode. Both simulation and experiment are carried out for validation. The results demonstrate an overall SR timing error of less than 0.6%, along with a maximum efficiency improvement of 0.34% compared to existing model-based strategies.**

***Index Terms*—LLC resonant converter, converter modeling, operation boundary recognition, synchronous rectification (SR), time domain analysis (TDA).**

I. Introduction

DUE to the outstanding electromagnetic interference characteristic and the high efficiency, the LLC resonant converter has been widely adopted in battery energy storage (BES) systems, electric vehicle charging systems and data centers [1], [2], [3], [4]. By leveraging the low conduction resistance of MOSFETs, the synchronous rectification (SR) technique mimics the switching behavior of the LLC converter's secondary-side rectifier diode, which can significantly reduce the conduction loss of the secondary side rectifier and enhances the overall efficiency of the LLC converter [5]. Over the past two decades, various SR strategies have been proposed. These strategies can be broadly categorized into two approaches based on whether high-frequency (HF) signals at the switching frequency level are sensed: the HF-signal-based approach and the model-based approach.

The HF-signal-based approach for SR control can be categorized into HF current sensing and HF voltage sensing methods. Initially, current sensing involved detecting the drain-source current of each SR MOSFET using a current transformer (CT) [6]. While effective and robust, this method introduced extra winding loss, reducing efficiency. Efforts to reduce winding loss led to sensing the primary-side resonant inductor current, but the need for CTs persisted, compromising power density and efficiency [7]. To eliminate extra losses, the voltage sensing approach is employed. The most common method detects the conduction of the SR MOSFET's reverse diode by sensing its drain-source voltage [8], [9], [10], [11]. This technique is prevalent in commercial SR chip designs [12]. However, package parasitic inductance can cause premature turn-OFF. To overcome this issue, primary side voltages (e.g., resonant inductor, resonant capacitor, and magnetizing inductor voltages) are sensed and modulated to generate the SR MOSFET gate drive signal [13], [14], [15]. Despite its effectiveness, this method requires complex auxiliary circuits for signal processing, posing hardware design challenges.

To sum up, implementing HF-signal-based strategies incurs extra costs due to the need for additional HF signal sensing and modulation devices [16]. Moreover, high-bandwidth isolators become essential if the primary side voltage signal is utilized in the SR strategy, further increasing the overall cost and complexity. Besides, the HF-signal-based SR strategy limits the possibility of LLC converters extending to bidirectional operation, where the phase-shift modulation is adopted during the reverse power transmission [17], [18]. In the bidirectional power

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transmission scenarios, secondary side devices must function as both SR and active devices. The dual functionality requires additional drive signal selection switches to reconfigure the gate drive signal source between the SR driver during SR mode and the microcontroller unit (MCU) during active device mode.

To achieve a scalable, cost-effective, and extra-loss-free SR strategy, the model-based SR strategies have been proposed and is widely adopted in cost-sensitive applications requiring bidirectional power transmission and involving relatively high voltage ports, such as on-board chargers and BES system [16], [19], [20], [21], [22], [23], [24], [25], [26], [27]. However, the performance of model-based SR approach significantly depends on the precision of model. Furthermore, since LLC converters operate in various modes, each requiring a distinct model, it is essential to accurately identify the operating mode to apply the appropriate model [28].

The SR strategy based on modified fundamental harmonic approximation (FHA) model has been proposed in [19], [20], and [21], which is effective across the entire switching frequency range. However, the excessive simplification inherent in the FHA model results in suboptimal accuracy for predicting SR timing. In addition, as the load decreases, extra discontinuous conduction mode (DCM) events occur, necessitating a delay in the SR turn-ON timing. However, identifying the presence of DCM and determining the appropriate delay using only the modified FHA model is challenging, potentially degrading SR strategy performance and overall converter efficiency.

The time domain analysis (TDA) model has been introduced in [22], [23], and [24], owing to the high accuracy of TDA model. However, due to the dual resonant frequencies in some operating modes, obtaining an analytical solution for SR timing is not feasible because of the presence of transcendental equations. As a result, fitting curves of the SR timing are adopted in [22], [23], and [24]. Nevertheless, the preparation procedure of the fitting curve is time-consuming, and different fitting curves must be generated for each set of resonant parameter. Moreover, there are still operation modes neglected in the SR strategy in [22], [23], and [24]. An advanced SR strategy employing deep learning techniques was proposed in [25] to determine the optimal SR MOSFET regulation principle with minimal loss. However, sampling the loss data using a thermocouple is cumbersome and time-intensive. In addition, there is a potential risk of system instability due to the lack of practical theoretical support for deep learning results.

To realize online SR timing calculation and thus eliminate the cumbersome process of fitting curve preparation, simplifications of the TDA model were performed in [26] and [27], enabling online calculation of SR timing. Yet, only a subset of typical operation modes was analyzed in [26] and [27], limiting the operational range of the SR strategies to the resonant frequency and the below-resonance region, respectively. An SR strategy based on geometrically simplified state plane analysis was proposed in [16]. In this approach, the state trajectory was simplified through geometrical principles to derive the SR timing expression. This method allows for real-time calculation of SR timing and includes an online DCM recognition strategy. However, due to the difficulty in calculation of the SR timing under light loads in state plane analysis, the operational range of the SR strategy in [16] is restricted to heavy load conditions in below- and above-resonance regions. To sum up, the operation range of the existing SR strategies cover only a subset of all typical operation modes, and there is an urgent need for an accurate online SR strategy that is effective across the full frequency and load range. This article proposes a novel simplified time domain analysis (STDA)-based SR strategy that incorporates both online SR timing algorithm and operation mode recognition algorithm. The proposed novel SR strategy is effective in both full switching frequency and full load range, thus improving the efficiency of the LLC converter over a wide range. Moreover, only dc signals—specifically input voltage, output voltage, and output current—need to be sampled. It should be noted that unlike other application, such as parameter design and switching frequency feedforward control, all the three state variables of TDA (voltage gain, load, and switching frequency) are known in the SR application, which reduces the need for simplification in the modeling process but necessitates new theoretical derivations. The main contributions of this article can be summarized as follows.

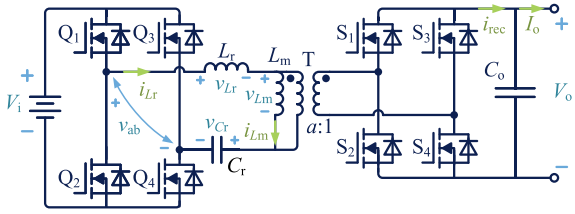

Fig. 1. Topology of the full-bridge LLC converter.

1) The analytical expressions for both the ideal SR turn-ON delay and duty cycle **across all typical operation mode** are derived using the STDA model.
2) An online operation mode recognition algorithm is introduced through STDA model **to accurately identify the operation mode of the LLC converter**.
3) Based on the proposed real-time algorithm of the ideal SR timing and the online operation mode recognition algorithm, a novel model-based online SR strategy for LLC converter is proposed. Different from the existing SR strategy, the proposed STDA SR strategy is effective in real-time over the full switching frequency and load range.

The rest of this article is organized as follows. In Section II, the SR process of LLC converter and the boundary between different operation modes is analyzed. In Section III, a novel STDA-based SR strategy is proposed, and the performance of the proposed control strategy is evaluated with simulation. In Section IV, experiments are carried out for validation. Finally, Section V concludes this article.

II. TDA of LLC Converter SR Process

The topology of full-bridge LLC converter is depicted as in Fig. 1. The full-bridge LLC converter consists of an H-bridge inverter module on the primary side, an H-bridge rectifier module on the secondary side and a resonant circuit. The devices

TABLE I
STATE VARIABLES AND NORMALIZATION OF THE FULL-BRIDGE LLC CONVERTER

State variables	Symbol	Normalized variable
Input voltage	$V_{\rm i}$	$V_{\rm in}=1$
Output voltage	$V_{\rm o}$	$V_{\rm on}=aV_{\rm o}/V_{\rm i}$
Output current	$I_{\rm o}$	$I_{\rm on}=I_{\rm o}Z_{\rm l}/(aV_{\rm i})$
Resonant capacitor voltage	v_{Cr}	$v_{Crn}=v_{Cr}/V_{\rm i}$
Resonant inductor voltage	v_{Lr}	$v_{Lrn}=v_{Lr}/V_{\rm i}$
Magnetizing inductor voltage	v_{Lm}	$v_{Lmn}=v_{Lm}/V_{\rm i}$
Primary side mid-point voltage	$v_{\rm ab}$	$v_{\rm abn}=v_{\rm ab}/V_{\rm i}$
Resonant inductor current	i_{Lr}	$i_{Lrn}=i_{Lr}Z_{\rm l}/V_{\rm i}$
Magnetizing inductor current	i_{Lm}	$i_{Lmn}=i_{Lm}Z_{\rm l}/V_{\rm i}$
Rectified current	$i_{\rm rec}$	$i_{\rm recn}=i_{\rm rec}Z_{\rm l}/(aV_{\rm i})$
Switching frequency	$f_{\rm s}$	$f_{\rm n}=f_{\rm s}/f_{\rm r}$
Time period	t	$\theta=t/\omega_{\rm r}$
Resonant frequency	$f_{\rm r}=1/(2\pi\sqrt{L_{\rm r}C_{\rm r}})$	-
Resonant angular frequency	$\omega_{\rm r}=1/\sqrt{L_{\rm r}C_{\rm r}}$	-
Inductor ratio	$k=L_{\rm m}/L_{\rm r}$	-
Characteristic impedance	$Z_{\rm l}=\sqrt{L_{\rm r}/C_{\rm r}}$	-

TABLE II
CRITERIA OF DIFFERENT STATE OF THE LLC CONVERTER AND IDEAL OPERATION OF SR MOSFETS

Item	State of Q_1-Q_4 and v_{Lmn}	Ideal Operation of SR MOSFETs	Equivalent State
State I	Q_1 and Q_4 ON; Q_2 and Q_3 OFF; v_{Lmn} clamped at $V_{\rm on}$	S_1 and S_4 ON; S_2 and S_3 OFF	P State
State IV	Q_2 and Q_3 ON; Q_1 and Q_4 OFF; v_{Lmn} clamped at $-V_{\rm on}$	S_2 and S_3 ON; S_1 and S_4 OFF	
State II	Q_1 and Q_4 ON; Q_2 and Q_3 OFF; v_{Lmn} clamped at $-V_{\rm on}$	S_2 and S_3 ON; S_1 and S_4 OFF	N State
State V	Q_2 and Q_3 ON; Q_1 and Q_4 OFF; v_{Lmn} clamped at $V_{\rm on}$	S_1 and S_4 ON; S_2 and S_3 OFF	
State III	Q_1 and Q_4 ON; Q_2 and Q_3 OFF; v_{Lmn} not clamped	S_1-S_4 OFF	O State
State VI	Q_2 and Q_3 ON; Q_1 and Q_4 OFF; v_{Lmn} not clamped	S_1-S_4 OFF	

on the primary side H-bridge module are denoted as Q_1-Q_4, while those on the secondary side are denoted as S_1-S_4. The resonant circuit includes the resonant capacitor $C_{\rm r}$, the resonant inductor $L_{\rm r}$, the magnetizing inductor $L_{\rm m}$, and the transformer T with a turns ratio of a. To generalize the analysis, all circuit state variables and their normalization benchmarks are listed in Table I. It should be noted that the time period t is normalized as the electrical angle θ.

Based on the state of the primary side H-bridge and the resonant circuit, as listed in Table II, the state of LLC converter can be classified into six distinct states. The equivalent circuits for these states are illustrated in Fig. 2. In states I and IV, the voltage across the magnetizing inductor v_{Lmn} is clamped at $V_{\rm on}$ and $-V_{\rm on}$, respectively, sharing the same polarity as $v_{\rm abn}$. Therefore, states I and IV are also referred to as positive states (P states). Similarly, states II and V are referred to as negative states (N states), and states III–VI are referred to as zero states (O states). The state expressions for states I–IV can be respectively

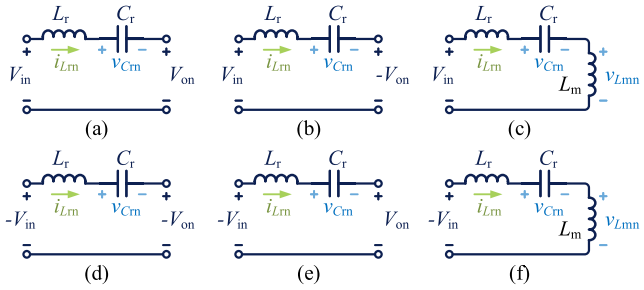

Fig. 2. Equivalent circuit of the LLC converter in (a) state I, (b) state II, (c) state III, (d) state IV, (e) state V, and (f) state VI.

written as [29]

$$(v_{Crn}-1+V_{\rm on})^2+i_{Lrn}^2=(V_{Cr0n}-1+V_{\rm on})^2+I_{Lr0n}^2 \quad (1)$$

$$(v_{Crn}-1-V_{\rm on})^2+i_{Lrn}^2=(V_{Cr0n}-1-V_{\rm on})^2+I_{Lr0n}^2 \quad (2)$$

$$(v_{Crn}-1)^2+g^2i_{Lrn}^2=(V_{Cr0n}-1)^2+g^2I_{Lr0n}^2 \quad (3)$$

$$(v_{Crn}+1-V_{\rm on})^2+i_{Lrn}^2=(V_{Cr0n}+1-V_{\rm on})^2+I_{Lr0n}^2 \quad (4)$$

$$(v_{Crn}+1+V_{\rm on})^2+i_{Lrn}^2=(V_{Cr0n}+1+V_{\rm on})^2+I_{Lr0n}^2 \quad (5)$$

$$(v_{Crn}+1)^2+g^2i_{Lrn}^2=(V_{Cr0n}+1)^2+g^2I_{Lr0n}^2 \quad (6)$$

where V_{Cr0n} and I_{Lr0n} are the normalized initial resonant capacitor voltage and the normalized initial resonant inductor current in each state, which are still remained unknown. g is equal to $1/(k+1)^{0.5}$.

By arranging these different states, the LLC converter can work in various operation modes, including OPO, PO, PON, PN, P, NP, and NOP mode, whose distribution is simultaneously determined by the switching frequency, voltage gain, and load of the converter. Fig. 3(a) and (b) illustrates the frequency-gain and frequency-load distributions of the operation mode, respectively. In the below-resonance region, the operation mode of LLC converter can be ordered as O mode, OPO mode, PO mode, PON mode, and PN mode, progressing from heavy load to light load, as shown in Fig. 3(b). In the above-resonance region, the operation modes can be arranged as O mode, OPO mode, NOP mode, and NP mode, again progressing from heavy load to light load, as shown in Fig. 3(b). At the resonant frequency, the LLC converter only operates in P mode and OPO mode. Herein, the "XYZ" mode refers to the operation mode where a half switching cycle of the LLC converter is composed of X state, Y state, and Z state in sequence. For example, the PO mode indicates that the half switching cycle of the LLC converter is composed of P state and O state in sequence.

It should be noted that the term "state" is utilized to denote the specific status of the LLC converter with a particular equivalent circuit. In contrast, the term "mode" refers to the scenario of LLC converter operation, which may involve a single "state" or a combination of several "states." The detailed

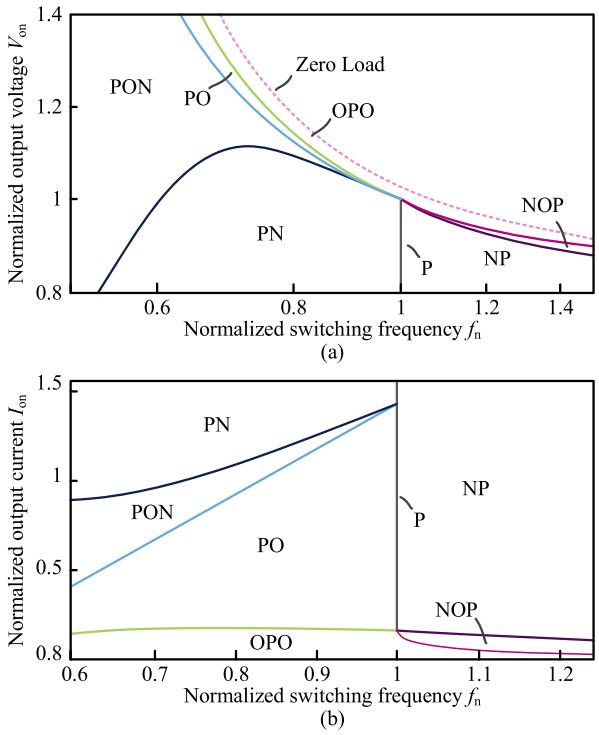

Fig. 3. Distribution of operation mode the LLC converter. (a) f_n-V_{on} distribution. (b) f_n-I_{on} distribution.

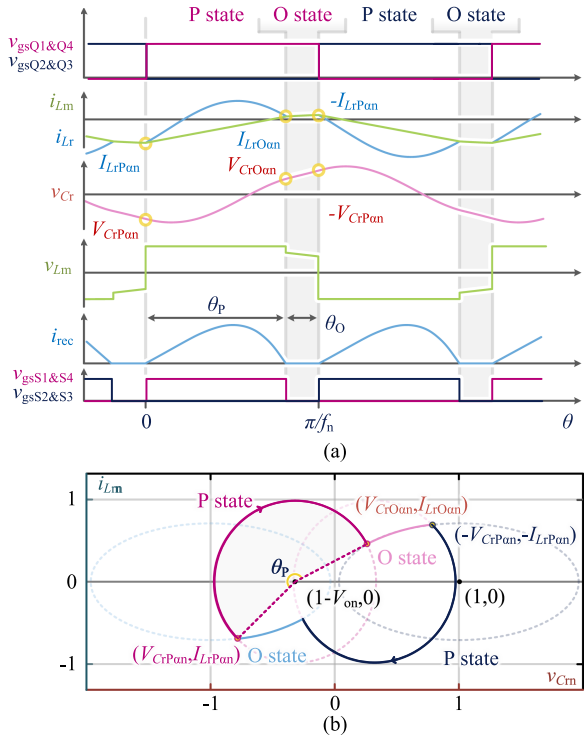

Fig. 4. (a) Key waveform and (b) state plane trajectory of the LLC converter in the PO mode.

quantitative analysis of the waveform and boundaries for each operation mode will be given in the subsequent sections. Due to space limitations, this article will not include a preliminary qualitative analysis of the formation mechanisms of each mode. For the basic information and qualitative analysis on LLC converter operation modes, please refer to Section III of [28].

A. Basic Operation Principle of Model-Based SR Strategy

The basic principle of model-based SR strategy is to regulate the gate signal of SR MOSFET so as to mimic the performance of rectifier diodes [16]. To be specific, as shown in Fig. 2, the corresponding rectifier diodes conduct during the P state, while the opposite rectifier diodes conduct during the N state. In the O state, all the diodes are cut off. The detailed corresponding operation principle of the model-based SR MOSFETs in different state is summarized in Table II, and the key to the model-based SR strategy lies in accurately modeling the duration of the P, O, and N states under different operation modes. However, due to variations in operating conditions, different models are required to determine the ideal timing for SR MOSFETs.

A novel model-based SR strategy is proposed in this article, where only input voltage V_i, output voltages V_o and output currents I_o are sensed. The model for all typical operating modes is analyzed through STDA. Both online SR timing and operation mode recognition algorithms are integrated into this approach, facilitating real-time prediction of SR timing and determination of the LLC converter operating conditions. This eliminates the need for a lookup table and fitting curves, streamlining the implementation process. The detailed derivation of the SR gate drive timing will be described in this section. Notably, due to the similarity between PON/PO mode boundary and the ZVS/ZCS (zero voltage switching, zero current switching) boundary, the LLC converter is typically designed to operate in PO, OPO, P, NP, and NOP mode to ensure full range ZVS [30]. In addition, because the P mode can be considered a special case within the PO mode, only the PO, OPO, NP, and NOP modes are discussed in this section.

B. STDA in the PO Mode

The key waveform of the LLC converter in the PO mode is depicted as in Fig. 4, where $I_{LrP\alpha n}$ and $I_{LrO\alpha n}$ denote the initial resonant inductor current in P state and O state of PO mode, respectively, and $V_{CrP\alpha n}$ and $V_{CrO\alpha n}$ refer to the initial resonant capacitor voltage in P state and O state of PO mode, respectively. As listed in Table II, the ideal operation of the SR MOSFETs in PO mode is to turn-ON in P state and turn-OFF in O state. The turn-ON delay duty $D_{SR,delay}$ and the duty cycle $D_{SR,duty}$ of SR MOSFETs in PO mode can be respectively written as

$$D_{SR,delay} = 0 \tag{7}$$

$$D_{SR,duty} = f_n \theta_P / \pi \tag{8}$$

where θ_P is the electrical angle of P state. Assuming that the converter has an ideal efficiency of 100%, the input charge of the resonant circuit within a half switching cycle can be

written as

$$\int_0^{\pi/f_n} V_{on} I_{on} \mathrm{d}\theta = \int_0^{\pi/f_n} i_{Lrn} \mathrm{d}\theta = (-V_{CrP\alpha n}) - V_{CrP\alpha n}. \tag{9}$$

From (9), the initial resonant capacitor voltage in P state $V_{CrP\alpha n}$ can be derived as

$$V_{CrP\alpha n} = -\frac{\pi V_{on} I_{on}}{2 f_n}. \tag{10}$$

As the magnetizing inductor voltage v_{Lmn} is always clamped at V_{on} in P state, it can be obtained that

$$I_{LrO\alpha n} - I_{LrP\alpha n} = \int_0^{\theta_P} \frac{V_{on}}{k} \mathrm{d}\theta = \frac{\theta_P}{k} V_{on}. \tag{11}$$

By combining (1), (3), (4), (6), (10), and (11), the simultaneous equation in the PO mode can be given as

$$\begin{cases} I_{LrP\alpha n} = -g(V_{CrO\alpha n} - 1)\sin(g\theta_O) - I_{LrO\alpha n}\cos(g\theta_O) \\ V_{CrP\alpha n} = \frac{I_{LrO\alpha n}}{g}\sin(g\theta_O) - (V_{CrO\alpha n} - 1)\cos(g\theta_O) - 1 \\ \theta_P = k(I_{LrO\alpha n} - I_{LrP\alpha n})/V_{on} \\ V_{CrP\alpha n} = -\pi V_{on} I_{on}/(2 f_n) \\ I_{LrO\alpha n} = I_{LrP\alpha n}\cos\theta_P + (V_{CrP\alpha n} + V_{on} - 1)\sin\theta_P \\ V_{CrO\alpha n} = (V_{CrP\alpha n} + V_{on} - 1)\cos\theta_P - I_{LrP\alpha n}\sin\theta_P \\ \qquad -V_{on} + 1 \end{cases} \tag{12}$$

where θ_O is the electrical angle of O state. By temporarily approximating θ_P as π, $\theta_O = \pi/f_n - \pi$ is equal to $(1/f_n - 1)\pi$. From (12), it can be obtained that

$$\begin{cases} I_{LrP\alpha n} = -\frac{\pi V_{on} + gk\sin(g\theta_O)(1+V_{CrP\alpha n})}{k[1+\cos(g\theta_O)]} \\ V_{CrP\alpha n} = -\pi V_{on} I_{on}/(2 f_n) \\ V_{CrO\alpha n} = 1 + \frac{\pi\sin(g\theta_O)V_{on}}{gk[1+\cos(g\theta_O)]} + V_{CrP\alpha n} - V_{on} \\ I_{LrO\alpha n} = I_{LrP\alpha n} + V_{on}\pi/k \end{cases} \tag{13}$$

where θ_O is still considered as $(1/f_n - 1)\pi$. With (13), the electrical angle of P state in PO mode can be derived as

$$\theta_P = \pi - \arctan\frac{I_{LrO\alpha n}}{V_{CrO\alpha n} + V_{on} - 1} + \arctan\frac{I_{LrP\alpha n}}{V_{CrP\alpha n} + V_{on} - 1}. \tag{14}$$

C. STDA in the OPO Mode

The key waveform of the LLC converter in the OPO mode is depicted as in Fig. 5, where $I_{LrOA\beta n}$, $I_{LrP\beta n}$, and $I_{LrOB\beta n}$ indicate the initial resonant inductor current in the first O state (O_A state), P state, and the second O state (O_B state) of OPO mode, respectively. Similarly, $V_{CrOA\beta n}$, $V_{CrP\beta n}$, and $V_{CrOB\beta n}$ refer to the initial resonant capacitor voltage in the first O state, P state and the second O state of OPO mode, respectively. As listed in Table II, the ideal operation principle of the SR MOSFETs in OPO mode is to turn-ON during P state with a delay of the first O state and to turn-OFF during the second O state. The turn-ON delay and the duty cycle of SR MOSFETs in PO mode can be,

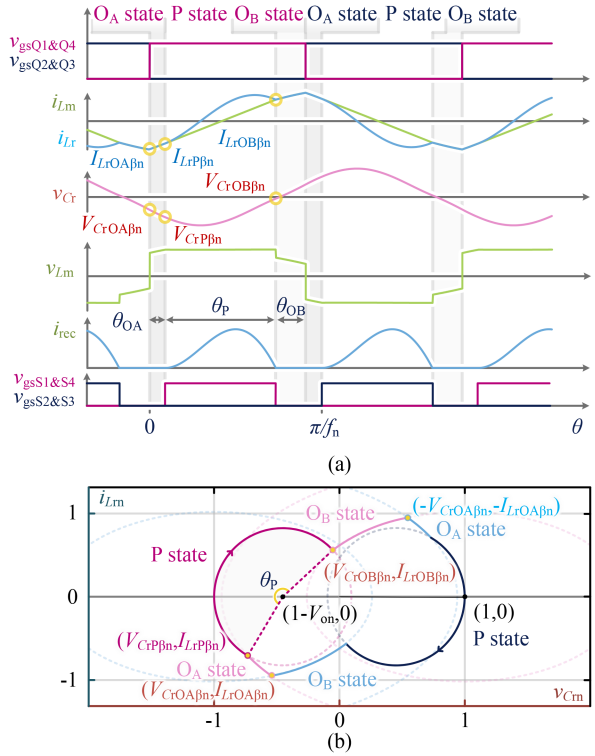

Fig. 5. (a) Key waveform and (b) state plane trajectory of the LLC converter in the OPO mode.

respectively, written as

$$D_{SR,delay} = f_n \theta_{OA}/\pi \tag{15}$$

$$D_{SR,duty} = f_n \theta_P/\pi. \tag{16}$$

In the O state, the resonant frequency f_r/g is significantly low compared to the switching frequency f_s. Consequently, the state variables in the O state can be regarded as constant under certain conditions for simplification. At the end of the first O state, the magnetizing inductor voltage v_{Lmn} is V_{on}. Thus, v_{Lm} can be approximated as a constant V_{on} during the first O state. As a result, the first O state can be treated as P state for simplification in the modeling process, and the conclusion in (14) can be adopted as

$$\theta_P + \theta_{OA} = \pi - \arctan\frac{I_{LrO\alpha n}}{V_{CrO\alpha n} + V_{on} - 1} + \arctan\frac{I_{LrP\alpha n}}{V_{CrP\alpha n} + V_{on} - 1} \tag{17}$$

where $I_{LrO\alpha n}$, $V_{CrO\alpha n}$, $I_{LrP\alpha n}$, and $V_{CrP\alpha n}$ can be calculated in (13).

Because v_{Lm} is assumed constant as V_{on} during the first O state and P state, it can be obtained that

$$I_{LrOB\beta n} - I_{LrOA\beta n} = \frac{1}{k}\int_0^{\theta_{OA}+\theta_P} V_{on}\mathrm{d}\theta = (\theta_{OA} + \theta_P)\frac{V_o}{k} \tag{18}$$

where the initial resonant current in the second O state $I_{LrOB\beta n}$ can also be written as

$$I_{LrOB\beta n} = I_{LrOA\beta n}\cos\frac{g\,(\pi-\theta_{OA}-\theta_P)}{f_n} - g\,(1+V_{CrOA\beta n})\sin\frac{g\,(\pi-\theta_{OA}-\theta_P)}{f_n}. \quad (19)$$

As similar in PO mode, the initial resonant capacitor voltage in the half switching cycle, i.e., the first O state, can be obtained from (9) as

$$V_{CrOA\beta n} = -\frac{\pi V_{on} I_{on}}{2f_n}. \quad (20)$$

From (18), (19), and (20), the initial resonant inductor current in the first O state $I_{LrOA\beta n}$ can be derived as

$$I_{LrOA\beta n} = \frac{\frac{V_o}{k}(\theta_{OA}+\theta_P)+g(1+V_{CrOA\beta n})\sin\frac{g(\pi-\theta_{OA}-\theta_P)}{f_n}}{1+\cos\frac{g(\pi-\theta_{OA}-\theta_P)}{f_n}}. \quad (21)$$

The resonant circuit exhibit both the characteristic of P state and O state at the beginning of P state. According the equivalent resonant circuit in Fig. 2(a) and (c), the expression of KVL at the beginning of P state can be written as

$$V_{CrP\beta n} + V_{LrP\beta n} + V_{LmP\beta n} = 1 \quad (22)$$

where $V_{LmP\beta n}$ is equal to V_{on}, and $V_{LrP\beta n}$ is equal to $V_{LmP\beta n}/k = V_{on}/k$, according to the voltage division between L_r and L_m. Thus, the initial resonant capacitor voltage in the P state can be obtained from (22) as

$$V_{CrP\beta n} = 1 - \frac{(1+k)V_{on}}{k}. \quad (23)$$

With (20), (21), and (23), the electrical angle of the first O state can be given as

$$\theta_{OA} = \arctan\frac{I_{LrOA\beta n}}{V_{CrOA\beta n}} - \arccos\frac{V_{CrP\beta n}}{\sqrt{I_{LrOA\beta n}^2 + V_{CrOA\beta n}^2}}. \quad (24)$$

By taking (17) and (24) into (15) and (16) the duty cycle and duty delay of the SR MOSFETs in the OPO mode can be calculated.

D. STDA in the NP Mode

The key waveform of the LLC converter in the NP mode is shown as in Fig. 6, where $I_{LrN\delta n}$ and $I_{LrP\delta n}$ represent the initial resonant inductor current in N state and P state of NP mode, respectively, and $V_{CrN\delta n}$ and $V_{CrP\delta n}$ refer to the initial resonant capacitor voltage in N state and P state of NP mode, respectively. According to the operation principle outlined in Table II, the corresponding SR MOSFETs in the last half switching cycle is required to turn-OFF after a delay period of θ_N, and the turn-ON delay and the duty cycle of SR MOSFETs in NP mode can be, respectively, expressed as

$$D_{SR,delay} = f_n\theta_N/\pi \quad (25)$$

$$D_{SR,duty} = f_n(\theta_N+\theta_P)/\pi = 0.5. \quad (26)$$

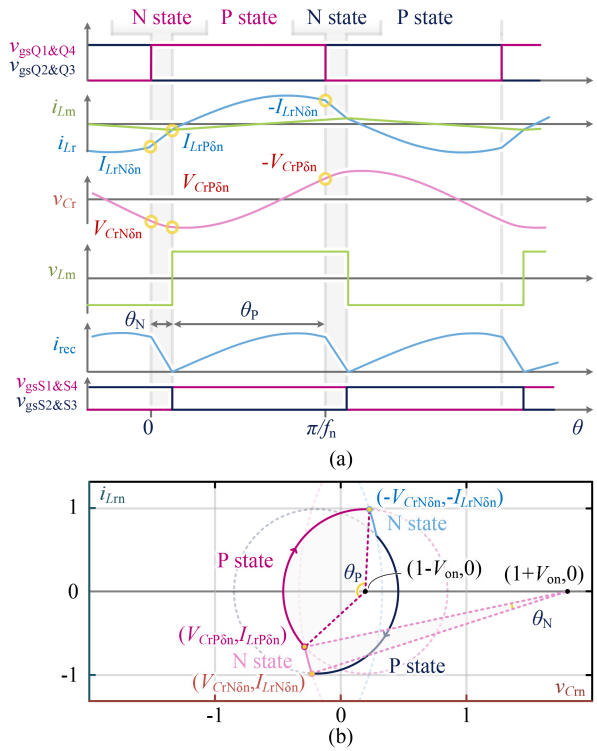

Fig. 6. (a) Key waveform and (b) state plane trajectory of the LLC converter in the NP mode.

The NP mode has been studied in [16] and [28]. The electrical angle of N state in NP mode can be calculated as

$$\theta_N = \arcsin\left[\frac{V_{on}}{2}\frac{\pi}{kf_n}\cos\frac{\pi}{2f_n} \times\left(\cos\frac{\pi}{2f_n}+\frac{V_{CrP\delta n}-V_{on}+1}{I_{LrP\delta n}}\sin\frac{\pi}{2f_n}\right)\right] \quad (27)$$

where the initial resonant capacitor voltage in P state $V_{CrP\delta n}$ and the initial resonant inductor current in P state $I_{LrP\delta n}$ can be, respectively, obtained as [16]

$$V_{CrP\delta n} = -\frac{\pi}{2f_n}I_{on} \quad (28)$$

$$I_{LrP\delta n} = -\frac{\pi V_{on}}{2kf_n}. \quad (29)$$

E. STDA in the NOP Mode

The key waveform of the LLC converter operating in the NOP mode is illustrated in Fig. 7, where $I_{LrN\gamma n}$, $I_{LrO\gamma n}$, and $I_{LrP\gamma n}$ are the initial resonant inductor current in N state, O state, and P state of NOP mode, respectively. Similarly, $V_{CrN\gamma n}$, $V_{CrO\gamma n}$, and $V_{CrP\gamma n}$ refer to the initial resonant capacitor voltage in N state, O state, and P state of NOP mode, respectively.

According to the operation principle in Table II, the corresponding SR MOSFETs in the last half switching cycle is required to turns-OFF after a delay period of θ_N. Then, all the SR MOSFETs turn-OFF in the O state, and the corresponding SR MOSFETs in this half switching cycle turns-ON during the P state. The turn-ON

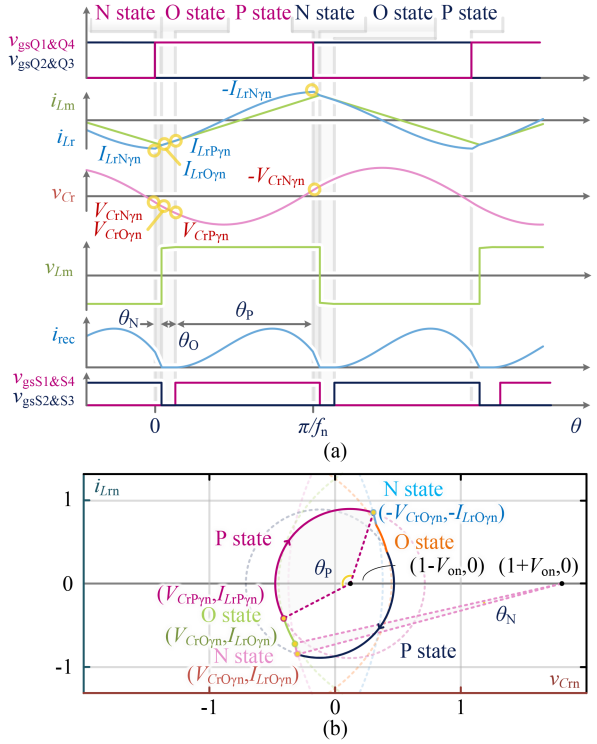

Fig. 7. (a) Key waveform and (b) state plane trajectory of the LLC converter in the NOP mode.

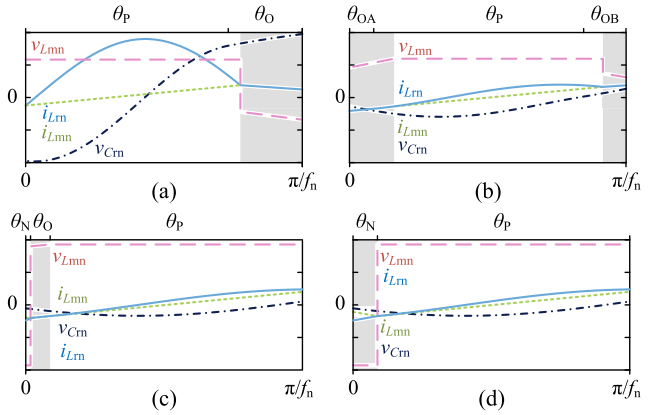

Fig. 8. Key waveform of the LLC converter within a half switching cycle in (a) PO mode, (b) OPO mode, (c) NOP mode, and (d) NP mode.

delay and the duty cycle of SR MOSFETs in NP mode can be respectively written as

$$D_{\mathrm{SR,delay}} = f_{\mathrm{n}}\left(\theta_{\mathrm{N}} + \theta_{\mathrm{O}}\right)/\pi \tag{30}$$

$$D_{\mathrm{SR,duty}} = f_{\mathrm{n}}\left(\theta_{\mathrm{P}} + \theta_{\mathrm{N}}\right)/\pi. \tag{31}$$

As the N state in NOP mode is very short, it can be approximated that its electrical angle $\theta_{\mathrm{N}} = 0$ during analysis.

Similar as the first O state in OPO mode, the voltage on the magnetizing inductor can be considered constant as V_{on} during the O state in NOP mode. Thus, according to the voltage second balance, it can be obtain that

$$\frac{1}{k}\int_0^{\pi/f_{\mathrm{n}}} V_{\mathrm{on}}\mathrm{d}\theta = \left(-I_{Lr\mathrm{O}\gamma\mathrm{n}}\right) - I_{Lr\mathrm{O}\gamma\mathrm{n}}. \tag{32}$$

From (32), the initial resonant inductor current in the O state can be obtained as

$$I_{Lr\mathrm{O}\gamma\mathrm{n}} = -\frac{\pi V_{\mathrm{on}}}{2kf_{\mathrm{n}}}. \tag{33}$$

The initial resonant capacitor voltage in the half switching cycle can be obtain from (9) as

$$V_{Cr\mathrm{O}\gamma\mathrm{n}} = -\frac{\pi V_{\mathrm{on}} I_{\mathrm{on}}}{2f_{\mathrm{n}}}. \tag{34}$$

The resonant circuit exhibit both the characteristic of P state and O state at the beginning of P state. Thus, the expression of Kirchhoff's voltage law (KVL) at the beginning of P state can be written as

$$V_{Cr\mathrm{P}\gamma\mathrm{n}} + V_{Lr\mathrm{P}\gamma\mathrm{n}} + V_{Lm\mathrm{P}\gamma\mathrm{n}} = 1 \tag{35}$$

where $V_{Lm\mathrm{P}\gamma\mathrm{n}}$ is equal to V_{on}, and $V_{Lr\mathrm{P}\gamma\mathrm{n}}$ is equal to $V_{Lm\mathrm{P}\gamma\mathrm{n}}/k = V_{\mathrm{on}}/k$, which are similar to those in OPO mode. Thus, the initial resonant capacitor voltage in the P state of NOP mode can be obtained as

$$V_{Cr\mathrm{P}\gamma\mathrm{n}} = 1 - \frac{(1+k)V_{\mathrm{on}}}{k}. \tag{36}$$

With (33), (34), and (36), the electrical phase of O state in the NOP mode can be obtained as

$$\theta_{\mathrm{O}} = \arccos\frac{V_{Cr\mathrm{P}\gamma\mathrm{n}}}{\sqrt{I_{Lr\mathrm{O}\gamma\mathrm{n}}^2 + V_{Cr\mathrm{O}\gamma\mathrm{n}}^2}} - \arctan\frac{I_{Lr\mathrm{O}\gamma\mathrm{n}}}{V_{Cr\mathrm{O}\gamma\mathrm{n}}}. \tag{37}$$

F. Operation Mode Recognition of LLC Converter

With the variation of voltage gain and load, the operation point of the LLC converter will shift between PO, OPO, NP, and NOP mode. Thus, online operation mode recognition is necessary for executing appropriate model analysis.

1) PO/OPO Mode: As mentioned in Section II-C, the moment at the boundary between two states exhibits characteristic of both the two states, which is the key to derive the expression of the boundary between two modes. In PO mode, once the moment with duality characteristic of O state and P state occurs at the beginning of the switching cycle, the LLC converter will shift to the OPO mode. As is shown in Fig. 8(a) and (b), on the boundary between PO and OPO mode, the moment at $\theta = 0$ exhibits characteristic of both O state and P state. Thus, the expression of KVL at $\theta = 0$ on the PO/PON boundary can be given as

$$v_{Crn}(0) + v_{Lrn}(0) + v_{Lmn}(0) = 1 \tag{38}$$

where $v_{Lmn}(0)$ is equal to V_{on}, and $v_{Lrn}(0)$ is equal to $v_{Lmn}(0)/k = V_{\mathrm{on}}/k$. The initial resonant capacitor voltage in the half switching cycle can be obtain from (9) as

$$v_{Crn}(0) = \frac{\pi V_{\mathrm{on}} I_{\mathrm{on}}}{2f_{\mathrm{n}}}. \tag{39}$$

Thus, the output current on the boundary between the OPO and PO mode can be given as

$$I_{\mathrm{oOPOn}} = \frac{2f_{\mathrm{n}}}{\pi}\left(1+\frac{1}{k}-\frac{1}{V_{\mathrm{on}}}\right). \tag{40}$$

2) NP/NOP Mode: Similarly, the criteria of NP/NOP boundary is that at the beginning of P state in NP mode, the resonant circuit exhibits the characteristic of both P and O state. The boundary between NP and NOP mode has been studied in [16], which can be written as

$$I_{\mathrm{oNOPn}} = \frac{2f_{\mathrm{n}}}{\pi}\left(\frac{V_{\mathrm{on}}}{k}+V_{\mathrm{on}}-1\right). \tag{41}$$

3) NOP/OPO Mode: Unfortunately, such duality characteristic in PO/OPO and NP/NOP boundary does not occur at the NOP/OPO boundary, because the existence of the second O state after P state in OPO mode is driven by the intersection of the resonant inductor current and magnetizing inductor current, and the magnetizing inductor voltage exhibit a sudden change at the end of P state. Therefore, the NOP/OPO boundary losses the duality characteristic.

Yet, the NOP/OPO boundary shows a unique characteristic that the NOP/OPO boundary is also the distribution trajectory of OP mode [28]. As the NOP mode analysis is carried out with the assumption that the N mode is omitted, the initial state variable in the OP mode share the same conclusion as

$$\begin{cases} I_{Lr\mathrm{O}\epsilon\mathrm{n}} = -\pi V_{\mathrm{on}}/(2kf_{\mathrm{n}}) \\ V_{C\mathrm{rO}\epsilon\mathrm{n}} = \pi V_{\mathrm{on}} I_{\mathrm{on}}/(2f_{\mathrm{n}}) \\ V_{C\mathrm{rP}\epsilon\mathrm{n}} = 1 - V_{\mathrm{on}}k/(1+k) \end{cases} \tag{42}$$

where $V_{C\mathrm{rO}\epsilon\mathrm{n}}$ and $V_{C\mathrm{rP}\epsilon\mathrm{n}}$ denote the initial resonant capacitor voltage in the O state and P state in the OP mode, respectively. $I_{C\mathrm{rO}\epsilon\mathrm{n}}$ refers to the initial resonant inductor current in the O state in the OP mode. The initial resonant inductor current in the P state $I_{Lr\mathrm{P}\epsilon\mathrm{n}}$ can be calculated from the perspective in O mode as

$$I_{Lr\mathrm{P}\epsilon\mathrm{n}}^2 = I_{Lr\mathrm{O}\epsilon\mathrm{n}}^2 + g^2\left(V_{C\mathrm{rO}\epsilon\mathrm{n}}-1\right)^2 - g^2\left(V_{C\mathrm{rP}\epsilon\mathrm{n}}-1\right)^2 \tag{43}$$

and from the perspective in O mode as

$$I_{Lr\mathrm{P}\epsilon\mathrm{n}}^2 = I_{Lr\mathrm{O}\epsilon\mathrm{n}}^2 + \left(V_{C\mathrm{rO}\epsilon\mathrm{n}}-1+V_{\mathrm{on}}\right)^2 - \left(V_{C\mathrm{rP}\epsilon\mathrm{n}}-1+V_{\mathrm{on}}\right)^2. \tag{44}$$

In contrast, the resonant inductor current at the end of P state is greater than $-I_{C\mathrm{rO}\epsilon\mathrm{n}}$ in the NOP mode, and is lower than $-I_{C\mathrm{rO}\epsilon\mathrm{n}}$ in the OPO mode. Thus, $I_{Lr\mathrm{P}\epsilon\mathrm{n}}$ in (44) is lower than $I_{Lr\mathrm{P}\epsilon\mathrm{n}}$ in (43) in NOP mode and is greater than $I_{Lr\mathrm{P}\epsilon\mathrm{n}}$ in (43) in OPO mode. Therefore, the criteria of NOP/OPO mode recognition can be expressed as

$$\Delta I_{Lr\mathrm{P}\epsilon\mathrm{n}}^2 = g^2\left(V_{C\mathrm{rO}\epsilon\mathrm{n}}-1\right)^2 - g^2\left(V_{C\mathrm{rP}\epsilon\mathrm{n}}-1\right)^2 - \left(V_{C\mathrm{rO}\epsilon\mathrm{n}}-1+V_{\mathrm{on}}\right)^2 + \left(V_{C\mathrm{rP}\epsilon\mathrm{n}}-1+V_{\mathrm{on}}\right)^2. \tag{45}$$

If $\Delta I_{Lr\mathrm{P}\epsilon\mathrm{n}}^2$ is positive, the LLC converter is in NOP mode. In the OPO mode, $\Delta I_{Lr\mathrm{P}\epsilon\mathrm{n}}^2$ is negative.

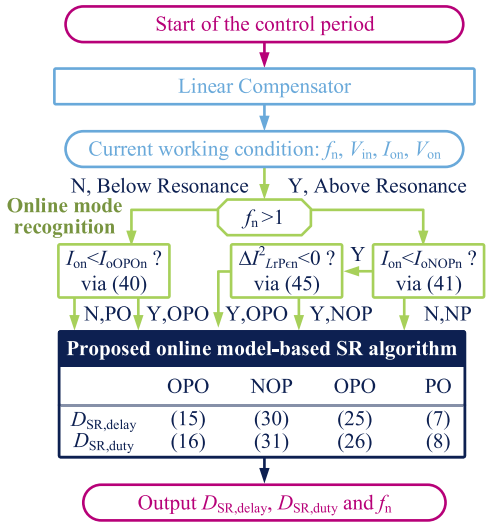

Fig. 9. Flowchart of the proposed STDA-based SR scheme. ABR and BBR denote for above-resonance region and below-resonance region, respectively.

III. Proposed STDA-Based SR Strategy

A. Principle of the Proposed STDA-Based SR Strategy

Based on the analysis in Section II, a novel STDA-based online SR strategy embedded with real-time operation mode recognition algorithm and online SR timing algorithm is proposed in this article. The flowchart of the proposed STDA-based SR scheme is shown in Fig. 9. First, the switching frequency is compared with the resonant frequency to determine whether the operating point is in the below-resonance or above-resonance region. Then, different criteria are used to recognize the operation mode of the LLC converter, as analyzed in Section II-F. In different operation mode, the appropriate expression is carried out to derive the ideal SR MOSFET duty delay $D_{\mathrm{SR,delay}}$ and duty cycle $D_{\mathrm{SR,duty}}$. The SR gate drive signal will be regulated through $D_{\mathrm{SR,delay}}$, $D_{\mathrm{SR,duty}}$, and f_{n}.

Notably, the trigonometric function can be implemented through a simple 1-D lookup list, which is independent of the LLC converter circuit parameters and requires minimal MCU storage space. In addition, no HF signal is required in the proposed SR strategy, making it suitable for cost-sensitive applications.

Moreover, with the online operation mode recognition algorithm, the operation mode can be identified in real time, and appropriate model can be adopted to obtain ideal SR timing.

B. Accuracy Analysis

The accuracy of the algorithm in the proposed SR strategy is evaluated through simulation with the circuit specification listed in Table IV. Fig. 10 illustrates the duty cycle $D_{\mathrm{SR,duty}}$ and duty delay $D_{\mathrm{SR,delay}}$ of SR MOSFET in the below-resonance region in simulation and calculation. The proposed algorithm demonstrates good accordance with the simulation result in the below-resonance region. The averaged error of the duty cycle and duty delay in the below-resonance region are 0.6% and

TABLE III
IMPACT OF THE RESONANT CIRCUIT PARAMETER ERROR ON THE PROPOSED SR STRATEGY

Tolerance	Above Resonance Region		Below Resonance Region	
	$D_{\mathrm{SR,duty}}$	$D_{\mathrm{SR,delay}}$	$D_{\mathrm{SR,duty}}$	$D_{\mathrm{SR,delay}}$
$+10\%L_{\mathrm{m}}$	+3.9%	+3.7%	+0.8%	-1.9%
$+5\%L_{\mathrm{m}}$	+1.8%	+1.8%	+0.4%	-0.9%
$-5\%L_{\mathrm{m}}$	-2.0%	-1.9%	-0.4%	+1.0%
$-10\%L_{\mathrm{m}}$	-4.2%	-4.3%	-0.9%	+2.0%
$+10\%L_{\mathrm{r}}$	-5.5%	+6.7%	+5.5%	+2.9%
$+5\%L_{\mathrm{r}}$	-2.7%	+3.2%	+2.8%	+1.5%
$-5\%L_{\mathrm{r}}$	+2.3%	-3.5%	-2.8%	-1.5%
$-10\%L_{\mathrm{r}}$	+4.5%	-7.4%	-5.7%	-3.2%
$+10\%C_{\mathrm{r}}$	-2.3%	+3.2%	+5.9%	+3.0%
$+5\%C_{\mathrm{r}}$	-1.1%	+1.6%	+2.9%	+1.5%
$-5\%C_{\mathrm{r}}$	+1.0%	-1.5%	-3.0%	-1.5%
$-10\%C_{\mathrm{r}}$	+2.1%	-3.2%	-6.3%	-3.2%

TABLE IV
SPECIFICATION OF THE PROTOTYPE

Item	Value
Operation settings	V_{in}: 400V, V_{o}: 280V-420V, I_{omax}: 16A
Switches Q_1-Q_4, S_1-S_4	UF3C065040K4S, Dead time: 200ns Body diode forward voltage: V_{SD} = 1.5V@I_{D} = 20A, T_{J} = 25°C
Transformer T	Turns ratio n: 12 : 10 Magnetizing inductor L_{m}: 80μH Primary side winding: 12 turns, single litz wire 0.1mm×500strands Secondary side winding: 10 turns, single litz wire 0.1mm×600strands
Resonant inductor L_{r}	Inductance: 14.3μH Winding: 9 turns, single litz wire 0.05mm×2500strands
Resonant capacitor C_{r}	17×5nF in parallel
Output filter capacitor C_{o}	3×4.7uF in parallel
MCU	SPC58nN84E7 (100MHz mode)
Resonant Frequency f_{r}	146kHz
Switching Frequency f_{s}	100kHz - 205kHz

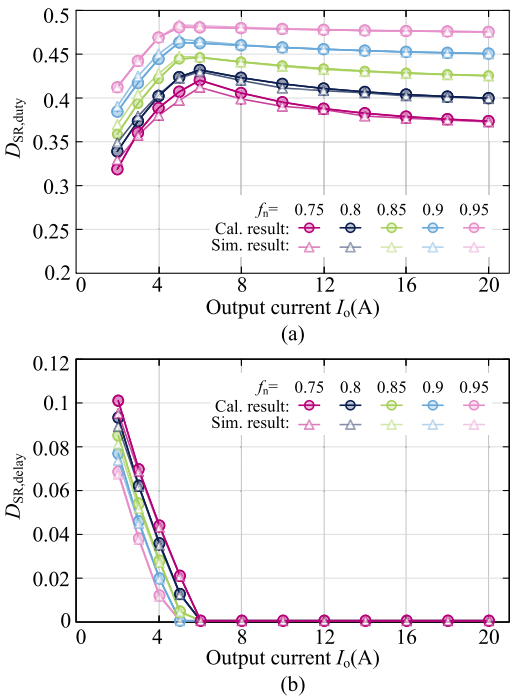

Fig. 10. (a) Duty cycle $D_{\mathrm{SR,duty}}$ and (b) duty delay $D_{\mathrm{SR,delay}}$ of SR MOSFET in the below-resonance region in simulation and calculation.

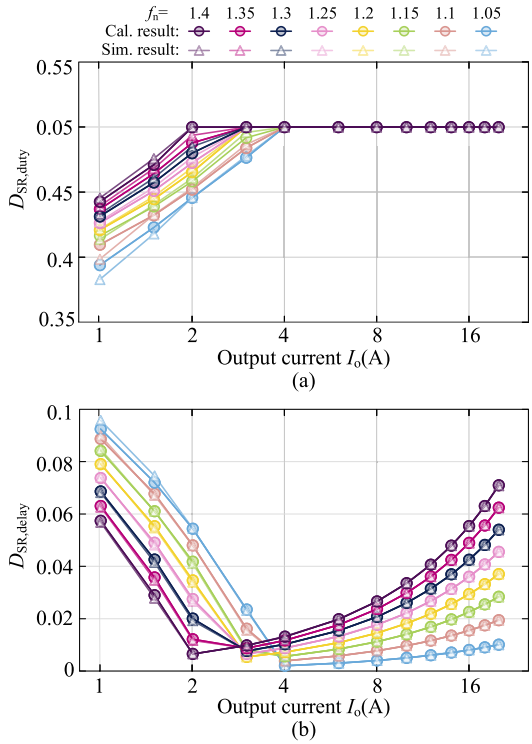

Fig. 11. (a) Duty cycle $D_{\mathrm{SR,duty}}$ and (b) duty delay $D_{\mathrm{SR,delay}}$ of SR MOSFET in the above-resonance region in simulation and calculation.

0.5%, respectively. The maximum error of the duty cycle and duty delay in the below-resonance region occur under light load condition at $f_{\mathrm{n}} = 0.75$, with values of 3.0% and 3.1%, respectively. The proposed algorithm also exhibits high accuracy in the above-resonance region. The average error of the duty cycle and duty delay in the above-resonance region are 0.1% and 0.5%, respectively. The maximum error for the duty cycle in the above-resonance region is 3.0%, which lies in the light load condition at $f_{\mathrm{n}} = 1.05$. The maximum error of the duty delay in the above-resonance region is 2.6%, which lies in the light load condition at $f_{\mathrm{n}} = 1.4$.

The comparison between the duty cycle obtained from the proposed algorithm and the existing algorithms in the below-resonance region is depicted in Fig. 12(a). It is shown that the proposed algorithm exhibits superior accuracy across the entire load range. While the algorithm in [16] shows good accordance with the simulation result, it introduces an extra SR conduction period under light load conditions, potentially leading to additional reactive current. The comparison between the duty delay of the proposed algorithm and the existing algorithms in the above-resonance region is illustrated in Fig. 12(b). It can be found that the result from the algorithm in [16] exhibits huge error compared with the simulation result as the inappropriate model is adopted. Notably, the duty delay in the below-resonance region and the duty cycle in the above-resonance region is not available in other online SR strategy due to the limited operation range, the comparison of these gate signals is not discussed.

Fig. 13 illustrates the operation boundary between the simulation and the proposed boundary recognition algorithm. It can

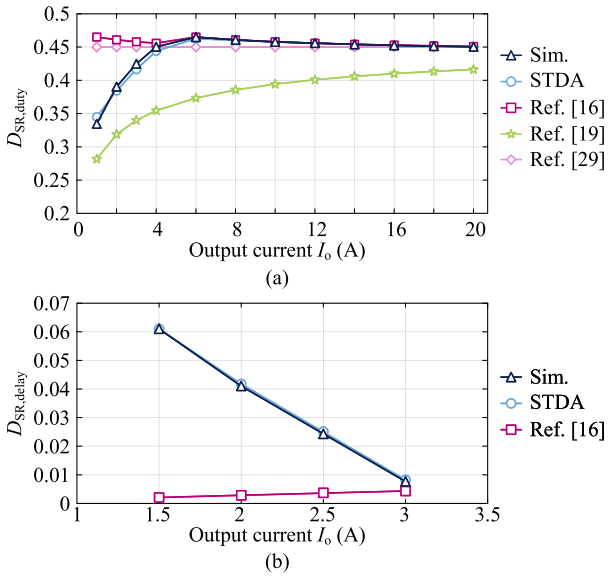

Fig. 12. Comparison between (a) the duty cycle in the below-resonance region and (b) the duty delay in the above-resonance region of different SR strategy at $f_n = 0.9$.

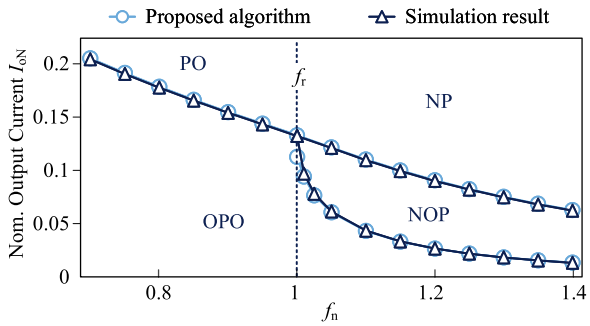

Fig. 13. Comparison between the proposed operation mode boundary algorithm and simulation.

be found that result of the algorithm proposed in this article is identical with the simulation result in the PO/OPO and NP/NOP boundaries. Although approximation is performed in the derivation process of NOP/OPO boundary, the calculated result shows excellent accuracy compared with the simulation result.

C. Component Tolerance

In practical operation, resonant parameter shifts with time and temperature, which may affect the performance of model-based SR schemes. The influence of resonant parameter offset on SR timing in the proposed SR strategy in both below- and above-resonance region are listed, as in Table III. The offset of $D_{\mathrm{SR,delay}}$ in above-resonance region and $D_{\mathrm{SR,duty}}$ in below-resonance region are calculated by averaging the estimation errors obtained under ten load points divided equally from full load to no load at different switching frequencies. As $D_{\mathrm{SR,duty}}$ and $D_{\mathrm{SR,delay}}$ are constant in NP and PO mode, respectively, the offset of $D_{\mathrm{SR,duty}}$ in above-resonance region and $D_{\mathrm{SR,delay}}$ in below-resonance region are calculated by averaging the estimation errors obtained under the load at the PO/OPO boundary and NP/NOP boundary and half of the boundary load at different switching frequencies.

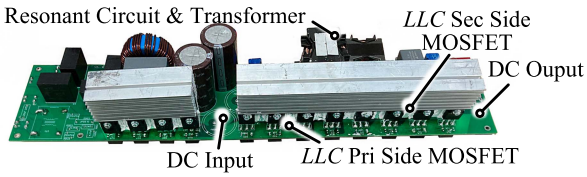

Fig. 14. Prototype of LLC converter.

The error of magnetizing inductor L_{m} is positively correlated with $D_{\mathrm{SR,duty}}$ and $D_{\mathrm{SR,delay}}$ in the above-resonance region and $D_{\mathrm{SR,duty}}$ in the below-resonance region, and negatively correlated with $D_{\mathrm{SR,delay}}$ in the below-resonance region. The error of resonant inductor L_{r} and resonant capacitor C_{r} are both positively correlated with $D_{\mathrm{SR,delay}}$ in the above-resonance region, and $D_{\mathrm{SR,duty}}$ and $D_{\mathrm{SR,delay}}$ in the below-resonance region, and negatively correlated with $D_{\mathrm{SR,duty}}$ in the above-resonance region.

The deviation of L_{r} exhibits the greatest impact on $D_{\mathrm{SR,duty}}$ and $D_{\mathrm{SR,delay}}$ in the above-resonance region. An error of 10% in L_{r} will lead to a error of –5.5% in delay cycle and +6.7% in duty delay. In the below-resonance region, the deviation of C_{r} exhibits the greatest impact on $D_{\mathrm{SR,duty}}$ and $D_{\mathrm{SR,delay}}$. An error of 10% in C_{r} will lead to a error of +5.9% in delay cycle and +3.0% in duty delay.

Thanks to advancements in passive device manufacturing technology, the drift of resonant components has now been reduced to acceptable levels. For example, multilayer ceramic chip capacitors, which are frequently adopted as the resonant capacitors, exhibit minimal temperature-induced variations (for temperature characteristic of C0G, less than 0.05% per 100) [31]. Similarly, the variation in resonant inductor and magnetizing inductor can be maintained within 3% under typical temperature changes [32]. As a result, even at the maximum drift of resonant components, analysis shows that this would lead to only a 2% error in the gate signal duty cycle (delay).

IV. Experiment Result

To validate the principle of the proposed STDA-based SR scheme for the LLC converter, the prototype and experimental setup are shown in Fig. 14, whose topology is identical to Fig. 2. The specifications of the prototype are shown in Table IV.

A. Steady State Performance

Fig. 15(a)–(d) shows the key waveform of LLC converter in PO mode, OPO mode, NP mode, and NOP mode, respectively. As shown in Fig. 15, the SR MOSFETs turn-OFF in the O state; turn-ON in the P state; and turn-ON during the opposite half switching cycle in the N state, which are identical with the operation principle, as in Table II. In practical operation, due to the mandatory existence of dead time, the SR MOSFETs turn-OFF in slight advance in the NP mode as illustrated in Fig. 15(c). The timing of SR MOSFET driver activation matches the time period when there is current in the drain-source channel of SR MOSFET

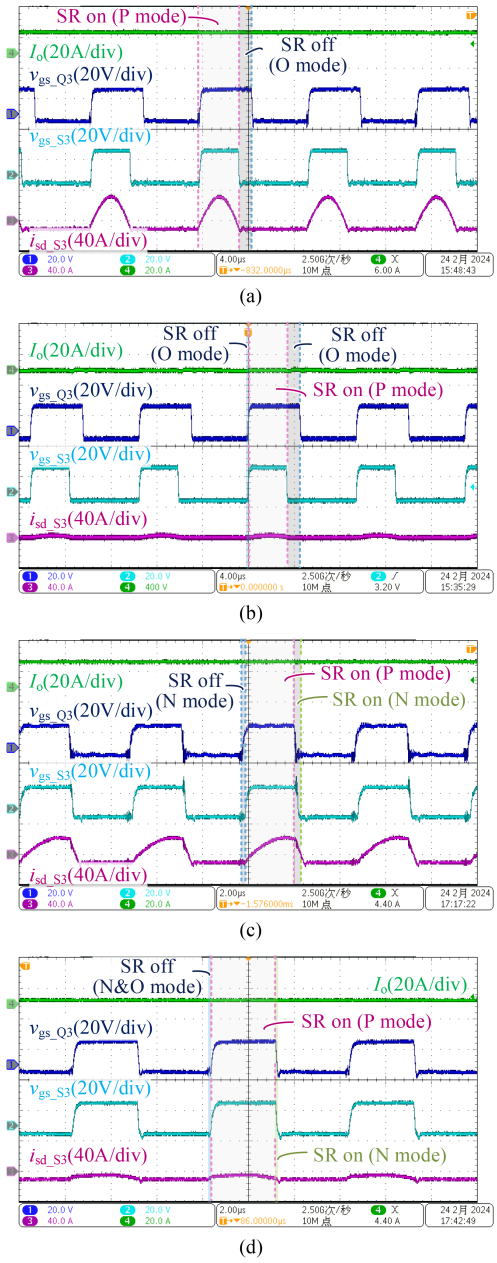

Fig. 15. Key waveform of the prototype in (a) PO mode, (b) OPO mode, (c) NP mode, and (d) NOP mode.

$i_{\mathrm{sd\_S3}}$, which indicates that the SR gate drive signal exhibits good accordance with the ideal conduction timing. It should be noted that Rogowski coil is adapted to measure $i_{\mathrm{sd\_S3}}$, thus a offset in the $i_{\mathrm{sd\_S3}}$ occurs in the waveform. The runtime of the proposed SR timing algorithm in PO mode, OPO mode, NP mode, and NOP mode are 2.24, 3.6, 1.58, and 1.06 us, respectively, which take less than 5% of the control cycle when the control frequency is 10 kHz.

B. Dynamic Performance

Load transition are performed to validate the dynamic performance of the proposed STDA-based SR strategy, and to evaluate its accuracy under different load. Fig. 16(a)–(d) shows the key waveform of the LLC converter with the proposed SR control strategy when the output current switches from 16 to 1 A in the above-resonance region around $f_{\mathrm{n}} = 1.1$, 1.2, 1.3, and 1.4, respectively. It can be found in the zoomed-in view that the proposed SR control can regulate the SR MOSFET gate signal with a high accuracy at different load in the dynamic process. The SR MOSFET gate drive signal is in accordance with the operation principle as listed in Table II. The online operation recognition strategy is also verified at $f_{\mathrm{n}} = 1.3$ and 1.4. It can be found in Fig. 16(c) and (d) that the SR MOSFETs are activated in both NP and NOP mode, and turn-OFF when the OPO mode is detected when the output current is 0.6 and 0.4 A, where the normalized switching frequency f_{n} is around 1.3 and 1.4, respectively.

Fig. 17(a)–(c) illustrates the key waveform of the LLC converter utilizing the proposed STDA-based SR control strategy when the output current transitions from 16 to 1 A in the below-resonance region around $f_{\mathrm{n}} = 0.7$, 0.8, 0.9, respectively. The SR MOSFETs are activated in both PO and OPO mode. The zoomed-in view in Fig. 17 demonstrates that the proposed SR control strategy can precisely regulate the SR MOSFET gate signal across different loads during dynamic transitions. Furthermore, the mode recognition is achieved with high precision.

Figs. 18 and 19 show the key waveform of the LLC converter with the proposed STDA-based SR control strategy during sudden load transition with extremely high load changing rate. In the below-resonance region scenario, the input voltage is 200 V; the reference output voltage is 180 V; the output current switches between 2 and 8 A. In the above-resonance region scenario, the input voltage is 200 V; the reference output voltage is 160 V; the output current switches between 3 and 7 A. In the below-resonance region, almost no mismatch is observed during the load step-down condition as shown in Fig. 18(b), because the SR gate signal is less sensitive to load variation in the below-resonance region. Despite some SR gate signal mismatches during the transient process, the system maintains stability after the load transition. These mismatches occur because the controller cannot promptly sample the operation condition of the LLC converter. The system remains stable during load transitions because the SR strategy can accurately regulate the SR gate signal after the transient process, even though the brief SR gate signal mismatch causes additional reactive current circulation during the load transition. It should be noted that if the load switching amplitude is too large, there will be a risk of instability in the converter. To mitigate this risk, the output current of each control cycle can be sampled and compared with that in the last cycle. When a large load transient occurs, the SR controller can be paused until the transient process ends.

Fig. 17(a)–(c) illustrates the key waveform of the LLC converter utilizing the proposed STDA-based SR control strategy when the reference output current transitions from 16 to 1 A in the below-resonance region around $f_{\mathrm{n}} = 0.7$, 0.8, 0.9, respectively. The SR MOSFETs are activated in both PO and OPO mode. The zoomed-in view in Fig. 17 demonstrates that the proposed SR control strategy can precisely regulate the SR MOSFET gate signal across different loads during dynamic transitions. Furthermore, the mode recognition is achieved with high precision.

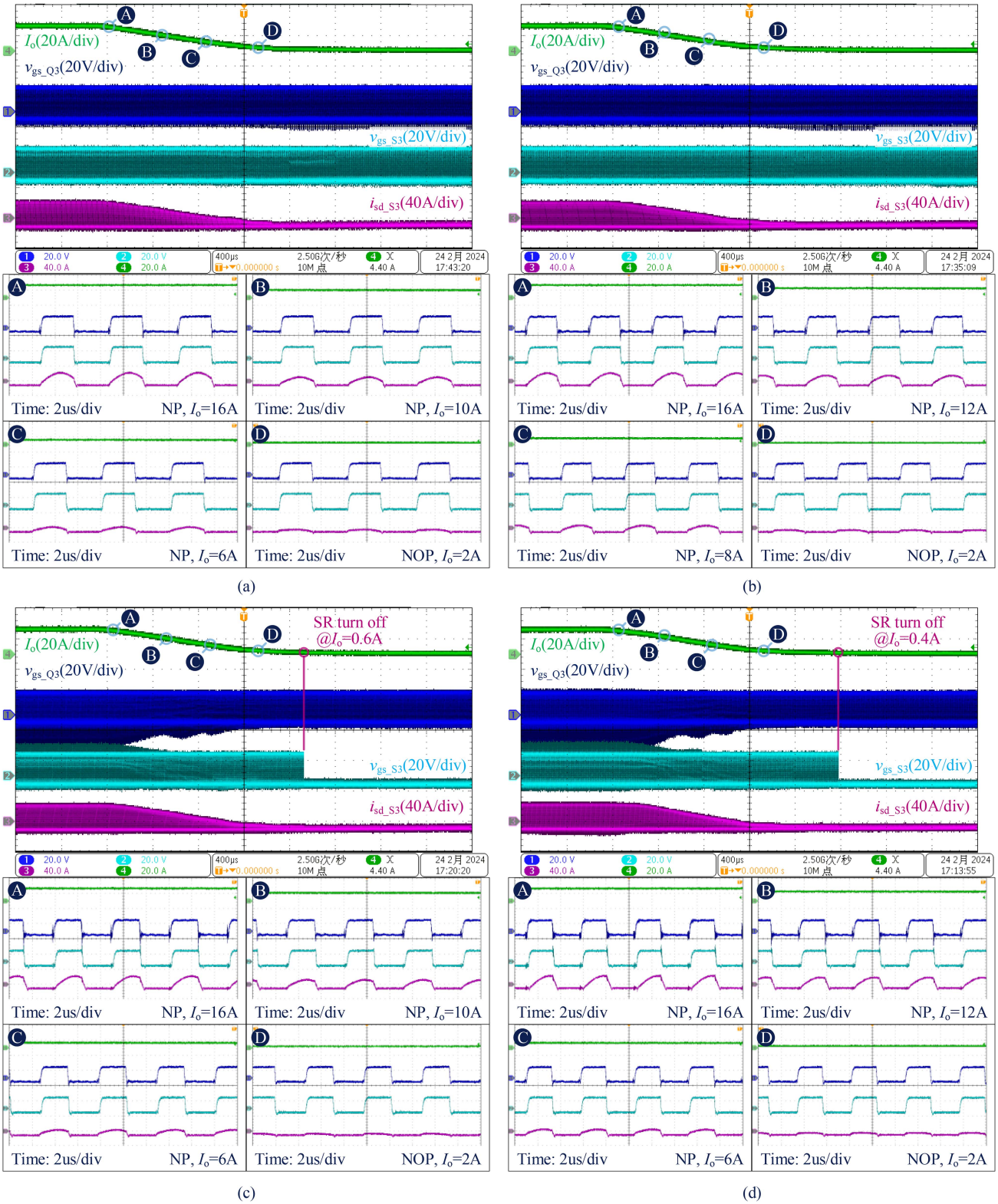

Fig. 16. Key waveform of the prototype when the output current changing from 16 to 0 A and the zoomed-in view (a) around $f_n = 1.1$, (b) around $f_n = 1.2$, (c) around $f_n = 1.3$, and (d) around $f_n = 1.4$.

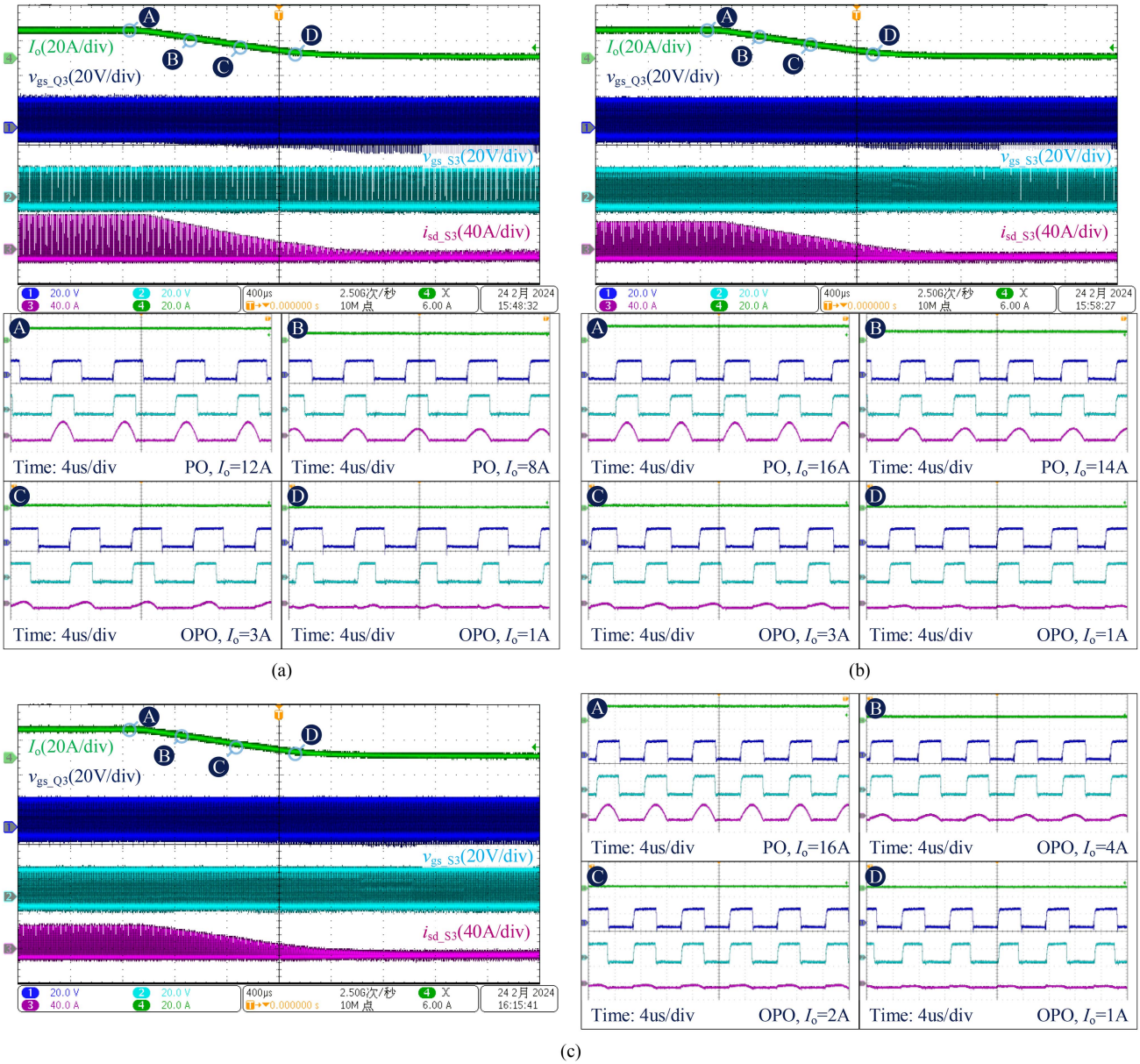

Fig. 17. Key waveform of the prototype when the output current changing from 16 to 0 A and the zoomed-in view (a) around $f_n = 0.7$, (b) around $f_n = 0.8$, and (c) around $f_n = 0.9$.

C. *Efficiency of the Prototype*

Fig. 20 compares the efficiency of the prototype employing the proposed STDA-based SR scheme and that of the existing model-based SR scheme discussed in [16]. The results indicate that the prototype with the proposed SR scheme achieves a rated efficiency of 97.8%. The efficiency improvement with the proposed SR strategy is not substantial under heavy load conditions, because both the proposed STDA-based SR scheme and the existing model-based SR scheme discussed in [16] shows good accuracy of the SR timing. However, there is a notable efficiency enhancement of 0.34% at 40% load in the below-resonance region, translating to a reduced power loss of approximately 10 W. The significant loss reduction is due to the fact that the SR scheme in [16] is not valid under light load conditions, i.e., OPO and NOP mode, because of the existence of the extra O state. To be specific, the secondary side MOSFET with the SR scheme in [16] will be kept deactivated under light load condition to prevent the unintentional turn-ON in the extra O state, and the secondary side current only flows through the reverse diode of the secondary side MOSFET, leading to higher conduction loss. The loss reduction occurs under lighter load conditions when the output voltage is 330 and 300 V than 420 V. This is because that the converter leaves PO mode and NP mode at a lower output current in a lower voltage gain, which is identical with the result in the mode distribution in Fig. 13.

TABLE V
COMPARISON BETWEEN THE PROPOSED SR SCHEME AND OTHER MODEL-BASED SR SCHEME

Item	Theoretical Model	Online Calculation	Frequency Range	Light Load Recognition	Available Operation Mode
Ref. [19], [20]	Modified FHA	Yes	Full Range	No	P, PO and NP
Ref. [21]	Modified FHA	Fitting Curve	Full Range	No	P, PO and NP
Ref. [22]	Accurate TDA	Fitting Curve	Full Range	Yes	P, OPO, PO and NP
Ref. [23]	Accurate TDA	Fitting Curve	BRR	Yes	PO and OPO
Ref. [24]	Accurate TDA	Fitting Curve	BRR	No	PO
Ref. [25]	Deep Learning	Fitting Curve	Full Range	No	P, OPO, PO, NP and NOP
Ref. [26]	Simplified TDA	Yes	Resonant Point	Yes	P and OPO
Ref. [27]	Simplified TDA	Yes	BRR	No	PO
Ref. [33]	Simplified TDA	Yes	Full Range	No	PO and NP
Ref. [16]	Simplified SPA	Yes	Full Range	Yes	P, PO and NP
This work	Simplified TDM	Yes	Full Range	Yes	P, OPO, PO, NP and NOP

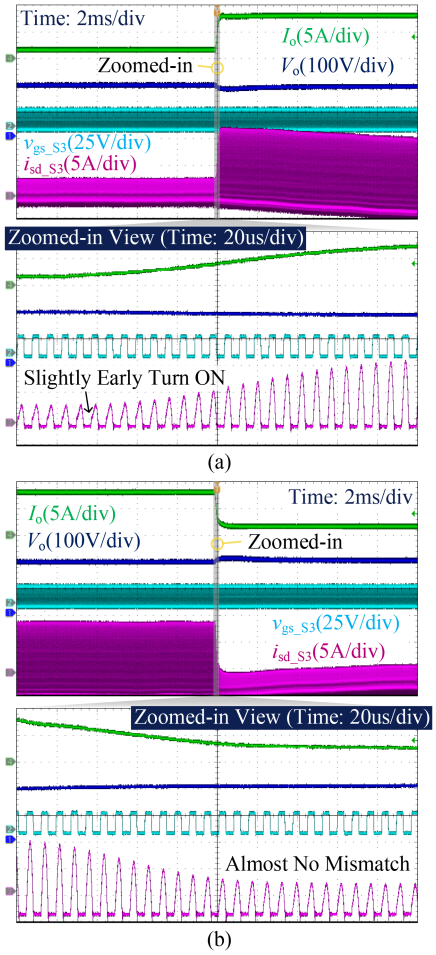

Fig. 18. Key waveform of the prototype under below-resonance region when output current (a) steps up and (b) steps down with extremely high changing rate and the zoomed-in view.

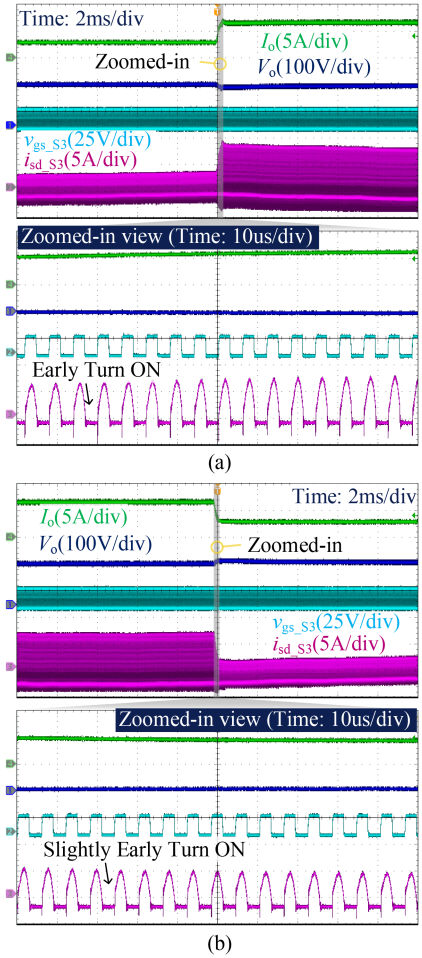

Fig. 19. Key waveform of the prototype under above-resonance region when output current (a) steps up and (b) steps down with extremely high changing rate and the zoomed-in view.

Fig. 21 illustrates the loss distribution of the prototype in Fig. 20 when implementing the proposed STDA-based SR scheme and the existing model-based SR scheme from [16]. This analysis is conducted under conditions of an input voltage of 400 V and an output voltage of 420 V at both full load and 40% load. It can be found that the loss distribution is similar at full load condition. The SR strategy in [16] exhibits an extra SR conduction loss of 10 W at 40% load due to the deactivation of the SR MOSFETs.

D. Comparison With Other SR Strategy and Prospect

A comparison between the existing model-based SR schemes for both LLC converter and $CLLC$ converter is detailed in Table V, where BRR refers to below-resonance region. The available operation range of different online SR strategies is depicted as in Fig. 22. To sum up, the proposed SR strategy can achieve online SR timing calculation, which has better scalability compared to SR algorithms based on lookup tables,

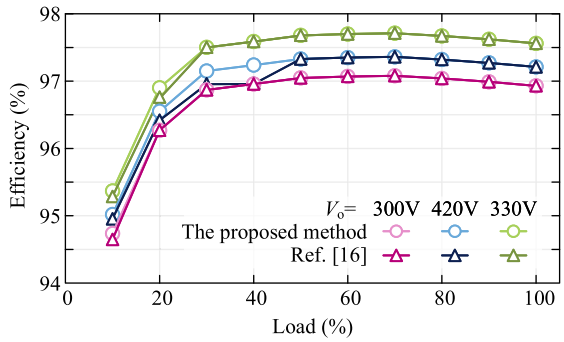

Fig. 20. Efficiency of the prototype with the proposed STDA-based SR scheme and the existing model-based SR scheme in [16].

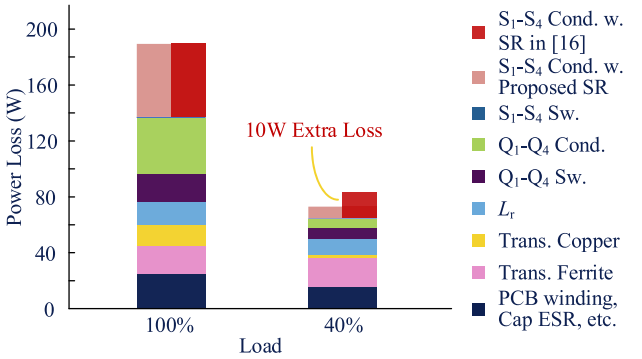

Fig. 21. Loss distribution of the prototype with the proposed STDA-based SR scheme and the existing model-based SR scheme in [16].

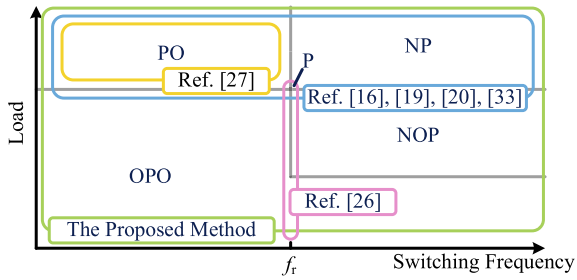

Fig. 22. Comparison between the available operation range of different online SR strategy.

and does not require excessive MCU memory space. In addition, compared to the existing online SR strategies, the proposed SR strategy can achieve accurate calculation of SR timing for operating conditions across the full switching frequency range and full load range. This not only enables the *LLC* converter to have high efficiency over a wide range, but also ensures that the *LLC* converter can accurately identify different operation modes to prevent reactive current through the SR MOSFET.

However, it should be noted that the analysis in this article ignores the influence of parasitic parameters, where the drain-source equivalent capacitance and dead time of the MOSFET have a significant impact on the accuracy of the SR strategy for the *LLC* converter [34], [35]. In future work, in-depth research about the impact of various parasitic parameters on SR strategies can be conducted on the basis of this article.

V. Conclusion

A novel STDA-based SR strategy for the *LLC* converter is proposed in this article, which is integrated with both online SR timing algorithm and online operation mode recognition algorithm. Different from the existing SR strategy, the proposed STDA SR strategy is effective in real-time over the full switching frequency and load range. Accurate recognition of operation mode can be achieved, and thus the appropriate model can be applied. Only input voltage, output voltage, and output current are sampled in the proposed SR strategy, and thus no extra circuit is required. Both simulation and experiment are performed for validation. The proposed SR strategy exhibits high accuracy in both SR timing prediction and operation mode recognition over the whole frequency and load range. The weighted SR timing accuracy is higher than 99.4%. Compared to the existing model-based strategies, a maximum efficiency improvement is about 0.34%

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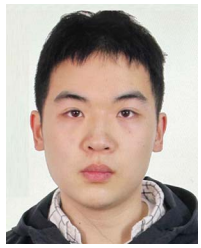

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