Variable-Gain *LLC* Converter With Series–Parallel Hybrid Switch-Controlled Capacitor Network

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***Abstract*—In this article, a variable-gain *LLC* converter with a series–parallel hybrid switch-controlled capacitor network is proposed. By tuning the duty cycle of two controlled switches, the resonant capacitance of converter can be regulated and will slightly shift the parameters of resonant tank. Meanwhile, the added switches will be turned ON at the zero-crossing point of resonant current to guarantee soft switching. Besides, a mode switching scheme based on the modulation of both switching frequency and capacitance is proposed, by which a group of converter voltage gain curves can be obtained and consequently expands its operation range. In order to verify the effectiveness of the proposed design, a 250 W prototype converter is designed and tested under different loads and modes. It shows that the proposed design can retain the characteristics of conventional *LLC* converter, such as soft switching and high efficiency, while it can achieve a wider range of input voltage and a robust control of output voltage against disturbances from input voltage.**

***Index Terms*—*LLC* converter, mode switching, soft switching, switch-controlled capacitor (SCC), variable-gain.**

I. Introduction

NOWADAYS, *LLC* resonant converters have been extensively studied and applied in new energy industry because of their advantages in soft switching, high efficiency, high power density, and wide working ranges [1], [2], [3]. However, factors such as switching frequency, resonant tank, and load will exert influence on the conventional *LLC* converter in the matter of dc gain [4], [5], i.e., either changes in frequency or system parameters, will inevitably affect the output voltage.

In some research works, the chopper unit has been employed as an entry point to tune the switching duty cycle so as to regulate the output voltage. Normally, conventional *LLC* converters' switches are operated with 50% duty cycle complementally and symmetrically. Whereas, the pulsewidth modulation (PWM) technology can simultaneously change the duty cycle of the complementary switches in the same leg and adjust the output voltage [6]. Similarly, a dual-bridge *LLC* converter with fixed frequency and variable duty cycle is proposed in [7], which controls the output voltage by tuning the operation time of half-bridge (HB) and full-bridge (FB) conductions. In addition, an FB *LLC* converter cooperating with boost circuits and asymmetric control is proposed in [8], which benefits from the fixed frequency. However, it will result in an increase in input current ripples. Furthermore, an HB *LLC* converter with a boost–buck circuit is proposed in [9], which can extend the gain range. However, its upper and lower transistors will suffer from asymmetric current stresses which will increase with the system gain.

Besides, the modification of the resonant tank is also an alternative for achieving adjustable gain of *LLC* converter. The resonant tank is composed of several magnetic components [10], [11], [12], [13], [14], [15] and capacitors [16], [17], [18], [19], [20], [21], [22], [23], [24], whose variations will impact on the converter gain and control effects of output voltages. In [10], dual transformers are adopted with an optimization of system design. In [11], a bidirectional switching is added to control the ratios of transformer turns, and the gain ranges can be extended to different degrees. In addition, a LLC converter with split two resonant tanks and control modes to switch between FB and HB is proposed to achieve a scale-down control of system gain [12], [13]. Besides, in [14], a capacitor is connected in series with the magnetic inductor to optimize the inductance value. Since the gain of the system will vary with the change of magnetic components, it will result in a complex analysis in both design and control algorithm. In [15], a current-controlled inductor adjusts the resonant frequency to compensate for the gain imbalance between two phases. This also triggers another line of thought: tuning the system gain via adjustable capacitance.

Switch-controlled capacitors (SCCs) can achieve an adjustable impedance [16] and usually have a quite low switching loss, which can be good alternatives to tune the overall impedance of converters. SCCs are categorized into half-wave and full-wave structures. In [17] and [18], the full-wave and half-wave SCCs are applied to a two-phase interleaved *LLC* converter, in which their duty cycles are tuned slightly to ensure constant or controllable output at either fixed or variable frequencies. Afterward, the SCCs are employed in the *LC* [19], [20] and *LCC* [21], [22] resonant networks, and then a constant output can be achieved by modulating the resonant frequency.

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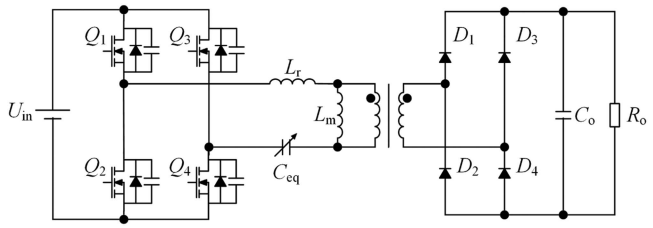

Fig. 1. Proposed *LLC* converter with series–parallel hybrid SCC.

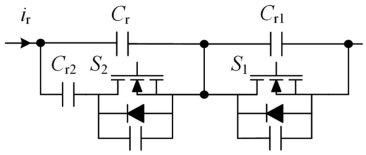

Fig. 2. Structure of series–parallel hybrid SCC.

In [23], a controlled switch is employed to adjust the conduction time of a diode so as to tune the equivalent impedance and stabilize the output voltage. However, an increase in diode loss is inevitable. In [24], a SCC is used to switch the control mode of a wireless power transmission system under two different working frequencies. Overall, the above methods can change the circuit impedance with limited increase in switching loss. However, compared with the rated capacitance, the modulated capacitance can only be larger or smaller, and consequently, the overall tuning range is quite limited.

In this article, an *LLC* converter with a series–parallel hybrid SCC network is proposed. It has four different switching modes and can be selected one or more of them to control according to actual demand. During switching among modes, both switching frequency modulation (SFM) and capacitance modulation are continuously adjustable. Therefore, the voltage gain can be flexibly and robustly adjusted without excessive spikes in resonant current and output voltage. Since controlled switches are turned on at the zero-crossing point of current, the system guarantees zero voltage switching (ZVS) to retain high efficiency. A 250 W prototype *LLC* converter is then fabricated to evaluate the effectiveness of the proposed design, which shows that the output voltage can be well controlled by the tuning of SCC with good stability and anti-interference capability. Meanwhile, a higher system gain can also be achieved.

II. Proposed LLC Converter With Series–Parallel Hybrid SCC

The proposed *LLC* converter a series–parallel hybrid SCCs network is introduced in Fig. 1. L_r and L_m are the resonant inductor and the magnetic inductor, respectively. C_{eq} is the equivalent capacitance, which is replaced by the series–parallel hybrid SCCs network shown in Fig. 2. C_r is the main resonant capacitor, C_{r1} and C_{r2} are the series and parallel SCCs, respectively, and S_1 and S_2 are corresponding controlled switches.

By controlling the states of S_1 and S_2, continuously variable capacitance values can be obtained. According to different

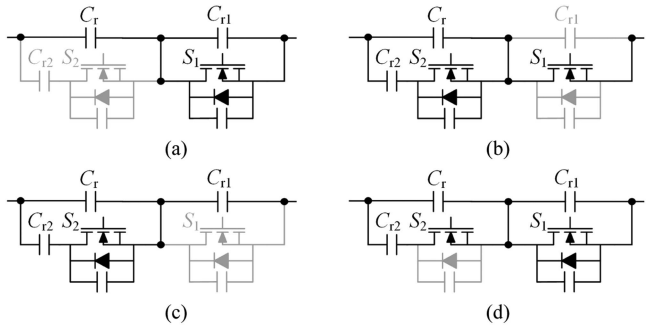

Fig. 3. Four switching modes of series–parallel hybrid SCC. (a), (b), (c), and (d) are Mode 1, Mode 2, Mode 3, and Mode 4, respectively.

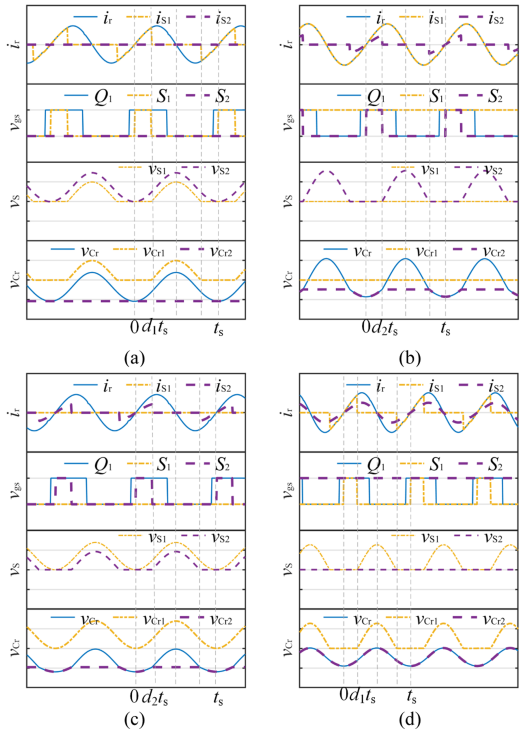

Fig. 4. Typical waveforms of *LLC* converter with series–parallel hybrid SCC. (a), (b), (c), and (d) are Mode 1, Mode 2, Mode 3, and Mode 4, respectively.

switch states, the control strategies for the proposed series–parallel hybrid SCCs are divided into four modes, which are detailed as follows.

Mode 1: S_1 is at switch-state while S_2 is at OFF-state. The C_{r1} and S_1 in parallel will be in series with C_r, which be of a series SCC structure, as shown in Fig. 3(a).When S_1 conducts at the zero-crossing point of i_r, the voltage of C_{r1} is clamped to zero and will be held for a duration, as depicted in Fig. 4(a). The equivalent capacitance of the series SCC C_{scc1} [16] and the hybrid SCC C_{eq1} can be respectively calculated as follows:

$$C_{scc1} = \frac{2C_{r1}}{2 - (4\pi d_1 - \sin 4\pi d_1)/\pi} \tag{1}$$

$$C_{eq1} = \frac{2\pi C_r C_{r1}}{2\pi C_{r1} + (2\pi - 4\pi d_1 + \sin 4\pi d_1)\, C_r} \tag{2}$$

where d_1 is the valid duty cycle of S_1, which overlaps with the positive half cycle of i_r and is within $0 \le d_1 \le 0.5$.

Mode 2: S_2 is at switch-state while S_1 is closed. The series C_{r2} and S_2 will be in parallel with C_r, which is of a parallel SCC topology, as shown in Fig. 3(b). From Fig. 4(b), when S_2 is at OFF-state, the voltage of C_{r2} is clamped to a high potential. The equivalent capacitance of the parallel SCC C_{scc2} and the hybrid SCC C_{eq2} can be expressed as (3). Their calculations are given in Appendix

$$C_{eq2} = C_{scc2} = \frac{2\pi C_r \left(C_r + C_{r2}\right)}{2\pi C_r + \left(2\pi - 4\pi d_2 + \sin 4\pi d_2\right) C_{r2}} \tag{3}$$

where d_2 is the effective duty cycle of S_2 and $0 \le d_2 \le 0.5$.

Mode 3: S_2 is at switch-state while S_1 is OFF. The series parallel SCC in series with C_{r1} will be one of series–parallel hybrid SCC combinations, as shown in Fig. 3(c). From Fig. 4(c), the voltage of C_{r2} is reversed clamped when S_2 is at OFF-state. The equivalent capacitance of the series–parallel hybrid SCC C_{eq3} is given as follows:

$$C_{eq3} = \frac{2\pi C_r C_{r1} \left(C_r + C_{r2}\right)}{2\pi C_r \left(C_r + C_{r1} + C_{r2}\right) + \left(2\pi - 4\pi d_2 + \sin 4\pi d_2\right) C_{r1} C_{r2}}. \tag{4}$$

Mode 4: S_1 is at switch-state while S_2 is closed. The series SCC and the parallel SCC form another series–parallel hybrid SCC combination, as shown in Fig. 3(d). In Fig. 4(d), the voltage of C_{r1} is clamped to zero as well as Mode 1. The equivalent capacitance of this Mode C_{eq4} can be obtained as follows:

$$C_{eq4} = \frac{2\pi C_{r1} \left(C_r + C_{r2}\right)}{2\pi C_{r1} + \left(C_r + C_{r2}\right) \left(2\pi - 4\pi d_1 + \sin 4\pi d_1\right)}. \tag{5}$$

To simplify discussion, the series capacitor C_{r1} and the parallel capacitor C_{r2} are guaranteed to be equal here. Define the capacitance ratio n as the ratio of C_{r1} or C_{r2} to C_r, and m is denoted as the ratio of C_{eq} to C_r.

Fig. 5 shows the distribution curves of m with changing duty cycle when $n < 1$, $n = 1$, and $n > 1$. When $n < 1$ or $n = 1$, Mode 4 can be selected to cover most of the capacitance adjustment range. Similarly, when $n > 1$, Mode 2 can be used as the main working mode. To maximize the impact of SCC, as many modalities as possible will be combined, such as Mode 1 and Mode 2 or Mode 3 and Mode 4. Also, when $n < 1$ or $n = 1$, the former control is more symmetrical, as in (6). When $n > 1$, the latter is better, as (7)

$$\begin{cases} \text{Mode 1} & m \in \left[\frac{n}{n+1}, 1\right] & d_1 \in [0, 0.5] \\ \text{Mode 2} & m \in [1, 1+n] & d_2 \in [0, 0.5] \end{cases}. \tag{6}$$

$$\begin{cases} \text{Mode 3} & m \in \left[\frac{n}{n+1}, \frac{n(1+n)}{1+2n}\right] & d_2 \in [0, 0.5] \\ \text{Mode 4} & m \in \left[\frac{n(1+n)}{1+2n}, 1+n\right] & d_1 \in [0, 0.5] \end{cases}. \tag{7}$$

On top of that, the combination of three modes allows for more accurate control, and it can be divided into the following situations.

When $n < 1$, the method can be easily determined as (8) by ignoring third powers and above terms in the Taylor formula of a sinusoidal function

$$\begin{cases} \text{Mode 3} & m \in \left[\frac{n}{n+1}, \frac{n(1+n)}{1+2n}\right] & d_2 \in [0, 0.5] \\ \text{Mode 1} & m \in \left[\frac{n(1+n)}{1+2n}, 1\right] & d_1 \in \left[\sqrt[3]{\frac{3n^2}{16\pi^2(1+n)}}, 0.5\right] \\ \text{Mode 2} & m \in [1, 1+n] & d_2 \in [0, 0.5]. \end{cases} \tag{8}$$

When $n = 1$, the concrete way can be expressed as follows:

$$\begin{cases} \text{Mode 3} & m \in \left[\frac{n}{n+1}, \frac{n(1+n)}{1+2n}\right] & d_2 \in [0, 0.5] \\ \text{Mode 1} & m \in \left[\frac{n(1+n)}{1+2n}, 1\right] & d_1 \in [0.25, 0.5] \cdot \\ \text{Mode2} & m \in [1, 1+n] & d_2 \in [0, 0.5] \end{cases} \tag{9}$$

When $n > 1$, the combination mode is described as

$$\begin{cases} \text{Mode 1} & m \in \left[\frac{n}{n+1}, 1\right] & d_1 \in [0, 0.5] \\ \text{Mode 3} & m \in \left[1, \frac{n(n+1)}{2n+1}\right] & d_2 \in \left[\sqrt[3]{\frac{3(n+1)}{16\pi^2 n^2}}, 0.5\right] \\ \text{Mode 4} & m \in \left[\frac{n(n+1)}{2n+1}, 1+n\right] & d_1 \in [0, 0.5]. \end{cases} \tag{10}$$

In practice, determine the capacitance value for the specific occasion. In a multi-modular converter system, $n < 1$ is chosen to compensate for device errors and achieve power balance. When input interference of the system is obvious, $n = 1$ can be selected to alleviate negative impacts brought by outside. To ensure sinusoidal of the resonant current, the common practice is to take n up to 1. However, $n > 1$ can be selected on some occasions where the sinusoidal degree of current is not high.

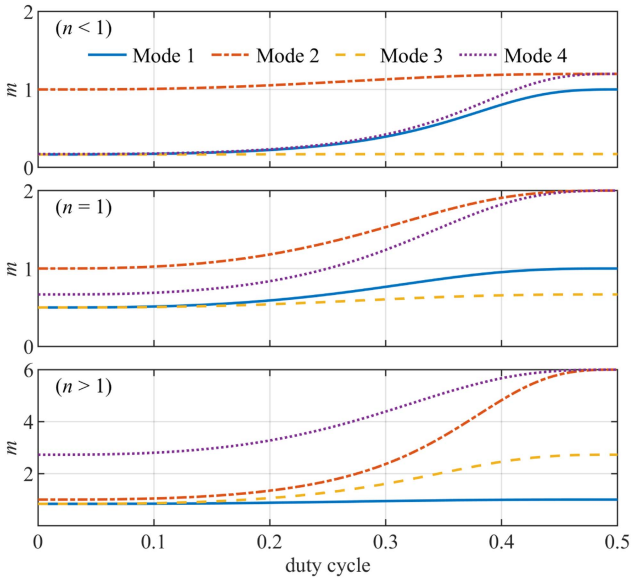

Fig. 5. Distribution curves of m with changing duty cycle.

III. Analysis and Parameter Design of the Proposed *LLC* Converter With Series–Parallel Hybrid SCC

The SFM mode of the proposed *LLC* converter with series–parallel hybrid SCC is similar to that of the conventional LLC converter. Meanwhile, the proposed scheme can also tune the system gain by adjusting the resonant frequency via the series–parallel hybrid SCC. In this chapter, the proposed *LLC* converter

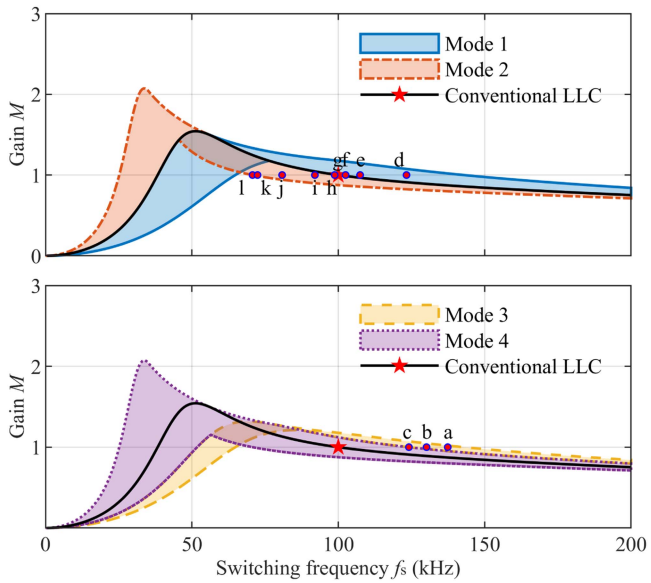

Fig. 6. External envelope diagram of gain curves of LLC converter with series–parallel hybrid SCC and conventional LLC converter.

performance is analyzed by taking three mode combinations with $n = 1$ as an example.

A. Analysis of the Proposed LLC Converter With Series–Parallel Hybrid SCC Under SFM Mode

Since capacitance is affected by the duty cycle of the controlled switch, the resonance frequency of the *LLC* converter with series–parallel hybrid SCC f_r is variable, and the specific formula is given by

$$f_r = \frac{1}{2\pi\sqrt{L_r C_{\text{eq}}}}. \tag{11}$$

The expression of dc gain is written as follows:

$$M = \frac{(m-1)f_n^2}{\sqrt{\left(mf_n^2-1\right)^2 + Q^2(m-1)^2 f_n^2\left(f_n^2-1\right)^2}} \tag{12}$$

where $f_{\text{n}} = f_{\text{s}} / f_{\text{r}}$, $m = (L_{\text{m}} + L_{\text{r}}) / L_{\text{r}}$, $Q = \sqrt{L_r/(C_{eq}^2 R_{eq}^2)}$, $R_{\text{eq}} = 8N^2R_o/\pi^2$. f_{s} is the switching frequency, N is the transformation ratio, and R_{o} is the load resistance.

Fig. 6 shows the gain curve comparison between the *LLC* converter with series–parallel hybrid SCC and the conventional *LLC* converter. The gain curve set of the proposed *LLC* converter in each mode can form an envelope region. The marked star is the resonant operating point of the conventional *LLC* converter. By only changing the capacitance, the operating point can be shifted up and down at a fixed frequency. If the capacitance and switching frequency are tuned, the operating point can move freely within the envelope region. In Mode 2 or Mode 4, it can be shifted to a maximum gain of 1.34 times the original theoretically. In other words, the *LLC* converter with series–parallel hybrid SCC can obtain a higher voltage gain, which is flexible and variable.

B. Realization of Zero Voltage Switch

Assume that the zero-crossing point of resonant current i_{r} from negative to positive is taken as a starting point of one period. The fundamental frequency component of i_{r} is expressed as follows:

$$i_r = I_r \sin(2\pi f_s t) \tag{13}$$

where I_{r} is the peak value of i_{r} and $I_{\text{r}} = \pi \text{MV}_{\text{in}}/(2N^2R_o)$.

Mode 1: S_1 is at switch-state while S_2 is at OFF-state.

Stage 1 [0, d_1t_{s}]: S_1 is turned ON and its voltage is clamp to zero, i.e., $u_{\text{S1}}(d_1t_{\text{s}}) = u_{\text{Cr1}}(d_1t_{\text{s}}) = 0$.

Stage 2 [d_1t_{s}, $0.5t_{\text{s}}$–d_1t_{s}]: S_1 is turned OFF and i_{r} charges the capacitor C_{r1}. The voltage across C_{r1} can be calculated as follows:

$$u_{\text{Cr1}}(0.5t_{\text{s}} - d_1t_{\text{s}}) = u_{\text{Cr1}}(d_1t_{\text{s}}) + \frac{1}{C_{\text{r1}}}\int_{d_1t_{\text{s}}}^{0.5t_{\text{s}}-d_1t_{\text{s}}} i_r(t)dt. \tag{14}$$

Stage 3 [$0.5t_{\text{s}}$–d_1t_{s}, t_{s}–d_1t_{s}]: S_1 is turned OFF. C_{r1} is discharged, which voltage can be obtained as follows:

$$u_{\text{Cr1}}(t_s - d_1t_s) = u_{\text{Cr1}}(0.5t_s - d_1t_s) + \frac{1}{C_{\text{r1}}}\int_{0.5t_s-d_1t_s}^{t_s-d_1t_s} i_r(t)dt = 0. \tag{15}$$

Obviously, the voltage across S_1 is equal to that of C_{r1}, i.e., $u_{\text{S1}}(t_{\text{s}}\text{-}d_1t_{\text{s}}) = u_{\text{Cr1}}(t_{\text{s}}\text{-}d_1t_{\text{s}}) = 0$. It creates ZVS conditions for the controlled switch S_1.

Stage 4 [t_{s}–d_1t_{s}, t_{s}]: the resonant current is negative, and the antiparallel body diode of S_1 starts conducting.

Mode 2: S_2 is at switch-state while S_1 is closed.

Stage 1 [0, d_2t_{s}]: S_2 is turned ON and its voltage is clamp to zero, thus both voltages of C_{r} and C_{r2} are the same, as shown in the following:

$$u_{\text{Cr}}(d_2t_s) = u_{\text{Cr2}}(d_2t_s). \tag{16}$$

Stage 2 [d_2t_{s}, $0.5t_{\text{s}}$–d_2t_{s}]: S_2 is turned OFF and i_{r} charges the capacitor C_{r}. The voltage across C_{r} can be given as follows:

$$u_{\text{Cr}}(0.5t_s - d_2t_s) = u_{\text{Cr}}(d_2t_s) + \frac{1}{C_r}\int_{d_2t_s}^{0.5t_s-d_2t_s} i_r(t)dt. \tag{17}$$

Stage 3 [$0.5t_{\text{s}}$–d_2t_{s}, t_{s}–d_2t_{s}]: S_2 is turned off. The capacitor C_{r} is discharged, which voltage can be written as follows:

$$u_{\text{Cr}}(t_s - d_2t_s) = u_{\text{Cr}}(0.5t_s - d_2t_s) + \frac{1}{C_r}\int_{0.5t_s-d_2t_s}^{t_s-d_2t_s} i_r(t)dt = u_{\text{Cr}}(d_2t_s). \tag{18}$$

Since C_{r2} has no current in Stages 2 and 3, the voltage remains unchanged, as shown in the following:

$$u_{\text{Cr2}}(t_s - d_2t_s) = u_{\text{Cr2}}(d_2t_s). \tag{19}$$

Therefore, the voltage across S_2 at this time is 0. It creates ZVS conditions for the controlled switch S_2.

Stage 4 [t_{s}–d_2t_{s}, t_{s}]: the resonant current is negative, and the antiparallel body diode of S_2 starts conducting.

The rest of the modes are analyzed similarly and hence omitted. From the above analysis, it is clear that the conduction of controlled switches at the point where i_{r} crosses zero is the only necessary condition for the realization of ZVS.

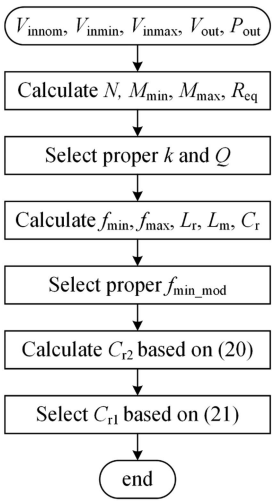

Fig. 7. Process of system parameters determination.

C. System Parameters Determination

The detailed process of design specification is presented in Fig. 7. This process is simple and clearly to determine system parameters. There are two key designs for the proposed *LLC* converter with a series–parallel hybrid SCC network.

One is to ensure that gain regulation can be realized within a certain switching frequency range. Particularly, the resonant state at high gain corresponding operating frequency is desired. Generally, this frequency is larger than the minimum frequency of *LLC* converter $f_{\min}$, avoiding overly wide frequency ranges. However, too large will have no effect. Therefore, it is necessary to select the appropriate frequency for the proposed *LLC* converter design. The minimum frequency that can be modulated capacitance $f_{\min\_\mathrm{mod}}$ affects the maximum $C_{\mathrm{eq,max}}$, like the following:

$$C_{\mathrm{eq,max}} = \frac{1}{4\pi^2 f_{\min\_\mathrm{mod}}^2 L_r}. \tag{20}$$

The other is to undertake ZVS. The function of C_{r1} is to stabilize the output voltage using variable duty cycle with fixed frequency when micro disturbance of input voltage occurs. Meanwhile, it should be safely switch to other modes. In other words, the input impedance of system needs to be maintained in inductive states all the time, i.e.

$$\mathrm{Im} = \frac{2\pi f_s L_m R_{\mathrm{eq}}^2}{4\pi^2 f_s^2 L_m^2 + R_{\mathrm{eq}}^2} + 2\pi f_s L_r - \frac{1}{2\pi f_s C_{\mathrm{eq}}} > 0 \tag{21}$$

where $f_{\mathrm{s}} \in [f_{\min\_\mathrm{mod}}, f_{\mathrm{r}}]$.

D. Selection of Tuning Caps and MOSFETs

The largest transients that cause largest voltages across switches (S_1 and S_2) and tuning caps (C_{r1} and C_{r2}) will occur at three scenarios, viz., capacitor C_{r1} charged by i_r to its maximum value (the first scenario), capacitors C_r and C_{r2} charged or discharged by i_r to the maximum value of $u_{Cr} - u_{Cr2}$(the second scenario), and capacitor C_{r2} charged by i_r to its maximum value (the third scenario) during the positive half cycle. For our prototype converters, according to our analysis by both calculation and simulation, the largest voltages across tuning caps (C_{r1} and C_{r2}) and switches (S_1 and S_2) during the largest transient will be 311.3, 242.0, 311.3, and 487.6 V, respectively. The working condition corresponding to the largest voltage 487.6 V across S_2 can be avoided, and u_{S2} can be reduced to 322.11 V with the same gain and mode and different duty cycles.

In Section III-B, since switches S_1 and S_2 guarantee ZVS in different modes, $u_{S1}(0) = 0$ and $u_{S2}(0) = 0$. Meanwhile, $i_r \propto i_o$ and $i_o \propto V_o$, consequently, the variation trend of i_r is similar to the system's gain. According to (12), when f_n and m are fixed, the voltage gain M and resonant current will increase with C_{eq}.

Scenario 1: When the positive half-cycle resonant current i_r charges C_{r1} to its maximum value, the voltage across S_1 is also at its largest value. It is worth noting that not all modes' resonant currents flow through C_{r1}. The equivalent capacitance $C_{\mathrm{eq,\ max}}$ that i_r flow through C_{r1} occurs at Mode 3 $d_2 = 0.5$. Therefore, the switch S_1 is subjected to the largest voltage condition of $V_{\mathrm{in}} = V_{\mathrm{in13}}, f_n = 1$, $C_{\mathrm{eq,\ max}} = C_{\mathrm{eq3}}(d_2 = 0.5)$ or $V_{\mathrm{in}} = V_{\mathrm{in31}}$, $f_n = f_{n31}$, $C_{\mathrm{eq,\ max}} = C_{\mathrm{eq3}}(d_2 = 0.5)$ at full load [17]. Where V_{in13}, V_{in31}, and f_{n31} are the input voltage of Mode 1 switching to Mode 3, the input voltage of Mode 3 switching to Mode 1 and its normalized frequency, respectively.

S_1 and C_{r1} are connected in parallel so that $u_{Cr1}(t) = u_{S1}(t)$. During positive half cycles, i_r charges C_{r1} from $u_{Cr1}(0) = u_{S1}(0) = 0$ to the peak voltage. The peak voltage across S_1 can be calculated as (22). The two operating parameters of S_1 to undergo the largest voltage are brought into (22) to obtain 200.16 and 222.40 V, respectively. Since the higher harmonics are neglected, the calculated peak voltages will be a little smaller. Simulation analysis of the two conditions withstands 259.8 and 311.3 V, respectively, which gives the design of S_1 and C_{r1} selection to provide a certain reference

$$u_{S_1,\max} = u_{C_{r1},\max} = u_{C_{r1}}(0) + \frac{1}{C_{r1}} \int_0^{0.5t_s} i_r(t)dt = \frac{\mathrm{MV_{in}}}{2N^2 f_s C_{r1} R_o}. \tag{22}$$

Scenario 2: When the positive half-cycle resonant current i_r charges and discharges C_r and C_{r2} so that $u_{Cr} - u_{Cr2}$ is maximum, the voltage across S_2 is also at the largest at this time. When C_{r1} is completely shorted, both C_r and C_{r2} are charged and discharged, or C_r is charged and discharged and C_{r2} is inversely clamped at some time during periods. The voltage across the switch S_2 is $u_{Cr} - u_{Cr2}$, so the latter will have the maximum u_{S2}. The conditions under which switch S_2 is subjected to the largest voltage are $V_{\mathrm{in}} = V_{\mathrm{in,nom}}$, $f_n = 1$, $C_{\mathrm{eq}} = C_{\mathrm{eq2}}(d_2 = 0)$ or $V_{\mathrm{in}} = V_{\mathrm{in,min,orig}}, f_n = f_{n,\mathrm{min,orig}}, C_{\mathrm{eq}} = C_{\mathrm{eq2}}(d_2 = 0)$. Where $V_{\mathrm{in,min,orig}}$ and $f_{n,\mathrm{min,orig}}$ are the minimum input voltage and normalized frequency of the conventional *LLC* converter, respectively.

In Mode 2 $d_2 = 0$, the equivalent capacitance value is C_r. When $t = 0$, $u_{Cr}(0) = -u_{Cr,\ \max}$, $u_{S2}(0) = 0$, so $u_{Cr2}(0) = u_{Cr}(0) - u_{S2}(0) = -u_{Cr,\ \max}$. During positive half cycles, i_r charges C_r from $-u_{Cr,\max}$ to $u_{Cr,\max}$, and hence the peak voltage across C_r can be calculated as (23). Since C_{r2} is clamped, $u_{Cr2}(0.5t_{\mathrm{s}}) = u_{Cr2}(0) = -u_{Cr,\max}$. Hence, the peak voltage across S_2 can be obtained as (24). The two working parameters of S_2 to undergo the largest voltage are brought into (24) to

get 200.16 and 307.95 V, respectively. Simulation analysis of the two conditions withstands 253.3 and 487.6 V. Although the voltage across the switch S_2 is larger at $V_{\text{in}} = V_{\text{in,min,orig}}, f_n = f_{n,\text{min,orig}}$, $C_{\text{eq}} = C_{\text{eq2}}(d_2 = 0)$, this is an avoidable condition. At the same gain Mode 2 $d_2 = 0.2$, the maximum voltage across S_2 is 322.1 V

$$u_{C_r,\max} = u_{C_r}(0.5t_s) = \frac{1}{2C_r}\int_0^{0.5t_s} i_r(t)dt = \frac{MV_{\text{in}}}{4N^2 f_s C_r R_o} \tag{23}$$

$$u_{S_2,\max} = u_{C_r}(0.5t_s) - u_{C_{r2}}(0.5t_s) = \frac{MV_{\text{in}}}{2N^2 f_s C_r R_o}. \tag{24}$$

Scenario 3: When the positive half-cycle resonant current i_r charges C_{r2} to its maximum value, the voltage across C_{r2} is also largest. When C_{r1} is completely shorted, both C_r and C_{r2} are charged and discharged, or C_r is charged and discharged and C_{r2} is inversely clamped at some time during periods. Both of the above scenarios have the potential to maximize u_{Cr2}. The conditions under which C_{r2} is subjected to the largest voltage are $V_{\text{in}} = V_{\text{in,nom}}, f_n = f_{n,\ r2,\ d2\ =\ 0.5}$, $C_{\text{eq}} = C_{\text{eq2}}(d_2 = 0.5)$, $V_{\text{in}} = V_{\text{in,min}}, f_n = f_{n,\text{min}}$, $C_{\text{eq}} = C_{\text{eq2}}(d_2 = 0.5)$, $V_{\text{in}} = V_{\text{in,nom}}$, $f_n = 1$, $C_{\text{eq}} = C_{\text{eq2}}(d_2 = 0)$ or $V_{\text{in}} = V_{\text{in,min,orig}}, f_n = f_{n,\ \text{min,orig}}$, $C_{\text{eq}} = C_{\text{eq2}}(d_2 = 0)$. Where $f_n = f_{n,\ r2,\ d2\ =\ 0.5}$ is the normalized resonant frequency of Mode 2 $d_2 = 0.5$.

In Mode 2 $d_2 = 0$, the equivalent capacitance value is C_r. During positive half cycles, i_r charges C_{r2} from $-u_{Cr2,\max}$ to $u_{Cr2,\max}$, and hence the peak voltage across C_{r2} can be calculated as (25). In Mode 2 $d_2 = 0.5$, C_r and C_{r2} are connected in parallel, and hence the peak voltage across C_{r2} can be obtained as (26). The four working parameters of C_{r2} to undergo the largest voltage are brought into (25) and (26) to get 71.49, 114.14, 100.08, and 153.98 V, respectively. Simulation analysis of the four conditions withstands 105.2, 199.4, 125.7, and 242.0 V, which gives the design of C_{r2} selection to provide a certain reference

$$u_{C_{r2},\max} = u_{C_r,\max} = \frac{MV_{\text{in}}}{4N^2 f_s C_r R_o} \tag{25}$$

$$u_{C_{r2},\max} = \frac{1}{2C_{r2}}\int_0^{0.5t_s} \frac{C_{r2}}{C_r + C_{r2}} i_r(t)dt = \frac{MV_{\text{in}}}{8N^2 f_s C_{r2} R_o} \tag{26}$$

Section III-B points out that the conduction of controlled switches at the point that i_r crosses zero is the only necessary condition for achieving the ZVS. In Stage 4 [t_s–d_1t_s, t_s] of Mode 1 and Mode 4, the antiparallel body diode of S_1 starts conducting, i.e., S_1's voltage is clamped to zero. To be more precise, $u_{S1}(0) = 0$ and $du_{S1}(0)/dt = 0$. In Mode 1, $i_r(0) = C_r du_{Cr}(0)/dt = C_r d[u_{Cr2}(0) + u_{S2}(0)]/dt = 0$ and C_{r2} is clamped, so $du_{S2}(0)/dt = 0$. In Mode 4, S_2 is at switch-state and then $du_{S2}(0)/dt = 0$. The rest of the modes are analyzed similarly. In Mode 2 and Mode 3, $u_{S2}(0) = 0$ and $du_{S2}(0)/dt = 0$. In Mode 2, S_1 is at switch-state and then $du_{S1}(0)/dt = 0$. In Mode 3, $i_r(0) = C_{r1} du_{Cr1}(0)/dt = 0$ and $u_{Cr1}(0) = u_{S1}(0)$, so $du_{S1}(0)/dt = 0$. According to $i_{Sx}(0) = du_{Sx}(0)/dt$ (x = 1, 2), controlled switches will not result in current transient disturbances at any moment of conduction. In summary, the conduction of controlled switches S_1 and S_2 will not produce large current transient disturbances regardless of the system's working mode. However, the system's measurement accuracy of currents and the control delay will produce slight current transient disturbances in the resonant current, which is quite negligible. Therefore, the selection principle of current ratings of switches S_1 and S_2 will be similar to that of conventional *LLC* converter.

E. Loss Analysis

The total power losses of *LLC* converter mainly come from: driving, conduction, and turn-OFF loss of MOSFET, core and copper losses of transformer, and loss of rectifier diode [25], [26]. Assuming the temperature influence is neglected, several simple approximation formulas can be derived to compute power losses.

1) Driving Loss of MOSFET: The driving loss is caused from charging and discharging the capacitor between the gate and source of MOSFET. The driving loss of MOSFETs is given by

$$P_{\text{drive}} = \frac{1}{2} C_{iss} \Delta V_{gs}^2 f_s \tag{27}$$

where C_{iss} is the input parasitic capacitance of MOSFET, and ΔV_{gs} is the driving voltage difference.

Thus, the driving loss of conventional I converter $P_{\text{drive\_LLC}}$ is $4P_{\text{drive}}$, while the proposed *LLC* converter with a series–parallel hybrid SCC network has one more driving loss.

2) Conduction Loss of MOSFET: The conduction losses in MOSFET can be calculated as (28) using the drain–source resistance (R_{ds})

$$P_{\text{MOS}} = \frac{1}{t_s}\int_0^{t_s} i_r^2(t) R_{ds} dt. \tag{28}$$

The conduction losses of antiparallel diodes can be estimated by diode forward voltage drop (V_{DF}), which is given by

$$P_{\text{anti\_diode}} = V_{DF} i_{r\_\text{rms}} t_{\text{body(on)}} f_s \tag{29}$$

where $t_{\text{body(on)}}$ is the conduction time of body diode and $i_{\text{r\_rms}}$ is the RMS of resonant current.

There are always two switches on in the conventional *LLC* converter, so its conduction loss is $2P_{\text{MOS}} + 4P_{\text{anti\_diode}}$. However, the conduction loss of the proposed *LLC* converter with a series–parallel hybrid SCC network is closely related to the duty cycle. For example, when the system enters Modes 1 or 3, the conduction loss of P_{c1} or P_{c3} relating to the controlled switch S_1 or S_2 is

$$P_{c1} = 2P_{\text{MOS}} + \frac{1}{d_1 t_s}\int_0^{d_1 t_s} i_r^2(t) R_{ds} dt \tag{30}$$

$$P_{c3} = 2P_{\text{MOS}} + \frac{1}{d_2 t_s}\int_0^{d_2 t_s} i_r^2(t) R_{ds} dt. \tag{31}$$

When the system enters Modes 2 or 4, one controlled switch is always on state. At this time, the conduction loss of P_{c2} or P_{c4} is

$$P_{c2} = 3P_{\text{MOS}} + \frac{1}{d_2 t_s}\int_0^{d_2 t_s} i_r^2(t) R_{ds} dt \tag{32}$$

$$P_{c4} = 3P_{\text{MOS}} + \frac{1}{d_1 t_s}\int_0^{d_1 t_s} i_r^2(t) R_{ds} dt. \tag{33}$$

3) Turn-off Loss of MOSFET: ZVS is considered for both *LLC* converters in the whole range of voltage. Therefore, only the turn-OFF loss of switches is considered and can be calculated by

$$P_{\text{turn - off}} = \int_0^{t_{\text{dis}}} v_{ds}(\tau) i_{ds}(\tau)\, d\tau \tag{34}$$

where $v_{\text{ds}}(t)$ is the drain–source voltage of MOSFET, $i_{\text{ds}}(t)$ is the drain current in the process of turn-OFF, and t_{dis} is the discharging time of two drain–source capacitors from V_{in} to 0 V.

According to working situations from Mode 1 to Mode 4, it can be found that the turn-OFF loss of the controlled switch is very small and can be ignored.

4) Core and Copper Losses of Transformer: The core loss of the transformer is generally calculated by Steinmetz empirical formula, which empirical formula is as follows:

$$P_{\text{core}} = K_h \times f_s^{\alpha} \times B_m^{\beta} \times V_{\text{core}} \tag{35}$$

where B_{m} is the peak magnetic induction intensity, V_{core} is the volume of the transformer, and K_{h}, α, and β are empirical parameters.

The copper loss is related to the current passing through the winding and is calculated as (36) using an ac resistance (R_{ac})

$$P_{\text{copper}} = i_{r\_\text{rms}}^2 R_{\text{ac\_pri}} + i_{\text{sec\_rms}}^2 R_{\text{ac\_sec}}. \tag{36}$$

5) Loss of Rectifier Diode: The loss of rectifier diode is calculated as follows:

$$R_{\text{sec\_diode}} = \left(\frac{P_o}{2V_o} V_F + i_{\text{diode\_rms}}^2 R_d\right) \tag{37}$$

where P_{o} and V_{o} are the output power and voltage, V_{F}, $i_{\text{diode\_rms}}$, and R_{d} are the forward voltage drop, the RMS current and the conduction resistance of the rectifier diode, respectively.

F. Comparative Analysis

To make a fair and comprehensive comparison, we evaluated the performances using many structures including adjustable transformers [11], split resonant branches [13], a variable magnetic inductor [14], and a switch-controlled capacitor [17]. Their working principles are all based on modifying the system gain characteristics through the resonant tank. Meanwhile, their gain range is wider or narrower than that of the proposed *LLC* converter. Thus, they will be good examples for performance comparison with the proposed method. As shown in Table I, five *LLC* converters can be simply classified into two categories based on the number of transformers: *LLC* converter with single transformer and *LLC* converter with dual transformers.

1) Both the *LCLC* converter [14] and the SCC-LLC converter [17] employ single transformers. Their gain ranges are all smaller than that of the proposed *LLC* converter. The proposed *LLC* converter neither needs to investigate the complex coupling design like the *LCLC* converter nor compensate for component errors only as same as the SCC-LLC converter.
2) Both the *LLC* converter with adjustable transformers [11] and the DSBS *LLC* converter [13] are of dual transformers. Compared with the proposed *LLC* converter, their system gains are wider thanks to their dual-transformer structure. However, their transformer designs are more complex and losses are inevitably higher. In [11], one set of bidirectional switching is added for the control of ratios of transformer turns, and its gain range can be extended to different degrees. Although its core losses are optimized, the transformer's size brings the disadvantage of low power density. In addition, the DSBS LLC converter has two split resonant tanks to achieve wide system gain [13], which has one more transformer and inductor than the proposed *LLC* converter. At the same time, a large overshoot current is introduced when two modes are switched.

TABLE I
COMPARISON WITH OTHER *LLC*-BASED CONVERTER TOPOLOGIES

	LLC converter with adjustable transformer [11]	DSBS LLC converter [13]	Proposed LLC converter	LCLC converter [14]	SCC-LLC converter [17]
Gain range	[1],[4]	[1,2.5]	[1,1.81]	[1,1.6]	[1,1.33]
Additional switches	2	0	2	0	2
Resonant capacitors	1	2	3	2	2
Resonant inductors	1	2	1	1	1
Trans-formers	2	2	1	1	1
Merits	Minimum core loss	Lower magnet-izing current	Flexible and ro-bust	Few addi-tional devices	Compen-sated compo-nents error
Demerits	Low power density	Larger overshoot of current	Slight asymmet-rical current	Com-plex cou-pling design	Nonex-tensive gain range

Thus, the results demonstrate the superiorities of the proposed LLC converter with series–parallel hybrid SCC despite additional capacitors, such as flexible and robust voltage control, extended gain range, and small voltage and current mutation changes. Theoretically, the resonant currents of the proposed control method are centrally symmetric, but there may be a slight asymmetry in the currents due to the hardware's layout and the transformer's influence, which is unavoidable.

G. Precautions Concerning Magnetic Components

The magnetic components in *LLC* converters mainly include transformers and inductors, and their design is closely related to the system's performance. Taking the design of the transformer as an example, saturation, core loss, and copper loss are analyzed to guarantee a high magnetic performance. The optimization methods mainly include enough margin in design, selection of magnetic material, reduction of core loss caused by high-frequency excitation, and optimization of copper losses.

1) Saturation is the main limit for working at low frequencies. This transformer can undergo a maximum current of 7A until the saturation occurs. However, the maximum current in low frequency working region so far is only 4.48 A, which is much smaller than 7 A. Thus, the proposed *LLC* converter can work normally within the frequency range of 50–150 kHz.

TABLE II
PARAMETERS OF TESTED PROTOTYPE *LLC* CONVERTER WITH SERIES PARALLEL HYBRID SCC

Items	Values
Input voltage	110–200 V
Rated output voltage	36 V
Switching frequency	50–150 kHz
Resonant inductor L_r	66.05 μH
Magnetic inductor L_m	270.2 μH
Resonant capacitor C_r	38.36 nF
Series switch-controlled capacitor C_{r1}	38.43 nF
Parallel switch-controlled capacitor C_{r2}	38.37 nF
Transformer ratio	5:1
Rated output power	250 W

2) For reducing the core losses, the proposed *LLC* converter with a series–parallel hybrid SCC network employs a ferrite PC95 series core from TDK, which is widely used in switching power supplies. There is the lowest overall core loss and is relatively unaffected by temperature in the PC95 series core compared with other series. In addition, the proposed *LLC* converter resonates at 100 kHz, and its main high-gain operating frequencies are within 50–100 kHz. At 100–150 kHz, the system gain range varies very little, and it seldom operates in this high-frequency band. This also avoids additional transformer losses associated with too high frequency.
3) For the optimization of copper losses, the proposed *LLC* converter mainly operates in the high-gain and low-frequency region. For working in frequencies 50–100 kHz, the copper loss is inevitably affected by the current flow through the circuit. The ratios of copper loss to total input power under different frequencies are obtained by simulation calculation. Theoretical and simulation results therefore provide a basis for actual transformer design and manufacturing.

IV. EXPERIMENTAL VERIFICATION

To verify the feasibility of the *LLC* converter with series–parallel hybrid SCC, a 250 W prototype is built. This hardware version can not only complete the verification of the *LLC* converter with series–parallel hybrid SCC but also realize the testing of the conventional *LLC*. The basic parameters are shown in Table II and the hardware photos are shown in Fig. 8.

The control core is the digital signal processor (DSP) controller TMS320F280049C from Texas Instruments (TI). Since closed-loop control is to be realized, a current transducer LAH 25-NP is added to the main loop to measure current. The control block diagram is shown in Fig. 9. The hardware circuit adds a zero-crossing comparison circuit of the resonant current for the ECAP module in DSP, making the controlled switch always realize soft switching. When the input voltage is disturbed, PI control is introduced to manipulate the duty cycle of controlled switches or the switching frequency of all switches to stabilize the output voltage.

From Fig. 10, users can choose the single mode, dual mode, and multimode switching. In single mode, when the input

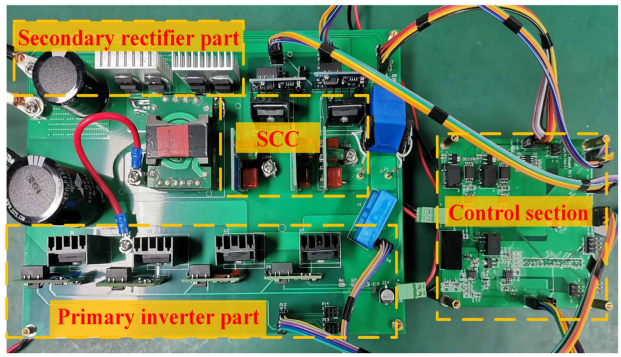

Fig. 8. Hardware of proposed *LLC* converter with series–parallel hybrid SCC.

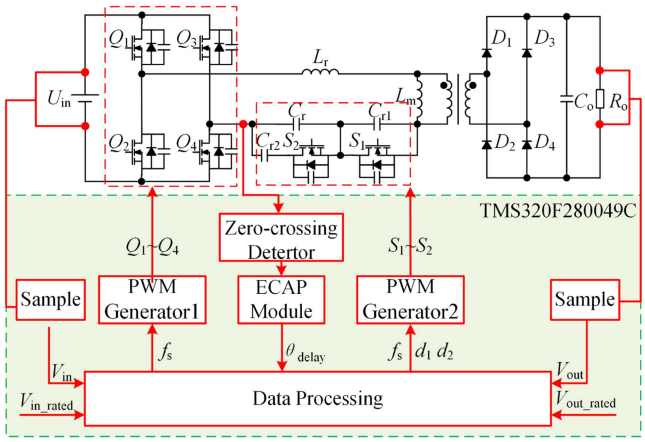

Fig. 9. Control chart of *LLC* converter with series–parallel hybrid SCC.

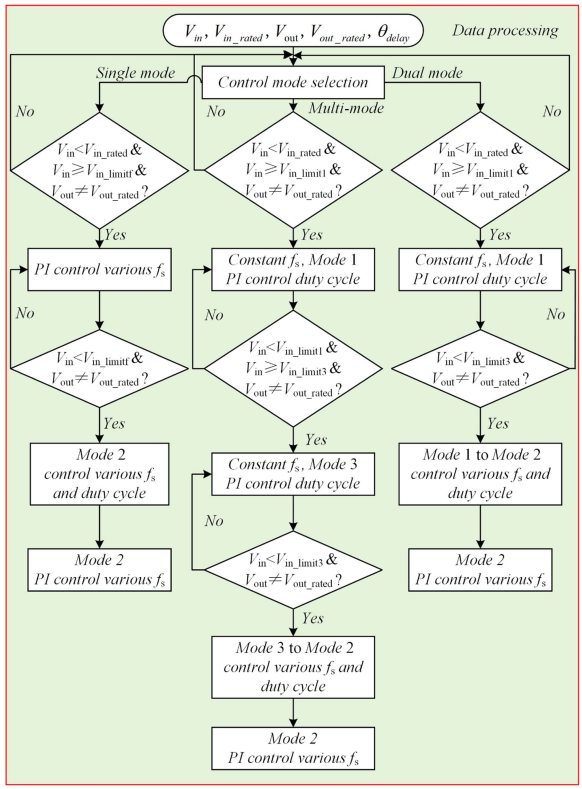

Fig. 10. Data processing of *LLC* converter with series–parallel hybrid SCC.

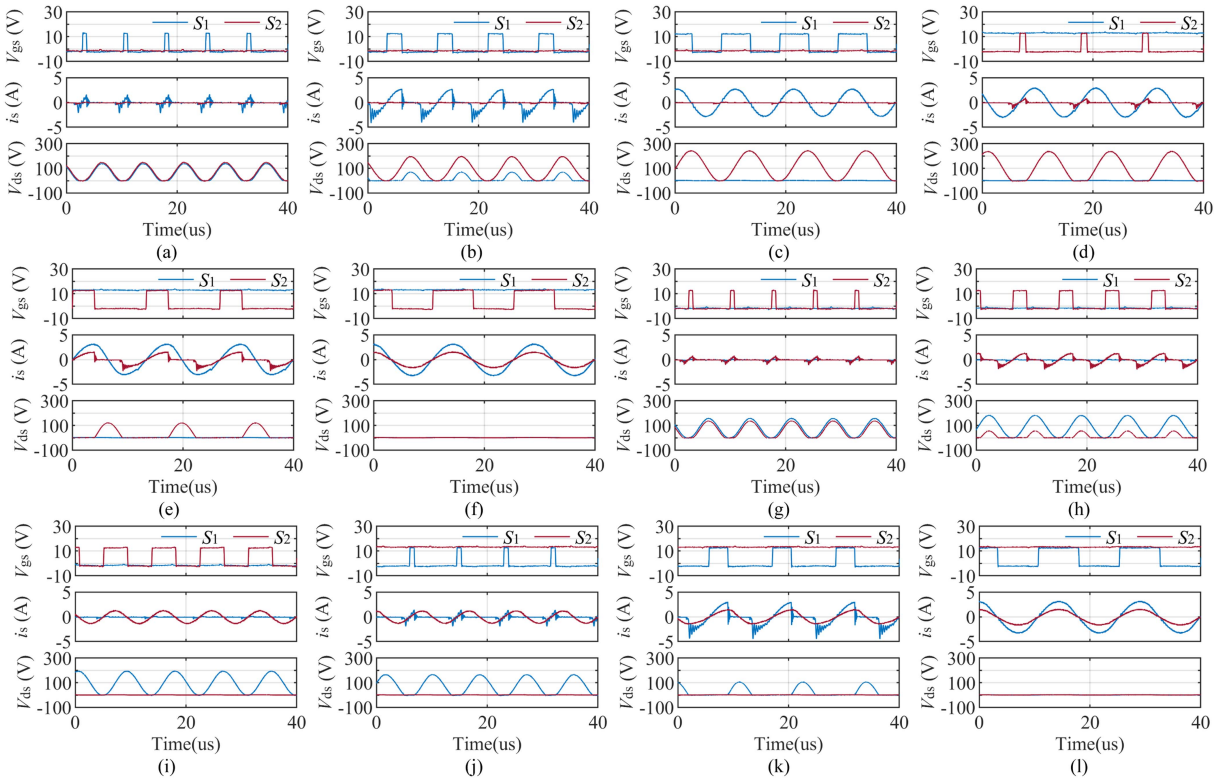

Fig. 11. Measured waveforms of different duty cycles under full load. (a), (b), and (c) are Mode 1. (d), (e), and (f) are Mode 2. (g), (h), and (i) are Mode 3. (j), (k), and (l) are Mode 4.

voltage falls below the rated voltage, the system performs SFM mode until it reaches SFM mode's limit. Once fails to stabilize the voltage, the system will move into Mode 2, which uses hybrid modulation of both switching frequency and capacitance. When the dual mode is enabled, the system enters Mode 1 through the controlled switch and then transfers to Mode 2 by the hybrid modulation for voltage stabilization. In addition, multimode switching initially moves from Modes 1 to 3 by adjusting the capacitance, then shifts to Modes 1 and 2 by hybrid modulation, and finally reaches Mode 2.

A. *Test Results Under Different Modes and Loads*

Fig. 11(a)–(l) presents the resonant operating point waveforms at $d_x = 0.1$, $d_x = 0.3$, and $d_x = 0.5$ ($x = 1$ or 2) in each mode under full load. V_{gssx} is the driving waveform of the controlled switch S_x and i_r is the resonant current. It can be found that S_x switches on when i_r is 0, which guarantees soft switching. When $d_x = 0.5$, currents are more resonant and symmetrical than others because capacitors are fully connected to the circuit. The duty cycle $d_x = 0.1$ or 0.3 means that the series–parallel hybrid SCC network accesses the circuit within 20% or 60% of cycle time, which leads to the asymmetry of i_r. Therefore, it is inevitable that the system has some asymmetry. Meanwhile, there are small positive and negative spikes in the PWM, which are caused by the periodic transients of the resonant tank's input voltage. However, this doesn't threaten the safety of switch tubes.

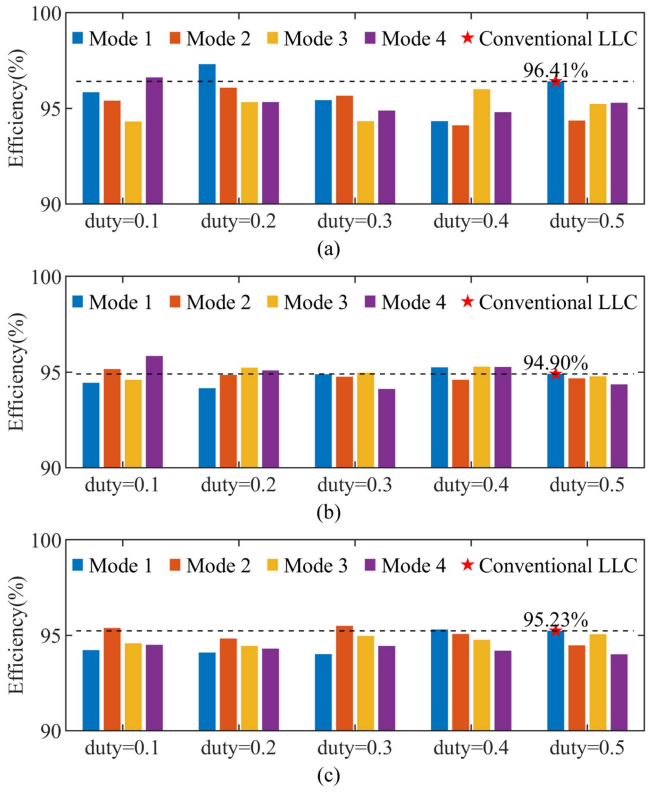

Fig. 12. Measured efficiency under different loads. (a), (b), and (c) are 20% load, 50% load, and 100% load, respectively.

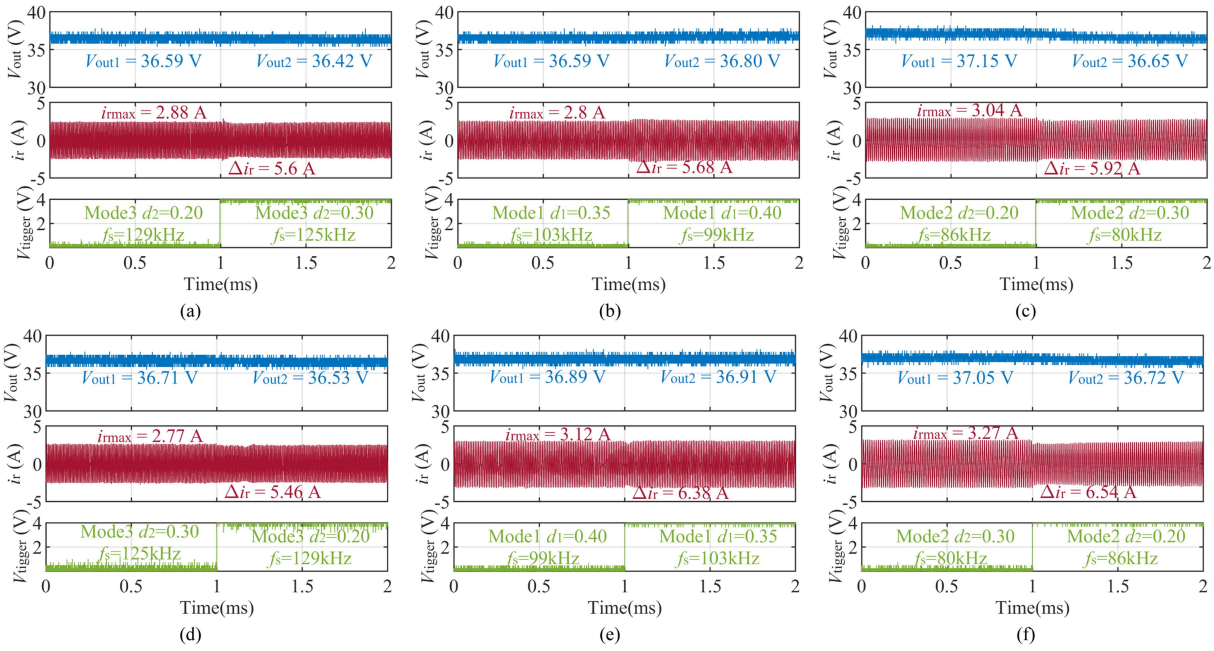

Fig. 13. Output voltages of the proposed *LLC* converter with series–parallel hybrid SCC under fixed modes and direct switching among various switching frequencies and duty cycles. (a) Mode 3 ($d_2 = 0.20\,f_s = 129$ kHz to $d_2 = 0.30\,f_s = 125$ kHz). (b) Mode 1 ($d_1 = 0.35\,f_s = 103$ kHz to $d_1 = 0.40\,f_s = 99$ kHz). (c) Mode 2 ($d_2 = 0.20\,f_s = 86$ kHz to $d_2 = 0.30\,f_s = 80$ kHz). (d) Mode 3 ($d_2 = 0.30\,f_s = 125$ kHz to $d_2 = 0.20\,f_s = 129$ kHz). (e) Mode 1 ($d_1 = 0.40\,f_s = 99$ kHz to $d_1 = 0.35\,f_s = 103$ kHz). (f) Mode 2 ($d_2 = 0.30\,f_s = 80$ kHz to $d_2 = 0.20\,f_s = 86$ kHz).

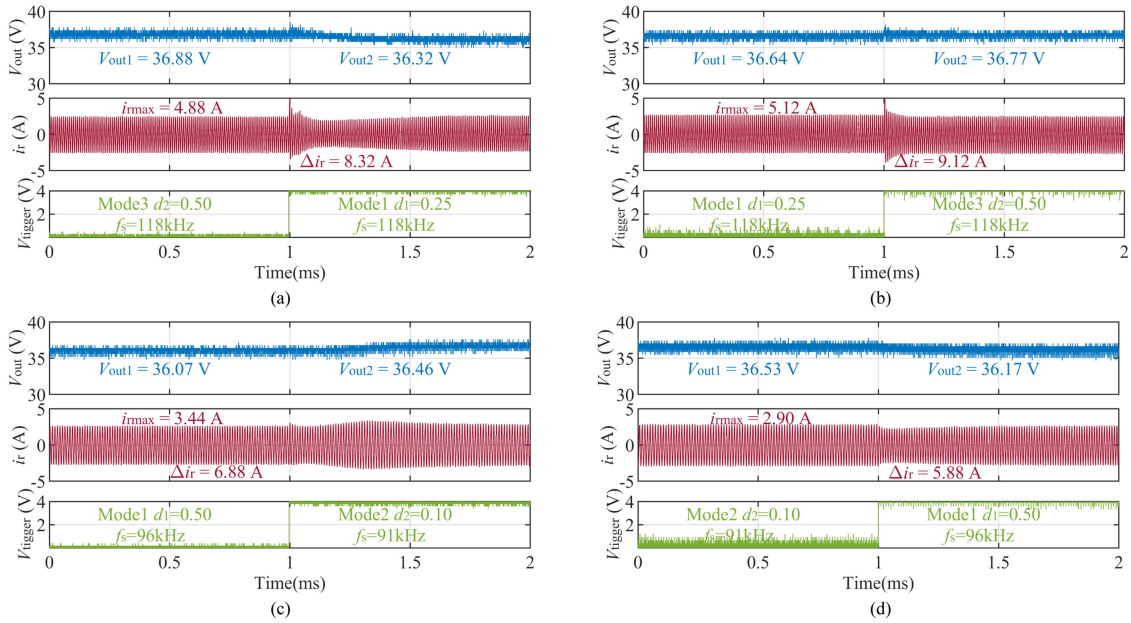

Fig. 14. Output voltages of proposed *LLC* converter with series–parallel hybrid SCC under direct switching among various switching frequencies, modes and duty cycles. (a) Mode 3 ($d_2 = 0.50\,f_s = 118$ kHz) to Mode 1 ($d_1 = 0.25\,f_s = 118$ kHz). (b) Mode 1 ($d_1 = 0.25\,f_s = 118$ kHz) to Mode 3 ($d_2 = 0.50\,f_s = 118$ kHz). (c) Mode 1 ($d_1 = 0.50\,f_s = 96$ kHz) to Mode 2 ($d_2 = 0.10\,f_s = 91$ kHz). (d) Mode 2 ($d_2 = 0.10\,f_s = 91$ kHz) to Mode 1 ($d_1 = 0.50\,f_s = 96$ kHz).

Fig. 12(a)–(c) shows the experimental results of various duty cycles in each mode under different loads. Among them, the conventional *LLC* converter used for comparison experiments is the case of Mode 1 $d_1 = 0.5$, indicated by a marked star. The efficiencies of the proposed *LLC* converter with series–parallel hybrid SCC are not much reduced compared to the conventional *LLC* converter under different loads. Overall, the proposed *LLC* converter with series–parallel hybrid SCC is capable of resonant operation in multiple modes with limited switching losses for operation under different loads.

B. Mode Switching Under Various Switching Frequencies

In order to achieve a wider range of tunable gain, the proposed *LLC* converter with series–parallel hybrid SCC needs to ensure smooth and flexible switching among different modes. Fig. 13

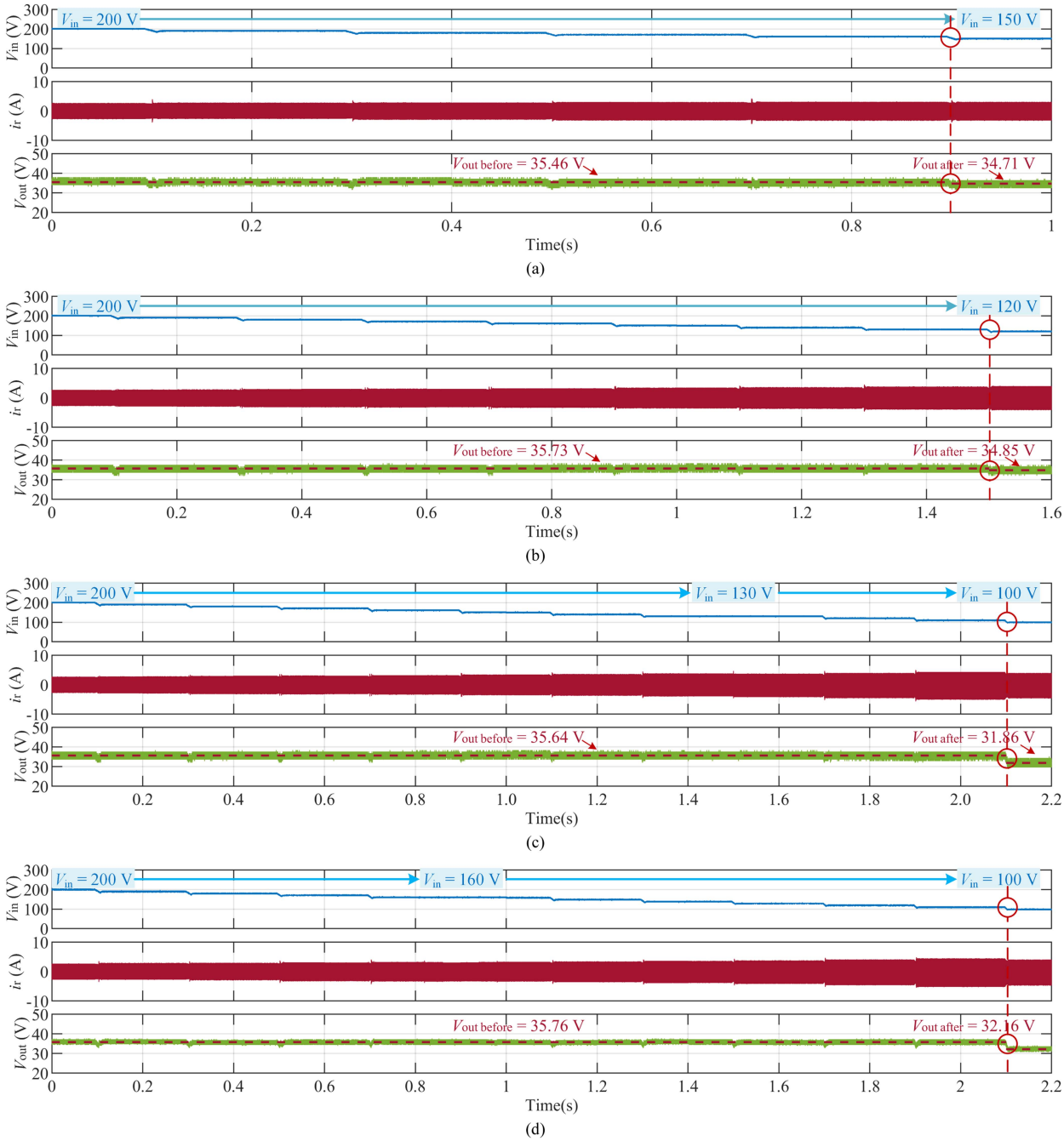

Fig. 15. Output voltage waveforms under input perturbation. (a) Modulation of capacitance under constant frequency with input voltage ranging from 200 to 150 V. (b) SFM mode with input voltage ranging from 200 to 120 V. (c) Single-mode modulation of both switching frequency and capacitance with input voltage ranging from 200 to 100 V. (d) Multimode modulation of both switching frequency and capacitance with input voltage ranging from 200 to 100 V.

shows the switching transients under various switching frequencies in the same mode. Fig. 13(a)–(c) exemplifies the variation of duty cycles in Modes 3, 1, and 2, respectively, which correspond to the switching points between a and b, e and f, and i and j in Fig. 6, respectively. Fig. 13(d)–(f) shows their inverse switching processes. In Fig. 13, the resonant current and output voltage both change slightly under direct switching among different frequencies and duty cycles. It shows that the proposed *LLC* converter accomplishes switching and anti-switching successfully in the same mode.

The direct switching transients among different modes are presented in Fig. 14. Fig. 14(a)–(b) shows the switching and anti-switching process between Modes 3 and 1. In Fig. 14(a), it switches from Mode 3 $d_2 = 0.50$ (point c in Fig. 6) to Mode 1 $d_1 = 0.25$ (point d in Fig. 6). The system gain will consequently change from 1.02 to 1.01. This process, in which both controlled switches are acted, causes a transient current change in the primary side, with the maximum resonant current $i_{\mathrm{rmax}} = 4.88$ A. During this process, C_{r1} and C_{r2} are rapidly charged and capacitive characteristics of MOS transistor will

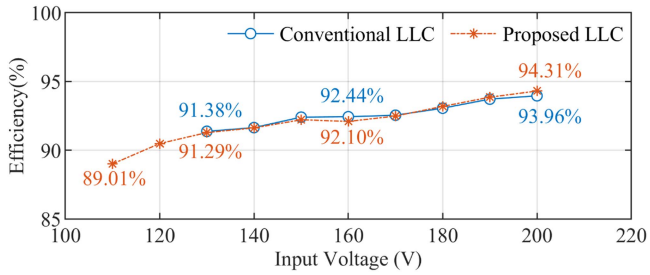

Fig. 16. Measured efficiencies under different input voltages.

also change with different drain–source voltages, resulting in the current surge. However, the recovery of the current to a steady state requires only 0.6 ms. Accordingly, during the inverse transformation, although i_{rmax} becomes larger, it is time to return to a steady state is shorter.

Similarly, Fig. 14(c)–(d) show mutual switching process between Mode 1 $d_1 = 0.50$ (point g in Fig. 6) and Mode 2 $d_2 = 0.10$ (point h in Fig. 6). During this process, only one controlled switch operates and C_{r2} is discharged, so the resonant current and output voltage don't vary much.

C. Stability of Output Voltage

In order to go ahead with proving that the proposed LLC converter has a higher gain in the original frequency range, so only modulation of capacitance, SFM, and modulation of capacitance and switching frequency at the same time are carried out under different input voltages, respectively.

Fig. 15(a) shows the effect of adjusting only series–parallel hybrid SCC at a constant frequency (fs = 100 kHz) with input voltage ranging from 200 to 150 V. It can be seen that the output voltage can still be stabilized at 35.46 V when the input voltage is greater than or equal to 160 V. However, when the input voltage is reduced to 150 V, the output voltage is decreased to 34.71 V. These before-and-after output voltage differences exceed the 2% rating, i.e., 0.72 V, and the system is considered to have lost its voltage regulation. This is the stability limit of the output voltage by adjusting the capacitor. In Fig. 15(b), the conventional *LLC* converter employs the SFM mode to stabilize the output voltage, which will also be used as a control experiment. For a given frequency range, the system can stabilize the output voltage at 35.73 V before the input voltage falls to 130 V. When the input voltage drops to 120 V, the output voltage can only be maintained at a maximum of 34.85 V, which has reached the stability limit of SFM.

Therefore, the SFM mode can achieve a higher gain than the modulation of capacitance.

Moreover, the proposed *LLC* converter is capable of modulating both switching frequency and capacitance, as shown in Fig. 15(c)–(d). The proposed converter will be modulated by the SFM first and then use the modulation of both switching frequency and capacitance if the input voltage is lower than the limited voltage. These solutions will ensure the stability of voltage regulation if the input voltage is higher than 110 V.

Fig. 16 shows measured efficiencies under different input voltages. It can be found that the proposed *LLC* converter with series–parallel hybrid SCC does not have much switching loss due to its soft switching, compared with the traditional *LLC* converter. In conclusion, the proposed *LLC* converter based on the modulation of both switching frequency and capacitance will guarantee the stability of voltage regulation over a wider range of input voltage with high efficiency.

V. Conclusion

In this study, a series–parallel hybrid SCC network is proposed and applied to an *LLC* resonant converter, which is modulated by a compound of switching frequency and variable resonant capacitance. It can change the gain characteristics of *LLC* converter and convert the resonant operating point into a group of resonant curves, which provides a good basis for mode switching. The gain of the proposed *LLC* converter with series–parallel hybrid SCC is higher than that of the conventional *LLC* converter, and it can work with a wider range of input voltage. Moreover, its wider range of variable gain can achieve a higher flexibility in control and can also improve the stability of output voltage. Furthermore, under different modes and loads, it can achieve both soft switching and high efficiency. It is worth noting that the proposed SCC structure cannot share source pins to simplify the gate driving circuitry. Since the proposed SCC is of half-wave structure, the resonant current of the *LLC* converter with series–parallel hybrid SCC will be asymmetrical except for duty cycles at 0 and 0.5. Thus, an investigation on the application of full-wave SCC to replace the proposed half-wave structure will be investigated in future work.

Appendix

For the convenience of analysis, the following hypotheses are put forward to explain.

1) All switching devices are ideal components without loss.
2) When analyzing the waveforms of timing sequence, the zero-crossing point of resonant current from negative to positive is taken as a starting point of one period.

Mode 1: S_1 is at switch-state while S_2 is at OFF-state.

Stage 1 [0, $d_1 t_{\mathrm{s}}$]: S_1 is turned ON. The resonant capacitor C_{r} and L_{r} participate in work. At this time, the RMS value of current I_{rms1} can be expressed as follows:

$$I_{\mathrm{rms1}} = \sqrt{\frac{1}{d_1 t_s}\int_0^{d_1 t_s} i_r^2\,(t)dt}. \tag{A.1}$$

Stage 2 and Stage 3 [$d_1 t_{\mathrm{s}}$, t_{s}- $d_1 t_{\mathrm{s}}$]: S_1 is turned OFF, i_{s1} drops to 0, and the resonant current i_{r} charges and discharges C_{r} and C_{r1}. At this time, C_{r} and C_{r1} work with the resonant inductor L_{r} until the voltage of C_{r1} decreases to zero. In this case, the RMS value of current I_{rms2} is

$$I_{\mathrm{rms2}} = \sqrt{\frac{1}{(1-2d_1)\,t_s}\int_{d_1 t_s}^{t_s - d_1 t_s} i_r^2\,(t)\,dt}. \tag{A.2}$$

Stage 4 [t_{s}– $d_1 t_{\mathrm{s}}$, t_{s}]: the resonant current is negative, and the antiparallel body diode of S_1 starts conducting. In this condition, C_{r} and L_{r} are involved in the operation and the RMS value of

the current is

$$I_{\mathrm{rms3}}=\sqrt{\frac{1}{d_1t_s}\int_{t_s-d_1t_s}^{t_s}i_r^2\left(t\right)dt}. \tag{A.3}$$

Based on the principle that thermal effects of ac and dc currents are equal, the following equation can be listed:

$$\begin{aligned}&d_1t_s\cdot I_{\mathrm{rms1}}^2Z_1+(1-2d_1)t_s\cdot I_{\mathrm{rms2}}^2Z_2\\&\quad+d_1t_s\cdot I_{\mathrm{rms3}}^2Z_3=I_{\mathrm{rms}}^2Z_Rt_s\end{aligned} \tag{A.4}$$

where $Z_1=Z_3=R_1+j(2\pi f_sL_{\mathrm{r}}-1/(2\pi f_sC_{\mathrm{r}}))$, $Z_2=R_2+j(2\pi f_sL_{\mathrm{r}}-(C_{\mathrm{r}}+C_{\mathrm{r1}})/(2\pi f_sC_{\mathrm{r}}C_{\mathrm{r1}}))$, R_1 and R_2 is the resistances in the circuit and Z_{R} is the equivalent impedance, I_{rms} is the RMS value of resonant current.

When it is completely resonant, substitute the formulas (A.1)–(A.3) into (A.4) and make $\mathrm{Im}\{Z_{\mathrm{R}}\}=0$ to obtain the equivalent capacitance of the series SCC *C*scc1 can be expressed as follows:

$$C_{\mathrm{scc1}}=\frac{2C_{r1}}{2-(4\pi d_1-\sin 4\pi d_1)/\pi} \tag{A.5}$$

which is consistent with the results of reference [20].

Since C_{r} is connected in series with C_{scc1}, the hybrid SCC C_{eq1} can be calculated as follows:

$$C_{\mathrm{eq1}}=\frac{2\pi C_rC_{r1}}{2\pi C_{r1}+(2\pi-4\pi d_1+\sin 4\pi d_1)\,C_r}. \tag{A.6}$$

Mode 2: S_2 is at switch-state while S_1 is closed.

Stage 1 [0, d_2t_{s}]: S_2 is turned ON, and C_{r}, C_{r2}, and L_{r} participate in work. At this time, the RMS value of current I_{rms1} can be expressed as follows:

$$I_{\mathrm{rms1}}=\sqrt{\frac{1}{d_2t_s}\int_0^{d_2t_s}i_r^2\left(t\right)dt}. \tag{A.7}$$

Stage 2 and Stage 3 [d_2t_{s}, t_{s}-d_2t_{s}]: S_2 is turned OFF, v_{Cr2} is clamped, and the resonant current i_{r} charges and discharges C_{r}. At this time, C_{r} work with L_{r} until the voltage of C_{r} decreases to equal $v_{\mathrm{Cr}}(d_2t_{\mathrm{s}})$. In this case, the RMS value of current I_{rms2} is

$$I_{\mathrm{rms2}}=\sqrt{\frac{1}{(1-2d_2)\,t_s}\int_{d_2t_s}^{t_s-d_2t_s}i_r^2\left(t\right)dt}. \tag{A.8}$$

Stage 4 [$t_{\mathrm{s}}-d_2t_{\mathrm{s}}$, t_{s}]: The resonant current is negative, and the antiparallel body diode of S_2 starts conducting. In this condition, C_{r}, C_{r2}, and L_{r} are involved in the operation and the RMS value of the current is

$$I_{\mathrm{rms3}}=\sqrt{\frac{1}{d_2t_s}\int_{t_s-d_2t_s}^{t_s}i_r^2\left(t\right)dt}. \tag{A.9}$$

Based on the principle that thermal effects of ac and dc currents are equal, the following equation can be listed:

$$\begin{aligned}&d_2t_s\cdot I_{\mathrm{rms1}}^2Z_1+(1-2d_2)t_s\cdot I_{\mathrm{rms2}}^2Z_2\\&\quad+d_2t_s\cdot I_{\mathrm{rms3}}^2Z_3=I_{\mathrm{rms}}^2Z_Rt_s\end{aligned} \tag{A.10}$$

where $Z_1=Z_3=R_1+j(2\pi f_sL_{\mathrm{r}}-1/(2\pi f_s(C_{\mathrm{r}}+C_{\mathrm{r2}})))$, $Z_2=R_2+j(2\pi f_sL_{\mathrm{r}}-1/(2\pi f_sC_{\mathrm{r}}))$.

Thus, the equivalent capacitance of the series SCC *C*scc2 can be expressed as follows:

$$C_{\mathrm{scc2}}=\frac{2\pi C_r\left(C_r+C_{r2}\right)}{2\pi C_r+(2\pi-4\pi d_2+\sin 4\pi d_2)\,C_{r2}}. \tag{A.11}$$

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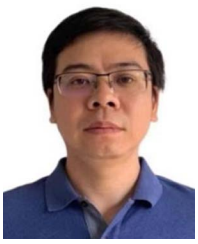

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