Fixed-Frequency K+D Modulation of Modular Multilevel Resonant DC–DC Converters for Output Voltage Overshoot Optimization

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***Abstract*—Modular multilevel resonant dc–dc converters (MMRDCs) are emerging as a competitive solution for medium wide input voltage–low voltage conversion, yet they often encounter output voltage overshoot when submodules insert or extract. In this article, a novel K+D control scheme of MMRDCs is proposed, which combines both inserted submodule number K and adjusting width D. Output voltage overshoot could be greatly suppressed and soft switching characteristics could also be improved enormously based on the proposed K+D modulation strategy. The design of magnetic components would benefit from fixed-frequency control. Continuous dc voltage gain is analyzed which could effectively simplify the control loop. Simulations on a 200 kW MMRDC that converts 9–18 kV to 750 V have been presented to verify the effectiveness of theoretical analysis and control strategies. Experimental results from a prototype are also provided to demonstrate its feasibility.**

***Index Terms*—Fixed-frequency K+D control, modular multilevel resonant dc–dc converters (MMRDCs), soft switching, wide input range.**

I. Introduction

MEDIUM-VOLTAGE dc (MV-DC) systems are increasingly being applied in various solutions due to their high efficiency, cost-effectiveness, reliability, and flexibility. Such applications span diverse fields such as renewable energy integration, large-scale energy storage, undersea power supply, and data centers [1], [2], [3], [4]. The power electronic dc converter that transitions from medium to low voltage is a key component of the dc distribution system [5], [6], [7], [8].

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A traditional medium to low voltage dc conversion scheme employs a cascaded H-bridge structure with series input and parallel output (ISOP) [9]. The advantages of this scheme include modularity and controllability. However, this approach introduces high-frequency transformers into each module. These transformers must operate in 10 kV environment, leading to increased module size and reduced power density. These drawbacks limit the application of the ISOP structure in high-power density scenarios [7], [10], [11], [12]. A viable solution to this problem is modular multilevel topology with a centralized transformer. In the application of MV-DC converters, series-based MV-LV converters are also used as the medium-voltage side to withstand medium-voltage and achieve soft-switching operation, but the dynamic voltage balance of multiple devices in series is still complicated to achieve [13], [14].

Another important requirement of MV-DC applications is wide range of input voltage. Voltage fluctuations can occur due to energy storage system voltage changes, renewable energy generation variability, or long distances between power supplies and loads. Flexible regulation to match the voltage levels on both the medium and low voltage sides accurately should be considered [15], [16]. To reduce the gap between the input and output voltages, multistage conversion can be considered, but that will increase system cost and reduce the conversion efficiency [17], [18].

The combination of modular multilevel converter (MMC) and resonant converters in an MV-LV system is a highly competitive solution. A typical MMRDC topology is shown in Fig. 1, which is similar to the single-string submodules (SMs) based LLC converter structure with SM voltage self-balance introduced in [19]. The MMC topology can handle the MV voltage pressure, while the resonant topology assists the system in achieving soft switching and efficient conversion. By changing the number of inserted SMs (K value) as well as the operating frequency and the ramp-in slope, a wide range of input voltage variations can be achieved. Hence, this scheme has exceptional modularity and control flexibility. A dual-string MMRDC for 9–15 kV wide input range to low-voltage conversion in submarine observation networks is proposed in [20]. This topology is improved from control strategy in [21].

The traditional control method of MMRDC inevitably has the problem of output voltage overshoot when SMs are switching.

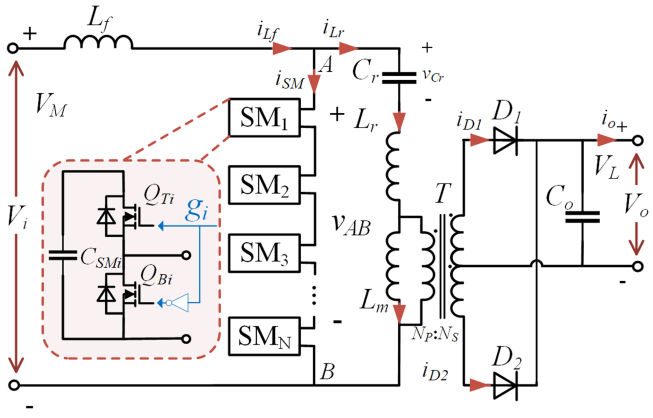

Fig. 1. Modular multilevel resonant DC–DC converter.

The traditional modulation method for MMRDCs combines pulse frequency modulation (PFM) with changing the number of inserted SMs. The number of inserted SMs is denoted by K value. This modulation method is abbreviated as PFM+K. As shown in Fig. 2, as the input voltage v_{in} increases, the number of inserted SMs K changes from 1 to 4 to keep the resonant cavity input voltage v_{AB} within the adjustable range. When the value of K increases by one, the operating frequency f changes from $f_{\max}$ to $f_{\min}$. Due to the instantaneous transition of f and K values, the output voltage v_{out} has to restabilize at the output value, resulting in a voltage overshoot.

Excessive voltage overshoot may damage equipment connected to the dc bus, especially voltage-sensitive electronic components. In addition, many dc systems have overvoltage protection mechanisms. If the voltage fluctuations exceed a certain range, these protection mechanisms may be triggered, leading to system shutdown. To reduce this overshoot, common methods are to increase the number of SMs and increase the output filter capacitance, but this usually increases the cost of the device greatly.

The traditional PFM+K control method requires a smaller value of $m = L_m/L_r$ to ensure the output voltage gain, which results in the use of a smaller magnetizing inductance L_m. A smaller L_m will lead to a larger resonant current and conduction loss. If a larger L_m can be used, the efficiency of the converter will be further improved.

Expanding the soft-switching operation range is used by MMRDC to improve the conversion efficiency. The exploration of internal-phase-shifted control, trapezoidal current control, and dual-phase-shifted control aim to extend the range of soft switching operations while reducing power loss [22], [23], [24], [25], [26]. Nonetheless, similar to MMC, MMRDCs inherently possess dc circulating current, which results in uneven soft switching behavior for the top and bottom SM switches. Due to the dc circulating current, some dual-series structures MMRDCs have 50% SM switches that are unable to achieve soft switching.

In this article, a novel K+D control scheme is proposed for MMRDCs. This control method operates at the fixed resonant frequency, adjusting the output voltage by changing inserted

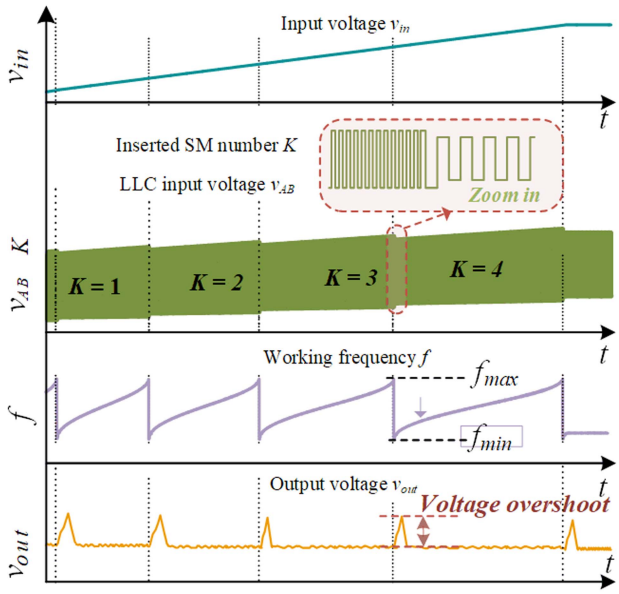

Fig. 2. Output voltage overshoot of MMRDCs with conventional PFM + K modulation.

SMs K and the pulsewidth D. The proposed K+D control scheme has the following advantages.

1) *Suppressed Voltage Overshoot:* Voltage overshoot associated with switch of K values is greatly suppressed. The proposed scheme allows the converter to continuously adjust as K steps. At the same time, the modulation can be simplified to a basic PI control mechanism.
2) *Enhanced Soft Switching:* Almost all primary switches of MMRDCs with the proposed K+D modulation scheme can achieve zero voltage switching (ZVS). In contrast, only 50% of the switches of multistack topologies can achieve ZVS.
3) *Reduced Loop Current:* A lager inductor ratio $m = L_m/L_r$ can be chosen to minimize excitation current and improve conversion efficiency. The fixed frequency remains constant, facilitating the design of magnetic components.

The rest of this article is organized as follows. Section II introduces the MMRDC topology and the proposed K+D modulation. In Section III, the operating modes and performance of the converters are investigated, followed by simulations on a 200-kW MMRDC that converts 9–18 kV to 750 V to verify the effectiveness of theoretical analysis and control strategies. Experimental results from a prototype MMRDC are also provided to demonstrate its feasibility in Section IV. Conclusions are finally drawn in Section V.

II. Topology and Modulation

As shown in Fig. 1, the MMRDC consists of a filter inductor L_f, a single string series-connected SM branch (SSB), a resonant capacitor C_r, a resonant inductor L_r on MV side, and a half-bridge on LV-side connected by a high-frequency transformer T with the magnetizing inductor L_m. The V_i on the left is the MV dc input, and the V_o on the right is the LV dc output.

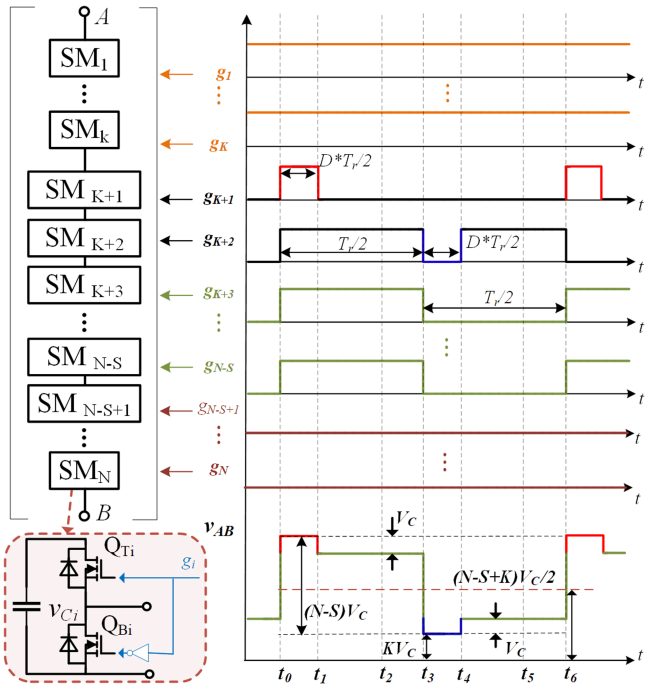

Fig. 3. Key waveforms of the proposed K+D modulation.

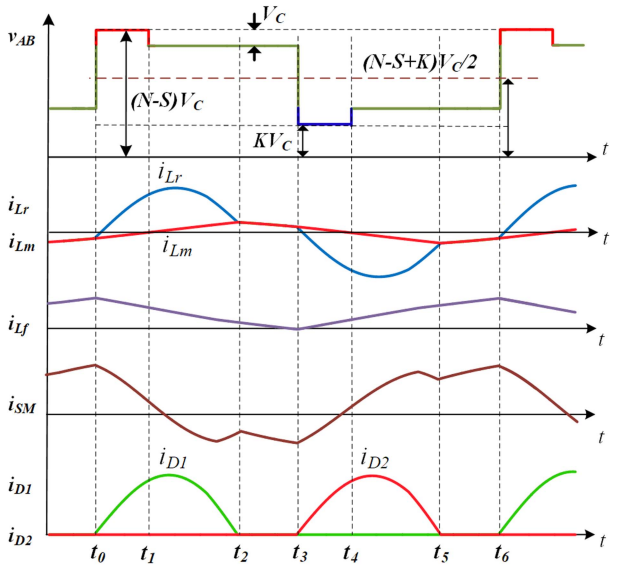

Fig. 4. Key operating waveforms of the MMRDC with the proposed K+D modulation.

The input dc voltage undergoes conversion into square wave as insertion and extraction of SMs. Filter inductor (L_f) is inserted into the input arms to mitigate the circulating current in the dc loop. The V_{AB} denotes the output voltage of SSB.

In each SM of the MV side, the gate signals for the top and bottom switches are designed to be complementary with sufficient dead time. When capacitors from different numbers of SMs are connected between AB, the voltage V_{AB} will fluctuate similarly to the full-bridge output voltage. The output voltage can be adjusted based on the number of inserted SMs and the width of the input pulses.

By Kirchhoff's Current Law at point A in Fig. 1, the current of SSB can be calculated as $i_{SM} = i_{Lf} - i_{Lr}$, where i_{Lf} is the MV terminal current and i_{Lr} is resonant cavity current.

A. Modulation Strategy

As shown in Fig. 3, g_i and V_{Ci} denote the driving signal and capacitor voltage of the ith SM, respectively (i = 1, 2, ..., N). The switching frequency is fixed at resonant frequency.

The driving signals g_1 to g_K remain high throughout the entire switching period, ensuring a continuous insertion of capacitors for SM_1 to SM_K, which is denoted as K value. The driving signals g_{N-S+1} to g_N remain low throughout the entire switching period, ensuring a continuous extraction of capacitors for SM_{N-S+1} to SM_N, which is denoted as S value. $K = S$ should be ensured in the proposed modulation.

The driving signal g_{K+1}in Fig. 3 is high from t_0 to t_1 and the duty cycle in the first half of the cycle is D while the second half of the cycle is all low. The high level part of g_{K+1} is marked in red, which constitutes the part of the V_{AB} with the highest voltage. The driving signal g_{K+2} is high during the first half. g_{K+2} keep low from t_3 to t_4 for the second half of the cycle. g_{K+2} maintains a low level for a duration of $D * T_r/2$. g_{K+2} is marked in blue, which constitutes the part of the V_{AB} with the lowest voltage.

The driving signals g_{K+3} to g_{N-S+1} are constantly working at 50% duty cycles.

As a result of the volt-second balance of L_f, (1) could be obtained, where T_r is the switching period and $T_r = 1/f_r$, V_C denotes average voltage of all SMs. D is the proportion of the adjustment ratio to half a period, ranging from [0,1]

$$(V_i - (N - S - D)V_C)\,T_r/2 + (V_i - (K + D)V_C)\,T_r/2 = 0. \tag{1}$$

Using (1), capacitor voltage of SM can be determined via: $V_C = 2V_i/(N - S + K)$. According to the waveform in Fig. 3, the amplitude of V_{AB} can be calculated by (2). V_{AB} is vertically translational symmetric about $(N - S + K)V_C/2$

$$V_{AB}(t) = \begin{cases} (N-S)V_C, & t_0 \le t < DT_r/2 \\ (N-S-1)V_C, & DT_r/2 \le t < T_r/2 \\ KV_C, & T_r/2 \le t < (1+D)T_r/2 \\ (K+1)V_C, & (1+D)T_r/2 \le t < T_r \end{cases} \tag{2}$$

where V_{AB} reaches its maximum value at $S = K = 0, D = 0$. When V_i gradually increases, the value of D can be increased to keep the output voltage constant. If D increases to 1, the value of S and K increases by one. Similarly, when D decreases to 0, the value of S and K decreases by one.

B. Operating Principle

As shown in Fig. 4, the proposed modulation of MMRDC can be divided into two half-cycles: $t_0 - t_3$ and $t_3 - t_6$. Since two half-cycles are symmetric, only the interval from t_0 to t_3 is introduced.

Resonant frequency f_r and resonant impedance Z_r and Z_m of the resonant tank are defined as follows:

$\omega_r = 1/\sqrt{L_r \cdot C_r}$, $f_r = \omega_r/2\pi$, $Z_r = \sqrt{L_r/C_r}$, $\omega_m = 1/\sqrt{(L_r + L_m) \cdot C_r}$, $f_m = \omega_m/2\pi$, $Z_m = \sqrt{(L_r + L_m)/C_r}$.

There are three operating steps during half a switching cycle. Since V_{AB} between two half-cycles is symmetric about $(N - S + K)V_C/2$ and the direct current is isolated by the C_r, i_{Lr}, and i_{Lm} are symmetrical about the time axis t.

N_{in} is employed to denote the number of SMs engaged in voltage distribution, calculated as $N_{in} = N - S$.

Mode 1 $[t_0 - t_1]$: At t_0, all g_i are turned ON except S SMs. N_{in} SMs are inserted into the circuit. and the string voltage V_{AB} is $N_{in}V_C$. The resonant current i_{Lr} is negative, and the string current i_{SM} is positive. The resonance between L_r and C_r begins. During $[t_0 - t_1]$, N_{in} SMs are inserted, V_{AB} increases to $N_{in}V_C$ after t_0, i_{D1} rises from zero. The top switches Q_{Ti} of SMs inserted during $[t_0 - t_1]$ can be turned ON with ZVS, while $i_{SM} > 0$. In this mode, the circuit's state equation can be expressed as follows:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + N_{in}V_C - nV_o \\ L_m \frac{di_{Lm}(t)}{dt} = nV_o \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{3}$$

Mode 2 $[t_1 - t_2]$: At t_1, g_{K+1} is turned OFF. $N_{\text{in}} - 1$ SMs are inserted into the circuit and the string voltage V_{AB} keeps $(N_{in} - 1)V_C$. The resonant current i_{Lr} is positive, and the string current i_{SM} is positive. The resonance between L_r and C_r continues until t_2. The lower switches Q_{BK+1} is turned ON and SM_{K+1} is removed during $[t_1 - t_2]$. In this mode, the circuit's state equation can be expressed as follows:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + (N_{in} - 1)V_C - nV_o \\ L_m \frac{di_{Lm}(t)}{dt} = nV_o \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t). \end{cases} \tag{4}$$

Mode 3 $[t_2 - t_3]$: At t_2, the resonant current i_{Lr} equals to magnetizing inductor current i_{Lm}, the resonance between $L_r + L_m$ and C_r begins. The string voltage V_{AB} keeps $(N_{in} - 1)V_C$. The resonant current i_{Lr} is positive, and the string current i_{SM} is negative. The resonance between $L_r + L_m$ and C_r continues until t_3. In this mode, the circuit's state equation can be expressed as follows:

$$\begin{cases} (L_m + L_r)\frac{di_{Lr}(t)}{dt} = -v_{Cr}(t) + (N_{in} - 1)V_C \\ i_{Lm}(t) = i_{Lr}(t) \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t) \end{cases}. \tag{5}$$

Mode 4 $[t_3 - t_4]$: At t_3, the $g_i - g_K$ are turned ON and other SMs are turned OFF. K SMs are inserted into the circuit. The resonance between L_r and C_r begins. The resonant current i_{Lr} is positive, and the string current i_{SM} is negative. During $[t_3 - t_4]$, V_{AB} decrease from $(N_{in} - 1)V_C$ to KV_C after t_3, i_{D2} rises from zero. The lower switches Q_{Bi} of SMs can be turned ON with ZVS during $[t_3 - t_4]$, while $i_{SM} < 0$.

Mode 5 $[t_4 - t_5]$: At t_4, the lower switches Q_{BK+2} is turned ON and SM_{K+2} is inserted during $[t_4 - t_5]$. $K + 1$ SMs are inserted into the circuit. The resonant current i_{Lr} is negative, and the string current i_{SM} is positive. The resonance between L_r and C_r continues to t_5.

Mode 6 $[t_5 - t_6]$: At t_5, the resonant current i_{Lr} equals to magnetizing inductor current i_{Lm}, the resonance between $L_r + L_m$ and C_r begins. $K + 1$ SMs are inserted into the circuit and the string voltage V_{AB} keeps $(K + 1)V_C$. The string current i_{SM} is positive. The resonance between $L_r + L_m$ and C_r continues until t_6.

III. Converter Performance Analysis

A. DC Voltage Gain

The traditional method for calculating voltage gain is the fundamental harmonic approximation (FHA) [27]. However, the FHA method neglects high-order harmonics in voltage and current waveforms, which leads to drops in accuracy. To achieve more precise gain characteristics, this article employs the time-domain analysis method [28].

By solving the differential equations for Mode 1 to Mode 3, (6), (7), shown at the bottom of this page, and (8) can be obtained

$$i_{Lm}(t) = \begin{cases} i_{Lr}(t_0) + (nV_o/L_m)t, & t_0 \le t < t_2 \\ i_{Lr}(t), & t_2 \le t < t_3. \end{cases} \tag{8}$$

Due to the waveforms of $v_{Cr}(t)$ and $i_{Lr}(t)$ are half-wave symmetric signals, the following relationships as shown in (9) can be established. At time t_2, both L_r and L_m are involved in resonance. These relationships can be expressed as

$$\begin{cases} i_{Lr}(t_0) = -i_{Lr}(t_3) \\ v_{Cr}(t_0) = -v_{Cr}(t_3) \\ i_{Lr}(t_2) = i_{Lm}(t_2). \end{cases} \tag{9}$$

In addition, the average value of the difference between the resonant current i_{Lr} and the magnetizing current i_{Lm} over half a cycle is the output average current. Therefore, the output current

$$i_{Lr}(t) = \begin{cases} i_{Lr}(t_0)\cos(\omega_r(t - t_0)) - (v_{Cr}(t_0) - (N_{in}V_C - nV_o))\frac{1}{Z_r}\sin(\omega_r(t - t_0)), & t_0 \le t < t_1 \\ i_{Lr}(t_1)\cos(\omega_r(t - t_1)) - (v_{Cr}(t_1) - ((N_{in} - 1)V_C - nV_o))\frac{1}{Z_r}\sin(\omega_r(t - t_1)), & t_1 \le t < t_2 \\ i_{Lr}(t_2)\cos(\omega_m(t - t_2)) - (v_{Cr}(t_2) - (N_{in} - 1)V_C)\frac{1}{Z_m}\sin(\omega_m(t - t_2)), & t_2 \le t < t_3 \end{cases} \tag{6}$$

$$v_{Cr}(t) = \begin{cases} i_{Lr}(t_0) & Z_r \sin(\omega_r(t - t_0)) \\ & +(v_{Cr}(t_0) - (N_{in}V_C - nV_o))\cos(\omega_r(t - t_0)) + (N_{in}V_C - nV_o), & t_0 \le t < t_1 \\ i_{Lr}(t_1) & Z_r \sin(\omega_r(t - t_1)) \\ & +(v_{Cr}(t_1) - ((N_{in} - 1)V_C - nV_o))\cos(\omega_r(t - t_1)) + ((N_{in} - 1)V_C - nV_o), & t_1 \le t < t_2 \\ i_{Lr}(t_2) & Z_m \sin(\omega_m(t - t_2)) \\ & +(v_{Cr}(t_2) - (N_{in} - 1)V_C)\cos(\omega_m(t - t_2)) + ((N_{in} - 1)V_C), & t_2 \le t < t_3. \end{cases} \tag{7}$$

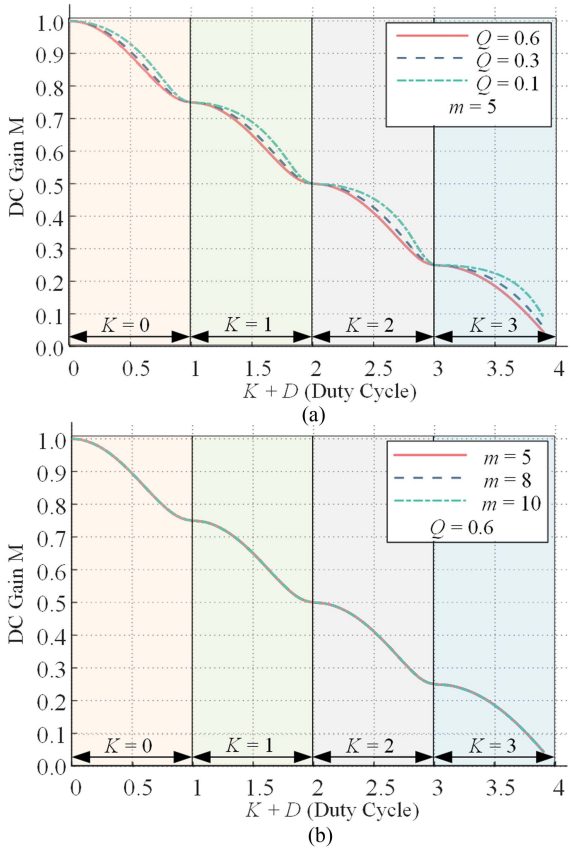

Fig. 5. Gain curves versus $K + D$ for the MMRDC: (a) $m = 5$; (b) $Q = 0.6$.

can be expressed as

$$\frac{1}{T_r}\int_0^{T_r}\left(i_{L_r}(t) - i_{L_m}(t)\right)dt = I_o/n = \frac{V_o}{nR_o} = \frac{8nV_oQ}{Z_r\pi^2} \tag{10}$$

$$Q = \frac{\pi^2 Z_r}{8n^2 R_o}. \tag{11}$$

When N, K, S, D, and V_i take different values, by numerically solving the above (6)–(10), the values of four parameters $(i_{Lr}(t_0), v_{Cr}(t_0), t_2, V_o)$ can be obtained. Therefore, the gain ratio $M = nV_o/V_i$ of the DC converter versus K values and duty cycle D inputs can be derived under different the quality factor Q and the inductor ratio $m = i_{Lm}/i_{Lr}$, which is illustrated in Fig. 5.

The parameter settings of the simulation environment are as follows. The input voltage of the circuit is 300 V, and the transformer turns ratio is 3:1:1. The resonant tank parameters are set as: $L_r = 69.7\mu$H and $C_r = 36.3$ nF. The switching frequency f_s is *LC* resonant frequency f_r 100 kHz.

Fig. 5 delineates the dependence curves of dc voltage gain M on control input $K + D$ for diverse values of Q at $m = 5$, as well as for varying m at a fixed $Q = 0.6$. As shown in Fig. 5(a), the range of dc voltage gain M remains constant when the duty cycle D changes from 0 to 1, indicating that the voltage gain range of the MMRDC is not contingent upon the quality factor Q. This contrasts with the traditional PFM+K LLC resonant converter, where the influence of Q on the voltage gain range is a key consideration.

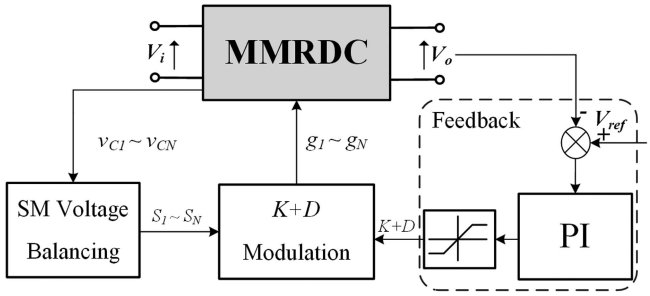

Fig. 6. Voltage balancing plus feedback control to regulate the MMRDC output voltage.

The quality factor Q has a minimal impact on the gain. It primarily affects the t_2 time of resonance for L_M and L_R. A larger value results in a smaller C_r and a larger V_{C_r}, which is not friendly to the voltage endurance of capacitors. Furthermore, larger L_m and L_r are beneficial in reducing the loop current of the resonant cavity and mitigating losses, but this will result in an enlargement of the inductor. Therefore, Q around 0.6 is considered a balanced choice.

In addition, the inductor ratio m exerts little impact on the gain characteristics, as depicted in Fig. 5(b). This behavior is markedly different from that of the conventional *LLC* converter with PFM control, where m is a significant factor to the voltage gain M. To reduce the magnetizing current i_{Lm} and loop currents i_{Lr}, a larger value of m can be adopted without affecting the soft-switching of MOSFETs.

B. Output Voltage Control Scheme

Fig. 6 illustrates the block diagram of the MMRDC with the proposed output voltage control scheme. The scheme incorporates an SM voltage balancing that samples the SM capacitor voltage V_{C_i} to regulate the output voltage V_o by altering the value of K and modulating duty cycle D of g_{k+1} and g_{k+2}. Within the feedback loop, V_o is compared with its reference V_{ref}, and any discrepancy is conveyed to a PI compensator to fine-tune the switching $K + D$.

As shown in Fig. 5, the output voltage gain is a monotonically increasing function of the input control variable $K + D$, and this function is smooth and continuous. Therefore, with a wide range of voltage input, simple PI feedback control can be used to stabilize the output voltage at the target value.

When K increases to $K + 1$, the amplitude of resonant tank voltage will suddenly decrease, which may lead to the voltage sag on V_o. The traditional method uses a feedforward loop to coarsely adjust the value of K, collecting the input voltage as the feedforward control signal to reduce voltage sag.

However, with the proposed modulation method, when K increases to K+1, the transition is made continuous through the value of D, thus essentially eliminating voltage step changes.

Therefore, this control scheme no longer requires the use of feedforward control.

The SM voltage balancing algorithm presented in [20] is employed in this study. The SM capacitor voltages are sorted to determine their relative order. Concurrently, the voltage variation for each SM is calculated as the difference between the current and previous voltage values. Subsequently, gate signals corresponding to larger voltage variations are assigned to SMs with lower voltages, and those with smaller variations to SMs with higher voltages. Therefore, the SM capacitor voltages can be balanced effectively under varying voltage gain and load conditions.

C. Soft Switching Analysis

In MMRDC, the voltage on the filter inductor L_f is determined by the input voltage and V_{AB} as

$$|v_{Lf}| = \frac{(N-S-K-2D)V_i}{(N-S+K)}. \tag{12}$$

Therefore, the input current ripple can be obtained as

$$\Delta i_{Lf} = \frac{|v_{Lf}|}{2L_f f_r}. \tag{13}$$

Furthermore, the current in the filtered inductor can be derived from the following formula:

$$i_{Lf}(t) = \begin{cases} I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(t - \frac{T_r}{4}\right), & 0 \le t \le \frac{T_r}{2} \\ I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(\frac{3T_r}{4} - t\right), & \frac{T_r}{2} < t \le T_r \end{cases} \tag{14}$$

where I_{Lf} indicates the average current of the input current.

The current of the SMs string can be obtained by combining the following formula with the $i_{Lr}(t)$ calculation formula:

$$i_{SM}(t) = \begin{cases} I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(t - \frac{T_r}{4}\right) - i_{Lr}(t), & 0 \le t \le \frac{T_r}{2} \\ I_{Lf} + \frac{|v_{Lf}|}{L_f}\left(\frac{3T_r}{4} - t\right) - i_{Lr}(t), & \frac{T_r}{2} < t \le T_r. \end{cases} \tag{15}$$

To realize the ZVS of the SM module switch, it is necessary to ensure the valve string current $i_{SM}(t) > 0$ and $i_{SM}(t) < 0$ when SM is inserted and cut out, respectively. In addition, the dead zone time t_d between and the top bottom switches is considered, while C_{oss} of the switching device is charged or discharged. Therefore, the conditions for implementing SM top switch Q_{Ti} and lower switch Q_{Bi} ZVS soft switches can be expressed as

$$\begin{cases} i_{SM}(t_d) \ge 0 \\ \left|\int_0^{t_d} i_{\text{SM}}(t)dt\right| > 2C_{oss}V_C \\ i_{SM}(t_1) \ge 0 \end{cases} \tag{16}$$

$$\begin{cases} i_{SM}(\frac{T_r}{2} + t_d) \le 0 \\ \left|\int_{\frac{T_r}{2}}^{\frac{T_r}{2}+t_d} i_{\text{SM}}(t)dt\right| > 2C_{oss}V_C \\ i_{SM}(\frac{T_r}{2} + t_1) \le 0. \end{cases} \tag{17}$$

Thus, by appropriately selecting the values L_f, in the vicinity of D changing to 0, soft switching is achieved for all SM modules except for g_{k+1} and g_{k+2}. Near D changing to 1, all primary-side MOSFETs can achieve ZVS. Consequently, the minimum soft switching ratio is (N−1)/N, which makes it easier to achieve ZVS compared to conventional MMRs.

D. Design Consideration

This part outlines the design process for the key parameters of the proposed converter. These parameters include the total number of submodules (SMs), resonant inductors, resonant capacitors, magnetizing inductors, SM capacitors, and filter inductors.

1) Input Filter Inductor Selection: To ensure all W switch SMs achieve ZVS ON, i_{Lf} at t_3 in Fig. 4 needs to be less than 0, $i_{Lf}(t_3) \le 0$, and $i_{Lf}(t)$ is expressed as

$$i_{Lf}(t) = I_{Lf} + \frac{2(N-S-K)V_i}{(N-S+K)L_f}\left(\frac{T_r}{4} - t\right). \tag{18}$$

The approximate maximum value of L_f can be obtained as: $L_f = V_{i-\min}/(4 \cdot f \cdot I_{Lf})$, where $I_{Lf} = P_o/V_{i-\min}$.

2) SM Module Quantity: The number of SM modules is determined by the voltage rating V_C of each SM. The relation is

$$V_C = \frac{2V_{i-\max}}{(N-S+K)}. \tag{19}$$

Based on the maximum input voltage, the minimum required number of SM modules can be calculated.

3) Resonant Cavity Parameters: Following the classical *LLC* design process, we choose $Q = 0.6$ to calculate the values of L_r and C_r. In this control method, a larger m-value (with $m = 10$, compared to the traditional design where m is typically 6) is used to calculate $L_m = m \cdot L_r$.

4) Transformer Turns Ratio: To minimize the RMS current in the primary winding, the transformer turns ratio should be as large as possible. The ratio is determined based on the ability to output the rated voltage at the minimum input voltage, while considering input margin and voltage losses in the output circuit.

5) SM Capacitor Value: As shown in Fig. 7, the SM capacitor voltage v_{C_SM} fluctuation, $\Delta v_{C\_SM\_PP}$, includes both dc and ac components:

$$\Delta v_{C\_SM\_PP} = \Delta v_{C\_SM\_DC} + \Delta v_{C\_SM\_AC}. \tag{20}$$

The dc voltage fluctuation is determined by integrating the dc current component over K cycles:

$$\Delta V_{C\_SM\_DC} = \int_{t_0}^{t_0+KT_R} i_{SM}(t)\, d\,t\, /C_{SM} = \frac{K \cdot I_{Lf} \cdot T_r}{C_{SM}} \tag{21}$$

where $I_{Lf} = P_o/V_{i-\min}$.

The ac fluctuation is caused by the ripple current i_{SM} and can be estimated by integrating the current during the SM up switch conducting period

$$\Delta V_{C\_SM\_AC} = \int_{t_0}^{t_1} i_{SM}(t)dt/C_{SM} = \frac{1}{2}T_r \cdot \frac{i_{Lr\_\text{rms}} - I_{Lf}}{C_{SM}} \tag{22}$$

where i_{Lr_rms} is the RMS value of the resonant current, estimated as

$$i_{Lr\_\text{rms}} = \sqrt{\frac{\pi^2 I_o^2}{8n^2} + \frac{n^2 V_o^2}{32L_m^2 f_r^2}}. \tag{23}$$

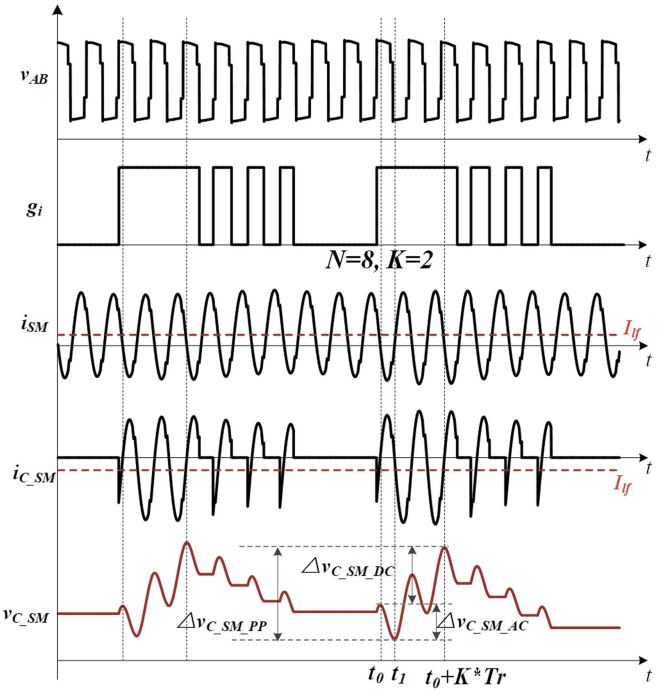

Fig. 7. Schematic diagram of the maximum SM capacitor voltage ripple calculation.

Thus, the minimum value of C_{SM} can be calculated using

$$C_{SM} = \frac{K \cdot I_{Lf} \cdot T_r + \frac{1}{2} T_r \cdot (i_{Lr\_\mathrm{rms}} - I_{Lf})}{\Delta V_{C\_SM\_PP}}. \tag{24}$$

With these parameters determined, the minimum required value for C_{SM} can be calculated.

E. Simulation Verifications

To validate the fixed frequency K+D control strategy, an MMRDC has been designed within the PLECS simulation environment. The hardware parameters were meticulously devised in alignment with the guidelines delineated in Section III. This setup accommodates a broad input voltage spectrum ranging from 9 to 18 kV, while maintaining a steady output voltage of 750 V and facilitating peak output power of 200 kW. Additional parameters are systematically cataloged in Table I.

Fig. 8 delineates the dynamic behavior of the proposed control strategy. Specifically, it depicts a scenario where the output power is maintained at 200 kW while the input voltage escalates from 9 to 18 kV. The voltage regulation approach employed simple PI control based on the inserted SM number K and inserted duty cycle D.

Due to the continuous and monotonic positive correlation between the converter's output voltage gain and the $K + D$ value shown in Fig. 5, there is no state jump when switching the K value. Compared to traditional feed-forward control methods, this method employs simple PI control to achieve regulation of voltage and power.

As the input voltage rises, the duty cycle D is escalated from 0 to 1. When D reaches 1, the K value is incremented by 1, and the D value resets to 0. Since there is no state jump during the continuous adjustment of $K + D$, there is virtually few voltage jump when switching the K value.

TABLE I
CIRCUIT PARAMETERS OF THE SIMULATION

Parameters	Value
MV terminal voltage V_i	9–18 kV
LV terminal voltage V_o	750 V
Transformer turns ratio n	12:1
Rated power P_w	200 kW
The number of SMs N	32
Filter inductance L_f	10 mH
SM capacitance C_{SM}	150 μF
Switching frequency f	10 kHz
Resonant capacitance C_r	81 nF
Resonant inductance L_r	3.12 mH
Magnetizing inductance L_m	31.2 mH
LV terminal capacitance C_o	3 mF
Primary switches	C3M0021120K 1200 V / 100 A from Wolfspeed
Diodes D1/D2	CAS300M17BM2 1700 V / 325 A from Wolfspeed

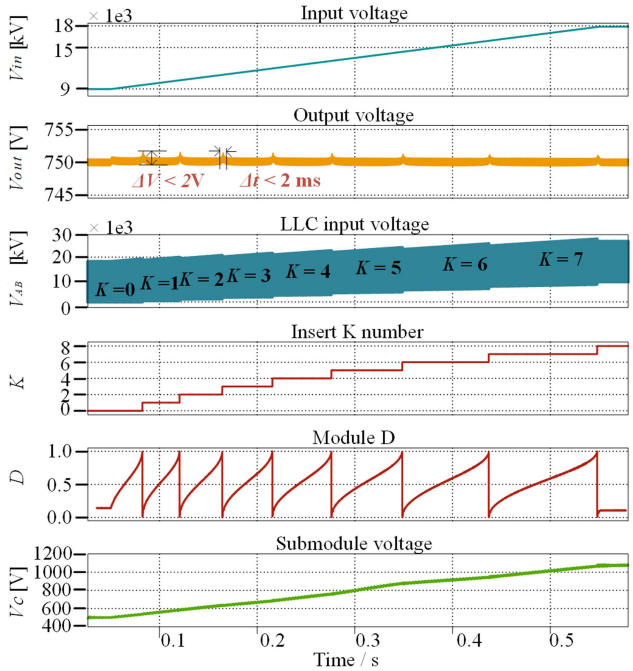

Fig. 8. Dynamic waveform of the proposed fixed frequency K+D control.

As illustrated in Fig. 8, the output voltage undergoes a nominal fluctuation of 2 V during the K value transition, compared to the sag voltage of 38 V in [20] and 20 V in [26]. The perturbation is persisting for a mere 2 ms or less. Furthermore, the SM capacitor voltage transitions smoothly, devoid of significant spikes or oscillations. The SM voltage consistently remains below 1.1 kV for input voltages ranging from 9 to 18 kV, corroborating the efficacy of the theoretical design.

IV. EXPERIMENTAL RESULTS

An experimental prototype was developed to validate the functionality and efficiency of the converter, as depicted in Fig. 9.

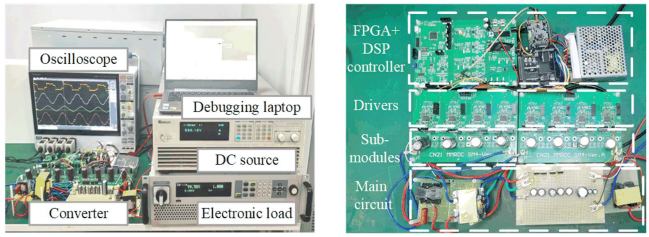

Fig. 9. Experimental prototype and platform.

TABLE II
CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameters	Value
MV terminal voltage V_i	300−600 V
LV terminal voltage V_o	100 V
Rated power P_w	1 kW
The number of SMs N	8
Filter inductance L_f	0.75 mH
SM capacitance C_{SM}	20 μF
Switching frequency f	20 kHz
Resonant inductance L_r	380 μH
Resonant capacitance C_r	166.5 nF
Transformer turns ratio n	43:16
Magnetizing inductance L_m	3.8 mH
LV terminal capacitance C_o	900 μF
Primary switches	IRFP90N20DPBF 200 V 94 A from Infineon
Diodes D1/D2	MBRF40250T 250 V 40 A from LGE

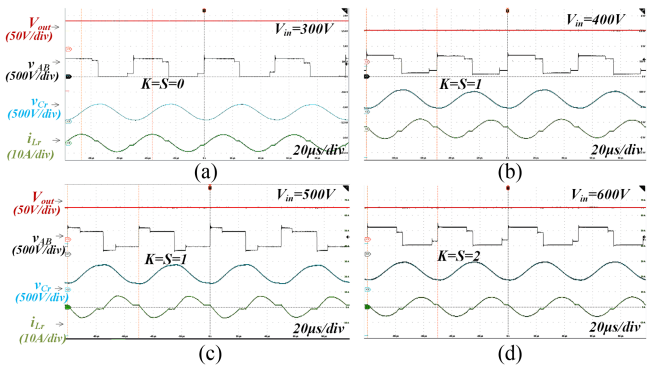

Fig. 10. Measured steady-state voltage and current waveforms under full load with various input voltages: (a) $V_{in} = 300$ V; (b) $V_{\text{in}} = 400$ V; (c) $V_{in} = 500$ V; (d) $V_{in} = 600$ V.

The key parameters and devices of the prototype are shown in Table II.

Fig. 10(a)–(d) illustrates the waveforms of the output voltage V_{out}, the resonant tank voltage V_{AB}, voltage of the resonant capacitor V_{Cr}, and the resonant current i_{Lr} at full load with different input voltages. Meanwhile, the values of K and S under varying input voltages are also provided.

As the voltage changes from 300 to 600 V, the K value varies from 0 to 2. The D value increases gradually, and when D changes from 0 to 1, it is equivalent to $K + 1$. Continuous adjustment and smooth transition of K value are achieved. By employing a simple PI control, the output voltage V_{out} stabilizes at 100 V.

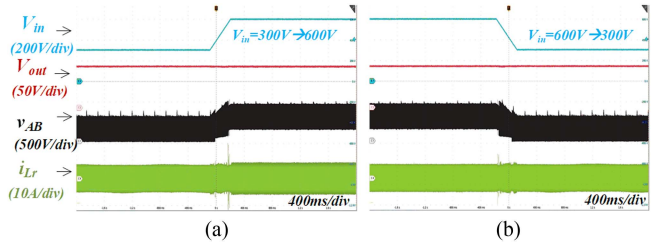

Fig. 11. Dynamic performance of the MMRDC in response to step changes in input voltage. (a) Step increase of input voltage from 300 to 600V. (b) Step decrease of input voltage from 600 to 300 V.

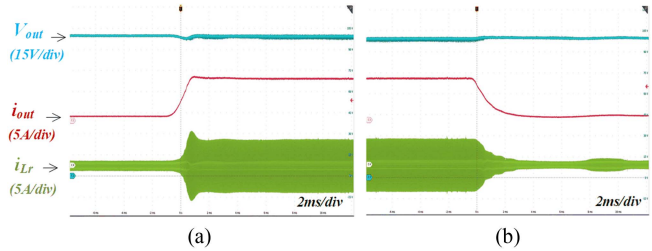

Fig. 12. Dynamic performance of the MMRDC in response to step changes in the load. (a) Step increase of load from 10% load to full load. (b) Step decrease of load from full load to 10% load.

Figs. 11 and 12 are shown to assess the dynamic performance of the MMR converter. Fig. 11 depicts responses to input voltage changes, while Fig. 12 shows responses to load changes. The output voltage V_o quickly stabilizes at 100 V after input voltage adjustments, exhibiting minimal overshoot and undershoot. This indicates dynamic performance for input variations. Similarly, the converter demonstrates a strong transient response under load changes in Fig. 12.

The SM operates in edge-switching mode, defined as E switching. E switching corresponds to g_{k+3} to g_{N-S} in Fig. 3, and the corresponding switching events are surrounded by a green dashed line area. The SM operates in pulsewidth switching mode, defined as W switching, corresponding to g_{k+1} and g_{k+2} in Fig. 3. The corresponding switching events are surrounded by a brown dashed line area in Fig. 13.

As shown in Fig. 13, at low voltage $V_{\text{in}} = 300$ V cases, due to i_{SM} being lower than 0 during the bottom SM switching ON, both E and W switching can achieve ZVS on. As shown in Fig. 13(c), at high voltage $V_{in} = 600$ V cases, due to i_{SM} being lower than 0 during the bottom SM E and W switching ON, both E and W switching can achieve ZVS ON. It can be observed that at 580 V input voltage and heavy load from Fig. 13(d), due to i_{SM} being greater than 0 during the bottom SM E switching, 1 ZVS is lost at this point. However, all conditions for ZVS on are met during W switching.

The percentage of ZVS on the switches is at least 7/8 and can reach up to 8/8, which translates to a range of 87.5% to 100%. If the number of SMs is increased, the soft-switching percentage can be calculated as $(N - 1)/N$. This means that as the number of SMs increases, the proportion of soft switching approaches 100%.

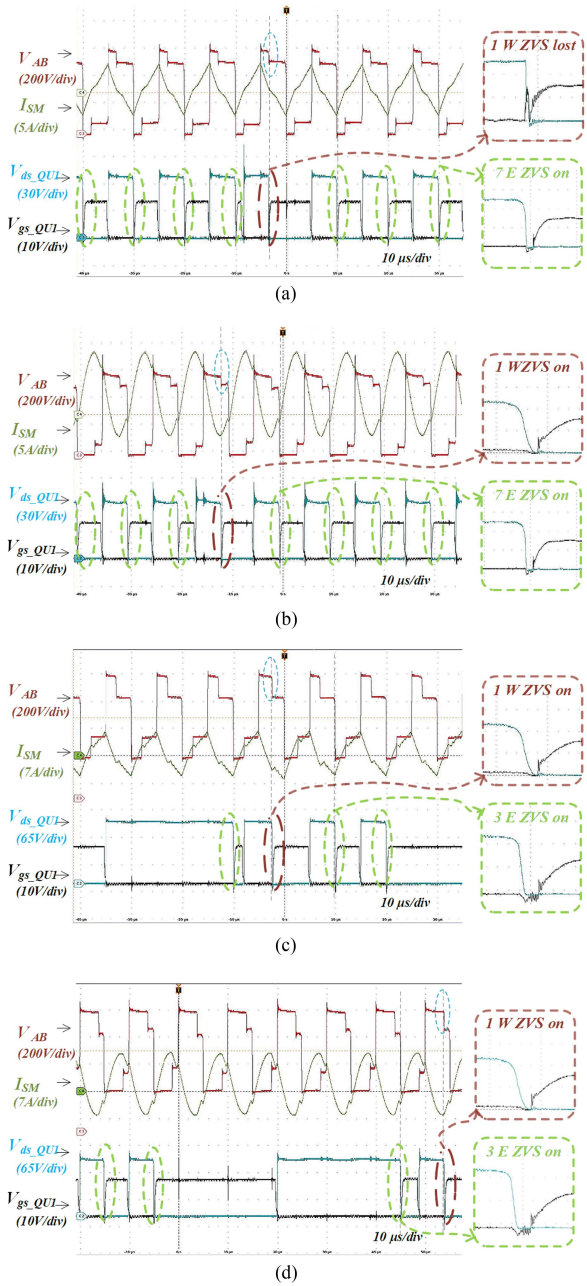

Fig. 13. Measured drive and drain-source voltages of the bottom SM switch: (a) $P_t = 100\,\text{W}$ and $V_{in} = 300\,\text{V}$; (b) $P_t = 1000\,\text{W}$ and $V_{in} = 300\,\text{V}$; (c) $P_t = 100\,\text{W}$ and $V_{in} = 600\,\text{V}$; (d) $P_t = 1000\,\text{W}$ and $V_{in} = 580\,\text{V}$.

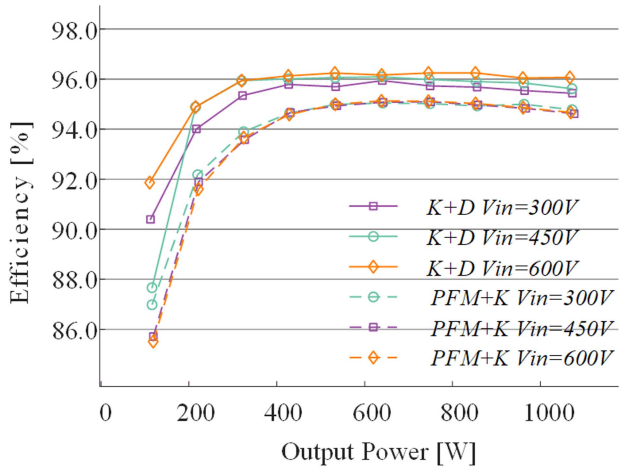

Fig. 14. Measured power stage efficiency of the K+D and PFM + K controlled converter under different voltages.

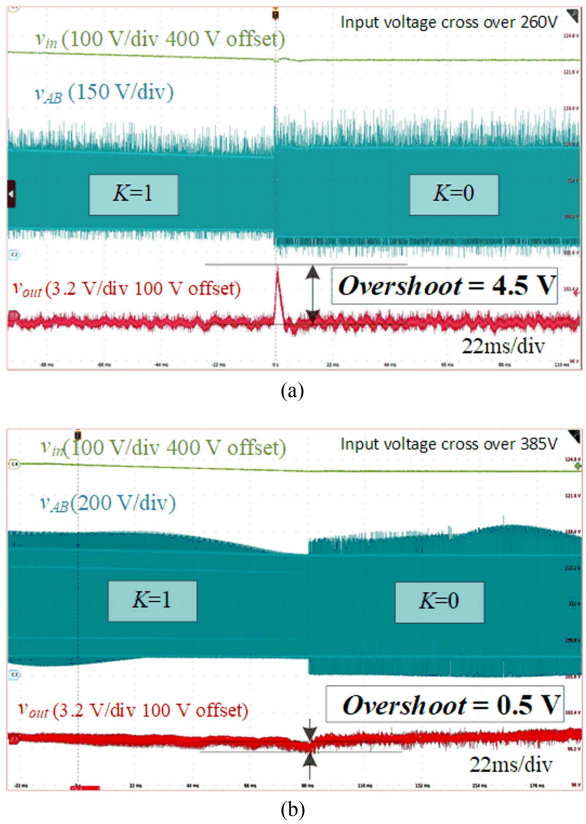

Fig. 15. Voltage overshoot of v_{out}. (a) Conventional PFM+K control. (b) Proposed K+D control.

Therefore, the proposed modulation is more easily to achieve ZVS, with fewer instances of hard switching occurring.

Fig. 14 illustrates the efficiency curve of this converter under different input voltages and loads.

With the PFM + K method, the value of m is set to 5, and the L_m inductance is 2 mH. In contrast, using the K + D control method, m can be increased to 10, with L_m set to 3.8 mH. As a result, the K + D control method exhibits lower conduction current and conduction losses, leading to slightly higher efficiency compared to the PFM + K control method.

Higher efficiency is attained at an input voltage of 600 V, contrasting with lower efficiency observed at lower input voltages. The peak efficiency reaches 96.2% when $P_t = 0.8$ kW and $V_{in} = 600$ V. Benefit from at least $(N-1)/N$ switches ZVS ON, the switching losses can be reduced and consequently, higher efficiency could be caught.

Fig. 15 shows the voltage overshoot experimental waveform of v_{in}, v_{AB}, and v_{out} with different modulation schemes when K steps from 1 to 0 under full load. According to Fig. 15(a), when the MMRDC employed the conventional PFM+K modulation.

TABLE III
COMPARISON RESULTS OF FOUR DC/DC CONVERTER SCHEMES

Parameter	MMR [20]	MMRDC [21]	MMRDC [26]	Proposed
MV terminal voltage /kV	9–15	8–16	9–18	9–18
Rated power /kW	200	100	50	200
output voltage /V	750	375	375	750
Number of string	2	2	2	1
Number of SM	32	32	36	32
Operating frequency /kHz	11.5-22	7-12	12	10
Control scheme	Feedforward + PI	Feedforward + PI	Feedforward + PI	PI
Larger magnetizing inductance L_m	no	yes	yes	yes
Percentage of ZVS ON switches	50%	50%	50%	96.9-100%
Voltage overshoot /Output voltage /V	25/750	25/375	30/375	2/750

v_{AB} steps from $K = 1$ to $K = 0$ while the frequency jumps from maximum to minimum. The voltage overshoot of v_{out} had a peak value of 4.5 V. In Fig. 15(b), where the optimized K+D modulation scheme is employed, although K steps from $K = 1$ to $K = 0$ and duty cycle D changes from 0 to 1, v_{AB} achieves a gradual transition. The voltage overshoot is effectively suppressed, and is limited to 0.5 V.

Table III presents the characteristics of the proposed K+D control strategy in comparison to previous works. Based on the review in Section I, several criteria have been established to compare the candidates for MMRDCs as follows.

1) Less output voltage overshoot: When using other modulation approaches, changes of K cause frequency modulation or phase shift jumps, resulting in significant output voltage overshoot. With the proposed modulation, the output gain remains continuous as K and D change, as shown in Fig. 5. Therefore, the output voltage overshoot is very small, only 2 V at a 750 V output.
2) Higher percentage of ZVS ON switch: Using traditional control methods, the arm current is no longer purely ac but contains dc component, leading to asymmetrical currents. This prevents half of the switches from achieving ZVS. Compared to previous control methods, the proposed modulation scheme utilizes the oscillation of the input current, enabling soft switching for all switches except those involved in duty cycle adjust SMs. In 32 SMs MMRDC, more than switches of 31 SMs can achieve soft switching. So the percentage of ZVS ON switch can reach 96.9%.
3) Larger magnetizing inductance: Since the ratio $m = L_m/L_r$ has little impact on the overall output gain, this scheme can use a larger magnetizing inductance to reduce output losses.
4) Control scheme: The combination of control variables K and D has a continuous linear relationship with the output voltage. Compared to previous methods using Feedforward + PI, this modulation scheme only requires simple PI control.

V. CONCLUSION

This work proposed a novel K+D control scheme of MMRDC to improve output voltage overshoot and soft switching. A comprehensive analysis of the modulation strategy and operational principle is analyzed. Based on this, dc voltage gain and the soft switching characteristic of the converter are presented. The control scheme not only allows the converter for continuous adjustment when the K value changes but also basic PI control mechanism can be chosen. The working frequency remains constant, facilitating the design of magnetic components. Importantly, the m value does not constrain the voltage gain and can be increased to minimize magnetizing current to improve conversion efficiency. Finally, simulations on a 200 kW MMRDC that converts 9–18 kV to 750 V have been presented to verify the effectiveness of theoretical analysis and control strategies. Experimental results from a prototype are also provided to demonstrate its feasibility. The findings indicate that the K+D control scheme of MMRDC is a promising candidate in MV-LV applications with wide input.

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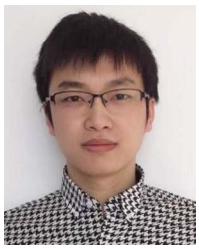

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