Diagnosing Thermal-Interface Aging of Power Devices Using Self-Sensing

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***Abstract*—In this article, we propose a unique and simple method that diagnoses multiple aging effects in power electronic devices minimally invasively and without the necessity of expensive sensors. Different degradation modes, e.g., fatigue of solder and thermal-interface layers, influence the phase of the thermal impedance frequency response function $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ at specific bandwidths. Thus, tracking changes of the thermal impedance's phase, i.e., the phase shift between periodic device-loss excitation at specific frequencies and the resulting junction temperature response allows identifying these degradation modes. This is exploited by the proposed method for degradation diagnosis, which takes advantage of the temperature dependency of the drain-source voltage. The method excites periodic conduction losses at selected frequencies via small-signal manipulation of the gate-source voltage and measures the phase delay between gate-source and drain-source voltage. The measurable phase delay results partially from the dynamic response of the thermal impedance, because the phase-delayed junction temperature impacts the ON-state resistance and therefore the drain-source voltage. Consequently, changes of the measurable phase delay allow identifying changes of $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ and thus diagnosing the above mentioned degradation modes. This article features a detailed analysis of the proposed method using a general sensitivity analysis. A detailed analysis shows that the discussed method is applicable for silicon (Si) MOSFETs, gallium nitride (GaN) high-electron-mobility transistor (HEMTs) as well as silicon carbide (SiC) MOSFETs. Experiments with SiC MOSFETs, being the most emerging technology in industry, demonstrate that the implemented method can effectively diagnose changes of the thermal path between the device and the heat sink that result from different degradation modes.**

***Index Terms*—Condition monitoring, degradation, fault location, power semiconductor devices, silicon carbide (SiC) devices, thermal impedance.**

I. Introduction

POWER electronic systems are emerging in a wide range of applications that demand zero-downtime and highly reliable operation. Examples, such as manufacturing plants, energy systems, and offshore wind parks, have in common that downtime is costly and unplanned maintenance difficult and expensive. Operating power converters reliably in these applications without costly over-sizing requires condition monitoring [2], [3], [4] and state-of-health diagnostics [5], [6], [7] as key technologies. The collected state-of-health data enables the use of predictive maintenance schemes [8], [9], [10] that operate converters systems safely over the maximal feasible lifetime. When critical degradation is reached, the predictive maintenance scheme triggers a replacement request, such that the converter unit is replaced in time during the next planned maintenance.

Bond wire lift-off [11], [12], chip failure, such as bias-temperature-instability [13], [14] or gate-oxide failures [15], solder fatigue [16], [17], delamination of chip and substrate [18], as well as the deterioration of the convection process [19] are critical degradation modes in power electronic modules that can lead to a converter failure. The last three degradation modes have in common that they change the heat dissipation path of the power device and thus its thermal response. This article focuses on these degradation modes that affect the thermal path. In recent years, various monitoring technologies have been proposed for identifying those degradation modes by monitoring changes of the following thermal characteristics.

1) Thermal interface resistance R_{th} [20], [21].
2) Transient thermal impedance $Z_{\mathrm{th}}(t)$ [22], [23].
3) Thermal impedance frequency response function $Z_{\mathrm{th}}(j\omega)$ [24], [25], [26].

These approaches fundamentally require static or dynamic loss excitation and the accurate measurement or derivation of devices losses and junction temperature. The loss excitation is realized either by controlling the current in the power device [27] or by variation of the switching frequency [28], gate resistance [25] or modulation pattern [29]. For junction temperature measurements, typically temperature-sensitive electrical parameters (TSEPs) [5], [30] are extracted and mapped to a junction temperature estimate $\hat{T}_{\mathrm{j}}$. The device losses are either estimated based on look-up tables or estimators [31], [32], [33]. Alternatively, if the device is operated continuously in conduction mode, the losses can be determined using the measured current and voltage values. However, these approaches show some limitations that make an industrial adaption challenging as follows.

1) Accurate TSEP-based junction temperature determination that is fully calibrated and insensitive to operation

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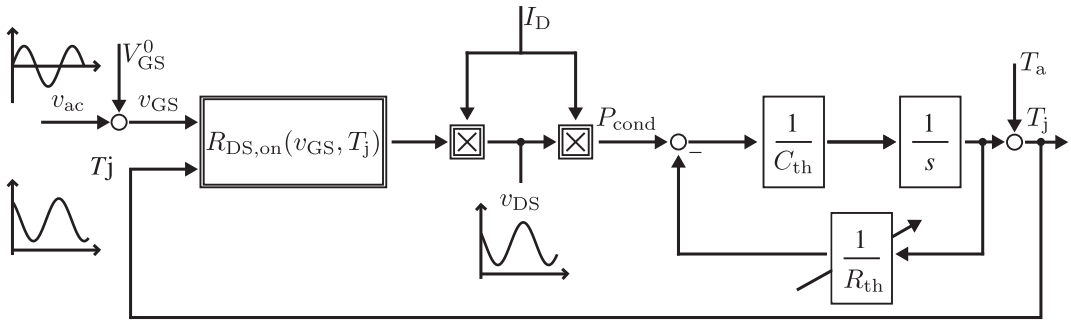

Fig. 1. Block diagram of the physical cause-and-effect relationship between junction temperature, device current and gate voltage in a power transistor using the example of a MOSFET.

point (OP) variations is complex and expensive [30], [34].

2) Device loss estimation either shows significant deviations or is complex due to additional sensors required [32], [33].
3) Most TSEPs are affected by device degradation and therefore require recalibration at different degradation levels [35].

Recent research has addressed the problem of erroneous junction-temperature and loss data by proposing monitoring the phase of the thermal impedance $\phi = \angle \underline{Z}_{\mathrm{th}}(j\omega)$. In [24] and [25], it was shown that thermal impedance frequency response phase $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ excellently reflects relevant degradation modes, such as solder fatigue, delamination and deterioration of the convection process at individual bandwidths. Using thermal impedance frequency response phase $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ is advantageous as it can be extracted with nearly zero error even if the junction temperature or the loss data have offsets or scaling errors, as discussed in [25] and [36]. However, determining $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ still requires junction temperature measurement and loss estimation.

To overcome these limitations, this article proposes a unique and simple method that takes advantage of the degradation-sensitive properties of the thermal impedance frequency response phase $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ without dedicated junction temperature measurement or loss estimation. The method modulates a small-signal excitation on the gate voltage of a power device at different frequencies. Consequently, it measures the resulting drain-source voltage, which is influenced by the junction temperature due to the temperature sensitivity of $R_{\mathrm{DS,on}}$, and extracts the phase delay between both voltages. This phase delay is influenced by the thermal impedance frequency response phase $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ that is affected by all aging effects in the heat dissipation path, e.g., in solder and thermal-interface layers as well as in the cooling system.

This article, which builds on [1], first presents the proposed degradation diagnosis method in general and analyzes its degradation sensitivity. Subsequently, the applicability of the degradation diagnosis method for state-of-the-art power devices, i.e., silicon (Si) MOSFETs, gallium nitride (GaN) HEMTs, and silicon carbide (SiC) MOSFETs, is evaluated. For the specific case of SiC MOSFETs, design considerations as well as the hardware and digital implementation are discussed. Experimental results demonstrate the feasibility of the approach. In this article, we conclude with a discussion of the remaining challenges of the proposed method and a conclusion.

II. Method for Degradation Diagnosis Based on Electrical Response

This section describes the proposed degradation diagnosis method using an n-channel MOSFET as an example. The method builds on the concept of in-situ thermal impedance spectroscopy for detecting and localizing degradation as presented in [37]. However, it does not require explicit temperature measurements, which strongly reduces the implementation effort, as described in the following. The block diagram in Fig. 1 illustrates the operation principle of the method that is explained in the following.

The method applies a constant drain current I_{D} to the MOSFET that is operated in conduction mode and superimposes a constant gate voltage V_{GS}^0 with a periodic small-signal excitation v_{ac}, e.g., a sinusoidal or rectangular voltage [1], [38]. In this article following, a sinusoidal excitation is assumed. The resulting conduction losses of the MOSFET can be calculated as follows:

$$P_{\mathrm{loss}} = v_{\mathrm{DS}} \cdot I_{\mathrm{D}} = R_{\mathrm{DS,on}}(v_{\mathrm{GS}}, T_{\mathrm{j}}) \cdot I_{\mathrm{D}}^2 \tag{1}$$

where v_{DS} is the forward voltage, $R_{\mathrm{DS,on}}$ is the ON-state resistance, and I_{D} is the drain current of the MOSFET. The excitation of the gate with the superimposed ac voltage v_{ac} leads to a periodic modulation of the $R_{\mathrm{DS,on}}$, v_{DS} and P_{loss} due to the dependency of the ON-state resistance $R_{\mathrm{DS,on}}$ on the gate-source voltage v_{GS} [39]. Neglecting temperature dependency and aging, the small-signal excitation of $R_{\mathrm{DS,on}}$, v_{DS}, and P_{loss} show a constant phase delay of $180\,^\circ$ with respect to the gate excitation v_{ac} at low excitation frequencies.

The thermal impedance $\underline{Z}_{\mathrm{th}}(j\omega)$, which is shown in Fig. 1 simplified as a thermal resistance R_{th} and a thermal capacitance C_{th}, determines the ac-response of the junction temperature T_{j} in magnitude and phase in response to the loss excitation. This response of the junction temperature T_{j} feeds back on $R_{\mathrm{DS,on}}$ and thus on v_{DS}, because the ON-state resistance $R_{\mathrm{DS,on}}$ is influenced by the junction temperature T_{j} as well.

Degradation, such as solder and thermal interface degradation as well as changes of the cooling conditions, change the phase of the thermal impedance $\angle \underline{Z}_{\mathrm{th}}(j\omega)$ at specific frequency bands, as investigated in [7], [26], and [37]. To evaluate the change in

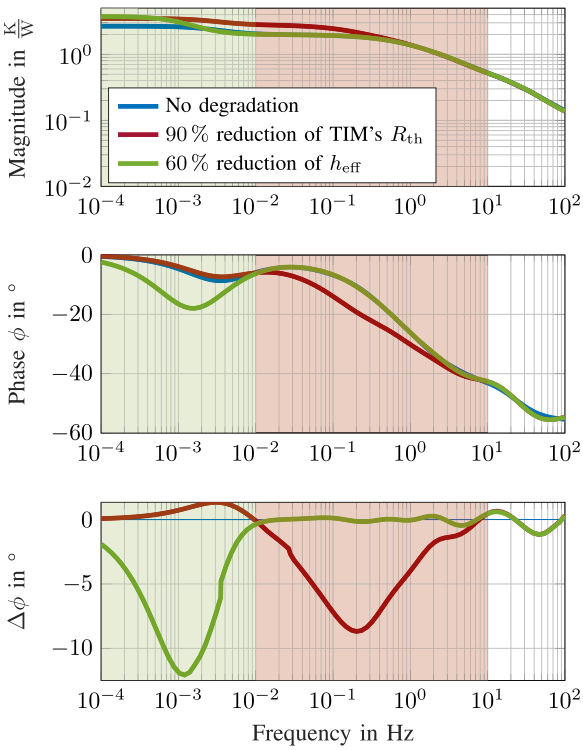

Fig. 2. Simulatively determined thermal impedance Zth for different exemplary degradation modes of the SiC MOSFET Easy 1B module (FF45MR12W1M1_B11) from Infineon.

thermal impedance due to different degradation modes, a 3-D finite volume model of an exemplary Easy 1B power module from Infineon has been created according to the work in [7], [40], and [41]. Three different degradation modes have been created: a non-degraded setup of a power module connected to a heat sink via thermal grease, a setup, where the thermal resistance has been decreased to 10% of its original value and a setup where the convection of the heat sink has been reduced by reducing the average heat transfer coefficient h_{eff} to 40%. Fig. 2 shows the magnitude and phase of the created thermal model as well as the change in phase relative to the non-degraded state. Most importantly for this work, the thermal impedance phases show individual valleys at 1 mHz for convection degradation and at 200 mHz for thermal interface material (TIM) degradation. Thus, tracking thermal impedance phase and phase changes around these two frequencies is of particular interest if the state-of-health of the TIM and the cooling system is monitored.

As a consequence of the junction temperature feedback, also the phase displacement between v_{DS} and v_{ac} changes when these degradation mechanisms occur. Thus, changes in the phase shift between v_{GS} and v_{DS} observed a specific frequency bands indicate changes of the thermal impedance phase $\angle\underline{Z}_{\text{th}}(j\omega)$ and thus allow diagnosing the above mentioned degradation modes. Therefore, the proposed method excites periodic device losses at degradation-sensitive frequency bands and measures the phase shift that is observed between v_{ac} and v_{DS}. This enables detecting and quantifying degradation modes, i.e., solder and thermal interface deterioration as well as changes of the cooling system conditions, without explicitly measuring junction temperatures or device losses.

III. Sensitivity Analysis

To investigate the sensitivity of the phase shift between v_{GS} and v_{DS} to changes of the thermal impedance phase $\phi(\omega)$ an OP analysis of the power device is conducted. The electrothermal conduction behavior of the power device is represented as a state block diagram in Fig. 1. The operating point analysis linearizes the non-linear dynamic behavior of the power device around a given operating point gate-source voltage V_{GS}^0, drain current I_{D} and junction temperature T_{j}^0. Thus, it predicts the ac response of the device voltage $v_{\text{DS}} = V_{\text{DS}}^0 + \hat{V}_{\text{DS}} \cdot \sin(\omega t + \phi)$ to a sinusoidal excitation of the gate voltage $v_{\text{GS}} = V_{\text{GS}}^0 + \hat{V}_{\text{GS}} \cdot \sin(\omega t)$.

First, the dependency of the ON-state resistance $R_{\text{DS,on}}$ from the gate-source voltage v_{GS} and the junction temperature T_{j}, which is generally non-linear, must be linearized. Therefore, the ON-state resistance is modeled as an OP component $R_{\text{DS,on}}^0$ that results from the OP gate-source voltage V_{GS}^0 and the operating point junction temperature T_{j}^0

$$R_{\text{DS,on}} = R_{\text{DS,on}}^0(V_{\text{GS}}^0, T_{\text{j}}^0) + \Delta R_{\text{DS,on}}. \tag{2}$$

Changes around this OP are modeled by $\Delta R_{\text{DS,on}}$ that results from the perturbations of the gate voltage Δv_{GS} and the junction temperature ΔT_{j} around their OP

$$\Delta R_{\text{DS,on}} = \frac{\partial R_{\text{DS,on}}}{\partial T_{\text{j}}}|_{\text{OP}} \cdot \Delta T_{\text{j}} + \frac{\partial R_{\text{DS,on}}}{\partial v_{\text{GS}}}|_{\text{OP}} \cdot \Delta v_{\text{GS}}. \tag{3}$$

The two partial derivatives can be assumed constant at a given OP defined by V_{GS}^0 and T_{j}^0 and are therefore represented by the following coefficients:

$$r_{\text{T}} = \frac{\partial R_{\text{DS,on}}}{\partial T_{\text{j}}}|_{\text{OP}} \quad \text{and} \quad r_{\text{V}} = \frac{\partial R_{\text{DS,on}}}{\partial v_{\text{GS}}}|_{\text{OP}}. \tag{4}$$

With this model, the ON-state resistance's small-signal ac-response $\underline{\hat{R}}_{\text{DS,on}}$ to junction temperature and gate-source voltage excitations, $\underline{\hat{V}}_{\text{GS}}$ and $\underline{\hat{T}}_{\text{j}}$, can be computed and analyzed using complex phasor analysis for a given excitation frequency ω_0

$$\underline{\hat{R}}_{\text{DS,on}} = r_{\text{T}} \cdot \underline{\hat{T}}_{\text{j}} + r_{\text{V}} \cdot \underline{\hat{V}}_{\text{GS}}. \tag{5}$$

The junction temperature phasor $\underline{\hat{T}}_{\text{j}}$ can be computed on the basis of the thermal impedance at the investigated excitation frequency $\underline{Z}_{\text{th}}(j\omega_0)$, the constant drain current I_{D} and the ac-resistance phasor $\underline{\hat{R}}_{\text{DS,on}}$

$$\underline{\hat{T}}_{\text{j}} = \underline{\hat{P}}_{\text{loss}} \cdot \underline{Z}_{\text{th}}(j\omega_0) = \underline{\hat{R}}_{\text{DS,on}} \cdot I_{\text{D}}^2 \cdot \underline{Z}_{\text{th}}(j\omega_0). \tag{6}$$

Inserting (5) provides an equation that can be solved for the junction temperature phasor

$$\underline{\hat{T}}_{\text{j}} = \left(r_{\text{T}} \cdot \underline{\hat{T}}_{\text{j}} + r_{\text{V}} \cdot \underline{\hat{V}}_{\text{GS}}\right) \cdot I_{\text{D}}^2 \cdot \underline{Z}_{\text{th}}(j\omega_0) \tag{7}$$

$$\underline{\hat{T}}_{\text{j}} = \frac{r_{\text{V}}}{\frac{1}{\underline{Z}_{\text{th}}(j\omega_0) I_{\text{D}}^2} - r_{\text{T}}} \cdot \underline{\hat{V}}_{\text{GS}}. \tag{8}$$

Inserting (8) into (5) provides an equation that determines $\hat{\underline{R}}_{\mathrm{DS,on}}$ on the basis of $\hat{\underline{V}}_{\mathrm{GS}}$ independently of the junction temperature

$$\hat{\underline{R}}_{\mathrm{DS,on}} = \left(\frac{1}{\frac{1}{\underline{Z}_{\mathrm{th}}(j\omega_0) I_{\mathrm{D}}^2 r_{\mathrm{T}}} - 1} + 1 \right) \cdot r_{\mathrm{V}} \cdot \hat{\underline{V}}_{\mathrm{GS}}. \tag{9}$$

Utilizing that the ac drain-source voltage $\hat{\underline{V}}_{\mathrm{DS}}$ can be computed on the basis of the ac ON-state resistance $\hat{\underline{R}}_{\mathrm{DS,on}}$ and the drain current I_{D}, the following OP transfer function can be derived for arbitrary excitation frequencies:

$$\frac{\hat{\underline{V}}_{\mathrm{DS}}(j\omega)}{\hat{\underline{V}}_{\mathrm{GS}}(j\omega)} = \left(\frac{1}{\frac{1}{\underline{Z}_{\mathrm{th}}(j\omega) I_{\mathrm{D}}^2 r_{\mathrm{T}}} - 1} + 1 \right) \cdot r_{\mathrm{V}} I_{\mathrm{D}} \tag{10}$$

$$= \frac{r_{\mathrm{V}} I_{\mathrm{D}}}{1 - |\underline{Z}_{\mathrm{th}}(\omega)| \cdot \exp\left(j\phi(\omega)\right) I_{\mathrm{D}}^2 r_{\mathrm{T}}}. \tag{11}$$

Introducing the variable $\mu(\omega)$ according to (12) allows to simplify this transfer function to (13)

$$\mu(\omega) = |\underline{Z}_{\mathrm{th}}(\omega)| I_{\mathrm{D}}^2 r_{\mathrm{T}} \tag{12}$$

$$\frac{\hat{\underline{V}}_{\mathrm{DS}}(j\omega)}{\hat{\underline{V}}_{\mathrm{GS}}(j\omega)} = \frac{r_{\mathrm{V}} I_{\mathrm{D}}}{1 - \mu(\omega) \exp\left(j\phi(\omega)\right)}. \tag{13}$$

The amplitude response depends strongly on $r_{\mathrm{v}} \cdot I_{\mathrm{D}}$. To make sure that the answer v_{DS} is measurable, $r_{\mathrm{v}} \cdot I_{\mathrm{D}}$ must be above a certain threshold such that excitations $\hat{\underline{V}}_{\mathrm{GS}}$ at excitation frequencies of interest lead to a measurable response $\hat{\underline{V}}_{\mathrm{DS}}$.

Based on the transfer function, the observable phase shift $\psi(\omega)$ between $\hat{\underline{V}}_{\mathrm{DS}}$ and $\hat{\underline{V}}_{\mathrm{GS}}$ can be effectively determined as a function of the magnitude $|\underline{Z}_{\mathrm{th}}(\omega)|$ and the phase $\phi(\omega)$ of the thermal impedance $\underline{Z}_{\mathrm{th}}(j\omega) = |\underline{Z}_{\mathrm{th}}(\omega)| \cdot \exp\left(j\phi(\omega)\right)$

$$\psi(\omega) = \angle \left(\frac{\hat{\underline{V}}_{\mathrm{DS}}}{\hat{\underline{V}}_{\mathrm{GS}}} \right) = \angle \left(\frac{-1}{1 - \mu(\omega) \exp\left(j\phi(\omega)\right)} \right) \tag{14}$$

$$= 180\,^\circ + \tan^{-1} \left(\frac{\sin(\phi(\omega))}{\mu^{-1}(\omega) - \cos(\phi(\omega))} \right). \tag{15}$$

The phase offset of $180\,^\circ$ in (15) results from the coefficient r_{V} that is always negative for MOSFETs as well as HEMTs. Depending of the sign of μ, the electrical phase is above or below $180\,^\circ$.

The value of $\mu(\omega)$ strongly influences how the thermal impedance phase $\phi(\omega)$ can be observed in the phase shift $\psi(\omega)$ between $\hat{\underline{V}}_{\mathrm{GS}}$ and $\hat{\underline{V}}_{\mathrm{DS}}$. At increasing excitation frequencies ω the value of $\mu(\omega)$ becomes smaller, because the magnitude of thermal impedance $|\underline{Z}_{\mathrm{th}}(\omega)|$ is reduced at high bandwidth. Depending on the polarity of r_{T}, whose characteristics are discussed in the following section for state-of-the-art power devices, the polarity of $\mu(\omega)$ can be either positive or negative.

The sensitivity of the voltage phase delay to changes of the thermal impedance phase $\phi(\omega)$ can be determined by calculating the partial derivative of (15)

$$\frac{\partial \psi}{\partial \phi} = \frac{\cos(\phi(\omega))\mu^{-1}(\omega) - 1}{\mu^{-2}(\omega) - 2\cos(\phi(\omega)\mu^{-1}(\omega) + 1}. \tag{16}$$

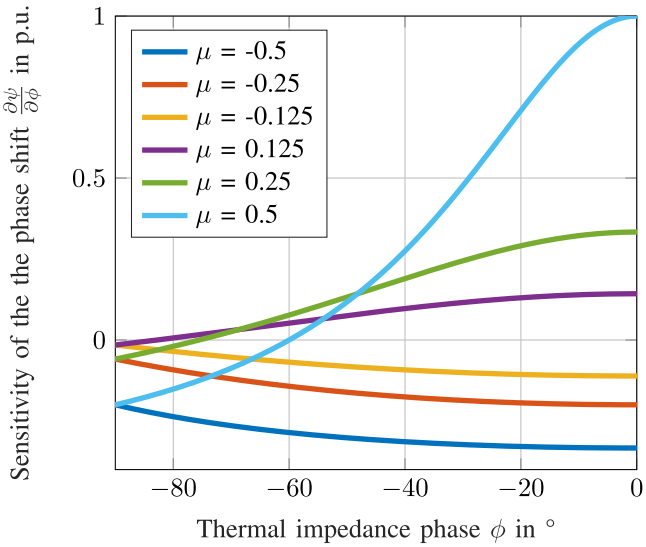

Fig. 3. Sensitivity of the voltage phase shift with respect to the thermal impedance phase as a function of μ [1].

TABLE I
DATA SHEET VALUES OF THE ANALYZED DEVICES

Semiconductor	Name	$V_{\mathrm{DS,max}}$	$I_{\mathrm{DS,max}}$	V_{th}
Si-MOSFET	STW30N80K5	800 V	24 A	4 V
GaN HEMT	GS66506	650 V	22.5 A	1.7 V
SiC-MOSFET	FF45MR12W1M1_B11	1200 V	25 A	4.5 V

The sensitivity is plotted for a range of values for $\mu(\omega)$ in Fig. 3. Both, positive and negative values of $\mu(\omega)$ allow observing thermal impedance phase changes $\Delta\phi$ via the electrical phase shift $\Delta\psi$. Degradation effects, such as defects of the solder or thermal interface layers as well as a change the of convection conditions impact the thermal impedance phase typically at phase values between $0\,^\circ$ to $-\,60\,^\circ$, as discussed in [37]. If μ approaches zero, the sensitivity gets lost. To avoid this, the temperature dependency of $R_{\mathrm{DS,on}}\, r_{\mathrm{T}}$ must not be zero.

The sensitivity is highest at a thermal impedance phase $\phi(\omega)$ of zero. The more the thermal impedance phase approaches $-60\,^\circ$, the more the sensitivity declines. As a negative $\mu(\omega)$ results in a better sensitivity at declining phases in comparison to a positive $\mu(\omega)$, this brings a small advantage. However, most degradation effects do not occur at highly negative phases such that a positive $\mu(\omega)$ can be practically utilized as well.

IV. APPLICABILITY FOR DIFFERENT SEMICONDUCTOR TECHNOLOGIES

The following section discusses the applicability of the discussed method for MOSFETs with Si and SiC as well as GaN-HEMTs. For this purpose, $R_{\mathrm{DS,on}}$ of exemplary devices for different currents I_{D}, gate-source voltages v_{GS} and temperatures T was measured using a curve tracer from Keysight. The device's data-sheet values of blocking voltage $V_{\mathrm{DS,max}}$, maximum continuous drain current $I_{\mathrm{DS,max}}$, and typical threshold voltage V_{th} are summarized in Table I. Each measurement was repeated three

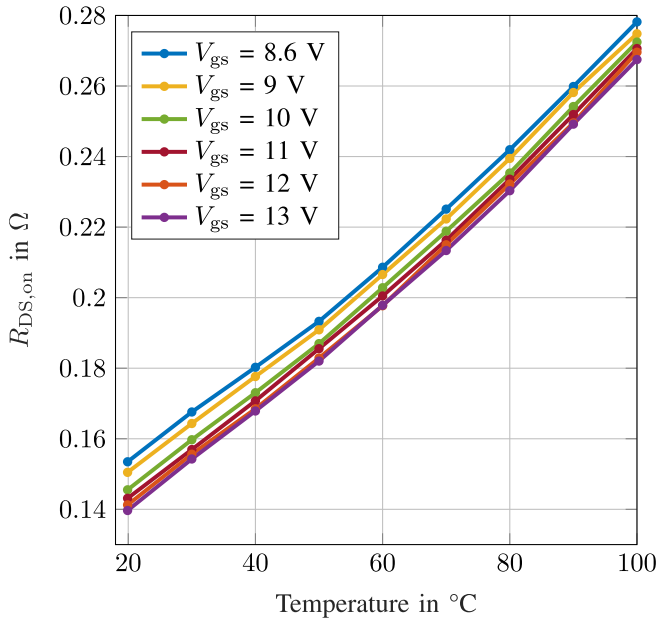

Fig. 4. Course of $R_{DS,on}$ of the exemplary Si MOSFET over temperature for different V_{gs} while I_D is kept constant at 5 A.

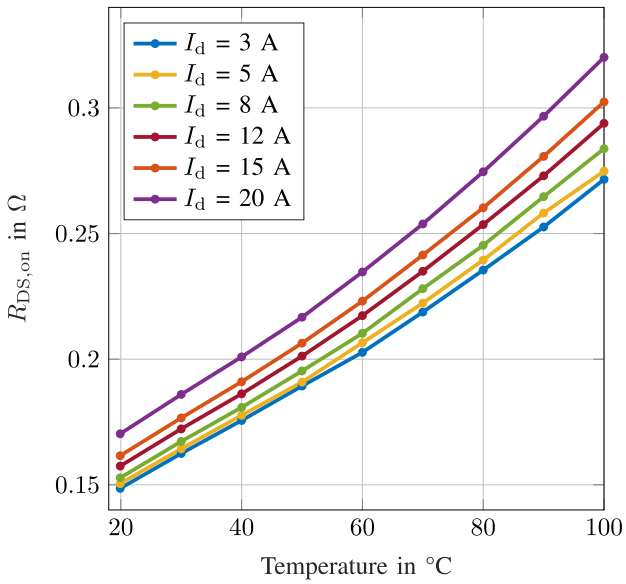

Fig. 5. Course of $R_{DS,on}$ of the exemplary Si MOSFET over temperature for different I_D while V_{gs} is kept constant at 9 V.

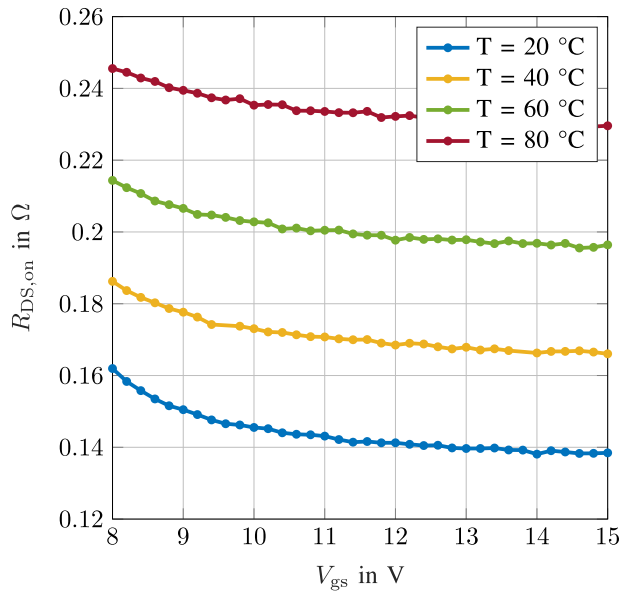

Fig. 6. Course of $R_{DS,on}$ of the exemplary Si MOSFET over gate voltage for different temperatures while I_D is kept constant at 5 A.

times. The plotted values of the graphs in the following section correspond to the median of the measured values.

A. Silicon MOSFETs

The Si MOSFET under consideration is the STW30N80K5 from STMictroelectronics. Its data sheet values are summarizes in Table I. Fig. 4 shows the course of $R_{DS,on}$ over temperature at different gate-source-voltages V_{gs} and a constant drain current of 5 A. The temperature dependency of the ON-state resistance r_T of this MOSFET is positive over the entire measured temperature range. Moreover, the temperature dependency has a constant value at around $r_T = 1.5\,\mathrm{m\Omega\,K^{-1}}$, independent of gate voltage and temperature. Therefore, a changed sensitivity of the described degradation diagnosis with changing ambient temperature or changed gate-source voltage offset is not expected. As can be seen in Fig. 5, $R_{DS,on}$ increases with rising drain current I_D. However, temperature dependency r_T is only slightly affected by this and becomes non-linear for high currents only. As shown in (12) and (15), the degradation-dependent phase shift, is nevertheless dependent on the amplitude of the drain current. Therefore, it should be kept constant for the measurement or must be calibrated for.

For all considered voltages, currents and temperatures of Si MOSFETs, temperature dependency r_T is positive. According to (12), a positive value of r_T causes a positive μ. Fig. 3 shows that positive values for μ lead to a non-constant sensitivity with a sign change, i.e., a zero crossing, depending on the phase of the thermal impedance, as can be seen in Fig. 3. Therefore, the expected angle of the thermal impedance ϕ has to be taken into account when choosing the drain current to ensure that the sensitivity is large enough. Moreover, the sign of μ influences the electrical phase. While a negative μ leads to an electrical phase $\psi \geq 180\,^\circ$ for $-90\,^\circ \leq \phi \leq 0\,^\circ$, the electrical phase for a positive μ can be either above or below $180\,^\circ$, depending on the absolute value of μ.

To evaluate r_V of the considered MOSFET, the data from Fig. 4 is replotted to show the course of $R_{DS,on}$ over V_{gs} for different temperatures in Fig. 6. It shows that the voltage dependency r_V of $R_{DS,on}$ decreases with increasing V_{gs} as the transistor enters saturation mode. Therefore, V_{GS}^0 needs to be chosen low enough to ensure that r_v stays above the threshold $r_{v,min}$.

B. GaN E-Mode HEMTs

To evaluate the applicability of the method with a GaN e-mode HEMT, the top side cooled GS66506T from GaN Systems

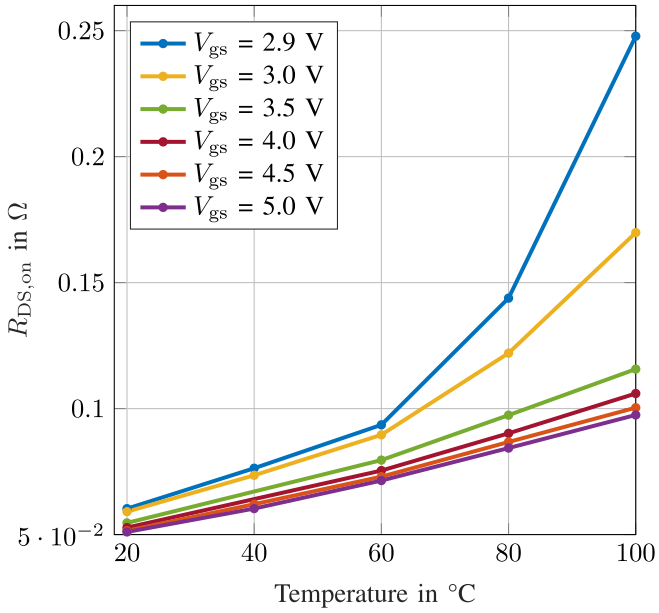

Fig. 7. Course of $R_{DS,on}$ of the exemplary GaN HEMT over temperature for different V_{gs} while I_D is kept constant at 5 A.

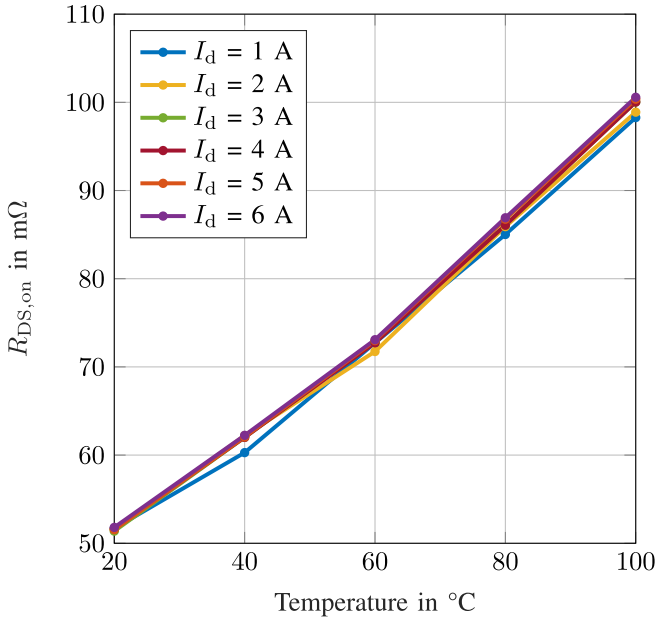

Fig. 8. Course of $R_{DS,on}$ of the exemplary GaN HEMT over temperature for different I_D while V_{gs} is kept constant at 4.5 V.

whose electrical parameters are summarized in Table I, was investigated.

Fig. 7 shows the measured temperature dependency of $R_{DS,on}$ for different V_{gs} at a drain current I_D of 5 A. It can be seen, that r_T is positive just as for the silicon device depicted in Section IV-A. Therefore, the consequences concerning variable μ discussed for the Si device apply here as well. However, unlike the Si device, the measured GaN device exhibits a non-linear temperature dependency. For the considered operating range, the temperature sensitivity increases with rising temperature. This applies in particular for low gate-source voltages. Fig. 8

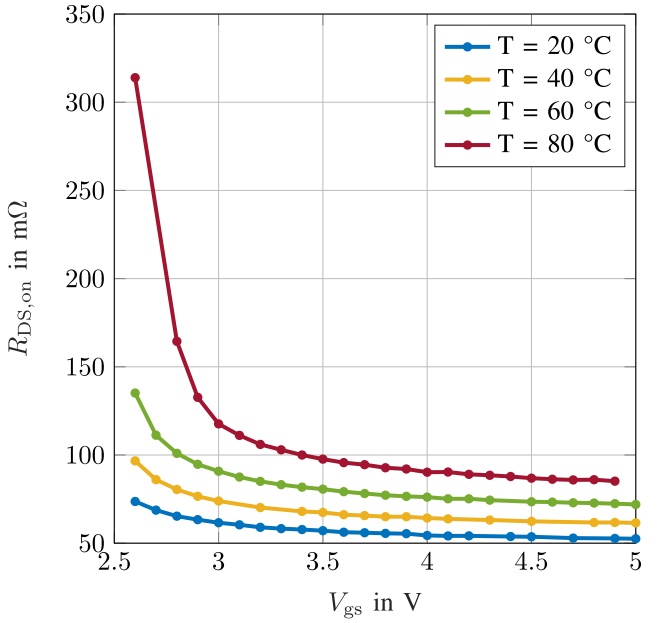

Fig. 9. Course of $R_{DS,on}$ of the exemplary GaN HEMT over gate voltage for different temperatures while I_D is kept constant at 5 A.

shows, that $R_{DS,on}$ does not show a current sensitivity, if the device currents remain small.

Consequently, the device current only influences the value of μ but does not have an effect on r_T. The decreasing gate-voltage sensitivity of $R_{DS,on}$ that has already been described for Si MOSFETs in Section IV-A, can also be observed for GaN HEMTS as shown in Fig. 9. It is noticeable that this voltage dependency increases for higher temperatures.

C. Silicon Carbide MOSFETs

To analyze the applicability of the proposed method with SiC MOSFETs, a MOSFET of the Infineon SiC Module FF45MR12W1M1_B11 from Table I has been investigated. In contrast to the temperature curves of $R_{DS,on}$ of Si MOSFETs and GaN HEMTs, the ON-state resistance of SiC MOSFETs is not monotonously increasing with temperature. At low temperatures and low gate voltages, $R_{DS,on}$ decreases with increasing temperatures. This effect will be explained in the following.

The ON-state resistance of SiC MOSFETs is made up of four resistance components with varying properties

$$R_{DS,on} = R_{drift} + R_{CH} + R_{JFET} + R_{contact} \quad (17)$$

with R_{drift} being the drift region, R_{CH} being the channel, R_{JFET} being the junction field effect transistor (JFET) region, and $R_{contact}$ being the contact resistance.

R_{drift} is the resistance of the drift region between the source and drain regions of the MOSFET. The resistance is proportional to the thickness and inversely proportional to the doping concentration of the drift region [42]. Due to the high breakdown field of SiC, the drift region can be thinner than in Si devices, reducing the drift resistance [43].

The channel of MOSFETs is generated by applying a positive gate bias voltage causing electrons to be attracted to form a

conductive path between source and drain. The channel resistance R_{CH} depends on the oxide interface quality and the charge carrier mobility [42]. The charge carrier mobility is usually significantly lower in SiC compared to Si MOSFETs, resulting in a higher channel resistance [43].

The JFET region is located in the n-drift region at the edge of the p-well fpr n-channel SiC MOSFETs and is so-called because of its similar behavior to a JFET. The resistance R_{JFET} is dominantly dependent on the width and the doping concentration. The resistance value is therefore strongly linked to the design of the JFET region [42].

The contact resistance R_{contact} is predominantly influenced by the metallization of the source and drain regions. The resistance value depends on the metallization technique used and the design of the contacting surfaces [42].

For high gate bias voltages, e.g., the data sheet recommended positive gate voltage, the ON-state resistor $R_{\mathrm{DS,on}}$ is dominated by the drift resistor R_{drift} and the JFET resistor R_{JFET}. Both resistor components have a positive temperature coefficient, resulting in the ON-state resistance also increasing with rising temperatures. This property helps with current balancing between parallel semiconductors and increases the short-circuit withstand time, which is why this resistor behavior is preferred. If the gate bias voltage is reduced in relation to the value recommended by the manufacturer, the channel resistance R_{CH} becomes more dominant in its influence on $R_{\mathrm{DS,on}}$. The channel resistance has a negative temperature coefficient, causing $R_{\mathrm{DS,on}}$ to decrease with increasing temperature. The negative temperature coefficient can be attributed to the low transconductance of SiC MOSFETs at lower gate bias voltages, which is distinctly different from Si MOSFETs. Low gate-source voltages are not recommended for normal operation of SiC MOSFETs, as this can lead to an uneven device current distribution of parallel semiconductors and thus to thermal runaway. [44], [45]

The negative temperature coefficient r_{T} at low gate-source voltages can be seen in Fig. 10. According to (12), this leads to a negative μ. This in turn leads to a phase shift ψ above $180\,^{\circ}$ (15). Moreover, a negative μ leads to a negative sensitivity of the electrical phase ψ to changes of the thermal impedance's phase ϕ in the relevant range of $-60^{\circ} < \phi < 0^{\circ}$. When operating the SiC MOSFET at an operating point where r_{T} is negative, no zero crossing of the sensitivity will occur. The magnitude of r_{T} is not only influenced by the gate-source voltage v_{GS} but also by the drain current I_{D} as shown in Fig. 11. The change in r_{T} due to variation of the OP shows that keeping I_{D} and T_{j}^{0} constant during the measurement is particularly important for SiC devices.

Fig. 12 shows the increased gate-voltage sensitivity of $R_{\mathrm{DS,on}}$ for low values of V_{gs}^{0} that has already been described above for the Si and GaN devices.

V. Degradation Sensing Design

This section discusses the degradation sensing design. For that purpose, the SiC MOSFET Module FF45MR12W1M1_B11 from Infineon is used as an example. The degradation modes of the power module, whose monitoring is investigated in this work, are degradation of TIM and convection.

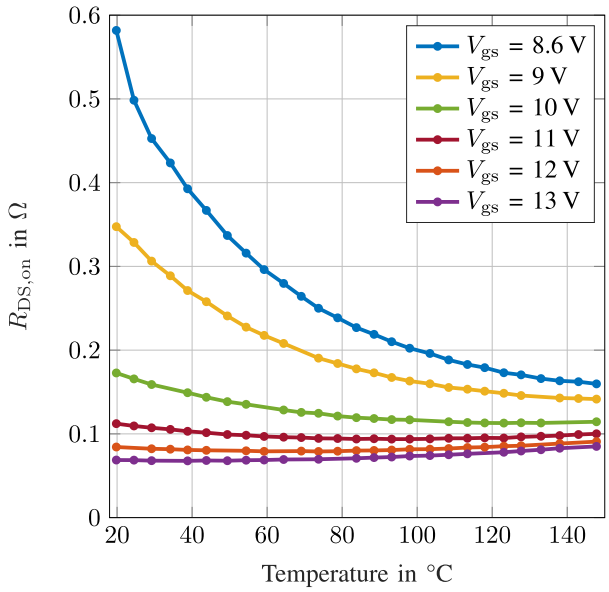

Fig. 10. Course of $R_{\mathrm{DS,on}}$ of the exemplary SiC MOSFET over temperature for different V_{gs} while I_{D} is kept constant at 5 A.

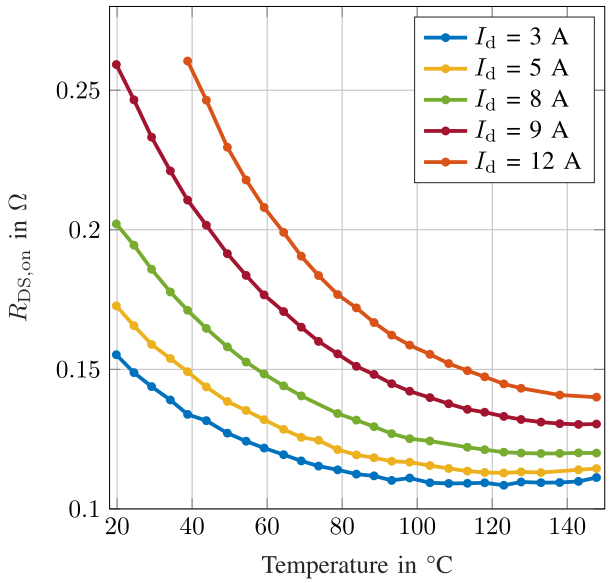

Fig. 11. Course of $R_{\mathrm{DS,on}}$ of the exemplary SiC MOSFET over temperature for different I_{D} while V_{gs} is kept constant at 10 V.

First, the frequencies are identified, at which each of the degradation modes of interest have the biggest impact on the thermal impedance phase. The degradation induced phase changes that are plotted in Fig. 2 reveal that the convection degradation creates the largest phase change at $f_1 = 1\,\mathrm{mHz}$ whereas the TIM degradation shows the largest phase change at $f_2 = 200\,\mathrm{mHz}$. Thus, the phase sensing should concentrate on these two frequencies. The thermal impedances of the healthy power module at the two frequencies of interest can be determined from Fig. 2

$$\underline{Z}_{\mathrm{th}}(j\omega_1) = 2.5\,\mathrm{K/W}e^{-\mathrm{j}5^{\circ}} \tag{18}$$

$$\underline{Z}_{\mathrm{th}}(j\omega_2) = 2\,\mathrm{K/W}e^{-\mathrm{j}20^{\circ}}. \tag{19}$$

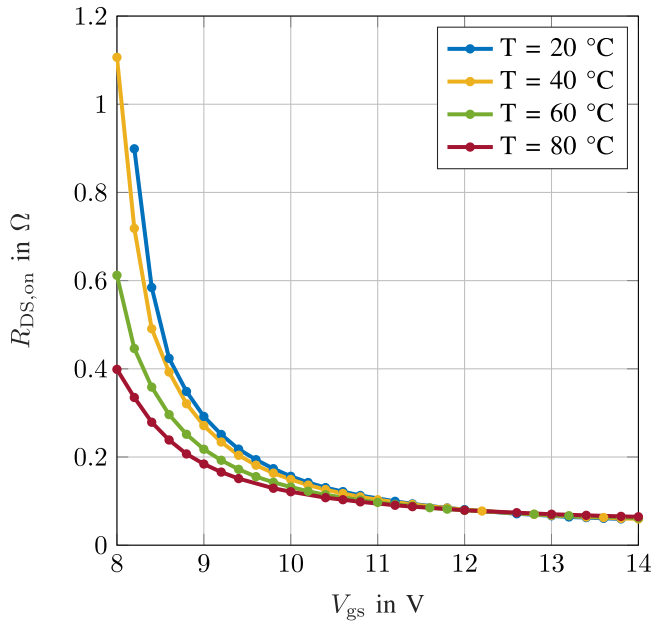

Fig. 12. Course of $R_{\mathrm{DS,on}}$ of the exemplary SiC MOSFET over V_{gs} for different temperatures while I_{D} is kept constant at 5 A.

In the following the selection of a suitable OP, i.e., junction temperature T_{j}^0, gate voltage V_{GS}^0 and device current I_{D}, is discussed. The OP should yield a measurable response to the gate voltage excitation whose phase reflects the changes of thermal impedance phase with high sensitivity at the identified frequencies and thermal impedances. The following equation links the introduced OP variables:

$$T_{\mathrm{j}}^0 = R_{\mathrm{th}} \cdot I_{\mathrm{D}}^2 \cdot R_{\mathrm{ds,on}}\left(V_{\mathrm{gs}}^0, T_{\mathrm{j}}^0, I_{\mathrm{D}}\right) + T_{\mathrm{a}}. \tag{20}$$

It is assumed that the ambient temperature is $T_{\mathrm{a}} = 25\,^{\circ}\mathrm{C}$. Previous findings in [46] have shown that a constant temperature for each measurement is critical to be able to compare phase data. Thus, the junction temperatures T_{j}^0 should be identical for the identification at each excitation frequency. The current I_{D} is given as a function of the selected junction temperature according to the following implicit equation:

$$I_{\mathrm{D}} = \sqrt{\frac{T_{\mathrm{j}}^0 - T_{\mathrm{a}}}{R_{\mathrm{th}} \cdot R_{\mathrm{ds,on}}\left(V_{\mathrm{gs}}^0, T_{\mathrm{j}}^0, I_{\mathrm{D}}\right)}}. \tag{21}$$

Consequently, only the OP gate voltage V_{gs}^0 and junction temperature T_{j}^0 can be freely selected.

The $R_{\mathrm{DS,on}}$ characteristics at different temperature and gate-voltages as well as the resulting sensitivity r_{T}, which are depicted in Fig. 10, are used to evaluate a suitable OP gate voltage V_{GS}^0. The following limitation lead to the selection of the a OP gate voltage of 10 V.

1) $R_{\mathrm{DS,on}}$ increases exponentially and becomes highly nonlinear at gate voltage below 9 V.
2) At gate voltages above 11 V the temperature sensitivity of $R_{\mathrm{DS,on}}$ becomes too small.

For the superimposed ac-voltage excitation of the gate, a voltage amplitude of 1 V is selected to ensure a linear response behavior close while maintaining a sufficient signal level of the excitation and the response.

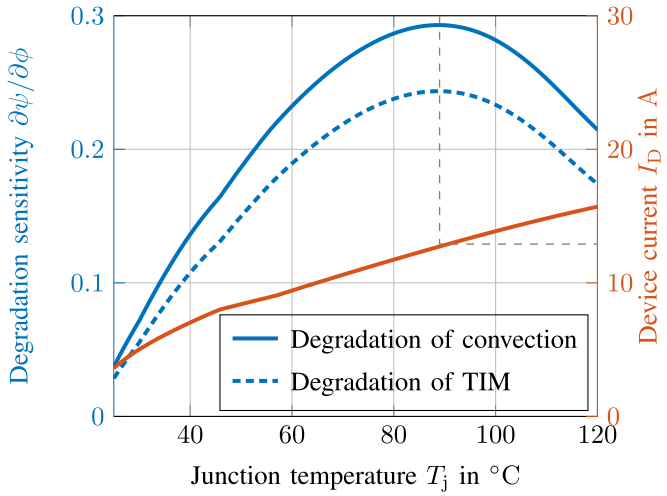

Fig. 13. Device current and degradation sensitivity as a function of the selected OP junction temperature.

Finally, the OP junction temperature needs to be selected. For this purpose, for the two excitation frequencies, ω_1 and ω_2, and a wide range of junction temperatures the required device current is iteratively determined according to (21). Then, the variable $\mu(\omega) = |\underline{Z}_{\mathrm{th}}(\omega)|I_{\mathrm{D}}^2 r_{\mathrm{T}}$ and consequently the sensitivity is calculated. The resulting device current and sensitivity is plotted in Fig. 13 The plot reveals that the maximal sensitivity for degradation of convection and degradation of TIM occurs at a junction temperature of 90 °C that can be obtained with a device current of 13 A. This local maximum of the sensitivity occurs as larger currents directly increase the variable μ. At elevated currents, a further current increment decreases $r_{\mathrm{T}}(I_{\mathrm{D}})$, as can be observed in Fig. 11, which in turn reduces μ . The maximal sensitivity reaches a value of 0.29 in case of convection degradation and 0.24 in case of TIM degradation, which is remarkably high.

VI. Implementation of Excitation and Extraction Circuitry

The following section explains the implementation of the method. For this purpose, the hardware structure to manipulate the gate-source voltage and to measure the gate-source voltage and drain-source voltage is explained first. Afterward, the data processing to extract the phase lag between these two voltages is discussed.

A. Hardware Implementation

To experimentally evaluate the presented method, an extraction circuit for power modules was developed, which is capable of modulating conduction losses and measuring gate-source voltage v_{GS} and drain-source voltage v_{DS}. It can be seen in Fig. 14.

The device under test (DUT), in this case an Infineon Easy 1B module using SiC-MOSFETs (FF45MR12W1M1_B11), is on its bottom side connected to a heat sink. The electrical contacts of

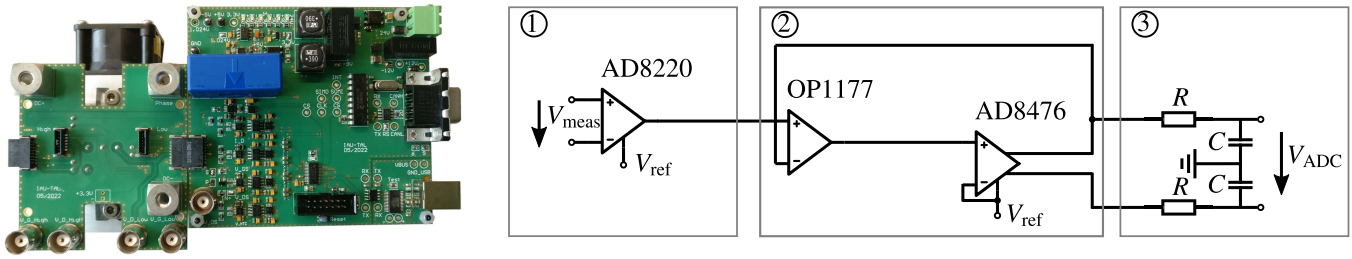

Fig. 14. Extraction circuit with the DUT underneath the PCB (left) and schematic structure of one measuring channel that is connected to the micro controller-internal analog-to-digital-converter (right) [1].

the module are connected to the PCB of the extraction circuitry. A microcontroller unit (MCU) is used to dynamically adjust the gate voltage v_{GS} of the MOSFET via a 12 bit digital-to-analog converter IC. Gate- and drain-source voltage are determined via a measuring unit and a microcontroller-integrated analogue-to-digital converter (ADC). The measuring unit can be divided into three parts: the voltages to be measured v_{meas} are connected to the measuring circuit via an instrumentation amplifier with high input impedance ①. A single ended to fully differential amplifier with a cascaded operation amplifier ② transforms the voltage into a differential signal, which can be transformed into a digital signal by the 24-bit sigma-delta ADC of the MCU after being filtered by an anti-aliasing filter ③.

B. Digital Implementation

The MCU sets the gate voltage by adjusting the output voltage of a 12 b digital-to-analog converter (DAC) via serial peripheral interface (SPI). This output voltage is connected to an instrumentation amplifier which transforms the output voltage to gate-source voltages ranging from -5 to 20 V. The modulation of the gate-source voltage is realized by producing a sinusoidal voltage with a variable sampling frequency at the output of the DAC. The variable update frequency is chosen so that the number of sampling points per period stays constant. The advantage of this method is that the values for one period of the sinusoidal voltage can be stored on the MCU and do not have to be calculated in real time.

The frequency at which the gate-source voltage and drain-source voltage values are updated via the DAC is equal to the sampling frequency of the ADCs. The measured data are sent to an external PC for evaluation.

In postprocessing, a fast Fourier transformation determines the fundamental frequency of v_{GS} and v_{DS}. Afterward, the phase information of the fundamental frequency is used to determine the phase shift between v_{GS} and v_{DS}.

VII. Experimental Verification

The following section describes the experimental verification. First, the experimental setup is explained. Afterward, the results of the measurements are discussed.

A. Experimental Setup

For the experimental verification of the proposed method, the DUT is permanently kept in ON-state and is conducting a constant drain-source current. In Section V, a current of 13 A was identified to lead to a maximum sensitivity of 0.29 for the detection of convection degradation and 0.24 in case of TIM degradation. As a sensitivity of 0.05 to 0.1 is sufficient for a systematic investigation, in this work a lower current of 5 A has been selected, to keep the power rating of the current injection unit low. A small-signal sinusoidal voltage with variable frequency and an amplitude of 1 V is modulated onto the constant gate-source voltage of 10 V. Each frequency is applied to the gate for one sinusoidal period. To investigate the degradation modes shown in Fig. 2, which occur at 1 to 200 mHz, the lowest excited frequency, that significantly determines the duration of the measurement, has been chosen to be 1 mHz.

Changes of the TIM layer are emulated by partially or completely removing the thermal paste between the base plate of the power module and the heat sink. First, the module is connected to the heat sink using an appropriate amount of thermal paste, which represents the "no degradation" condition. The "weak degradation" condition of the thermal path is artificially created by removing the thermal paste at the inner area of the module to decrease the thermal connection between the module and the heatsink. To reduce the heat coefficient between the DUT and the heat sink even further, the thermal paste is removed completely, which corresponds to a "strong degradation" condition of the interface. To emulate changes of the cooling system, the speed of the cooling fan is reduced. The experiment is conducted in a climate chamber at a constant ambient temperature of 25 °C. Each measurement is repeated three times to verify the reproducibility.

B. Experimental Results

The courses of the measured voltages v_{GS} and v_{DS} are shown exemplarily for three frequencies in Fig. 15. It can be seen that the periodic gate-source voltage v_{GS} modulates the drain-source voltage v_{DS} with the same fundamental frequency. The phase shift between these two voltages is extracted for each measured frequency as described in Section VI. This phase shift is shown in Fig. 16 for the three different TIM degradation conditions described in Section VII-A.

As aforementioned, the measurements are repeated three times. The error bars show the maximum and the minimum value of the measured phase shift for each frequency. According to Section II, a change in phase due to TIM degradation is expected at at 200 mHz. This expectation is confirmed by the

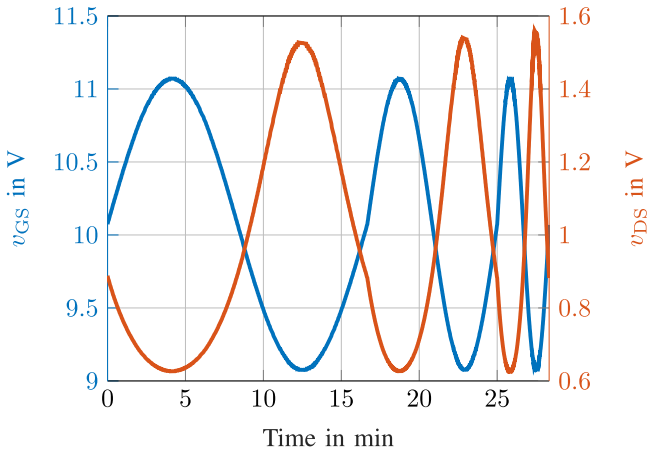

Fig. 15. Courses of the voltages v_{GS} and v_{DS}.

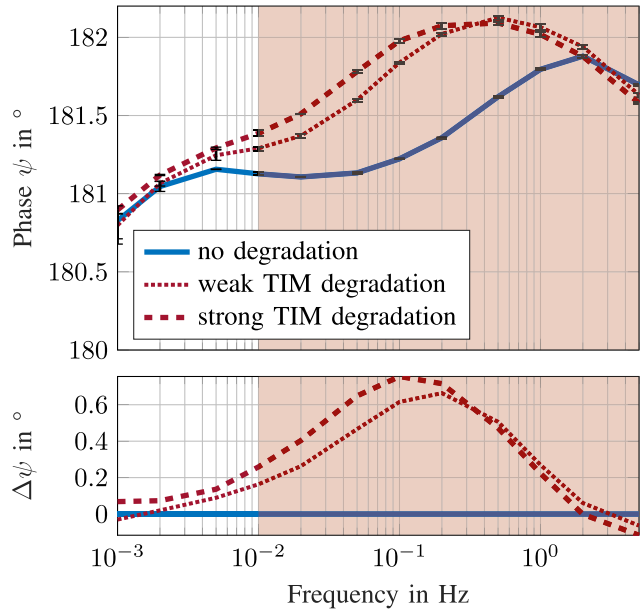

Fig. 16. Extracted phase shift for different states of TIM degradation.

measurement that can be seen in the bottom plot of Fig. 16 that shows the change in phase lag compared to the non-degraded setup. The maximum difference in phase shift of $0.755\,^{\circ}$ appears at $100\,\mathrm{mHz}$ for the "strong degradation" setup. Furthermore, the change in phase shift increases with increasing degradation. It can be seen, that the change in phase shift reaches a peak for the "weak degradation" setup at $200\,\mathrm{mHz}$ with a change in phase shift of $0.664\,^{\circ}$. For the "strong degradation" setup, this peak is slightly shifted toward lower frequencies.

Besides the degradation of the thermal interface, degradation of the cooling system is emulated by reducing the speed of the cooling fan. Fig. 17 shows that significant changes in the phase shift occur at frequencies below $10\,\mathrm{mHz}$.

These findings are consistent with the expectations from Section II, as the bandwidths, at which changes of degradation of a certain location can be seen, are the same.

The results show that even for a small loss excitation in the range of a few watts, changes in the thermal path can easily be

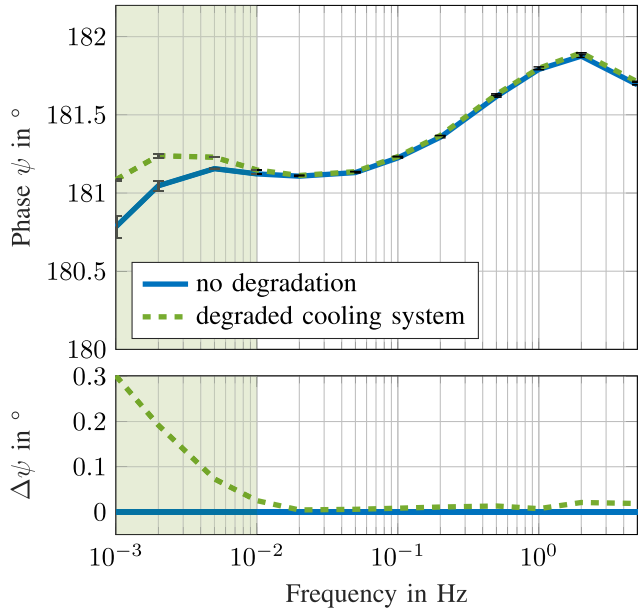

Fig. 17. Extracted phase shift for different degradation states of the cooling system.

detected. Different degradation modes lead to changes of the phase shift at specific bandwidths. Thus, this method is able to localize the degradation. Even though the change in phase shift is relatively small, it can be detected using a simple measuring setup. Multiple repetitions of the described measurement have shown that the results are reproducible.

In [38] and [46], the general applicability of the proposed method was validated via measurements with different power modules, drain currents, and gate-modulation wave forms. Moreover, it could be shown that several degradation effects that occur simultaneously the thermal path can be identified as the distinctive bandwidth does not change for superimposed degradation.

VIII. Discussion of Limitations

The method presented provides a valuable tool to detect degradation in the thermal path of SiC, Si and GaN HEMT power modules. However, there are limitations to the proposed methods, which will be discussed in the following.

1) The degradation detection as presented in this work is not possible during converter operation as the measurements must be carried out at a constant operating point. Further investigation needs to be done to enable online condition monitoring during converter operation, e.g., by decoupling the influence of the drain current and ambient temperature.
2) Experimental verification of the degradation detection method was only shown for SiC MOSFETs. In the future, phase-shift measurements must be carried out for Si-MOSFETs and GaN HEMTs.
3) So far, the influence of electrical aging (e.g., gate-oxide degradation or bond wire lift-off) as well as degradation modes that affect both the electrical and the thermal path

(e.g., die solder delamination) has not been investigated and needs to be taken into account in future research.

4) To be able to estimate the calibration effort, the spread in phase shift between different modules of the same kind in non-degraded condition needs to be examined.
5) This work's focus is the investigation of the proposed method for MOSFETs and HEMTs. As IGBTs are still widely applied in power electronic applications, the applicability of the proposed method for IGBTs is an important topic for future research.

IX. Conclusion

This work presents a new method to diagnose aging of power electronic modules that neither requires loss nor temperature measurements. The method manipulates the gate voltage to excite periodic conduction losses and measures the response of the temperature sensitive drain-source voltage. The temperature sensitivity allows indirectly extracting changes in the phase of the thermal impedance $\angle \underline{Z}_{\mathrm{th}}(j\omega)$. The phase offset of the two voltages can be used to identify several aging effects of the thermal path that would manifest in the thermal impedance phase. Repetitive phase-shift extractions at different excitation frequencies allow localizing degradation modes, as different degradation modes affect specific bandwidths of the thermal impedance. The applicability of the method has been discussed for Si and SiC MOSFETs as well as for GaN HEMTs. Experimental verification has been conducted using the example of a SiC MOSFET.

Acknowledgment

The opinions expressed here are entirely that of the authors.

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