A Soft Startup Method With Natural Short-Circuit Tolerance Features for CLLC Converters

Huan Chen, *Member, IEEE*, Kai Zhang, *Student Member, IEEE*, Leheng Wang, *Student Member, IEEE*, Kai Sun, *Fellow, IEEE*, and Yongdong Li, *Senior Member, IEEE*

***Abstract*—The *CLLC* converter is a high-frequency, high-efficiency isolated bidirectional dc–dc converter. In outdoor application scenarios like electric vehicle fast charging station, short-circuit failure caused by harsh environments is very challenging for the *CLLC* converter. Especially, such short-circuit failure is more likely occurring in startup stage. In this article, a soft startup method with natural short-circuit tolerance features is proposed for *CLLC* converters. A special fixed frequency fixed duty cycle driving scheme is designed and used for realizing soft startup. An operation mode analysis is conducted for proposed soft startup driving scheme, showing its detailed working process and energy transmission characteristics. Besides, a practical startup method using proposed soft startup driving scheme is also illustrated. To clarify the mechanism of natural short-circuit fault tolerance features in the proposed method, a comprehensive dynamic state trajectory analysis is provided, showing that the dynamic state trajectory after short-circuit failure can be restricted within a boundary automatically. As a result, very large short-circuit current is avoided and natural short-circuit tolerance features is realized. Finally, a lab-level prototype is built to verify the proposed method and the corresponding analysis. Experimental results proves that the proposed method achieves excellent short-circuit tolerance performance (short-circuit current is less than 4% of that in conventional method) and similar soft startup performance compared to the conventional method.**

***Index Terms*—*CLLC* converter, operation mode analysis, short-circuit tolerance, soft startup, state trajectory.**

DEFINITION OF IMPORTANT VARIABLES

Variable	*Physical meaning*
f_r	Resonant frequency.
f_s	Switching frequency.
D_{ref}	Critical duty cycle.
k	Inductance ratio.
k_1	Scale factor of the eigen frequency in the P and N mode stages to f_r.
k_2	Scale factor of the eigen frequency in the Z and Z_0 mode stages to f_r.
P_1 to P_4	Undetermined coefficients of time domain expressions in the *P* mode.
N_1 to N_4	Undetermined coefficients of time domain expressions in the N mode.
Z_{01} to Z_{02}	Undetermined coefficients of time domain expressions in the Z_0 mode.
Z_1 to Z_2	Undetermined coefficients of time domain expressions in the Z mode.
ϕ_P	Duration of the *P* mode stage.
ϕ_N	Duration of the N mode stage.
ϕ_{Z0}	Duration of the Z_0 mode stage.
ϕ_Z	Duration of the Z mode stage.
M	Voltage gain.
M_T	Target voltage gain.

Received 25 August 2024; revised 19 October 2024; accepted 31 October 2024. Date of publication 21 November 2024; date of current version 26 December 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52407210 and in part by State Key Laboratory of Power System Operation and Control, Tsinghua University. Recommended for publication by Associate Editor H. H.-C. Iu. *(Huan Chen and Kai Zhang are co-first authors.) (Corresponding author: Kai Sun.)*

The authors are with the State Key Laboratory of Power System Operation and Control, Tsinghua University, Beijing 100084, China (e-mail: chenh18@mails.tsinghua.edu.cn; zhangkai22@mails.tsinghua.edu.cn; wang-lh21@mails.tsinghua.edu.cn; sun-kai@mail.tsinghua.edu.cn; liyd@mail.tsinghua.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3503555.

Digital Object Identifier 10.1109/TPEL.2024.3503555

I. INTRODUCTION

THE *CLLC* converter is a high-frequency and high-efficiency isolated bidirectional dc–dc converter that has gained significant attention from academia and industry due to its excellent soft-switching characteristics [1]. Having a promising topology for bidirectional power transmission, the *CLLC* converter's application spans uninterrupted power supply systems, vehicle-to-grid systems, battery energy storage (BES) systems, electric aircraft, and reversible solid oxide fuel cell systems [2], [3], [4], [5], [6], [7]. The existing researches on *CLLC* converters mainly focus on the parameter design and control methods in different scenarios and better loss modeling of high frequency transformer [8], [9], [10]. In terms of the theoretical modeling of *CLLC* converters, apart from the first harmonic approximation (FHA) method, mode equations, and state trajectories are used for time-domain modeling [11], [12], [13].

Reliability is also an important evaluation criterion for *CLLC* converters, short-circuit fault is one of the most hazardous challenges. Specifically, short-circuit fault may occur randomly at any time during circuit operation, either during steady-state operation, or during startup process [14]. Short-circuit fault in steady-state process is usually caused by circuit faults and are relatively common, but there are also many scenarios that have special requirements for short-circuit faults during the startup process, such as the black startup of the BES system [14], [15], [16] or some sensitive load like aerospace vehicles and electric aircraft [17], [18].

Taking the application scenario of *CLLC* converter for electric vehicle (EV) charging as an example, short-circuit fault protection during charging process is crucial. Xu et al. [19] and Zia et al. [20] indicated that the short-circuit fault depends more on the external environment than the operation state of the converter. Due to the fact that EV charging systems typically operate outdoors, equipment is more susceptible to aging caused by environmental factors such as water immersion, dust accumulation, and salt corrosion, making it more sensitive to voltage changes during startup and prone to short-circuit faults.

The protection methods for the short-circuit fault in steady-state operation are relatively mature, existing short-circuit fault protection methods can be divided into two level: 1) External protection circuits for the hardware level and 2) special control methods for the software level.

More specifically, some typical over-current protection circuits are outlined in [21] and [22], external diodes or other devices are used, but there are some associated reliability and economic challenges need to solve. Recently, researchers have proposed short-circuit fault protection methods at the control level to circumvent additional circuits using the theoretical modeling of *LLC* converters. Duan et al. [23] and Fei et al. [24] limiting the maximum current through state trajectory to achieve constant current control when a short-circuit fault occurs. Similarly, short-circuit protection of *CLLC* converters can be accomplished through control method innovations. Zhuo et al. [25] proposed a short-circuit fault current limiting method for *CLLC* converters using inverted displacement phase control based on the FHA method.

However, the abovementioned methods are mainly for the short-circuit protection in steady-state operation, there still lacks of methods especially aim to the short-circuit fault in startup process. Besides, published researches on soft startup control methods for *CLLC* converters can be categorized into methods based on switching frequency modulation [26], [27], [28], [29] and duty cycle modulation [30], [31], [32]. Details are as follows.

The key of switching frequency modulation methods is to set a high switching frequency at the startup moment and then reduce it to the resonant frequency. Jia et al. [26] pointed out that decreasing the switching frequency can limit the surge current at the startup moment. In order to enhance the accuracy of the frequency modulation process, an alternative soft startup control strategy based on state trajectory is presented in [27], [28], and [29]. The critical initial switching frequency can be obtained by adding a current limit on the state trajectory. However, the abovementioned frequency modulation methods necessitate device operation at higher frequencies, posing challenges for device selection and introducing EMI issues.

To mitigate issues caused by high switching frequency, duty cycle modulation methods are proposed to achieve the same soft startup target. Sadangi et al. [30] and Jung et al. [31] proposed a three-stage hybrid control by integrating duty cycle control to substitute the ultimate pursuit of such a high initial frequency. Furthermore, several pure duty cycle modulation startup control methods are given in [32] by using different modulation rules to achieve nonlinear rise and linear rises of output voltage, respectively. However, both the duty cycle modulation and the frequency modulation methods mentioned above lack the ability of short-circuit protection.

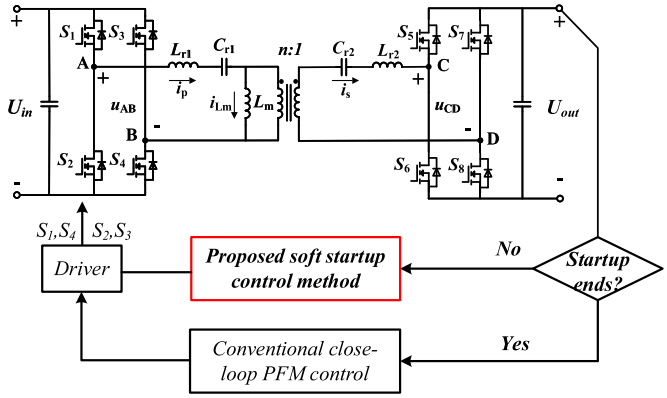

Fig. 1. Schematic diagram of the control logic of the proposed method.

In this article, a soft startup method with natural short-circuit tolerance features for *CLLC* converters is proposed. The corresponding control logic is illustrated in Fig. 1. The basic idea of proposed method is to limit the theoretical maximum transmission energy in every switching cycle, so that damage caused by short-circuit failure in startup stage can be minimized. Based on the basic idea, a special fixed frequency fixed duty cycle driving scheme is designed and used for realizing soft startup. An operation mode analysis is also conducted to analyze the detailed working process and quantitative energy transmission characteristics of proposed driving scheme. After that, a practical startup method using proposed soft startup driving scheme is provided for actual implementation. To further indicate and visualize the mechanism of the natural short-circuit fault tolerance features, a comprehensive dynamic state trajectory analysis is provided. The analysis shows that the dynamic state trajectory after short-circuit failure can be restricted within a boundary automatically. As a result, transmission energy is limited, and very large short-circuit current can be avoided. Verification experiments are conducted and experimental results proved the capability of proposed soft startup method as well as the correctness of corresponding analysis.

The rest of this article is organized as follows. In Section II, the idea of the proposed soft startup control is illustrated ahead. Then, a detailed operation mode analysis is also provided to clarify the detail startup process of proposed soft startup control method. Moreover, the practical work pattern using proposed soft startup control method is given. In Section III, a static state trajectory analysis is introduced to illustrate the startup characteristics and a comprehensive dynamic state trajectory analysis is provided to explain the mechanism of natural short-circuit fault tolerance features under proposed soft startup method. In Section IV, corresponding experimental validation results are provided to verify the proposed soft startup strategy, and the short-circuit fault comparison experimental results of different soft startup control methods are given. Finally, Section V concludes this article. Some boundary rules for the critical duty cycle are given in Appendix A.

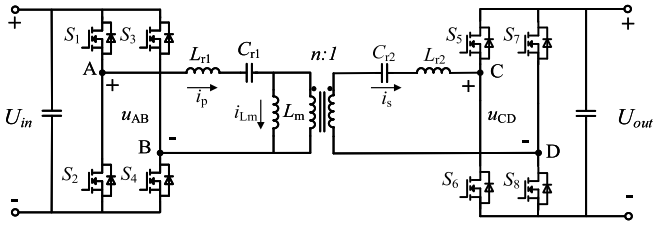

Fig. 2. Topology of a typical *CLLC* converter.

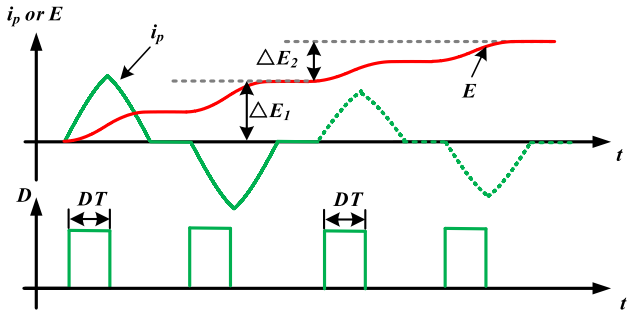

Fig. 3. Imaginary drive scheme with energy limitation features.

II. Proposed Soft Startup Control Method for CLLC Converters and Its Operation Mode Analysis

A. Operating Process Under the Proposed Soft Startup Control Method

Fig. 2 illustrates the topology of a typical *CLLC* converter. S_1 to S_4 are the primary side switches, and S_5 to S_8 are the secondary side switches. The magnetizing current in primary side and secondary side are indicated by i_p, i_s, and i_{Lm}, respectively. The positive directions of voltage and current used in the analysis are also indicated, and the turn ratio of the transformer is denoted as *n*.

Different from traditional soft startup methods based on equivalent voltage gain, this article focuses more on the actual working principle of the circuit, attempting to limit the energy transmitted in each switching cycle during the startup process, so that the converter has short-circuit protection capability while achieving soft startup. To realize such an energy limited startup, Fig. 3 illustrates an imaginary drive scheme: S_1 to S_4 only conduct a short time in a period, and drive signals of S_5 to S_8 are always at off state. As shown in Fig. 3, in every switching period, i_p will rise from zero when S_1 and S_4 are conducting and drop down to zero before the next on state. By this way, the amplitude of i_p is limited instead of increasing cycle by cycle so that the transmitted energy in a cycle is limited, which means the abovementioned energy limitation feature can be realized.

To identify the energy transfer law exactly, the time-domain operation mode analysis method is used, which can be summarized as into five steps named distinguish operation modes, establish equivalent circuits, derive time domain expressions, illustrate boundary conditions, and solve for required characteristics [33]. The following analysis is conducted under the condition that duty cycle $D \leq D_{ref}$, where D_{ref} is a critical value computed in Appendix A to ensure energy limitation characteristics.

Distinguish Operation Modes: As shown in Fig. 4(a), the operating process under the proposed soft startup control method comprises four operation mode stages, they are named as the *P* mode stage, *N* mode stage, Z_0 mode stage, and *Z* mode stage. Since the operating processes in the positive and negative half cycles are symmetrical, the subsequent analysis focuses on the positive half cycle. Details about the operating process are given in [33].

Establish Equivalent Circuits: The circuit working process of each mode is shown in Fig. 4(a), and the equivalent circuits of *P* mode stage, *N* mode stage, Z_o mode stage, and *Z* mode stage employed in the operation mode analysis can be established, as illustrated in Fig. 4(b), respectively.

In the *P* mode stage, the entire resonant tank participates in resonance, where $u_{AB} = U_{\text{in}}$ and $u_{CD} = U_{\text{out}}$. In the *N* mode stage, the whole resonant tank participates in resonance, where $u_{AB} = -U_{\text{in}}$ and $u_{CD} = U_{\text{out}}$. In the Z_o mode stage, only the secondary side of the resonant tank participates in resonance, where $u_{AB} = 0$ and $u_{CD} = U_{\text{out}}$. In the *Z* mode stage, only secondary side of the resonant tank participates in resonance, where $u_{AB} = 0$ and $u_{CD} = -U_{\text{out}}$.

Derive Time Domain Expressions: According to Fig. 4(b), equivalent circuits of *P* mode stage and *N* mode stage are both four-order resonance circuits, and equivalent circuits of Z_0 mode stage and *Z* mode stage are two-order resonance circuits. Therefore, time domain expressions of i_p, i_s, u_{cr1}, u_{cr2} in *P* mode stage, *N* mode stage, Z_o mode stage, and *Z* mode stage can be derived by solving the corresponding resonance circuits.

For simplicity, per-unit form time domain expressions are employed, with the transformer's turn ratio *n* set to 1. The base values for the voltage, current, and impedance are defined as follows:

$$Z_{\text{base}} = \sqrt{\frac{L_r}{C_r}} \quad u_{\text{base}} = U_{\text{in}} \; i_{\text{base}} = \frac{u_{\text{base}}}{z_{\text{base}}} \tag{1}$$

where $L_r = L_{r1} = L_{r2}$, $C_r = C_{r1} = C_{r2}$.

Then the per-unit form time domain expressions of i_p, i_s, u_{cr1}, and u_{cr2} in the *P* mode stage, *N* mode stage, Z_o mode stage, and *Z* mode stage can be expressed in Table I.

Illustrate Boundary Conditions: Boundary conditions are included to solve undetermined variables so that the steady-state condition of *CLLC* converters can be described completely and accurately. Apart from P_1, P_2, P_3, P_4, N_1, N_2, N_3, N_4, Z_{01}, Z_{02}, Z_1, Z_2, another four variables, ϕ_P, ϕ_N, ϕ_{Z0}, and ϕ_Z are defined in Fig. 4(c). They are the durations of the *P* mode stage, *N* mode stage, Z_o mode stage, and *Z* mode stage, respectively.

For the time domain continuity of the primary side current i_p, the secondary side current i_s, the voltage across the primary resonant capacitor u_{cr1}, and the voltage across the secondary side resonant capacitor u_{cr2}, the following boundary conditions

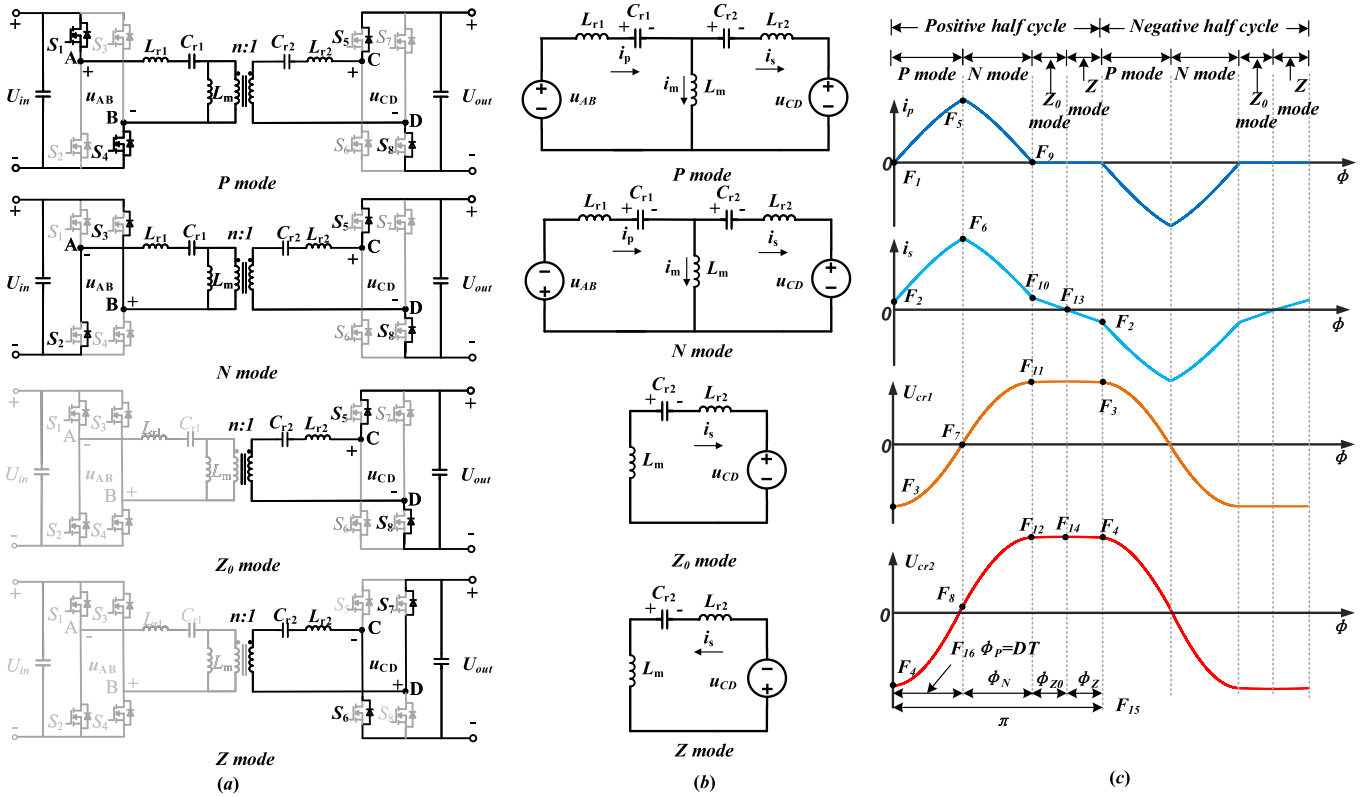

Fig. 4. Operation mode analysis of *CLLC* converters under proposed soft startup control method. (a) Distinguish operation modes. (b) Establish equivalent circuits. (c) Illustrate boundary conditions.

(F_1 to F_{14}) should be satisfied, as Fig. 4(c) shows:

$$\begin{cases} \boldsymbol{F_1} = i_{p,P}\ (0) = 0 \\ \boldsymbol{F_2} = i_{s,P}\ (0) + i_{s,z}\ (\phi_Z) = 0 \\ \boldsymbol{F_3} = u_{cr1,P}\ (0) + u_{cr1,z}\ (\phi_Z) = 0 \\ \boldsymbol{F_4} = u_{cr2,P}\ (0) + u_{cr2,z}\ (\phi_Z) = 0 \\ \boldsymbol{F_5} = i_{p,P}\ (\phi_P) - i_{p,N}\ (0) = 0 \\ \boldsymbol{F_6} = i_{s,P}\ (\phi_P) - i_{s,N}\ (0) = 0 \\ \boldsymbol{F_7} = u_{cr1,P}\ (\phi_P) - u_{cr1,N}\ (0) = 0 \\ \boldsymbol{F_8} = u_{cr2,P}\ (\phi_P) - u_{cr2,N}\ (0) = 0 \\ \boldsymbol{F_9} = i_{p,N}\ (\phi_N) = 0 \\ \boldsymbol{F_{10}} = i_{s,N}\ (\phi_N) - i_{s,z0}\ (0) = 0 \\ \boldsymbol{F_{11}} = u_{cr1,N}\ (\phi_N) - u_{cr1,z0}\ (0) = 0 \\ \boldsymbol{F_{12}} = u_{cr2,N}\ (\phi_N) - u_{cr2,z0}\ (0) = 0 \\ \boldsymbol{F_{13}} = i_{s,z0}\ (\phi_{Z0}) = 0 \\ \boldsymbol{F_{14}} = u_{cr2,z0}\ (\phi_{Z0}) - u_{cr2,z}\ (0) = 0 \end{cases} \tag{2}$$

where the subscript P, N, Z_0, Z means corresponding variables use the expressions of P mode stage, N mode stage, Z_0 mode stage, and Z mode stage, respectively. ϕ_P, ϕ_N, ϕ_{Z0}, ϕ_Z are the lengths of the P mode stage, N mode stage, Z_o mode stage, and Z mode stage, respectively. They are all undetermined variables too.

There are now 14 boundary equations (F_1 to F_{14}) and 16 undetermined variables (P_1, P_2, P_3, P_4, N_1, N_2, N_3, N_4, Z_{01}, Z_{02}, Z_1, Z_2, ϕ_P, ϕ_N, ϕ_{Z0}, ϕ_Z) in (2). Which means two additional constraint equations are needed to solve these undetermined variables

$$\begin{cases} \boldsymbol{F_{15}} = \phi_P\ + \phi_N + \phi_{\mathrm{Z0}} + \ \phi_{\mathrm{Z}} = \frac{T}{2} \\ \boldsymbol{F_{16}} = \phi_P = DT. \end{cases} \tag{3}$$

It can be found from Fig. 4(c) that the total duration of the four modes is half a cycle, and the duration of the first P mode stage corresponds to the conduction time of the switch tube, so F_{15} and F_{16} can be illustrated as (3) shows.

Solve for Required Characteristics: Solving for the required characteristics involves combining (2) and (3) to determine the undetermined variables. Fig. 5 illustrates the variation rule of $i_{p\max}$ and E_{pc} during startup, where E_{pc} is the energy input in a cycle.

More specifically, $i_{p\max}$ can be extracted from the mode analysis result of i_p (use $M = 0.5$, as an example in Fig. 5) and E_{pc} can be calculated by

$$E_{pc} = 2U_{in}\left(\int_0^{\phi_P} i_{p,p}d\phi + \int_{\phi_P}^{\phi_P+\phi_N} i_{p,N}d\phi\right). \tag{4}$$

Fig. 5 shows that i_p decreases along the startup process until the voltage gain $M = 1$, which proves that the proposed control method can achieve a successful soft startup to $M = 1$. Moreover, the energy transfer rule reflected in Fig. 5 verifies that the proposed method has energy limitation characteristics, wherein as the startup progresses, M gradually increases, and the energy transmitted in each cycle (E_{pc}) gradually decreases.

TABLE I
TIME-DOMAIN EQUATIONS OF i_p, i_s, u_{cr1}, AND u_{cr2} FOR EACH MODE

***P* mode stage**	***N* mode stage**
$\begin{cases} i_{p,P}(\phi) = P_1 cos\phi - P_2 sin\phi + k_1 P_4 \sin(k_1\phi) + P_3 \cos(k_1\phi) \\ i_{s,P}(\phi) = P_1 cos\phi - P_2 sin\phi - k_1 P_4 \sin(k_1\phi) - P_3 \cos(k_1\phi) \\ u_{cr1,P}(\phi) = P_1 sin\phi + P_2 cos\phi - P_4 \cos(k_1\phi) + \frac{P_3}{k_1}\sin(k_1\phi) + 1 \\ u_{cr2,P}(\phi) = P_1 sin\phi + P_2 cos\phi + P_4 \cos(k_1\phi) - \frac{P_3}{k_1}\sin(k_1\phi) - M \end{cases}$	$\begin{cases} i_{p,N}(\phi) = N_1 cos\phi - N_2 sin\phi + k_1 N_4 \sin(k_1\phi) + N_3 \cos(k_1\phi) \\ i_{s,N}(\phi) = N_1 cos\phi - N_2 sin\phi - k_1 N_4 \sin(k_1\phi) - N_3 \cos(k_1\phi) \\ u_{cr1,N}(\phi) = N_1 sin\phi + N_2 cos\phi - N_4 \cos(k_1\phi) + \frac{N_3}{k_1}\sin(k_1\phi) - 1 \\ u_{cr2,N}(\phi) = N_1 sin\phi + N_2 cos\phi + N_4 \cos(k_1\phi) - \frac{N_3}{k_1}\sin(k_1\phi) - M \end{cases}$
***Z_0* mode stage**	***Z* mode stage**
$\begin{cases} i_{p,z0}(\phi) = 0 \\ i_{s,z0}(\phi) = Z_{01}\, cos(k_2\phi) - k_2 Z_{02}\, sin(k_2\phi) \\ u_{cr1,z0}(\phi) = u_{cr1,p0} \\ u_{cr2,z0}(\phi) = Z_{02}\, cos(k_2\phi) + \frac{Z_{01}}{k_2} sin(k_2\phi) - M \end{cases}$	$\begin{cases} i_{p,z}(\phi) = 0 \\ i_{s,z}(\phi) = Z_1\, cos(k_2\phi) - k_2 Z_2\, sin(k_2\phi) \\ u_{cr1,z}(\phi) = u_{cr1,z0} \\ u_{cr2,z}(\phi) = Z_2\, cos(k_2\phi) + \frac{Z_1}{k_2} sin(k_2\phi) - M \end{cases}$

Note: P_1, P_2, P_3, P_4 denote undetermined variables in the P mode stage, N_1, N_2, N_3, N_4 represent undetermined variables in the N mode stage, Z_{01}, Z_{02}, Z_1, Z_2 are undetermined variables in the Z_0 mode stage and Z mode stage. M is the voltage gain. Other variables are as follows: $\phi = 2\pi f_r t$, $f_r = 1/\left(2\pi\sqrt{L_{r1}C_{r1}}\right) = 1/\left(2\pi\sqrt{L_{r2}C_{r2}}\right)$, $k = L_m/L_{r1}$, $k_1 = \sqrt{1/(1+2k)}$, $k_2 = \sqrt{1/(1+2k)}$

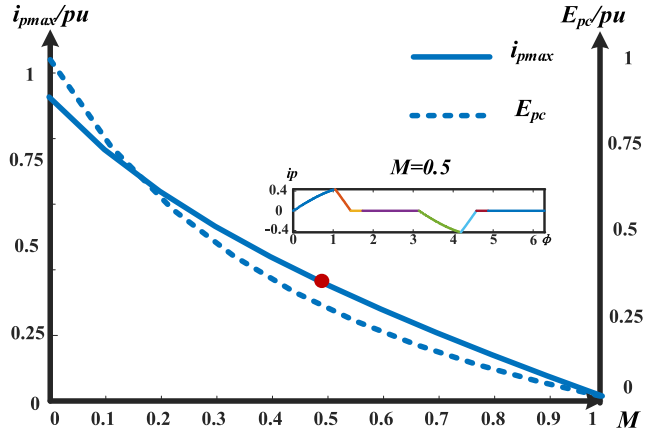

Fig. 5. Variation rule of i_{pmax} and E_{pc} during startup process.

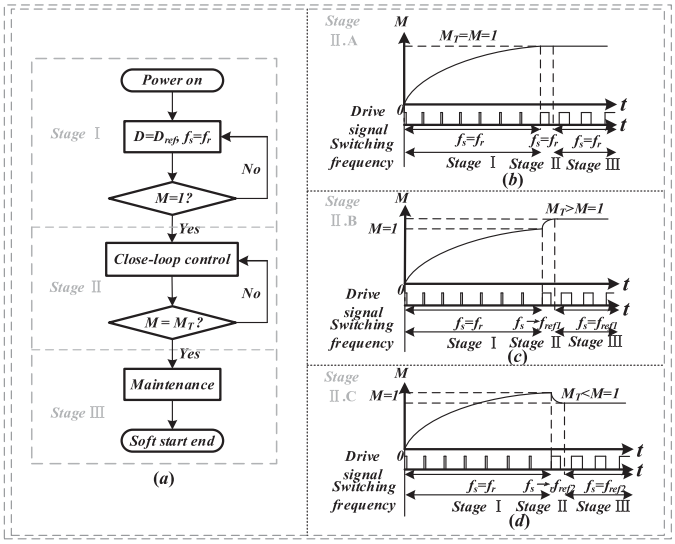

Fig. 6. Schematic diagram of the full work pattern. (a) Three stages of the full work pattern. (b) Schematic diagram of Stage II.A. (c) Schematic diagram of Stage II.B. (d) Schematic diagram of Stage II.C.

B. Practical Full Work Pattern for CLLC Converters Using the Proposed Soft Startup Control Method

For a no-load startup, the target gain of the proposed open-loop soft startup control method is M = 1. However, *CLLC* converters must attain varying voltage gains for common application scenarios with three primary requests: $M_T > 1$, $M_T = 1$ and $M_T < 1$. To achieve such different targets, the whole control process consists of three stages, which are the open-loop control stage for soft startup, the close-loop control stage for voltage modulation and the close-loop control stage for steady-state maintenance, respectively. The block diagram of the full work pattern is pictured in Fig. 6.

Stage I: Set $D = D_{ref}$ and $f_s = f_r$ to generate a fixed narrow pulse for the open-loop soft startup stage, where D_{ref} denotes the critical duty cycle calculated in Appendix A. This stage develops from M = 0 to M = 1 under the control of the proposed energy limitation based soft startup method.

Stage II: Once the voltage gain M = 1 is achieved, set $D = 0.5$ and regulate f_s to attain the target gain M_T through close-loop control. This stage can be categorized into the following three situations.

Stage II.A: If $M_T = 1$, just keep $f_s = f_r$, which means the target is already achieved at the end of Stage I, this case is illustrated in Fig. 6(b).

Stage II.B: If $M_T > 1$, decrease f_s to rise the gain until M = M_T. This is a close-loop control stage and the final switching frequency is $f_{ref1} < f_r$, which will be maintained in the next steady-state stage, this case is illustrated in Fig. 6(c).

Stage II.C: If $M_T < 1$, increase f_s to f_{ref2} for a lower gain, and keep $f_s = f_{ref2}$ in the steady-state maintenance too, this case is illustrated in Fig. 6(d).

Stage III: This stage is for the close-loop steady-state maintenance, the target gain is realized in the last stage, so the new control parameters should be same as the end of the close-loop voltage modulation stage. The full startup period ends.

Since the surge current typically occurs at the startup's onset, the open-loop soft startup process is particularly crucial. The analysis of the proposed soft startup control strategy reveals

TABLE II
SHAPE OF THE STATE TRAJECTORIES FOR DIFFERENT MODES

	P mode	N mode	Z_o mode	Z mode
Trajectory	Circle	Circle	Ellipse	Ellipse
Circle center	$(1-M,0)$	$(-1-M,0)$	/	/

that in practical applications, the essential action is to transmit a suitable narrow pulse control signal at the beginning of the open-loop control stage. This approach eliminates the tedious modulation process of the conventional soft startup methods.

III. STATE TRAJECTORY ANALYSIS FOR SHORT-CIRCUIT FAULT OF THE PROPOSED SOFT STARTUP CONTROL METHOD

A. Static State Trajectory Analysis for the Proposed Soft Startup Method

According to Fig. 6, the close-loop control stage only exists for a relative short time. Consequently, the fault analysis can mainly focus on the open-loop soft startup process. In order to clarify the mechanism of short-circuit tolerance features of the proposed method, the state trajectory analysis method for *CLLC* converter [34] is employed.

Following the approach in [34], the sum of i_p and i_s, together with the sum of u_{cr1} and u_{cr2} are chosen as state variables to simplify the state trajectory analysis. Otherwise, there would be four state variables (i_p, i_s, u_{cr1}, and u_{cr2}), and the state trajectory cannot be plotted in an intuitive two-dimensional (2-D) state plane. Specific state variables in different operation modes are defined as follows.

Set $i_P = i_{p,P} + i_{s,P}$ and $u_P = u_{cr1,P} + u_{cr2,P}$ in the P mode stage, $i_N = i_{p,N} + i_{s,N}$ and $u_N = u_{cr1,N} + u_{cr2,N}$ in the N mode stage, $i_{zo} = i_{p,zo} + i_{s,zo}$ and $u_{zo} = u_{cr1,zo} + u_{cr2,zo}$ in the Z_o mode stage and $i_z = i_{p,z} + i_{s,z}$ and $u_z = u_{cr1,z} + u_{cr2,z}$ in the Z mode stage.

Based on the time domain expressions of P mode stage, N mode stage, Z_o mode stage, and Z mode stage shown in Table I, relationships between state variables in different operation modes can be derived as follows:

$$\begin{cases} {i_P}^2 + (u_P - (1-M))^2 = 4\left({P_1}^2 + {P_2}^2\right) \\ {i_N}^2 + (u_N - (-1-M))^2 = 4\left({N_1}^2 + {N_2}^2\right) \\ {i_{z0}}^2 + \left(k_2 u_{z0} - k_2\left(u_{cr1,p0} - M\right)\right)^2 = {Z_{01}}^2 + {k_2}^2 {Z_{02}}^2 \\ {i_z}^2 + \left(k_2 u_z - k_2\left(u_{cr1,z0} - M\right)\right)^2 = {Z_1}^2 + {k_2}^2 {Z_2}^2. \end{cases} \tag{5}$$

Refer to (5), the shapes of the state trajectories for different modes are listed in Table II. The detail trajectories are illustrated in Fig. 7.

Specifically, take the case of $M = 0$ shown in Fig. 7(a) as an example to analyze the detail trajectory. The trajectory from point A to E indicates the positive half cycle. Trajectory AB is the P mode stage, which is a circular arc with a center at (1,0). Trajectory BC is the N mode stage, which is a circular arc with a center at (-1,0). Trajectory CD is the Z_0 mode stage, which is a segment of ellipse. Trajectory DE is the Z mode stage, which is a segment of ellipse too. The other part of trajectory indicates the symmetric negative half cycle.

Combine Fig. 7(a)–(c), two main characteristics of the state trajectory are as follows: On the one hand, the state trajectory is symmetric about the center of the origin (0,0) due to the symmetry of the positive and negative half cycles. Especially, the state trajectory will be horizontal symmetry if $M = 0$, because $u_{cr1} + u_{cr2} = 0$ at the end of the P mode stage. However, with the increase of M, i_p decreases, and the P_0 mode stage will be shortened, so the Z mode stage will be extended, the trajectory will not be horizontal symmetry, but just keep central symmetry. The above law is reflected in the form of dislocation reduction shown in Fig. 7(b), which means the trajectory will not be simply scaled down (from AB to $A_1{}'B_1{}'$), but will approximate rotational shrinking (from AB to A_2B_2). Since the starting point of the P mode stage (same as the end point of the previous Z mode stage) will be raised (from $A_1{}'$ to A_2), while the duty cycle is fixed, the trajectory will be extended to B_2 in order to ensure that the duration of P mode stage [θ_1 in Fig. 7(b)] keeps unchanged.

On the other hand, the state trajectory will shrink with the increasement of M. Due to the fact that the trajectory is composed of the resonant elements, the area of the trajectory can reflect the energy change law of the resonant cavity to some extent. This law is verified in Fig. 7(c), which illustrates the trajectory of the whole startup process with short-circuit fault. The trajectory shrinks along the startup process until the short-circuit fault occurs, which is coincident with the energy transfer rule shown in Fig. 5.

Moreover, to explain the natural short-circuit tolerance feature more clearly, the corresponding variation rule of i_p is illustrated in Fig. 7(d). When a short-circuit fault occurs, no additional control is needed, i_p is limited and will be stabilize to the same state as at the startup moment [the final trajectory is the same with the trajectory at the startup moment in Fig. 7(c)]. The specific transient short-circuit protection process will be analyzed in the next part.

B. Dynamic State Trajectory Analysis for the Short-Circuit Fault Process Under the Proposed Soft Startup Control Method

Based on the abovementioned state trajectory modeling, the dynamic state trajectory analysis of proposed soft startup method with short-circuit fault can be conducted as follows.

Assuming an output side short circuit occurs at moment of $M = M_1$, and M decreases to zero immediately at moment of short-circuit fault [as shown in Fig. 7(e)]. The dynamic state trajectory during the short-circuit fault is depicted in Fig. 7(f), commencing from point A. From point A to point C is the trajectory of positive half cycle, and the trajectory from point C to point E is the negative half cycle. Trajectory EF means a new circulation.

Since the trajectories of Z_o mode stage and Z mode stage exist briefly around the end of N mode stage when $M = 0$ [refer to Fig. 7(a)], the following analysis predominantly considers the P and N mode stage trajectories.

Trajectory AB: The trajectory AB in Fig. 7(f) represents the positive cycle P mode stage trajectory when the short-circuit fault occurs. At this moment, the voltage gain (M) decreases to

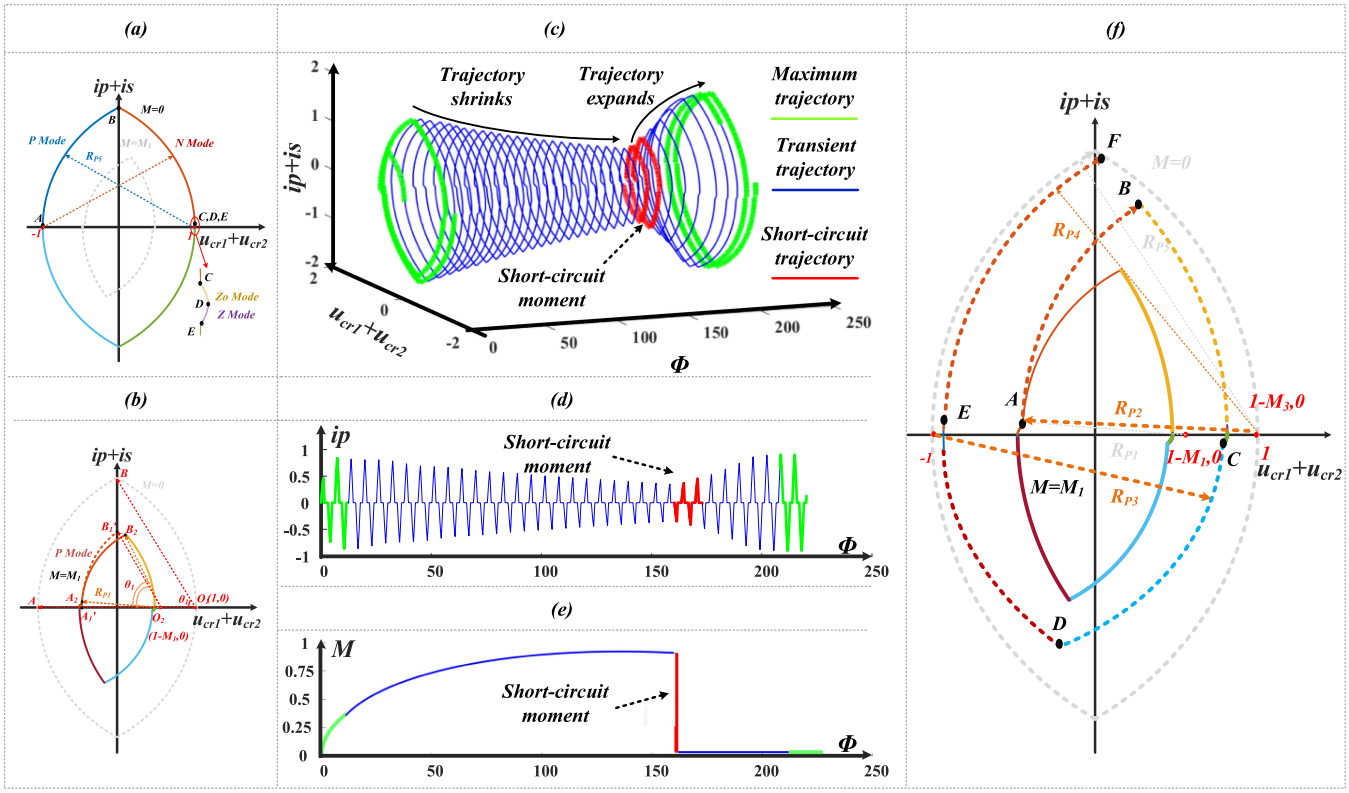

Fig. 7. State trajectory analysis for the startup process of proposed method. (a) Trajectory at $M = 0$. (b) Trajectory at short-circuit moment. (c) Trajectory of the whole startup process with short-circuit fault. (d) Variation rule of i_p during the startup process. (e) Variation rule of M during the startup process. (f) Transient trajectory after the short-circuit fault.

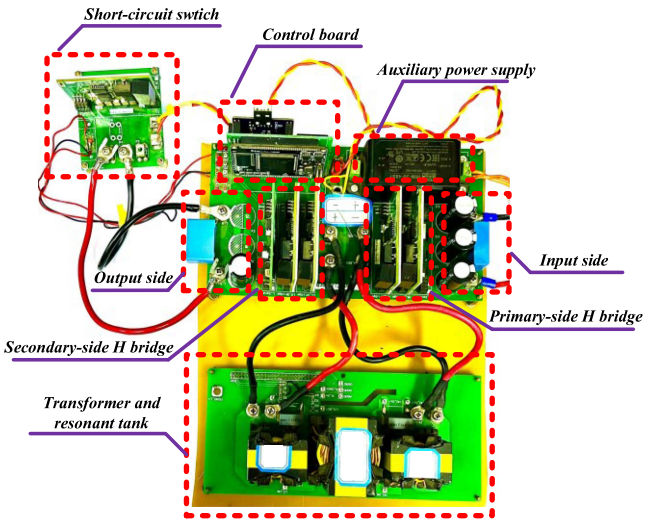

Fig. 8. Picture of lab-level *CLLC* prototype.

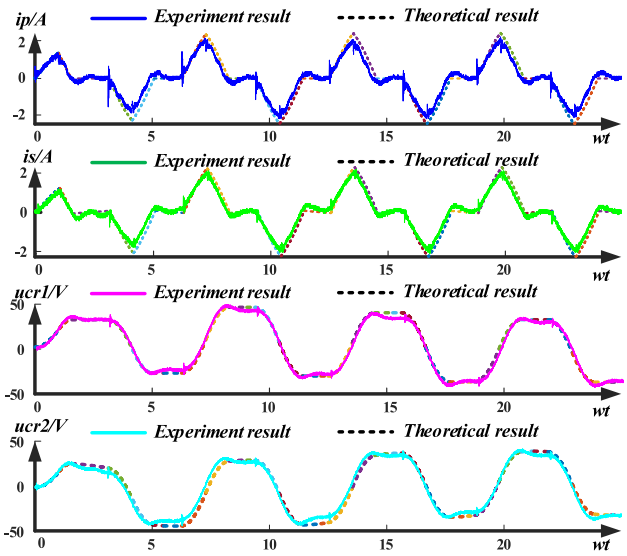

Fig. 9. Comparative analysis of experimental and theoretical results.

zero immediately, shifting the circle center from $(1 - M_1, 0)$ to $(1, 0)$ and increasing the radius from R_{P1} to R_{P2}. Since point A lies on the trajectory of $M = M_1$, the new radius R_{P2} must be smaller than R_{P5} (radius of the P mode stage at $M = 0$) and the duration of the P mode stage is fixed (since the duty cycle is fixed), the trajectory will expand but still be limited inside the trajectory of $M = 0$.

Trajectory BC: The trajectory BC in Fig. 7(f) encompasses the positive cycle N mode stage, Z_o mode stage, and Z mode stage. Since $R_{P2} < R_{P5}$ and the duration of the P mode stage remains constant, point B still not lies on the trajectory of $M = 0$, so the radius of the following N mode stage will be larger than that when $M = M_1$ but smaller than that when $M = 0$, which

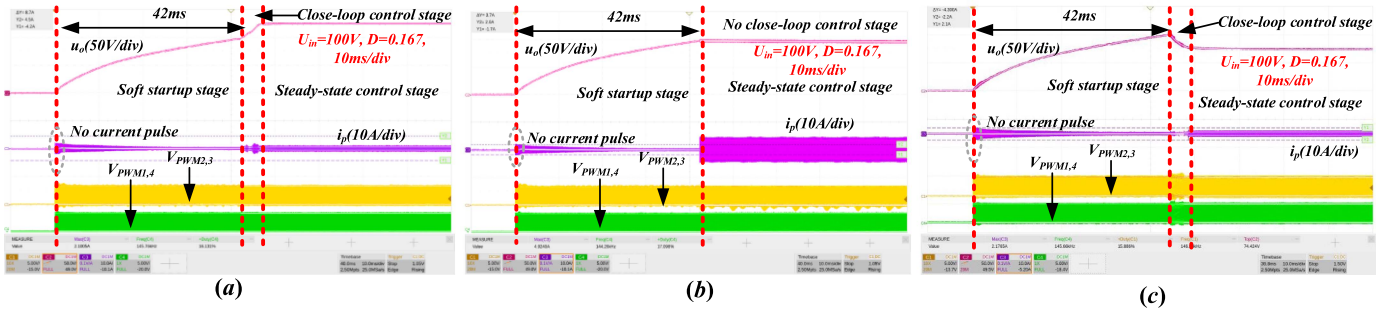

Fig. 10. Experimental waveforms for proposed soft startup method. (a) Overall startup waveforms when $M_T > 1$. (b) Overall startup waveforms when $M_T = 1$. (c) Overall startup waveforms when $M_T < 1$. (d) Overall startup waveforms for duty cycle modulation control.

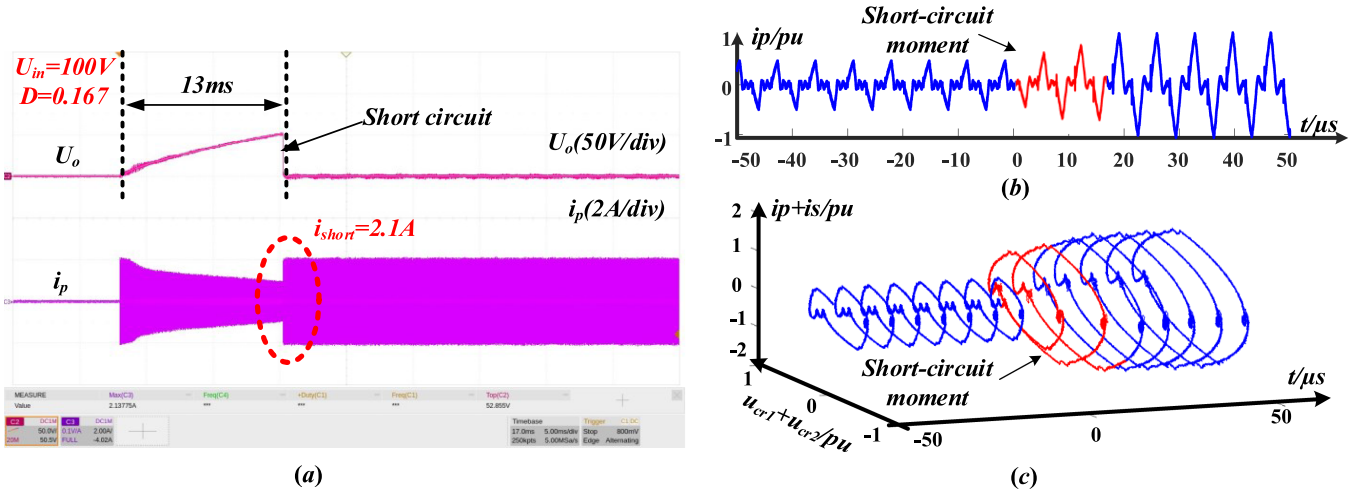

Fig. 11. Experiment results with input voltage $U_{in} = 100\ V$ and corresponding state trajectories. (a) Experiment waveforms for a short-circuit fault at 13 ms. (b) Detail waveforms of normalized i_p near the short-circuit moment. (c) State trajectory near the short-circuit moment.

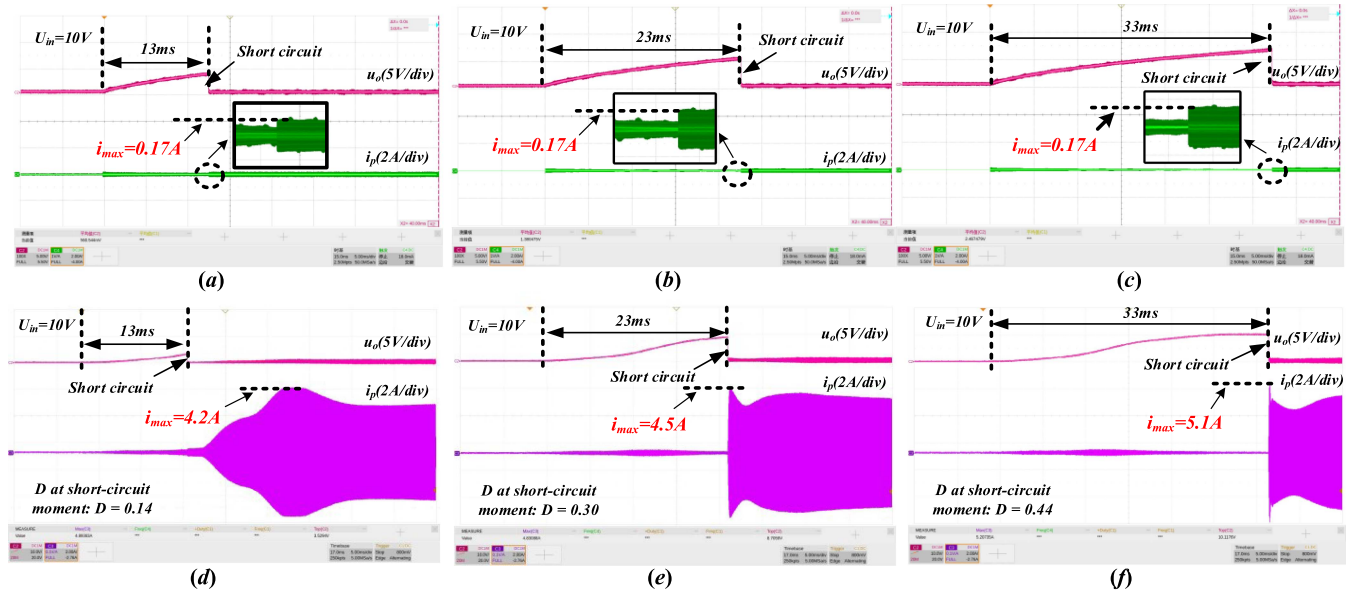

Fig. 12. Experimental results of applying short-circuit faults on the output side at different moments during the soft startup of the proposed method and the duty cycle modulation method. (a) Short-circuit fault moment: 13 ms for proposed method. (b) Short-circuit fault moment: 23 ms for proposed method. (c) Short-circuit fault moment: 33 ms for proposed method. (d) Short-circuit fault moment: 13 ms for duty cycle modulation method. (e) Short-circuit fault moment: 23 ms for duty cycle modulation method. (f) Short-circuit fault moment: 33 ms for duty cycle modulation method.

TABLE III
PARAMETER TABLE OF THE EXPERIMENTAL PROTOTYPE

Resonant tank			
Turns ratio	1	L_m	386 μH
L_{r1}/L_{r2}	35 μH	C_{r1}/C_{r2}	34 nF
Resonant frequency		145.9 kHz	
Switching tubes (SiC MOSFET)		C3M0120090J	

means the trajectory BC will expand than that of $M = M_1$, but it will be inside of the trajectory when $M = 0$ and the end of the trajectory will be near with the horizonal axis ($i_p = 0$ at the end of N mode stage).

Trajectory CD: The trajectory CD in Fig. 7(f) represents a negative cycle P mode stage trajectory during the short-circuit process. The circle center shifts to $(-1, 0)$, and the radius increases to R_{P3} ($R_{P2} < R_{P3} < R_{P5}$), causing the trajectory to expand but be constrained within the trajectory of $M = 0$ too.

Trajectory DE: The trajectory DE in Fig. 7(f) consists of negative cycle N mode stage, Z_o mode stage, and Z mode stage. Similarly, since point D still not lies on the trajectory of $M = 0$, trajectory DE will expand, but it will also be smaller than the trajectory of $M = 0$.

Trajectory EF: The trajectory EF in Fig. 7(f) is a positive cycle P mode trajectory during the short-circuit process. The circle center changes to $(1, 0)$, and the radius increases to R_{P4} ($R_{P2} < R_{P3} < R_{P4} < R_{P5}$), the following trajectory will repeat the abovementioned cycle, which means the trajectory will expand and continue to approach the trajectory of $M = 0$.

The conclusion is: The state trajectory will expand when the short-circuit fault occurs, and the largest trajectory is the same with the trajectory at the initial startup moment ($M = 0$), which is safe for the converter absolutely. Therefore, the proposed soft startup method exhibits natural short-circuit tolerance, obviating the need for additional protection circuits.

IV. EXPERIMENTAL VERIFICATION

A lab-level prototype is constructed to validate the proposed soft startup control method and corresponding analysis. The figure of the prototype is illustrated in Fig. 8. Parameters of the prototype are shown in Table III.

For this prototype, using $D_{ref} = 0.167$ to realize the whole soft startup process follow the rules mentioned in Appendix A. The experimental results are as follows.

First, the accuracy of the operation mode analysis is verified: In order to verify the accuracy of the operation mode analysis used above, a comparison is realized as Fig. 9 shows. The colored dashed lines represent the results of theoretical operation mode analysis while the colored thick solid line is the experimental results of i_p, i_s, u_{cr1}, u_{cr2}, which are drawn from the measured data. According to the comparison results, the experimental and theoretical results are highly consistent, which means the operation mode analysis has high accuracy in analyzing the startup process of *CLLC* converters.

Second, the full soft startup process under proposed soft startup control method is verified: The no-load experimental results for the full startup process corresponding to three different voltage gain targets at $U_{\text{in}} = 100$ V, $D = 0.167$ are illustrated in Fig. 10(a)–(c). The experiment results of the proposed method show that the overall startup time of the open-loop control stage is about 42 ms with obviously current suppression effect and the whole startup process consists of three stages, which are the open-loop soft startup stage, the close-loop control stage for voltage modulation (only exists for about 5 ms) and the close-loop control stage for steady-state maintenance, the full work pattern given in Fig. 6 is verified.

Moreover, the startup time for the conventional soft startup methods is in millisecond too (50 ms for duty cycle modulation control method in [32], 400 ms for hybrid control method in [31]), which means the proposed soft startup method can achieve an effective soft startup.

Specifically, Fig. 10(a) shows the case of $M_T > 1$, in which the open-loop control stage ends at $M = 1$, and the close-loop voltage modulation control stage aims to regulate the gain of the *CLLC* converter to $M > 1$. Another two conditions are verified in Fig. 10(b) and (c). For the case of $M_T = 1$, the whole startup process can be simplified, enabling a direct transition from open-loop startup to subsequent steady-state control stage. Similarly, the startup process of $M_T < 1$ is verified as Fig. 10(c) shows, featuring an increased switching frequency during the closed-loop voltage modulation stage to reach the goal. The switching process of different control stage is smooth without any pulse.

Third, the short-circuit fault tolerance features are verified: The short-circuit experiment for the proposed method is conducted at the rated operating voltage of the prototype with input voltage $U_{\text{in}} = 100V$. The corresponding experimental waveform is given in Fig. 11(a), the detail waveforms of i_p near the short-circuit moment [see cycled in Fig. 11(a)] is shown in Fig. 11(b), and the trajectory near the short-circuit moment plotted from the experimental data is shown in Fig. 11(c). Obviously, the proposed method effectively suppresses the surge current, and naturally clamps the short-circuit current to the same value of the startup moment.

To further demonstrate the ability of proposed method to protect the short-circuit fault during the startup process, a traditional soft startup method based on duty cycle modulation (refer to [32]) is selected for comparative experiments. For safety reasons, the comparative experiment is conducted under the condition of input voltage $U_{\text{in}} = 10V$. More specifically, the experiment results of proposed method are shown in Fig. 12(a)–(c)(the waveforms near the short-circuit moment is enlarged for clear explanation), and the corresponding results of conventional duty cycle modulation based method are given in Fig. 12(d)–(f). Part of the key results are listed in Table IV for comparison.

For the short-circuit fault experiment of proposed control method, the results show that i_p is natural limited below 0.17 A at fault moment, which proves that regardless of the moment that a short-circuit fault occurs during the startup process, the resonant current will naturally be limited below the initial startup current and there will be no surge current.

For the short-circuit fault experiment of conventional duty cycle modulation control method, the results show that the inrush current is related to the moment of the short-circuit fault, and the largest short-circuit current is $i_{\text{short}} = 5.1A$ for $U_{\text{in}} = 10V$

TABLE IV
CORE INDEXES OF SHORT-CIRCUIT FAULT EXPERIMENT AT DIFFERENT MOMENTS OF PROPOSED METHOD AND DUTY CYCLE MODULATION CONTROL METHOD

	Proposed soft startup control ($U_{in} = 10V$)		Duty cycle modulation control ($U_{in} = 10V$)	
Fault moment	D at fault moment	Max i_p after fault moment	D at fault moment	Max i_p after fault moment
13 ms	$D = 0.167$	$i_{max} = 0.17A$	$D = 0.14$	$i_{max} = 4.2A$
23 ms	$D = 0.167$	$i_{max} = 0.17A$	$D = 0.30$	$i_{max} = 4.5A$
33 ms	$D = 0.167$	$i_{max} = 0.17A$	$D = 0.44$	$i_{max} = 5.1A$
Note: the predictive i_{max} for the duty cycle modulation method under $U_{in} = 100V$ is near 50A, which is unsafe for the prototype.				

(10 V for safety considerations), which means the short-circuit current of proposed control method is less than 4% (see 0.17/5.1 refer to Table IV) of the classic duty cycle modulation control method under tested condition.

V. CONCLUSION

In this article, a soft startup method with natural short-circuit tolerance features is proposed for *CLLC* converters. By using a specially designed fixed frequency fixed duty cycle driving scheme, dynamic state trajectory after short-circuit failure can be restricted within a boundary automatically (means short-circuit current is limited). As a result, the soft startup with natural short-circuit tolerance features is realized. Main contributions of this article can be summarized as follows.

1) The important but less focused soft startup problem of *CLLC* converter is investigated comprehensively, and an effective solution is proposed.
2) A novel short-circuit failure handling principle (i.e., natural short-circuit tolerance) is proposed and demonstrated, which also has the potential to be used in failure handling of other condition.
3) Dynamic state trajectory analysis is introduced to *CLLC* converter for analyzing the complex dynamic process after short-circuit failure. Such tool can also be used in analyzing other dynamic process of *CLLC* converter.

The soft startup method proposed in the article achieves natural short circuit protection while balancing soft startup. The next step is to optimize control and derive the optimal soft startup control strategy from the energy perspective to achieve fast and safe soft startup.

APPENDIX A

This part gives a prerequisite of the duty cycle for the energy limitation features. The key point of the mode analysis above is that i_p will be fixed to zero after the first reduction to zero.

Assume $i_p = 0$ after the N mode stage. Fig. 13 shows the critical condition of the Z mode stage, if the sum of u_{cr1} and u_{Lm} is larger than U_{in}, the body diodes of S_1 and S_4 will turn ON, i_p will rise as a negative value, which contradicts the assumptions above. Therefore, a criterion to ensure $i_p = 0$ can be derived as

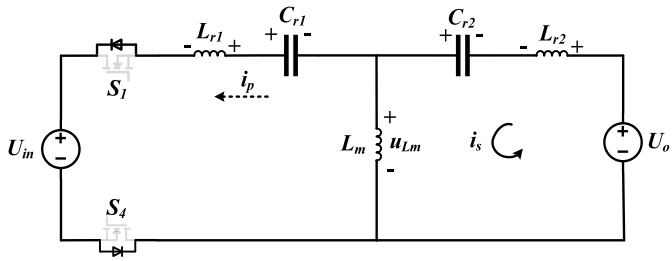

Fig. 13. Schematic diagram of the critical condition for four mode operation.

follows:

$$u_{cr1} + (u_{cr2} + U_o) \cdot \frac{k}{1+k} \le U_{\text{in}}. \tag{A.1}$$

The worst case is the no-load startup, so the criterion can be simplified to (A.2)

$$u_{cr1} + u_{cr2} \cdot \frac{k}{1+k} \le U_{\text{in}} \tag{A.2}$$

where $k = L_m/L_r$, u_{cr1}, and u_{cr2} can be solved by the operation mode analysis, U_{in} is the input voltage.

Since the result of operation mode analysis is related to the duty cycle for proposed soft startup control method, by adding (A.2) as a criterion, a prerequisite for duty cycle can be solved. Subsequently, by iteratively solving a simple optimization problem [as shown in (A.3)] with the startup speed as the optimization objective, the duty cycle D_{ref} for the fastest startup with energy limitation features can be computed

$$\begin{cases} \max & i_o = f(D) \\ \text{s.t.} & D < D_{\max} \\ & i_s \le i_{s\max} \\ & i_p \le i_{p\max} \\ & u_{cr1} \le u_{cr1\max} \\ & u_{cr2} \le u_{cr2\max} \end{cases} \tag{A.3}$$

where the output current i_o is introduced to measure the startup speed, which is calculated by (A.4) and $i_{s\max}$, $i_{p\max}$, $u_{cr1\max}$, $u_{cr2\max}$ are the upper limit of the devices

$$i_o = \frac{1}{T} \int i_s dt. \tag{A.4}$$

The final range of D is fixed as (A.5) shows, where D_{ref} is the optimal duty cycle for a fastest startup with natural energy limitation features

$$D \le D_{ref}. \tag{A.5}$$

REFERENCES

[1] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.
[2] S. Mocevic et al., "Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter," *iEnergy*, vol. 1, no. 1, pp. 100–113, Mar. 2022, doi: 10.23919/IEN.2022.0001.
[3] H. Chen, K. Sun, H. Shi, J. -I. Ha, and S. Lee, "A battery charging method with natural synchronous rectification features for full-bridge CLLC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2139–2151, Feb. 2022, doi: 10.1109/TPEL.2021.3108622.

[4] S. Chen, G. Zhang, and S. Yu, "A review of isolated bidirectional DC-DC converters for data centers," *Chin. J. Elect. Eng.*, vol. 9, no. 4, pp. 1–22, 2023, doi: 10.23919/CJEE.2023.000034.
[5] Y. Li, Y. Wang, Y. Guan, and D. Xu, "Design and optimization of high-gain bidirectional DC–DC converter for electric vehicles," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11221–11232, Sep. 2023, doi: 10.1109/TPEL.2023.3285627.
[6] H. Chen, L. Wang, K. Sun, and L. Lu, "A switching delay strategy for sensorless synchronous rectification in CLLC converters," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 280–293, Jan. 2024, doi: 10.1109/TPEL.2023.3321604.
[7] X. Lin, K. Sun, J. Lin, Z. Zhang, and W. Kong, "A multi-port bidirectional power conversion system for reversible solid oxide fuel cell applications," in *Proc. Int. Power Electron. Conf.*, Niigata, 2018, pp. 3460–3465.
[8] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. -S. Lai, "Design of bidirectional DC–DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015, doi: 10.1109/TTE.2015.2476035.
[9] Y. Wang, W. Chen, and Z. Shen, "Modeling of Litz wire winding AC resistance based on improved segmented equivalent circuit," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1135–1149, Jan. 2024, doi: 10.1109/TPEL.2023.3321327.
[10] Z. Lv, X. Yan, Y. Fang, and L. Sun, "Mode analysis and optimum design of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1513–1520, doi: 10.1109/ECCE.2015.7309873.
[11] H. Li et al., "Bidirectional control with fitting model-based synchronous rectification and input ripple current feedforward for SiC bidirectional CLLC EV charger," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9136–9146, Sep. 2023, doi: 10.1109/TIE.2022.3212382.
[12] A. Jung et al., "Bi-directional operation mode of LLC/CLLC DC/DC converter for on board charger of 800V battery systems," in *Proc. 11th Int. Conf. Power Electron. ECCE Asia*, Jeju Island, South Korea, 2023, pp. 2814–2819, doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213471.
[13] X. Zhang et al., "Design and modeling of CLLC converter for bidirectional on-board charger," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6095–6102, Sep./Oct. 2023, doi: 10.1109/TIA.2023.3281300.
[14] Y. Zhuang, F. Liu, X. Zhang, Y. Huang, X. Zha, and Z. Liu, "Short-circuit fault-tolerant topology for multiport cascaded DC/DC converter in photovoltaic power generation system," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 549–561, Jan. 2021, doi: 10.1109/TPEL.2020.3004070.
[15] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018, doi: 10.1109/TIE.2017.2758741.
[16] R. Emamalipour and J. Lam, "A multi-mode full-bridge/modified-stacked-switches structured CLLC resonant converter for energy storage applications," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5967–5981, May 2024, doi: 10.1109/TPEL.2024.3364233.
[17] X. Li, W. Liu, N. Jiao, C. Sun, and S. Mao, "Fault diagnosis of rotating rectifier in aircraft wound-rotor synchronous starter–Generator based on stator currents under all operational processes," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 16072–16084, Dec. 2023, doi: doi: 10.1109/TPEL.2023.3309252.
[18] L. Hao, Z. Zedong, L. Yongdong, Y. Ruidi, and X. Zheng, "Urban Rail Transit Power system integrated with electric vehicles based on CLLC resonant and buck-boost converter," in *Proc. IEEE Int. Conf. Elect. Syst. Aircr., Railway, Ship Propulsion Road Veh. Int. Transp. Electrific. Conf.*, Nottingham, U.K., 2018, pp. 1–7, doi: 10.1109/ESARS-ITEC.2018.8607797.
[19] Y. Xu, X. Ge, R. Guo, and W. Shen, "Online soft short-circuit diagnosis of electric vehicle Li-ion batteries based on constant voltage charging current," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 2, pp. 2618–2627, Jun. 2023, doi: 10.1109/TTE.2022.3208066.
[20] K. Zia, W. -J. Lee, A. Papasani, and P. -E. Su, "Li-ion battery resistance study due to an external short circuit using a zero bouncing circuit and its comparison to cyclic ageing," *IEEE Trans. Ind. Appl.*, vol. 60, no. 2, pp. 2453–2461, Mar./Apr. 2024, doi: 10.1109/TIA.2023.3346846.
[21] W. Wang, Y. Liu, P. Zhang, Y. Yuan, J. Zhao, and P. C. Loh, "A fault-tolerant LLC converter with high reliability and low cost for two-stage converters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9647–9659, Aug. 2023, doi: 10.1109/TPEL.2023.3281601.
[22] X. Xie, J. Zhang, C. Zhao, Z. Zhao, and Z. Qian, "Analysis and optimization of LLC resonant converter with a novel over-current protection circuit," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 435–443, Mar. 2007, doi: 10.1109/TPEL.2006.889919.
[23] F. Duan, M. Xu, X. Yang, and Y. Yao, "Canonical model and design methodology for LLC DC/DC converter with constant current operation capability under shorted load," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6870–6883, Oct. 2016, doi: 10.1109/TPEL.2015.2508671.
[24] C. Fei, F. C. Lee, and Q. Li, "Digital implementation of soft start-up and short-circuit protection for high-frequency LLC converters with optimal trajectory control (OTC)," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8008–8017, Oct. 2017, doi: 10.1109/TPEL.2016.2631467.
[25] C. Zhuo, X. Yang, X. Zhang, and X. Zhang, "Research on current limiting method used for short circuit fault current of resonant DC transformer based on inverted displacement phase control," *IEEE Access*, vol. 8, pp. 143412–143422, 2020, doi: 10.1109/ACCESS.2020.3014235.
[26] H. Jia et al., "Design of high frequency and wide voltage range isolated bidirectional DC-DC converter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, Shenzhen, China, 2018, pp. 1–6.
[27] T. Yu, G. Sicheng, and X. Shaojun, "Research on open-loop soft-start strategy of CLLLC bi-directional resonant converter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6, doi: 10.1109/PEAC.2018.8590641.
[28] L. Xiong, J. Song, and Y. Gao, "An adaptive current-limit soft start method for asymmetric CLLC resonant converter," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, to be published, doi: 10.1109/JESTIE.2024.3401731.
[29] A. Nabih, F. Jin, Q. Li, and F. C. Lee, "Soft start-up of three phase CLLC converter based on State trajectory control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Phoenix, AZ, USA, 2021, pp. 1927–1932, doi: 10.1109/APEC42165.2021.9487467.
[30] B. V. Sadangi, P. Chaturvedi, S. K. Patro, and S. Nema, "Soft starting algorithm to minimize the transient inductor current and transient capacitor voltage in series resonant dual active bridge converter," in *Proc. IEEE 2nd Int. Conf. Sustain. Energy Future Electric Transp.*, Hyderabad, India, 2022, pp. 1–6, doi: 10.1109/SeFeT55524.2022.9909331.
[31] J.-H. Jung, H.-S. Kim, M.-H. Ryu, and J.-W. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.
[32] Q. Chen, J. Wang, Y. Ji, and S. Liang, "Soft starting strategy of bidirectional LLC resonant DC-DC transformer based on phase-shift control," in *Proc. 9th IEEE Conf. Ind. Electron. Appl.*, 2014, pp. 318–322, doi: 10.1109/ICIEA.2014.6931180.
[33] K. Zhang, H. Chen, and K. Sun, "A constant frequency constant duty cycle soft startup control method with energy limitation features for CLLC converters," in *Proc. 4th Int. Conf. Smart Power Internet Energy Syst.*, Beijing, China, 2022, pp. 784–789, doi: 10.1109/SPIES55999.2022.10082628.
[34] H. Chen, K. Sun, L. Lu, S. Wang, and M. Ouyang, "A constant current control method with improved dynamic performance for CLLC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1509–1523, Feb. 2022, doi: 10.1109/TPEL.2021.3108631.

Huan Chen (Member, IEEE) received the B.E. and Ph.D. degrees in electrical engineering in 2018 and 2023, respectively, from Tsinghua University, Beijing, China, where he is currently working toward the Postdoctoral degree in electrical engineering.

His research interest includes the isolated bidirectional dc–dc converter.

Kai Zhang (Student Member, IEEE) received the B.E. degree in electrical engineering in 2022 from Tsinghua University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interest includes isolated bidirectional dc–dc converter.

Leheng Wang (Student Member, IEEE) received the B.E. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2021. He is currently working toward the Ph.D. degree in electrical engineering with Tsinghua University, Beijing, China.

His research interests include the isolated bidirectional dc–dc converter and modeling of power semiconductor devices.

Kai Sun (Fellow, IEEE) received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2000, 2002, and 2006, respectively.

In 2006, he joined the Faculty of Electrical Engineering, Tsinghua University, where he is currently a Tenured Associate Professor (Research Professor). From September 2009 to August 2010, he was a Visiting Scholar with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. From January to August 2017, he was a Visiting Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His research interests include power electronics for renewable generation systems, microgrids, and energy internet.

Dr. Sun is an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the TPC Vice Chair of IEEE ECCE2017 and IEEE ECCE-Asia2017, the Organization Committee Chair of IEEE eGrid2019, the Publicity Chair of IEEE ECCE2020, and the General Co-Chair of IEEE SYPS2023. He was the General Co-Chair of 2018 International Future Energy Challenge (IFEC2018). He is the PELS Asia Pacific Regional Vice Chair, PELS Beijing Chapter Chair, and PELS Electronic Power Grid Systems Technical Committee (TC8) Secretary. He was the recipient of Delta Young Scholar Award in 2013, Youth Award of China Power Supply Society (CPSS) in 2017, IEEE TRANSACTIONS ON POWER ELECTRONICS OUTSTANDING Reviewers Award in 2019, and IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Award in 2022. He is selected as IEEE PELS Distinguished Lecturer in 2021–2024.

Yongdong Li (Senior Member, IEEE) was born in Hebei, China, in 1962. He received the B.S. degree from the Harbin Institute of Technology, Harbin, China, in 1982, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Institute National Polytechnique de Toulouse, Toulouse, France, in 1984 and 1987, respectively, all in electrical engineering.

Since 1996, he has been a Professor with Department of Electrical Engineering, Tsinghua University, Beijing, China. He is the Lead Developer of the Power Electronics and Motor Control Laboratory, Tsinghua University. He was also an Invited Professor with the Institute National Polytechnique de Toulouse and the Dean with the School of Electrical Engineering, Xinjiang University, Urumchi, China. His current research interests include power electronics, machine control, and wind power generation.

Dr. Li is a Senior Member of the China Electro-Technique Society, the Vice Chairman of the China Power Electronics Society, and the Vice Chairman of the Electrical Automation Committee of China Automation Association.