A Single-Switch Non-Isolated Ripple-Less Step-Up DC-DC Converter With Ultra-High Gain Capability

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***Abstract*—This article introduces a nonisolated ultrahigh step-up dc–dc converter that utilizes one coupled-inductor (CI) and a voltage multiplier circuit to enhance the voltage gain. The proposed topology integrates a quadratic boost converter with a voltage multiplier circuit (diode-capacitor cell). Furthermore, the recommended converter uses one coup CI led-inductor in a small turn ratio which has achieved high voltage gain and is classified as an ultrahigh step-up dc–dc converter. In addition, the proposed design is appropriate for renewable energy sources with the minimal input current ripple. Moreover, the notable benefits of the proposed converter include high voltage gain, low voltage stress across the single switch and diodes, continuous input current, common ground, simple structure and control, and low weight which enhance its performance. Subsequently, the relationships between the operation modes and steady-state analysis thoroughly are provided. Eventually, a 300 W laboratory prototype is constructed to validate the expressed claims with 24–400 V, input and output voltages, respectively.**

***Index Terms*—Coupled-inductor (CI), low input current ripple (ICR), nonisolated dc–dc converter, ultrahigh gain.**

I. Introduction

OVER the past few decades, environmental concerns and the negative impact of greenhouse gas emissions have become increasingly prominent. During this time, there has also been a growing focus on the use of renewable energy sources (RES) [1]. Additionally, low power step-up dc–dc topologies are widely used in various applications, including RES. Ensuring a continuous input current with minimal ripple is essential for optimal performance and efficiency. To address these significant challenges, dc–dc converters are often introduced. Recently, a powerful integration of a quadratic step-up converter with various voltage boosting approaches are presented. Currently, due to the numerous applications like uninterruptible power supplies, medical devices, aerospace, and electric vehicles, extensive research is done [2], [3]. Several methods for boosting voltage, such as voltage multiplier cells, cascade, interleaved, and multilevel converters are recommended. Moreover, the various levels of the output voltage can be obtained by regulating the turn ratio of the magnetizing coupled-inductor (CI) in the structures that the CIs incorporated into them [4]. On the other hand, it is notable that the leakage inductance of the CI causes voltage spikes. Therefore, it is recommended to utilize distinctive strategies and active clamp circuits to address this issue. In [5], a new ultrahigh step-up dc–dc converter merges boosting stages, voltage multiplier cell, and one CI is introduced. The presented converter achieves high voltage gain, and low voltage stress across semiconductor devices and comprises two switches simultaneously activating. In [6], a quadratic ultra-high step-up dc–dc converter consisting of a voltage double rectifier and two CIs to enhance the high voltage conversion ratio is suggested. Besides, utilizing the voltage double rectifier circuit causes a high number of the components. In [7], a single-switch three winding CI high step-up dc–dc converter is presented. However, it has a low number of the components and a simple structure, but the switching and conduction power losses affect the efficiency. In [8], a current-fed step-up dc–dc converter-based CI is suggested. The presented structure has low input current ripple (ICR) and low voltage stress on the switches and diodes but there is shared ground between the input source and the output load. To enhance the high voltage conversion ratio, the active switched-inductor and one trans-inverse CI technique are propounded in [9]. Furthermore, the presented structure operates over an extended duty cycle and a low number of components. However, there is a shared ground between the input source and output load that limits its performance. In [10], a dual input high step-up dc–dc converter-based CI and voltage multiplier cell is introduced. There is a high RCR and three CI built-in transformers which causes the high cost and volume. In [11], a cascade step-up dc–dc converter consisting of a CI and active snubber circuit is suggested. The resistor-capacitor-diode snubber circuit is adapted to address the voltage spike across the switches. Despite this, the high voltage gain is obtained at a high turn ratio and duty cycle. In [12], for photovoltaic (PV) applications a high gain dc–dc converter featuring minimal RCR is introduced. However, the suggested converter is used for low power applications. A novel high step-up dc–dc converter comprising a CI and switched-capacitor circuit with high voltage gain is presented in [13]. Also, the high voltage stress of the components and high current ripple are notable challenges. An interleaved step-up dc–dc converter with a combination of the CI and multiplier cell technique is introduced in [14]. Nonetheless, the high RCR

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and the count of the elements have an unpleasant effect on the power losses and cost. In [15], a CI employed in a nonisolated high gain dc–dc converter with low RCR which is suitable for PV applications. In [16], a switched-capacitor-inductor step-up dc–dc converter is presented. Although, the high RCR is limited its performance. In [17], a nonisolated high gain dc–dc converter using CI, bootstrap capacitors, and an active clamp circuit is suggested. In this structure, the leakage inductance energy is transferred to the output through the active clamp circuit which improves the efficiency. Also, the high RCR is a significant point in its competence. In [18], an interleaved high gain dc–dc converter with CI built-in a transformer is reported. A buck-boost-cuk combination with high gain capability is introduced in [19]. There is no common ground and discontinuous input current. In [20], a high gain dc–dc converter consisting of a voltage multiplier cell is presented. In [21], [22], [23], several high step-up dc–dc converters are propounded. However, the discontinuous input current or shared ground have restricted their performance. In [24], a high step-up combination boost-flyback dc–dc converter is presented. The presented converter comprises the inductor-diode parallel is connected in series with the switch to reduce the current stress. This topology can be utilized at low power and low frequency applications. In [25] and [26], a high step-up dc–dc converters-based CI and voltage multiplier cells to enhance high voltage gain are suggested. In [27], [28], and [29], an integrated step-up dc–dc converters based CI-capacitor with acceptable benefits are presented. In [27], the introduced structure is achieved a significant voltage gain while maintaining low voltage stress on the components. In [28], a topology is presented characterized by minimal component usage and high efficiency. In [29], a configuration is demonstrated with an excellent voltage gain and efficiency at high output power. However, the high RCR limits their performance. In [30], [31], and [32], multiple innovative controller design methods are introduced to address the difficulties in managing various parameters. These approaches aim to enhance the dynamic response and increase flexibility. In this article, a single-switch ultra-high step-up dc–dc converter by integrating one CI and boosting voltage circuit with a high voltage conversion ratio, minimal voltage stress across the single switch and diodes, elevated output voltage, and low RCR is propounded. The proposed converter attains significant voltage gain at a low turn ratio range and duty cycle. Over and above that, due to a limited number of components, the main merits of the proposed converter, such as high power density, and continuous input current make it particularly suitable for RESs. In the following, a description of the proposed structure, operation principles, steady-state, and power loss analyses are expressed, completely. Then, the results of the comparison with other presented converters are given. Finally, a 300 W, laboratory prototype of the introduced configuration is constructed to validate the theoretical analyses.

II. Proposed Topology and Principle

Fig. 1 illustrates the proposed topology. The proposed configuration comprises an input inductor L_i, one CI T(with the primary and secondary turn ratio N_1 and N_2), a single switch S, five diodes (D_1, D_2, D_3, D_4 and D_o), and four capacitors (C_1, C_2, C_3 and C_o). Notably, the L_k and L_m are the leakage inductance and magnetizing of the CI, respectively. In addition, the turn ratio primary and secondary of the CI is denoted as $N_1/N_2 = N$. The proposed topology operates in three intervals. Subsequently, the key waveforms are derived to ascertain three operation modes of the proposed topology and corresponding equivalent circuit intervals are depicted in Figs. 2 and 3. The recommended converter operates in continuous conduction mode (CCM) and the input voltage source is considered dc, without ripple. Also, the output capacitor is assumed large enough and the output voltage ripple (OVR) can be ignored. The operation modes are elaborated completely as follows:

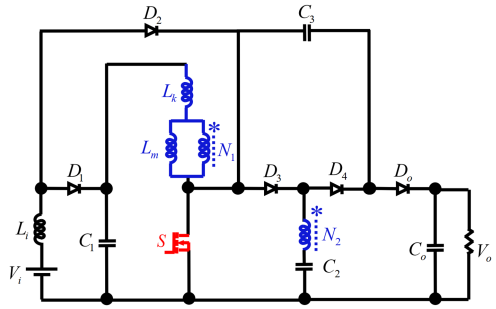


Fig. 1. Proposed topology.

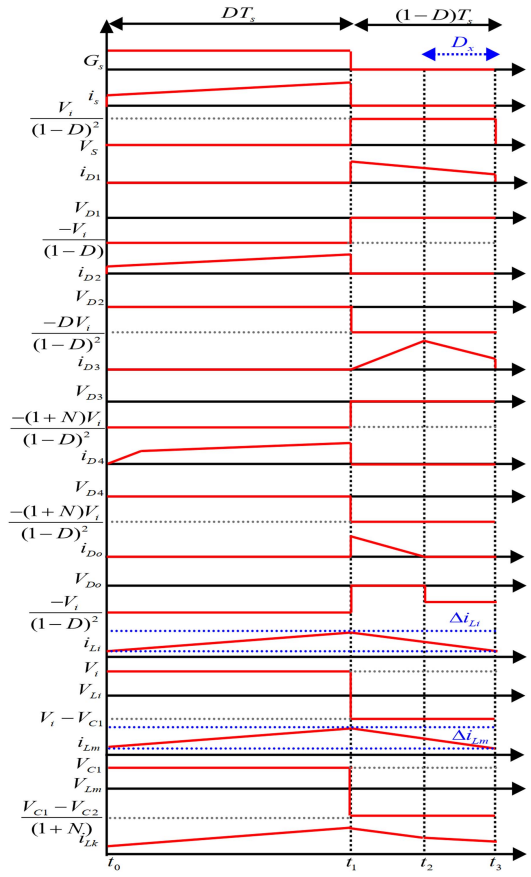


Fig. 2. Key waveforms of the proposed topology.

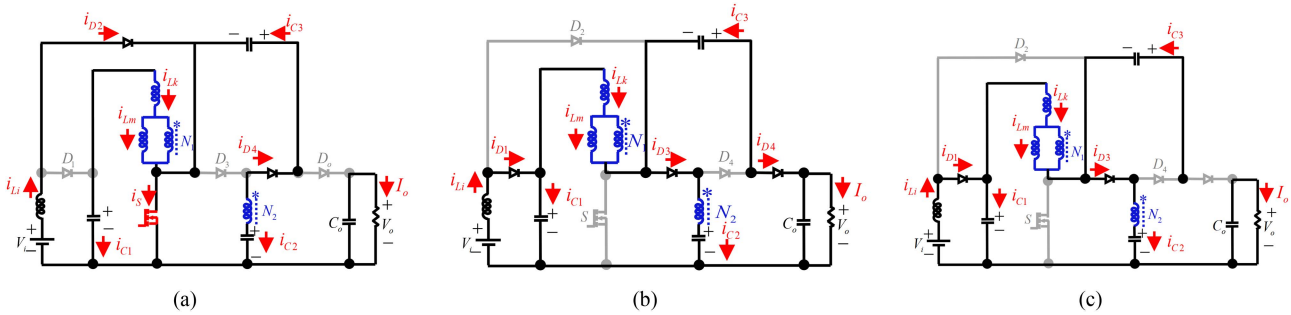


Fig. 3. Operation modes of the proposed converter. (a) Mode 1 $(t_0 - t_1)$. (b) Mode 2 $(t_1 - t_2)$. (c) Mode 3 $(t_2 - t_3)$.

First Switching Mode [see Fig. 3(a), $(t_0 - t_1)$]: In the first mode, a pulse is sent to the power switch S, activating it. During this interval, the input inductor L_i is charged via the input source V_i, causing i_{Li} to increase linearly. As depicted in Figs. 2 and 3(a), diodes D_1, D_3, and D_o remain in reverse bias during this mode, while D_2 and D_4 begin to conduct. Concurrently, the circuit path comprising the primary winding of the CI, C_1 and the switch S, the magnetizing inductor L_m experiences a positive voltage, resulting in a linear increase in the current i_{Lm}. By the end of this mode, i_{Li} and i_{Lm} reach their peak values. The current of the secondary winding is increased causing the capacitor C_2 can be discharged, completely. The relationships in this mode are determined as follows:

$$V_{Li} = V_i \tag{1}$$

$$V_{Lm} = V_{C1} = \frac{V_{C3} - V_{C2}}{N} \tag{2}$$

$$i_{Li} = I_i \tag{3}$$

$$i_{C1} = -i_{Lk} \tag{4}$$

$$i_{C2} = -i_{C3} = i_{N2}. \tag{5}$$

Second Switching Mode [see Fig. 3(b), $(t_1 - t_2)$]: In the second mode at t_1, the power switch S is OFF and the diodes D_1, D_3 and D_o initiate conduction. C_1 is charged through the path input source V_i, L_i, and D_1. Therefore, the i_{Li} is reduced linearly. Also, based on the Figs. 2 and 3(b), the currents passed across the CI, i_{N1} is decreased linearly and drop to its lowest point. Thus, C_2 is charged. At the end of this interval, the current of the D_o tends to zero. The relationships are obtained as follows:

$$V_{Li} = V_i - V_{C1} \tag{6}$$

$$V_{Lm} = \frac{V_{C1} - V_{C2}}{(1+N)}. \tag{7}$$

Also, in (7) the correlation between the voltage across the capacitors C_1 and C_2, and the turn ratio of the CI is defined

$$V_{Lm} = V_{C1} + V_{C3} - V_o \tag{8}$$

$$i_{C1} = I_i - i_{Lk} \tag{9}$$

$$i_{C3} = i_{N2} - i_{Lk}. \tag{10}$$

Third Switching Mode [see Fig. 3(c), $(t_2 - t_3)$]: At t_2, the diodes D_1 and D_3 are still ON, and the power switch S is still OFF. L_i is completely discharged through the path input source V_i, D_1 and C_1. So, it reaches to its minimum value linearly. Also, i_{Lm} attains its minimum value. In addition, according to Fig. 3(c), the current of the leakage inductance and the second winding of the CI, i_{Lk} and i_{N2} reach their minimum values, that means that the C_2 is fully charged. During this mode, the output load is supplied through C_o. The relationships are similar to the second mode.

III. Steady-State Analysis

The steady-state analysis of the suggested topology in CCM is explained by considering the relationships depicted in each switching mode and the equivalent circuits of the proposed converter, as are illustrated in Fig. 3.

A. Ideal Voltage Gain

Applying the volt-second balance principle to the input and magnetizing inductors of the proposed converter enables the computing of the capacitor voltage and the correlation between input and output voltage. Furthermore, this article excludes consideration of the leakage inductance. The following relationships are determined based on operation modes

$$V_i D + (V_i - V_{C1})(1 - D) = 0. \tag{11}$$

The voltage of C_1 is derived from (11) as follows:

$$V_{C1} = \frac{V_i}{(1-D)}. \tag{12}$$

By using the volt-second law can be written as follows:

$$V_{C1} D + \left(\frac{V_{C1} - V_{C2}}{(1+N)}\right)(1 - D) = 0. \tag{13}$$

By placing the (12) in (13) the voltage of C_2 is determined:

$$V_{C2} = \frac{(1+ND)V_i}{(1-D)^2}. \tag{14}$$

Utilizing (2) and (14), the voltage of C_3 is performed

$$V_{C3} = \frac{(1+N)V_i}{(1-D)^2}. \tag{15}$$

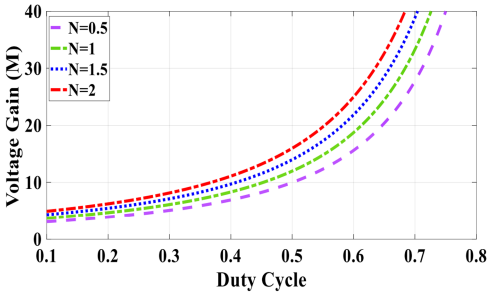


Fig. 4. Voltage gain versus duty cycle for different turn ratio, *N*.

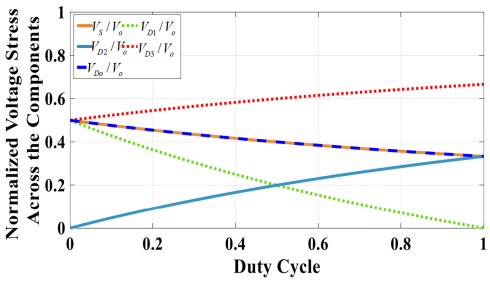


Fig. 5. Normalized voltage stress versus duty cycle and $N = 1$.

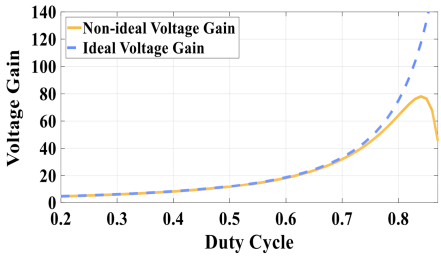


Fig. 6. Ideal and nonideal voltage gain versus duty cycle.

By inserting (7) in (8) the below equal is obtained as

$$\frac{NV_{C1}}{(1+N)} + \frac{V_{C2}}{(1+N)} + V_{C3} - V_o = 0. \tag{16}$$

By substituting (12), (14) and (15) in (16) the voltage gain is calculated as follows:

$$M = \frac{V_o}{V_i} = \frac{2+N(3+N)}{(1+N)(1-D)^2}. \tag{17}$$

Fig. 4 depicts the relationships between voltage gain and duty cycle across various turn ratios. Meanwhile, it is obvious that as the duty cycle extends over a wide range, the voltage gain is increased proportionally with the variation of the turn ratios. Therefore, the voltage gain is drawn for different turn ratios from 0.5 to 2 and $0<D<1$.

B. Nonideal Voltage Gain

This section presents the nonideal voltage gain of the recommended converter by making several assumptions and incorporating the losses of the various components. The nonideal voltage gain is derived as (18). In the following, the main parameters are defined, i.e., r_{DS}, is drain-source on resistance of the MOSFET, $V_{FDi}, i = 1, 2, 3, 4, o$, is the forward voltage drop of the diodes, r_{Dj}, $j = 1, 2, 3, 4, o$, is the parasitic resistance of the diodes which is neglected in nonideal voltage gain calculation, and r_{Lx}, $x = i, k$, represent the parasitic resistance of the input inductor and CI, and r_{Cy}, $y = 1, 2, 3, o$, is the parasitic resistance of the capacitors. Although, V_{FD1} and V_{FDo} are assumed the forward voltage drop of the input diodes D_1 and D_2, and the output diodes D_3, D_4, and D_o, respectively. Fig. 6 depicts both the ideal and nonideal voltage gain of the proposed configuration. It is evident that when the voltage gain is less than 40, the discrepancy between the ideal and nonideal voltage gain remains within acceptable limitation.

C. Voltage Stress on the Devices

The semiconductor devices maximum voltages are calculated by considering the operation modes and taking into account the relationships (12), (14), and (15) in the following:

$$\begin{aligned}
M_{non-ideal} &= \frac{(2+N(3+N))}{(1+N)(1-D)^2} - \frac{2V_{FDo}}{V_i} - \frac{V_{FD1}}{V_i(1-D)^2} \\
&\quad - \frac{M_{ideal(CCM)}}{R_L} \\
&\quad \times \Big[r_{DS-on} \times [A] - r_{Li} \times [B] - r_{Lk} \times [C] \\
&\quad - r_{C1} \times [D] - r_{C2} \times [E] - r_{C3} \times [F] - r_{Co} \Big] \\
A &= \frac{(2+3N-D(1+N)+D^2(1+N)}{(1+N)(1-D)^2}, \\
B &= \frac{1}{(1-D)^2}, \\
C &= \frac{(2+N^2+3N-D(N^2+N+2)}{(1+N)} \\
D &= \frac{\Big(N(1-D)-2D-(1-D)^2(1+D(1+N)) - N(1+N)(1-D)^2\Big)}{(1+N)^2(1-D)^2}, \\
E &= \frac{1}{N(1+N)}\left(-\frac{N}{2} - 1 + D(2D+N)\right), \\
F &= \frac{(2D-1)}{N}
\end{aligned} \tag{18}$$

$$V_S = \frac{V_i}{(1-D)^2} = \frac{(1+N)}{(2+N(3+N))} V_o \tag{19}$$

$$V_{D1} = \frac{-V_i}{(1-D)} = \frac{-(1+N)(1-D)}{(2+N(3+N))} V_o \tag{20}$$

$$V_{D2} = \frac{-DV_i}{(1-D)^2} = \frac{-(1+N)D}{(2+N(3+N))} V_o \tag{21}$$

$$V_{D3} = V_{D4} = \frac{-(1+N)V_i}{(1-D)^2} = \frac{-(1+N)^2}{(2+N(3+N))} V_o \tag{22}$$

$$V_{Do} = \frac{-V_i}{(1-D)^2} = \frac{-(1+N)}{(2+N(3+N))} V_o. \tag{23}$$

In Fig. 5, the voltage stress across the components during variations of the duty cycle is presented. As per the illustration, the maximum voltage stress and the voltage stress across the power switch S, D_3 and D_o are decreased by increasing the duty cycle.

D. Currents Analysis

Following Fig. 2 and the relationships of the operation modes, the maximum currents of the semiconductor devices are presented as follows:

$$i_{S(\text{peak})} = \frac{(M-1)}{D} I_o \tag{24}$$

$$i_{D1(\text{peak})} = i_{D2(\text{peak})} = M I_o \tag{25}$$

$$i_{D3(\text{peak})} \approx \frac{I_o}{(1-D)} \tag{26}$$

$$i_{D4(\text{peak})} \approx \frac{I_o}{D} \tag{27}$$

$$i_{Do(\text{peak})} \approx \frac{2I_o}{(1-D)}. \tag{28}$$

By applying the ampere-second law to the capacitors and according to the equivalent circuits through each operation mode, and placing (23)–(27) in (28)–(30), the current of the capacitors C_1, C_2 and C_3 are obtained. Also, the average and rms current values of the components are provided in Table I

$$i_{C1}{}^{\text{mod } e1} = i_S - i_{D2} - i_{D4}, i_{C2}{}^{\text{mod } e1} = -i_{C3}{}^{\text{mod } e1} = -i_{D4} \tag{29}$$

$$i_{C1}{}^{\text{mod } e2} = i_{D1} - i_{D3} - i_{Do}, i_{C2}{}^{\text{mod } e2} = i_{D3}, i_{C3}{}^{\text{mod } e2} = -i_{Do} \tag{30}$$

$$i_{C1}{}^{\text{mod } e3} = i_{D1} - i_{D3}, i_{C2}{}^{\text{mod } e3} = i_{D3}, i_{C3}{}^{\text{mod } e3} = 0. \tag{31}$$

Based on Fig. 3 and (29)–(31) the D_x is defined as follows:

$$D(i_{D4}) + (1 - D - D_x)(-i_{Do}) = 0. \tag{32}$$

By placing the (27) and (28) in (32) can be written as

$$D_x = \frac{(1-D)}{2}. \tag{33}$$

E. Power Losses Analysis

In this section, the approximation of the individual power losses distribution of the components by considering the equivalent parasitic resistance and the rms current values which are given in Table I, are expressed. Meanwhile, according to the proposed configuration and evaluation indicate the satisfactory performance of the proposed topology. The aggregate of the switching and conduction losses of the power switch is obtained subsequently.

$$P_S = V_{DS} I_{S(ave)} (t_{\text{on}} + t_{\text{off}})/2T_S + C_{\text{oss}} {V_{DS}}^2/2T_S$$

TABLE I
AVERAGE AND RMS VALUES

Components		Average	Rms
Switch	S	$i_{S(ave)} = (M-1)I_o$	$i_{S(rms)} = \frac{(M-1)}{\sqrt{D}} I_o$
Diodes	D_1	$i_{D1(ave)} \approx \frac{M}{2} I_o$	$i_{D1(rms)} = M I_o \sqrt{(1-D)}$
	D_2	$i_{D2(ave)} \approx \frac{M}{2} I_o$	$i_{D2(rms)} = M I_o \sqrt{D}$
	D_3	$i_{D3(ave)} = I_o$	$i_{D3(rms)} = \frac{I_o}{\sqrt{(1-D)}}$
	D_4	$i_{D4(ave)} = I_o$	$i_{D4(rms)} = \frac{I_o}{\sqrt{D}}$
	D_o	$i_{Do(ave)} = I_o$	$i_{Do(rms)} = \sqrt{\frac{2}{(1-D)}} I_o$
Capacitors	C_1	$i_{C1(rms)} = \frac{(2+M(D-1))I_o}{\sqrt{D}} + \frac{2(M(1-D)-2)I_o}{\sqrt{(1-D)}}$	
	C_2	$i_{C2(rms)} = i_{N2(rms)} = \frac{I_o}{\sqrt{D}} + \frac{I_o}{\sqrt{(1-D)}}$	
	C_3	$i_{C3(rms)} = \frac{I_o}{\sqrt{D}} + \sqrt{\frac{2}{(1-D)}} I_o$	
Inductors	L_k	$i_{Lk(rms)} = (1-D)MI_o$	
	L_m	$i_{Lm(ave)} \approx \frac{M}{2} I_o$	

$$+ r_{DS,\text{on}} {I_{S(\text{rms})}}^2. \tag{34}$$

Based on the preceding expressions, the determination of the total power losses of the diodes can be described as

$$P_D = V_{\text{FD}} I_{D(\text{ave})} + r_D {I_{D(\text{rms})}}^2. \tag{35}$$

Moreover, the power losses of the capacitors are calculated as

$$P_C = r_C {I_{C(\text{rms})}}^2. \tag{36}$$

As depicted in the proposed configuration, it incorporated an input inductor and one CI. Consequently, the power losses associated with these inductors include both ohmic and core losses which can be ascertained as

$$P_L = r_L {I_{L(\text{rms})}}^2 + P_{\text{Core}(L_i,T)}. \tag{37}$$

Eventually, the total power losses of the proposed topology can be calculated as follows:

$$P_{\text{Loss(total)}} = P_S + P_D + P_C + P_L. \tag{38}$$

As well as, it can be mentioned the efficiency of the proposed converter is determined as

$$\eta = \frac{P_o}{P_{\text{Loss(total)}} + P_o}. \tag{39}$$

To evaluate the efficiency of the proposed converter the expressing parasitic values of the components based on the datasheet information are given in the Table IV. Using the parasitic components are given in Table IV, a curve involving efficiency along with the nonideal voltage gain versus duty cycle under the output load is plotted. As shown in Fig. 7,

TABLE II
COMPARISON OF THE PROPOSED TOPOLOGY WITH THE OTHER CONVERTERS

Ref.	M	V_S/V_o	V_D/V_o	No. of Components $S^*+G.D^*,\ D^*,\ C^*,\ M.C^*/T^*$	TG*	CG*	$V_i(V),\ V_o(V),\ f_S(\text{kHz}),\ P_o(W)$ h (%) at Rated Power	η_{Peak} (%)
Lee and Do [11]	$(1+nD)/(1-D)^2$	$1/(1+nD)$	$(1+n)/(1+nD)$	1+1, 6, 4, 2, /14	8.33	✓	48, 400, 50, 200 92.2	94.8
Yang et al. [12]	$(1+n)/(1-D)^2$	$1/(1+n)$	$n/(1+n)$	1+1, 5, 5, 3 /15	15.4	✓	12, 196.2, 40, 150 -	94
Ye et al. [13]	$(2+n)/(1-D)$	$1/(2+n)$	$(1+n)/(2+n)$	2+2, 2, 3, 1 /10	8.3	✓	24, 200, 50, 200 92.2	93
Alghaythi et al. [14]	$2(1+n)/(1-D)$	$1/2(1+n)$	$1/(1+n)$	2+2, 7, 7, 2 /20	25	✓	32, 800, 118, 400 96.7	96.7
Ardi et al.[15]	$(2+n)/(1-D)$	$1/(2+n)$	$(1+n)/(2+n)$	1+1, 3, 3, 2 /10	11.1	✓	27, 300, 30, 225 93.2	95.5
Axelrod et al. [16]	$(1+n+nD)/(1-D)$	$1/(1+n+nD)$	$1/(1+n+nD)$	1+1, 4, 4, 4 /14	9.16	✓	24, 220, 50, 125 92	-
Hwu and Yau [17]	$(1+N)(2-D)/(1-D)$	$1/(1+N)(2-D)$	$1/(1+N)(2-D)$	2+2, 3, 4, 1 /12	10	✓	20, 200, 100, 160 93.5	95.4
Wang et al. [18]	$2+n(1+D)/(1-D)$	$1/2+n(1+D)$	$2(1+n)/2+n(1+D)$	4+4, 4, 5, 2 /19	7.9	✓	48, 380, 50, 1000 92.5	94.5
Rong et al. [19]	$(1+N)(1+D)/(1-D)$	$1/(1+N)(1+D)$	$1/(1+D)$	1+1, 4, 5, 2 /13	10	×	20, 200, 50, 150 93.8	94.4
Radmehr et al. [20]	$(2+D+2N)/(1-D)$	$1/(2+D+2N)$	$(1+2N)/(2+D+2N)$	2+2, 4, 4, 2 /14	16	✓	25, 400, 50, 300 95.7	96
Liu and Li [21]	$1+D(1+2N)/(1-D)$	$1/(1+D(1+2N))$	$2N/(1+D(1+2N))$	2+2, 3, 3, 2 /12	9.5	×	40, 380, 100, 400 94.8	96
Zhu et al. [22]	$2D/(1-D)$	$1/(2D)$	$1/(2D)$	1+1, 2, 3, 2 /9	8.33	✓	48, 400, 100, 300 94.1	94.3
Lai et al. [23]	$2+(nD(1-D))/(1-D)$	$1/2+(nD(1-D))$	$2/2+(nD(1-D))$	2+2, 4, 3, 1 /12	8.33	✓	24, 200, 50, 225 94	95.8
Choudhury et al. [24]	$(1+nD)/(1-D)^2$	$1/(1+nD)$	$1/(1+nD)$	1+1, 5, 3, 3 /13	6	✓	12, 72, 10, 40 87	88
Majarshin and Babaei [27]	$(2N-1)+ND(N-1)/(N-1)(1-D)$	$(N-1)/(2N-1)+ND(N-1)$	$N/(2N-1)+ND(N-1)$	2+2, 4, 4, 2 /14	15.7	✓	28, 440, 50, 200 94.6	95
Afzal et al. [28]	$(1+N)/(1-D)$	$(1+N)/(1-D)$	$(1+N)/(1-D)$	1+1, 2, 2, 1 /7	10	✓	30, 400, 100, 250 96.1	96.7
Guepfrih et al. [29]	$n(D-D^2)+nD+1/(1-D)^2$	$1/n(D-D^2)+nD+1$	$n/n(D-D^2)+nD+1$	1+1, 5, 4, 2 /13	11.1	✓	72, 800, 50, 1000 90.5	94.8
Prop.	$(2+N(3+N))/(1+N)(1-D)^2$	$(1+N)/(2+N(3+N))$	$(1+N)/(2+N(3+N))$	1+1, 5, 4, 2 /13	16.6	✓	24, 400, 50, 300 93.8	96

TG^*: Test gain, S^*: Switch, $G.D^*$:Gate Driver, D^* : Diodes, C^* : Capacitors, $M.C^*$: Magnetic core, T^* : Total components, CG^*: Common ground.

TABLE III
COMPARISON ICR AND OCR OF THE PROPOSED TOPOLOGY WITH THE OTHER CONVERTERS

Ref.		Lee and Do [11]	Yang et al. [12]	Ye et al. [13]	Alghaythi et al. [14]	Ardi et al. [15]	Axelrod et al. [16]	Hwa and Yau [17]	Wang et al. [18]	Rong et al. [19]	Radmehr et al. [20]	Liu and Li [21]	Zhu et al. [22]	Lai et al. [23]	Choudhury et al. [24]	Majarshin and Babaei [27]	Afzal et al. [28]	Guepfrih et al. [29]	Prop.
ICR*	$\Delta i_{Li}(A)$	2.4	0.3	22.2	6	1.8	8.8	7.3	7.2	18	28	10	8.3	12.4	0.5	7	16	12.5	1.6
	Ripple factor (%)	>20	<20	>20	>20	<20	>20	>20	>20	>20	>20	>20	>20	>20	<20	>20	>20	>20	<20
		H	L	H	H	L	H	H	H	H	H	H	H	H	L	H	H	H	L
OCR*	$\Delta i_o(mA)$	0.06	0.42	0.8	0.34	0.25	4.27	0.14	1.99	0.59	3.15	0.13	2.81	0.19	42.4	0.6	0.01	0.02	0.16

ICR*: Input current ripple, OCR*: Output current ripple.

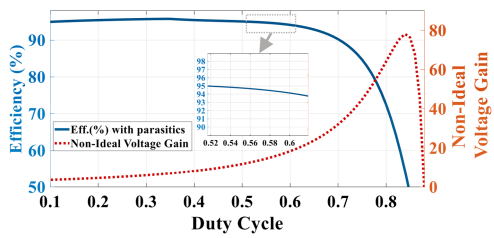


Fig. 7. Efficiency and nonideal voltage gain of the proposed topology versus duty cycle.

the parasitic components affect the efficiency and the voltage gain. Moreover, within the duty cycle range $0.52 \leq D \leq 0.6$, the efficiency remains relatively constant from 94% to 95%. A noticeable decline in efficiency occurs when the duty cycle exceeds 0.7.

IV. DESIGN CONSIDERATIONS

A. Inductors Design

The input inductor size is important to reduce RCR for RESs applications. Thus, the minimum current ripple is preferred. Also, it is notable that the average current of the inductors is more than half of their current ripple ($2I_{L(ave)} \geq \Delta i_L$). The value of the input inductor L_i can be computed as follows:

$$L_i \geq \frac{V_i D}{\Delta I_{Li} f_S}. \tag{40}$$

The current ripple of the input inductor L_i can be determines as follows:

$$\Delta i_{Li} \leq \frac{2(2+N(3+N))I_o}{(1+N)(1-D)^2}. \tag{41}$$

TABLE IV
PARAMETERS SPECIFICATION SETUP

Parameters	Values
Input Voltage	24 V
Output Voltage	400 V
Output Power	300 W
Power Switch	$S: IXTH94N20X4$ $(r_{DS,on}=10m\Omega, t_{on}=9ns, t_{off}=7ns)$
Diodes	$D_1, D_2: STPS30H100, (V_{FD}=0.5V)$ $D_3, D_4: MUR540, (V_{FD}=0.5V)$ $D_o: MUR860, (V_{FD}=0.55V)$
Input Inductor	$L_i=250uH, (r_{Li}=16m\Omega)$
Coupled Inductor	$T: ETD49, n_p=n_s=30$ 20 *strands of wire is litzed* $(D=0.5)$ $(r_{L(\text{total})}=16\text{m}\Omega, L_m=330uH, L_K=4.7uH)$
Capacitors	$C_1=68\ uF, 100V$; $C_2=82\ uF, 250V$ $C_3=82uF, 350V$; $C_o=100\ uF, 450V$
Switching Freq.	50 kHz
Controller Type	*Digital Voltage Controller, (Differential Amplifier Feedback)*
Gate Driver	ICL7667

By replacing (41) in (40) the bellow relationship is obtained as

$$L_i \geq \frac{R_L D(1+N)^2(1-D)^4}{f_S 2(2+N(3+N))^2}. \tag{42}$$

Based on the approach for calculating input inductor, in order to obtain the value magnetizing inductor L_m the current ripple is determined as follows:

$$L_m \geq \frac{V_{Lm} D}{\Delta i_{Lm} f_S}. \tag{43}$$

Calculating current ripple of L_m is given as

$$\Delta i_{Lm} \leq \frac{(2+N(3+N))I_o}{(1+N)(1-D)^2}. \tag{44}$$

Subsequently, the value can be calculated as follows:

$$L_m \geq \frac{R_L D(1+N)^2(1-D)^3}{f_S(2+N(3+N))^2}. \tag{45}$$

B. Capacitors Design

By considering the permissible voltage ripple across the capacitors ($\Delta V_C \approx 1\% V_C$), the minimum capacitance values are designed through the subsequent relationships as follows:

$$C_1 \geq \frac{(M(1-D)-3)V_o}{\Delta V_{C1} 2R_L f_S} \tag{46}$$

$$C_2 \geq \frac{V_o}{\Delta V_{C2} 2R_L f_S} \tag{47}$$

$$C_3 \geq \frac{V_o}{\Delta V_{C3} R_L f_S}. \tag{48}$$

In some cases, minimizing the OVR ripple is crucial. Thus, the selection and design of the output capacitor are essential. To achieve this, the OVR is computed to guide the design and value determination of the output capacitor.

Based on the Fig. 3(a), during T_{on} the output capacitor current is related to the load current

$$i_{Co}(T_{on}) = -I_o. \tag{49}$$

Moreover, the OVR is determined as follows:

$$V_{Co,pp}{}^{CCM} = V_{Cop} - V_{Cov} = \frac{1}{C_o}\int_0^t i_{Co}(t)dt. \tag{50}$$

The relationship (50) can be rewritten as follows:

$$\Delta V_{Co} = V_{Co,pp}{}^{CCM} = \frac{V_o t}{R_L C_o}. \tag{51}$$

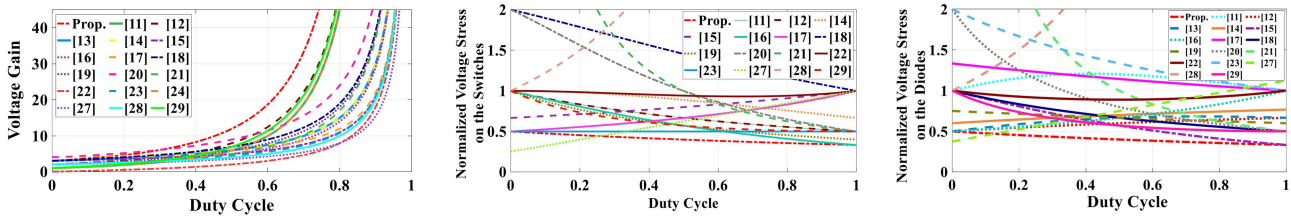
According to the first or third operation mode and based on the (51), the output capacitor's value is computed

$$C_o \geq \frac{(1-D)V_o}{\Delta V_{Co} 2R_L f_S}. \tag{52}$$

Based on the aforementioned computations, capacitors with values around 100 μF are chosen to minimize voltage ripple.

V. COMPARISON OF THE PROPOSED TOPOLOGY

Due to the validation of the benefits mentioned in the proposed topology, it has undergone a thorough comparison with various existing references. The comparative findings are given in Table II, which provides details on the analysis of main factors among the other converters like voltage gain, the normalized voltage stress on the power switches, the normalized voltage stress on the diodes, the number of components, the experimental ratio of output voltage to input voltage (test gain), common ground between the input source and output load, the electrical characteristics, such as input voltage, output voltage, switching frequency, output power, experimental efficiency at rated power, and peak of the experimental efficiency. Also, as depicted in Fig. 8(a), a comparison is provided regarding the voltage gain versus duty cycle for various converters. Fig. 8(b) illustrates the normalized voltage stress on the power switches versus the duty cycle, while Fig. 8(c) shows the normalized voltage stress on the diodes versus the duty cycle. As can be demonstrated in Table II and Fig. 8(a), the voltage gain of the suggested topology is more than the types of the other references based on the CIs, [11], [13], [15], [17], [21], [22], [23] and based on the CIs and voltage multiplier cells with $N=1$, [12], [14], [16], [19], [20], [24], [27], [28], and [29]. Nevertheless, for D<0.3, both [17] and [20] exhibit a higher voltage gain compared to the proposed topology. Furthermore, it is evident that the voltage stress across the power switch is lower than compared to the other topologies and as the duty cycle increases, the voltage stress on the power switch in the suggested converter diminishes, which is shown in Fig. 8(b). Hence, it can function within an ultrahigh step-up range while maintaining low voltage stress on the power switch. In most structures, the voltage stress is mostly on the output diodes. The output diode is chosen for comparison in all references. Throughout the all range of the duty cycle $0 < D < 1$, the voltage stress on the output diode is lower than the other converters which is observed in Fig. 8(c).



(a) (b) (c)

Fig. 8. Comparison studies of the proposed converter. (a) Voltage gain versus duty cycle. (b) Normalized voltage stress over the power switches versus duty cycle. (c) Normalized voltage stress over the diodes versus duty cycle.

Furthermore, the proposed topology features a single switch, one CI, and one input inductor, resulting in fewer components in the presented topology compared to references [11], [12], [14], [16], [18], [20], and [27]. The quantity of components is consistent compared to [19], [24], and [29]. However, the other topologies are provided with fewer components. In addition, a significant factor is provided in Table II is the experimental ratio of output voltage to input voltage, known as the test gain. Furthermore, according to the reported data the proposed topology achieves a favorable test gain compared to its counterparts. The presented topology exhibits a common ground along with continuous input current, which making it well-suitable for RESs applications. As are given in Table II, there is no common ground in [19] and [21]. In terms of the experimental efficiency, the proposed topology achieves competitive and appropriate performance at both rated power and peak efficiency, despite variations in the reference operating conditions. As given in Table II, this suggested structure exhibits higher experimental efficiency at rated power and peak level compared to most other comparable topologies. For particular applications, such as RES, keeping the ICR within an acceptable range is crucial. Table III presents the ICR for the proposed structure and other references. Based on Table III, in [12], [15], [24], and the proposed topology, the normalized ICR (ripple factor) is typically lower than 20%, which clearly demonstrates the effectiveness of these topologies for RES. However, in other referenced topologies, the ripple factor exceeds this value, which negatively impacts their overall performance. Table III considers the output current ripple (OCR), defined as the ratio of OVR to load resistance. As indicated, the OCR in the proposed structure is lower than that of most of its counterparts. While the compared topologies generally offer an acceptable level of OCR, some structures exhibit more reduction of OCR. In addition, another crucial key factor in comparing the proposed configuration's specifications with other structures is its power density. Moreover, Fig. 9 illustrates the power density of the proposed structure and several references. As noted, the primary factors contributing to the calculation of the power density are the components such as capacitors, inductors, and transformers. This comprehensive approach ensures an accurate assessment of power density by considering the physical volume occupied by essential components. Consequently, the effectiveness increases as the count of the components decreases. The recommended topology is achieved a power density 5.09 (W/cm^3), surpassing the values reported in references [11], [12], [14], [21], and [23].

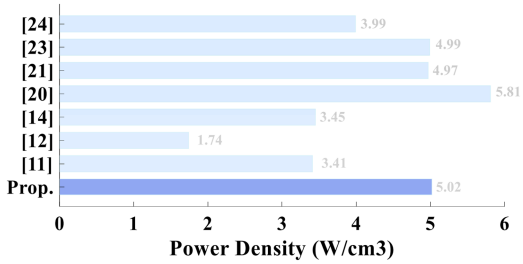


Fig. 9. Comparison power density of the proposed converter and the other topologies.

The power density is determined as follows:

$$PowerDensity(W/cm^3) = \frac{P_o(W)}{Totalvolume(cm^3)}. \quad (53)$$

VI. Control Scheme and Modeling

In order to control and model the propounded converter, the voltages of the four capacitors, the leakage and magnetizing currents of the CI, and the input inductor current are steady-state variables that are determined as follows:

$$x = [i_{Li}, i_{Lk}, i_{Lm}, , V_{C1}, V_{C2}, V_{C3}, V_{Co}]. \quad (54)$$

In addition, it is imperative to develop an appropriate controller to maintain the stable output voltage of the suggested converter in the face of load and input voltage variations. Also, a type III controller is applied to derive the transfer function. Thereupon, the transfer function of the output voltage to the duty cycle is computed as (55), shown at the bottom of the next page. As well as, Fig. 10 displays the bode diagram for both open-loop and closed-loop systems. A suitable controller is established to fine-tune the phase margin and gain margin. Phase margin $-.417°$ and -85.6 dB are derived for the open-loop system, respectively. By the same token, the closed-loop system yields a phase margin of 44.1° and 18.7 dB, respectively. Therefore, the results of the bode diagram after applying an appropriate controller validate the stability of the closed-loop system. Subsequently, the performance and the effectiveness of the closed-loop controller are confirmed in its simple design, which makes it flexible to implement

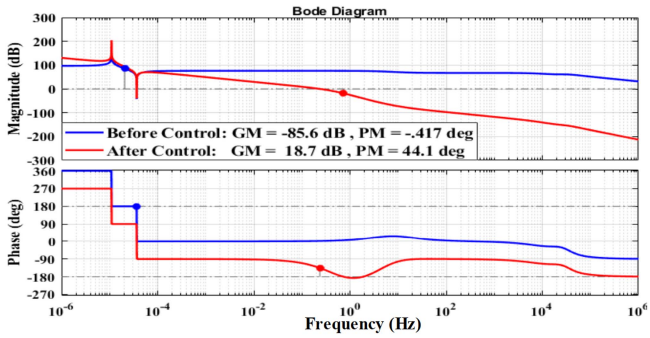


Fig. 10. Open-loop and closed-loop bode diagrams of the proposed converter transfer function.

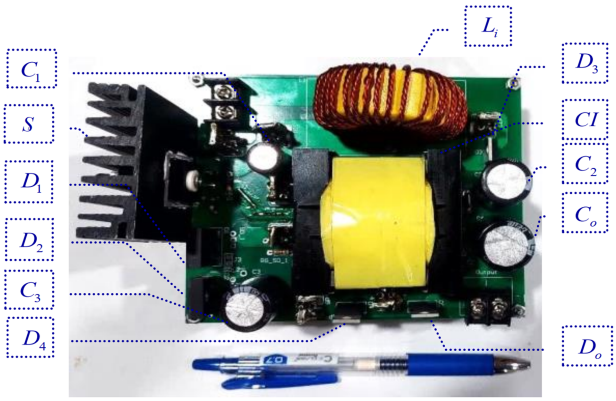


Fig. 11. Photograph prototype of the proposed converter.

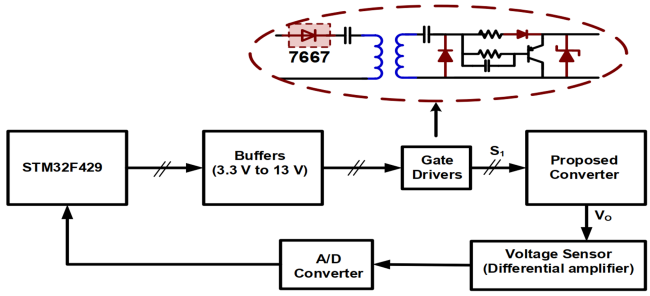


Fig. 12. Schematics of the controller type of the proposed topology.

VII. Experimental Results

In this section, a 300 W, 24 V to 400 V laboratory prototype of the propounded structure at 50 kHz switching frequency is constructed to confirm the accuracy of the theoretical analysis, utilizing the parameter values outlined in Table IV. Also, the photograph prototype of the proposed converter is shown in Fig. 11. It is noteworthy that to achieve a 400 V output voltage from 24 V input voltage, the duty cycle of the power switch is adjusted to 0.58 and N = 1 as determined in (17). The digital control of the propounded topology is executed using the STM32f429, as depicted in Fig. 12. It should be noted that, in Fig. 12 a differential amplifier feedback is utilized to implement the controller. Consequently, the subsequent steps involve verifying the proper functionality of the designed closed-loop controller. In the following, the experimental results are depicted in Fig. 13(a), (b), (c), (d), (e), (f), and (i). Fig. 13(a) presents the voltage and current of the input diode D_1. As shown in Fig. 13(a), the voltage stress on D_1 is $V_{D1} = 57.12V$, which corresponds to (20). Subsequently, Fig. 13(b) illustrates the voltage and current of D_2. It is obvious that, the voltage stress across D_2, is around $V_{D2} = 77.5\ V$, which is determined by (21) and prove the theoretical analysis. Furthermore, from these Fig. 13(a), (b), and (c), the voltage stresses across the input stage diodes are low, which causes less power losses. In Fig. 13(c), the voltage and current of D_3 are displayed. As can be seen, the voltage stress on D_3 is $V_{D3} = 267\ V$, which is close to (22). As well as, the voltage and current on the single power switch S is illustrated in Fig. 13(d). As depicted, the voltage stress on the power switch is $V_S = 133.5\ V$, which corresponds to (19). Based on the Fig. 13(d), the maximum voltage stress on the power switch is lower than the output voltage. Therefore, the MOSFET with the acceptable rise and fall time and low r_{DS-on} is selected. As a result, the power losses of the MOSFET are achieved at an acceptable level. Fig. 13(e) depicts the current of the input inductor L_i. The input inductor current maintains continuity with a minimal ripple lower than 20%, which this feature imputes it appropriate for renewable energy applications. Fig. 13(f) presents the current of the CI. The voltages of the capacitors C_1, C_2 and C_3 are shown in Fig. 13(g). As can be seen, these values are close to (12), (14), and (15). So, the theoretical analysis is proved. Eventually, the input voltage and output voltage of the proposed topology are shown in Fig. 13(h). In addition, in Fig. 13(i) the dynamic response of the propounded topology is illustrated. It is evident that, the output voltage can be swiftly regulated when the input voltage changes between 24 to 30 V. Moreover, in Fig. 14 the swift adjustments in output voltage are achievable when the output load shifts from 200 to 300 W or from 300 to 200 W. As a result, it can be comprehended the correctness of the controller performance, which applied to the proposed converter. Fig. 15(a) illustrates the theoretical and experimental efficiency of the proposed converter from 150 to 350 W. Notably, the suggested structure exhibits a substantial theoretical efficiency of 96.65% at 200 W, while achieving a commendable theoretical efficiency of 94.42%

$$G_{vd}(S) = \frac{v\tilde{}_o(s)}{d\tilde{}(s)} = \frac{(77.89e03)s^7+(9.189e10)s^6+(3.1866e14)s^5-(1.3026e20)s^4+(1.0467e22)s^3-(9.4995e12)s^2+(5.571e14)s+77.9}{(73.75)s^7+(12.084e06)s^6-(407.35e09)s^5-(57.209e15)s^4+(1.678e18)s^3+(1.387e09)s^2+(8.021e09)s-1}. \quad (55)$$

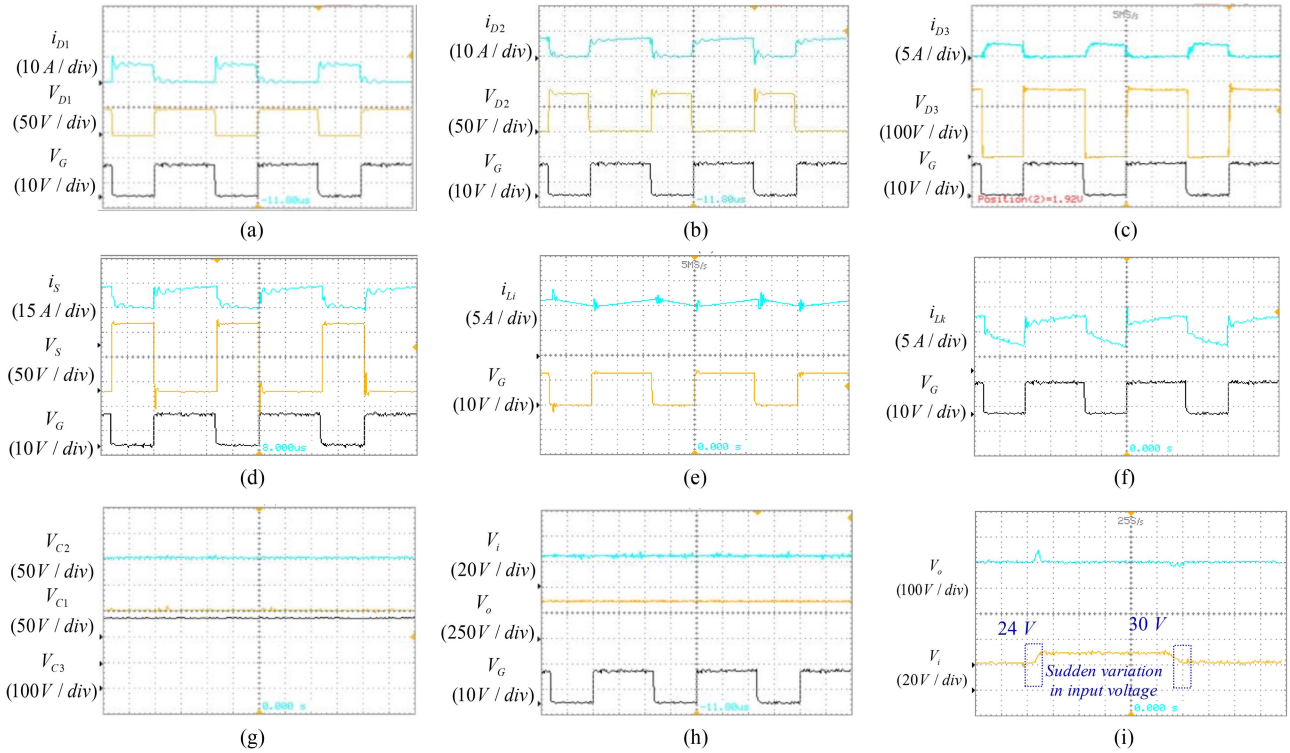


Fig. 13. Experimental results of the proposed converter prototype at 300 W output power, (a) i_{D1}, V_{D1} and V_G, (b) i_{D2}, V_{D2} and V_G, (c) i_{D3}, V_{D3} and V_G, (d) i_S, V_S and V_G, (e) i_{Li} and V_G, (f) i_{Lk} and V_G, (g) V_{C1}, V_{C2} and V_{C3}, (h) V_i, V_o and V_G. (i) Dynamic response under input voltage variation.

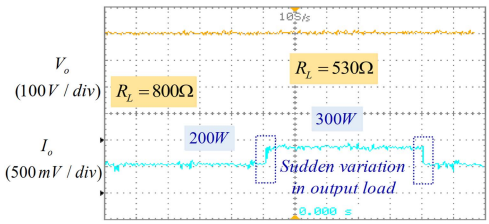


Fig. 14. Dynamic response of the proposed topology during output power variations from 200 to 300 W.

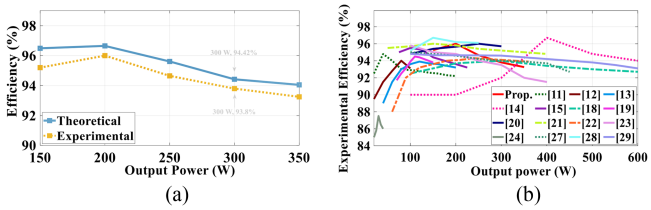


Fig. 15. Efficiency versus output power (a) Theoretical and experimental efficiency of the proposed structure versus output power. (b) Experimental power efficiency comparison of the proposed topology with the other counterparts.

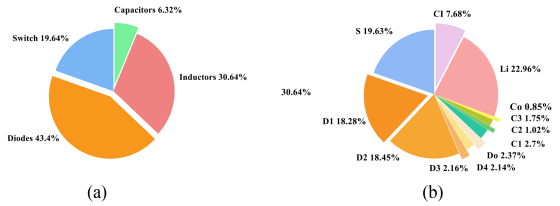


Fig. 16. Power losses distribution. (a) In nominal output power 300 W and 17.72 W total power losses. (b) Power losses on each component in detailed at 300 W.

at the rated power of 300 W in nominal load. Additionally, the propounded converter demonstrates consistently high efficiency across an acceptable range of the output power. Although, the highest experimental efficiency is recorded 96% at 200 w and 93.8% at a nominal load of 300 W. The graph in Fig. 15(b) illustrates the proposed structure's experimental efficiency compared to the other referenced topologies within the reported output power range. As depicted in Fig. 15(b), the suggested topology demonstrates competitive experimental efficiency at output power levels, which validates its performance. At rated power of 300 W and output voltage 400 V, the distribution power losses of the components based on the theoretical calculations are represented in Fig. 16(a) and (b). The total power losses are reported at 17.72 W, which the switching and conducting power losses of the MOSFET is 3.48 W and the power losses of the diodes, CI, input inductor, and capacitors are 7.69, 5.43, and 1.12 W, respectively. Ultimately, the efficiency of 94.42% is estimated and reported in 300 W output power. Also, Fig. 16(b) illustrates the power loss distribution among the components of the recommended converter. The inductors L_i and CI exhibit the highest total power losses 30.64%, followed by the power switch S at 19.64%, the input diodes D_1 and D_2 at 18.28% and 18.45%. The power losses of the diodes D_3, D_4, and D_o are 2.16%, 2.14%, and 2.37%, respectively. In addition, the capacitors C_1, C_2, C_3, and C_o experience the power losses, 2.7%, 1.02%, 1.75%, and 0.85%, respectively.

VIII. Conclusion

An ultra-high gain single-switch nonisolated dc–dc converter based on the CI with continuous and minimal RCR is introduced in this article. The propounded converter is achieved the ultra-high gain at a low turn ratio and duty cycle range which makes the proposed structure reach excellent performance and proper for RES applications. At nominal point of the proposed converter with $V_i = 24\ V$, $N = 1$, and $D = 0.58$ the voltage gain $M = 16.66$ is achieved. In addition, the suggested converter can minimize the voltage stress on the semiconductor devices. The voltage stress on the single power switch and diodes are significantly lower than the output voltage ratio. Moreover, the low voltage ripple across the capacitors, common ground between input source and output load, low number of components, high power density, and high efficiency are the benefits of the propounded converter. Consequently, the steady-state analysis and design consideration, a comparison study with other references from diverse viewpoints. As demonstrated in controller design section, the controller adjusts the output voltage 400 V when there are changes in input voltage from 24 to 30 V and output load from 800 to 530 W. A 300 W prototype of the presented structure is tested to validate the theoretical analysis with an efficiency of 94.42% at full load. Finally, these recommendations can be offered to enhance the performance through the implementation of the proposed configuration. By incorporating snubber circuits or soft-switching cells the propounded topology can demonstrate improved performance. Also, the semiconductor devices operate under soft-switching conditions, resulting in reduced power losses and increased efficiency.

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