Three-Dimensional Electro-Thermal Coupling Temperature Evaluation Modeling of Wire-Bonded Power Chips Under Surge Conditions

Feilin Zheng, Binqi Liang, Xiang Cui, *Senior Member, IEEE*, Xuebao Li, *Member, IEEE*, and Lei Qi

***Abstract*—The relationship between the failure of power semiconductor chips under surge conditions and the resultant high temperatures due to self-heating underscores the importance of acquiring the chip's temperature during surge conditions for reliability assessment. However, the current experimental approach for directly obtaining the chip's transient junction temperature is not readily applicable in practical engineering under surge conditions. Hence, there is a critical need for accurate modeling to calculate the chip's transient temperature rise. This article presents a pioneering fully-coupled electro-thermal model that integrates chip physical properties with three-dimensional (3-D) packaging structures. It facilitates the computation of the chip's 3-D temperature distribution under surge conditions without resorting to destructive surge experiments. The article elucidates the modeling principles and process, demonstrating that the surge I-V trajectory and temperature distribution derived from the model closely match experimental measurements.**

***Index Terms*—Electro-thermal model, surge condition, temperature distribution.**

I. Introduction

With the continuous increase in power levels of electrical systems, phenomena like surge current and short circuits are becoming more prevalent, leading to heightened scrutiny on the problem of power device failures during overcurrent conditions [1], [2]. Taking surge conditions as an example, when a surge current significantly exceeds the rated value flowing through power devices, the power diode chip inside the device may undergo thermal breakdown due to severe self-heating effects, resulting in failure. Extensive research has shown a substantial connection between surge failures of power diodes and the melting of metallization at the melting point [3], [4]. Hence, it is necessary to promptly capture the transient temperature changes of the power diode chip under surge conditions to evaluate potential performance degradation.

Temperature measurement of chips can be categorized into two methods: 1) experimental techniques and 2) modeling calculations. However, experimental methods are not viable for use in surge conditions, the subsequent explanation will detail the reasons for this limitation. Experimental methods can be categorized into direct measurement and indirect measurement. Direct measurement methods involve the utilization of temperature measuring devices such as thermocouples or infrared thermal imaging cameras to directly gather the temperature of the chip [5], [6]. While these methods are convenient and accurate, they are not suitable for application in surge conditions due to the limited sampling rates of thermocouples and their inability to support high-speed transient temperature capture. Cooling type infrared thermal imaging cameras can satisfy the temperature measurement requirements of surge conditions, but this entails high costs and the use of IR technology necessitates depackaging the device, which is not permitted in practical engineering scenarios. The indirect measurement method mentioned above primarily refers to the thermally sensitive electrical parameters (TSEPs) method, which can be used to estimate the chip's transient junction temperature by continuously monitoring a series of TSEPs of the power chip [7]. While this method is widely applied in condition monitoring, it is not suitable for surge conditions. This is because this method requires prior calibration of the TSEPs for the corresponding operating conditions. For example, in the case of silicon(Si) based chips, temperature calibration can only be conducted within 200 °C without causing harm to the chip. However, chip temperatures in surge conditions can exceed 400 °C, indicating that the TSEPs method is not appropriate for extremely high temperature ranges.

Given the ineffectiveness of experimental methods, it is essential to utilize modeling techniques to calculate the temperature variations of power chips under surge conditions. Hunger et al. [8] constructed a finite element (FE) model to evaluate the three-dimensional (3-D) temperature distribution of Si p-i-n diodes under surge conditions. They developed a chip heating model based on the equivalent resistance of the static forward I-V characteristics, but there was a discrepancy between the modeling of the bonding wires and the actual packaging structure. Heinze et al. [9] utilized TCAD to create a finite element model for

Received 30 May 2024; revised 12 September 2024; accepted 31 October 2024. Date of publication 6 November 2024; date of current version 18 December 2024. This work was supported by National Outstanding Youth Science Fund Project of National Natural Science Foundation of China under Grant 52225701. Recommended for publication by Associate Editor L. Wang. *(Corresponding author: Xiang Cui.)*

The authors are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China (e-mail: feilin_zheng@ncepu.edu.cn; binqiliang@ncepu.edu.cn; x.cui@ncepu.edu.cn; lxb08357x@ncepu.edu.cn; qilei@ncepu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3492917.

Digital Object Identifier 10.1109/TPEL.2024.3492917

calculating the temperature and voltage of silicon p-i-n diodes under surge conditions. The majority of the models developed using TCAD software were 2-D semiconductor cell models, which do not incorporate the actual 3-D packaging structure of the chip. Carastro et al. [10] utilized a fitting formula based on the static forward I-V characteristics provided in the device's datasheet to calculate the overall voltage drop of the device. They further employed a thermal network model to calculate the temperature of the diode device under surge conditions. However, this method is limited to 1-D scenarios and requires datasheets from device manufacturers. Palanisamy et al. [11] utilized a FE model to analyze the temperature distribution of Silicon Carbide (SiC) merged pin Schottky (MPS) diodes under surge conditions. The model considered the actual packaging structure of the device but continued to use the equivalent resistance method based on static forward I-V characteristics as the chip heating model. Wu et al. [12] developed an electro-thermal coupling model with distributed heat sources for calculating the temperature of SiC MPS diodes under surge conditions. This model offers faster computations but is limited to considering the 1-D temperature distribution of the chip.

In conclusion, the current calculation methods typically employ the equivalent resistance based on static forward I-V characteristics to establish the behavior model of the entire chip, which disregards the actual heating conditions inside the chip. Additionally, these models struggle to achieve 3-D chip temperature distribution calculations, and all of these methods lack direct experimental validation. Consequently, this article presents a novel fully coupled electro-thermal model, integrating the chip's physical characteristics with the 3-D packaging structure for the first time, enabling for the calculation of the chip's temperature distribution under surge conditions. The rest of this article is organized as follows. Section II introduces the three primary issues associated with the heating of power diode chips under surge conditions. In Section III, three subphysical models are developed to address these issues individually, followed by comprehensive electro-thermal coupling of all submodels to form a final complete computational model. Section IV compares experimental validation results with modeling calculation results. Finally, Section V concludes this article.

II. Issues Encountered in Constructing a Chip Temperature Model Under Surge Conditions

Fig. 1 presents the outlines of current, voltage, and maximum temperature of the chip under 10 ms sine half wave single pulse surge conditions, along with the temperature and heat flux distribution within the chip at a specific moment. When the peak surge current surpasses ten times the rated current of the chip, internal heating of chip becomes highly uneven, with local temperatures potentially exceeding 600 °C. This can lead to thermal breakdown of the chip as the metallization approaches its melting point.

To develop a precise temperature assessment model, it is essential to grasp the core essence of power chip heating under surge conditions. Actually, the heating of chips under surge conditions are distinct from those under other current overload

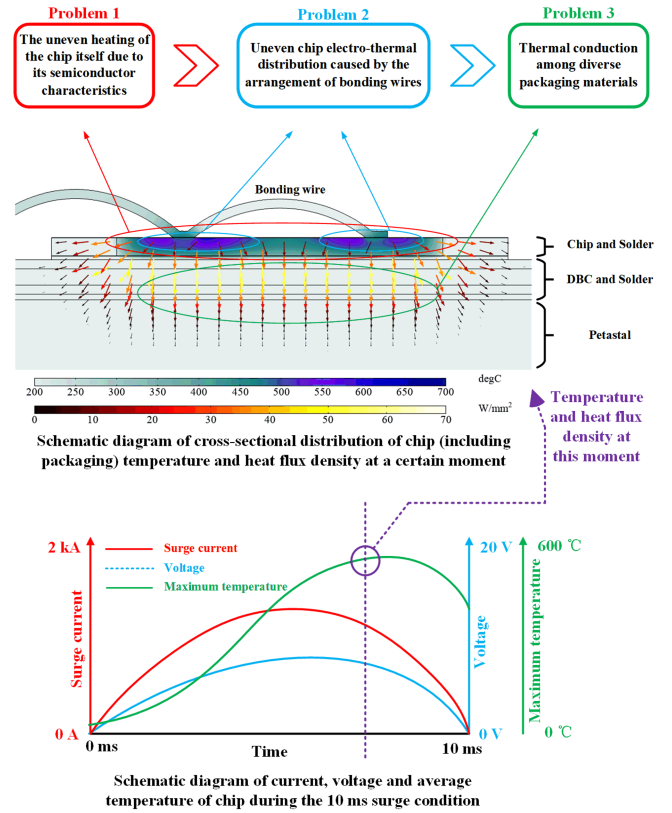

Fig. 1. Problems faced in establishing a chip temperature model under 10 ms sine half wave single pulse surge conditions.

conditions and can be distilled into three levels of problems: 1) The chip's heating is uneven due to its semiconductor characteristics; 2) The uneven distribution of chip thermal is caused by the arrangement of bonding wires; 3) Thermal conduction occurs among diverse packaging materials.

A. Problem 1: Uneven Heating of the Chip Itself Due to Its Semiconductor Characteristics

The analysis focuses on Si p-i-n diodes to illustrate semiconductor properties, as shown in Fig. 2. During surge conditions, the diode's drift region undergoes significant injection, causing a chain-like distribution of charge carriers within the chip [13]. Equation (1) can be employed to estimate the voltage of the chip in the drift, where V_{drift} is the voltage of the drift region, j is the current density, q is the electron charge, d_{B} is the width of drift region, p is the hole concentration, μ_{n} and μ_{p} are the electron mobility and hole mobility, respectively. It can be approximately inferred from (1) that the voltage drop across the chip vertically is not uniform. The concentration of carriers is lower in the middle of the drift region, leading to a higher voltage drop, whereas it is higher near the junction, resulting in a lower voltage drop accordingly

$$V_{\text{drift}} = \frac{j}{q\left(\mu_{\text{n}} + \mu_{\text{p}}\right)} \int_{0}^{d_{\text{B}}} \frac{\mathrm{d}x}{p\left(x\right)}. \tag{1}$$

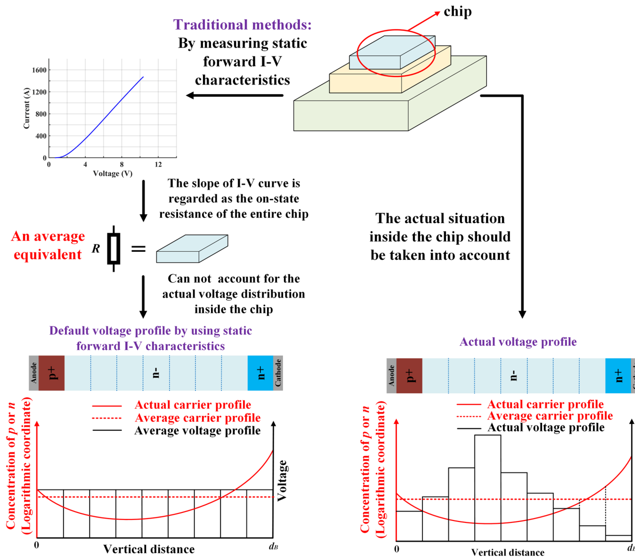

Fig. 2. Uneven voltage caused by carrier distribution in p-i-n diodes.

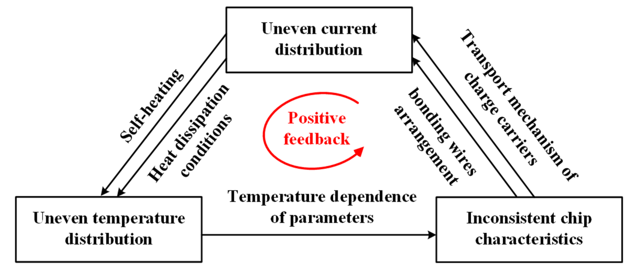

Fig. 3. Arrangement of bonding wires intensifies current localization.

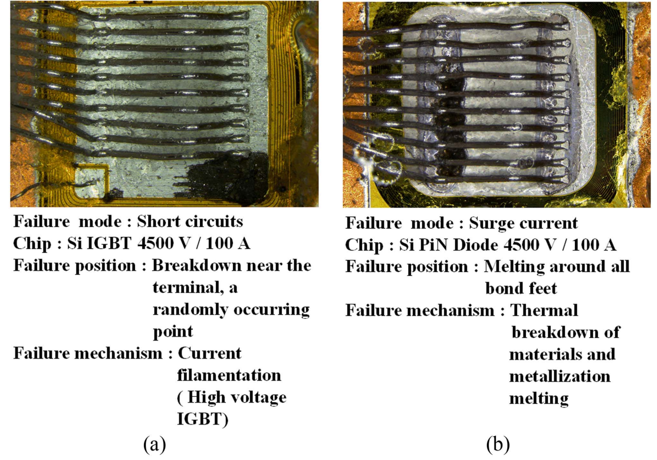

Fig. 4. Different failure modes of short circuit and surge. (a) Short circuit failure. (b) Surge failure.

Variations in voltage drops can induce nonuniform Ohmic heating in the chip, making the heat generation at different locations dependent on the local carrier concentration. Thus, the assumption of uniform heat generation across the chip is not applicable. The modeling methodologies [8], [10], [11], [12] referenced in the Introduction frequently consider the chip as a uniform volume heat source within finite element models, deriving the overall chip's equivalent resistance from its static forward I-V characteristics. In such circumstances, the internal voltage drop within the chip is generally assumed to be uniform, constituting a form of averaged approximation. These documented methods primarily investigate heat dissipation from the chip to the packaging material, disregarding the uneven distribution of heat power generated inside the chip due to variations in carrier concentration. Yet, it is precisely the internal self-heating of the chip during surge conditions that merits the utmost attention.

B. Problem 2: Uneven Chip Electro-Thermal Distribution Caused by the Arrangement of Bonding Wires

Because power chips possess larger dimensions while bonding wires have smaller diameters, the arrangement of bonding wires inherently causes nonuniform current distribution within the chip, this, in turn, leads to uneven heat generation. As depicted in Fig. 1, the chip experiences relatively higher temperatures near the bond feet and lower temperatures in areas distant from bond feet. This phenomenon is commonly referred to as current localization [8]. The causes of this phenomenon can be traced to two factors: 1) substantial differences in size and conductivity characteristics among bond corners, metallization, and the die; 2) the chip's current-carrying capacity fluctuates with variations in temperature and injection level, rather than remaining constant. As shown in Fig. 3, the heating of the chip under surge conditions is characterized by a complex positive feedback electrothermal coupling process: initially, nonuniform current distribution within the chip is caused by the arrangement of bonding wires. With the increasing current and subsequent heating, the variations in the conductivity of materials in different regions occur. This leads to the gradual amplification of differences in conductivity among different chip locations, resulting in further accentuation of current crowding.

C. Problem 3: Thermal Conduction Among Diverse Packaging Materials

In accordance with JEDEC standards [14], the surge testing current for power devices usually lasts 10 ms, differing from transient overheating conditions lasting only microseconds, such as short-circuit durations. At the millisecond time scale, the self-heating generated by the chip can be conducted through the packaging material rather than being solely confined within the chip itself.

Fig. 4 presents the chip's morphology following short-circuit and surge failures, highlighting their differences. The former [see Fig. 4(a)] is linked to the formation of current filaments, with failure points randomly occurring near the chip's terminal. This indicates that short-circuit failure is a semiconductor characteristic failure, the occurrence of thermal breakdown at a specific point on the chip is often induced by semiconductor mechanisms. Conversely, the locations of surge failures shown in Fig. 4(b) are distributed around all bond feet, exhibiting a more regular pattern. As mentioned in the Introduction, surge failures are not classified as semiconductor characteristic failures but

are more closely associated with metallization melting. Heat within the 10 ms period is adequate to spread across various locations within the chip and continue dispersing towards the heat dissipation path. As depicted in Fig. 1, there exists a significant heat flux density between the packaging materials. Consequently, the packaging structure inevitably influences the chip's temperature distribution under surge conditions. However, the semiconductor model constructed using TCAD, as mentioned earlier [9], is constrained by software computing capabilities and can only describe the characteristics of individual chip cells, incapable of illustrating the electro-thermal properties of chips with packaging structures.

In summary, for an accurate evaluation of chip temperature distribution under surge conditions through modeling and computation, all three crucial issues mentioned above must be thoroughly addressed. Therefore, this article elucidates each of these issues using three distinct physical models and ultimately establishes a comprehensive computational model that fully couples electrical and thermal aspects.

III. Principles of Modeling

A . Lumped-Charge Model of p-i-n Diode

As highlighted in Section II-A, it is crucial to account for the uneven heat generation throughout the chip resulting from the distribution of carriers. Therefore, unlike the approach adopted in all cited literature, which extracts the overall chip's equivalent resistance using static forward I-V characteristics, this article introduces a physical model based on the internal properties of the chip. This model, known as the lumped-charge (LC) model, comprehensively considers the carrier transport mechanism inside the chip [14], [15], [16]. The LC model involves positioning charges at specific locations within the chip to represent the charge control effect inside. Rooted in semiconductor physics of power chips, this model offers an analytical approach, circumventing the complexity of solving carrier bipolar transport equations (second-order differential equations). It proficiently describes both the microscopic carrier distribution inside the chip and the macroscopic electrical characteristics outside.

Fig. 1 shows that a certain quantity of lumped charge points are placed in the low-doped drift region, and it is approximately assumed that the carrier concentration between the charge points follows a linear distribution. Here, $p_{,\mathrm{i}}$ represents the hole concentration at point i, $d_{,\mathrm{i(i+1)}}$ denotes the distance between $p_{,\mathrm{i}}$ and $p_{,\mathrm{i+1}}$, and the hole current density $j_{\mathrm{p,i(i+1)}}$ flowing from $p_{,\mathrm{i}}$ to $p_{,\mathrm{i+1}}$ can be expressed as

$$j_{\mathrm{p,i(i+1)}} = -qD_{\mathrm{p}}\frac{\mathrm{d}p}{\mathrm{d}x} + q\frac{p_{,\mathrm{i}} + p_{,\mathrm{(i+1)}}}{2}\mu_{\mathrm{p}}\left|\boldsymbol{E}_{,\mathrm{i(i+1)}}\right| \quad (2)$$

where D_{p} is the diffusion coefficient of holes, and $\boldsymbol{E}_{,\mathrm{i(i+1)}}$ represents the electric field strength on $d_{,\mathrm{i(i+1)}}$. The first term on the right-hand side of (2) represents the diffusion current component, and the second term represents the drift current component. Based on the linear approximation of the carrier concentration between the charge points, the differential term in the diffusion current can be expressed as

$$\frac{\mathrm{d}p}{\mathrm{d}x} = \frac{p_{,\mathrm{(i+1)}} - p_{,\mathrm{i}}}{d_{,\mathrm{i(i+1)}}}. \quad (3)$$

In the drift current component, based on the Poisson's equation approximation and the charge neutrality principle, and by disregarding the built-in electric field, the magnitude of the electric field strength between $p_{,\mathrm{i}}$ and $p_{,\mathrm{i+1}}$ can be considered constant, which can be expressed as

$$\left|\boldsymbol{E}_{,\mathrm{i(i+1)}}\right| = \frac{v_{,\mathrm{i(i+1)}}}{d_{,\mathrm{i(i+1)}}} \quad (4)$$

where $v_{,\mathrm{i(i+1)}}$ is the voltage drop between $p_{,\mathrm{i}}$ and $p_{,\mathrm{i+1}}$. As the drift current is primarily affected by the lower carrier concentration, it can be approximated as

$$\frac{p_{,\mathrm{i}} + p_{,\mathrm{(i+1)}}}{2} \approx p_{,\mathrm{(i+1)}}. \quad (5)$$

By normalizing the carrier concentration to the total volume of the chip (or cell), i.e., $q_{\mathrm{p,i}} = Aqd_{\mathrm{B}}p_{,\mathrm{i}}$, where A represents the cross-sectional area of the chip (or cell), and d_{B} is the total width of the drift region, (1) can be reformulated as

$$i_{\mathrm{p,i(i+1)}} = \frac{q_{\mathrm{p,i}} - q_{\mathrm{p,(i+1)}}}{T_{\mathrm{p,i(i+1)}}} + \frac{q_{\mathrm{p,(i+1)}}}{T_{\mathrm{p,i(i+1)}}}\frac{v_{,\mathrm{i(i+1)}}}{V_{\mathrm{T,i(i+1)}}} \quad (6)$$

where $i_{\mathrm{p,i(i+1)}}$ represents the hole current flowing through the entire chip (or cell), $T_{\mathrm{p,i(i+1)}}$ is the transit time of holes between $p_{,\mathrm{i}}$ and $p_{,\mathrm{i+1}}$, and $V_{\mathrm{T,i(i+1)}}$ denotes the thermal voltage.

In the LC model, instead of using the large injection assumption, i.e., $n \approx p$, it is assumed that the electron concentration at the charge points is always higher than the hole concentration by the thermal equilibrium electron concentration $n_{0,\mathrm{i}}$ at that point, i.e., $q_{\mathrm{n,i}} = q_{\mathrm{p,i}} + Q_{\mathrm{n0,i}}$, where $q_{\mathrm{n,i}}$ is the normalized lumped electron charge, and $Q_{\mathrm{n0,i}} = Aqd_{\mathrm{B}}n_{0,\mathrm{i}}$ is the normalized lumped charge of the thermal equilibrium electron concentration in the drift region. Therefore, the electron current $i_{\mathrm{n,i(i+1)}}$ flowing from $p_{,\mathrm{i}}$ to $p_{,\mathrm{i+1}}$ can be expressed as

$$i_{\mathrm{n,i(i+1)}} = -\frac{q_{\mathrm{p,i}} - q_{\mathrm{p,(i+1)}}}{T_{\mathrm{n,i(i+1)}}} + \frac{q_{\mathrm{p,(i+1)}} + Q_{\mathrm{n0,}(i+1)}}{T_{\mathrm{n,i(i+1)}}}\frac{v_{,\mathrm{i(i+1)}}}{V_{\mathrm{T,i(i+1)}}} \quad (7)$$

where $i_{\mathrm{n,i(i+1)}}$ represents the electron current flowing through the entire chip (or cell), $T_{\mathrm{n,i(i+1)}}$ is the transit time of holes between $p_{,\mathrm{i}}$ and $p_{,\mathrm{i+1}}$.

In the field of semiconductor device physics, there is an additional important equation that must be taken into account, which is the current continuity equation. Using holes as an example

$$\frac{\partial p}{\partial t} = G_{\mathrm{p}} - U_{\mathrm{p}} - \frac{1}{q}\nabla \cdot \boldsymbol{J}_{\mathrm{p}} \quad (8)$$

where G_{p} and U_{p} represent the generation and recombination rates of holes, respectively. In the case of high injection, the generation rates of electrons and holes can be neglected. Therefore, integrating (8) from $p_{,\mathrm{i-1}}$ to $p_{,\mathrm{i+1}}$ and considering $q_{\mathrm{p,i}}$ as the total lumped charge on $d_{,\mathrm{(i-1)i}} + d_{,\mathrm{i(i+1)}}$ yields

$$i_{\mathrm{p,(i-1)i}} - i_{\mathrm{p,i(i+1)}} = \frac{q_{\mathrm{p,i}} - Q_{\mathrm{n0,i}}}{\tau_{,\mathrm{i}}} + \frac{\mathrm{d}q_{\mathrm{p,i}}}{\mathrm{d}t} \quad (9)$$

Where $\tau_{,\mathrm{i}}$ stands for the average carrier lifetime on $d_{,(\mathrm{i-1})\mathrm{i}} + d_{,\mathrm{i(i+1)}}$. Similarly, the current continuity equation in the form for electrons can be obtained, and only one of these forms needs to be employed in practical applications.

Regarding the nodes $p_{,2}$ near the p-n junction and $p_{,\mathrm{n}}$ near the NN$^+$ junction, there is no requirement to explicitly write the current continuity equations. Instead, the lumped charge at these locations is expressed using the Boltzmann formula. Taking $p_{,2}$ as an example

$$q_{\mathrm{p},2} = Q_{\mathrm{p0,i}} \exp\left(\frac{v_{,12}}{V_{\mathrm{T},12}}\right) \tag{10}$$

where $Q_{\mathrm{p0,i}} = Aqd_{\mathrm{B}}p_{0,\mathrm{i}}$ represents the normalized lumped charge of the equilibrium hole concentration in the drift region. Similarly, for the nodes $p_{,1}$ within the p-n junction and $p_{,\mathrm{n+1}}$ within the NN$^+$ junction, the Boltzmann formula is used to express the lumped charge at these locations. Taking $n_{,1}$ as an example

$$q_{\mathrm{n},1} = (q_{\mathrm{p},1} + Q_{\mathrm{n0},1}) \exp\left(\frac{v_{,12} - \Phi_{,12}}{V_{\mathrm{T},12}}\right) \tag{11}$$

where $\Phi_{,12}$ is the built-in voltage of the p-n junction. For the nodes $p_{,1}$ and $p_{,\mathrm{n+1}}$, the recombination effects in the heavily doped regions can be represented by listing the respective current continuity equations.

Finally, in accordance with Kirchhoff's current law (KCL), the ensuing current equations can be written for the internal nodes in the drift region

$$i_{\mathrm{p,(i-1)i}} + i_{\mathrm{n,(i-1)i}} = i_{\mathrm{p,i(i+1)i}} + i_{\mathrm{n,i(i+1)}}. \tag{12}$$

Based on the Kirchhoff's voltage law (KVL), the sum of the voltage drops across the layers of the chip is equal to the total voltage V_{c}

$$V_{\mathrm{c}} = \sum_{i=1}^{n} v_{,\mathrm{i(i+1)}}. \tag{13}$$

At this point, the three basic equations of semiconductor device physics, including the transport equation, Poisson's equation, and the current continuity equation, have all been considered. When a total of n+1 nodes are placed within the chip (or cell), the chip is divided into n layers, as shown in Fig. 5. To establish a square system of nonlinear equation system, the current continuity equations, KCL current equations, and KVL voltage equations need to be written for the internal nodes in the drift region. By solving this nonlinear equation system, the distribution of charge carriers, the voltage components, and the current components within the chip (or cell) can be obtained under a given external voltage V_{c}.

B. Chip Circuit Model With Bonding Wire Arrangement

As mentioned in Section II-B, the bonding wires layout inevitably results in current localization. This article employs a self-designed Si PiN power diode device (4500 V/100 A) as an example of device under test (DUT) to abstract the underlying physical model of current localization. As depicted in Fig. 6, the device is consistent with the ones shown in Figs. 4(b) and 1, the

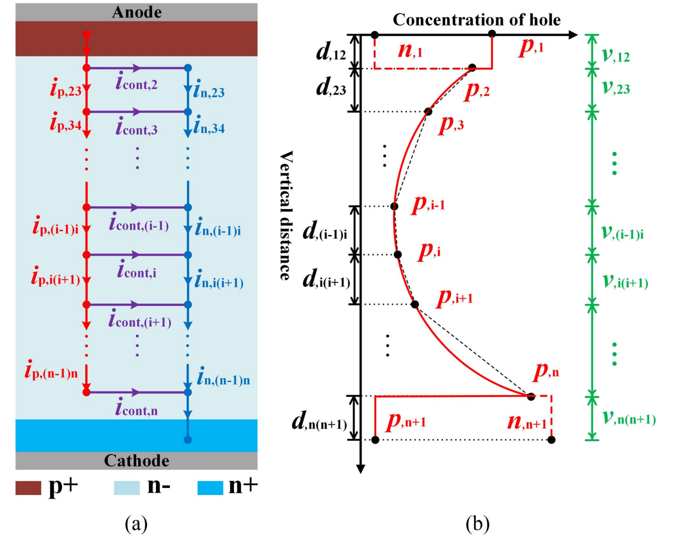

Fig. 5. LC model of p-i-n diode. (a) Current component inside the chip. (b) Carrier distribution.

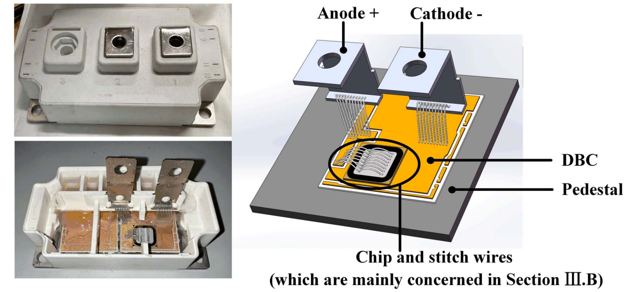

Fig. 6. Schematic of device under test.

test chip is soldered onto a substrate and adopts a stitch-bonded wires scheme to attain higher current-carrying capacity. However, as can be observed in Figs. 4(b) and 1, current localization is still quite pronounced, with larger currents flowing through the areas around the bonding wires, leading to more severe heating in those areas.

Concerning the chip structure presented in Fig. 6, we have abstracted an equivalent circuit model that exclusively includes the active region of the chip, the metallization, and the stitch-bonded wires, as shown in Fig. 7. This model adopts a unit-cell approach, dividing the active region of the chip into M × N individual units, with each unit consisting of a metallization cell and a chip cell. The segment of the current flowing from the anode-side direct bonded copper (DBC) through the bonding wires to the first bond feet has been disregarded. It is assumed that the current flowing through each bonding wire is uniform and is represented by the current source $i_{\mathrm{s,i}}$. Initially, the current on each stitch-bonding wire reaches the first bond feet, i.e., all the metallization cells on Row,2 in Fig. 7. Then, the current separates into three parts: 1) the first part conducts laterally in various directions within the metallization, 2) the second part flows vertically into the chip cells below, and 3) the final part passes through the stitch-bonding wires to the second bond feet, i.e., all the metallization cells on Row,M-1 in Fig. 7, before continuing

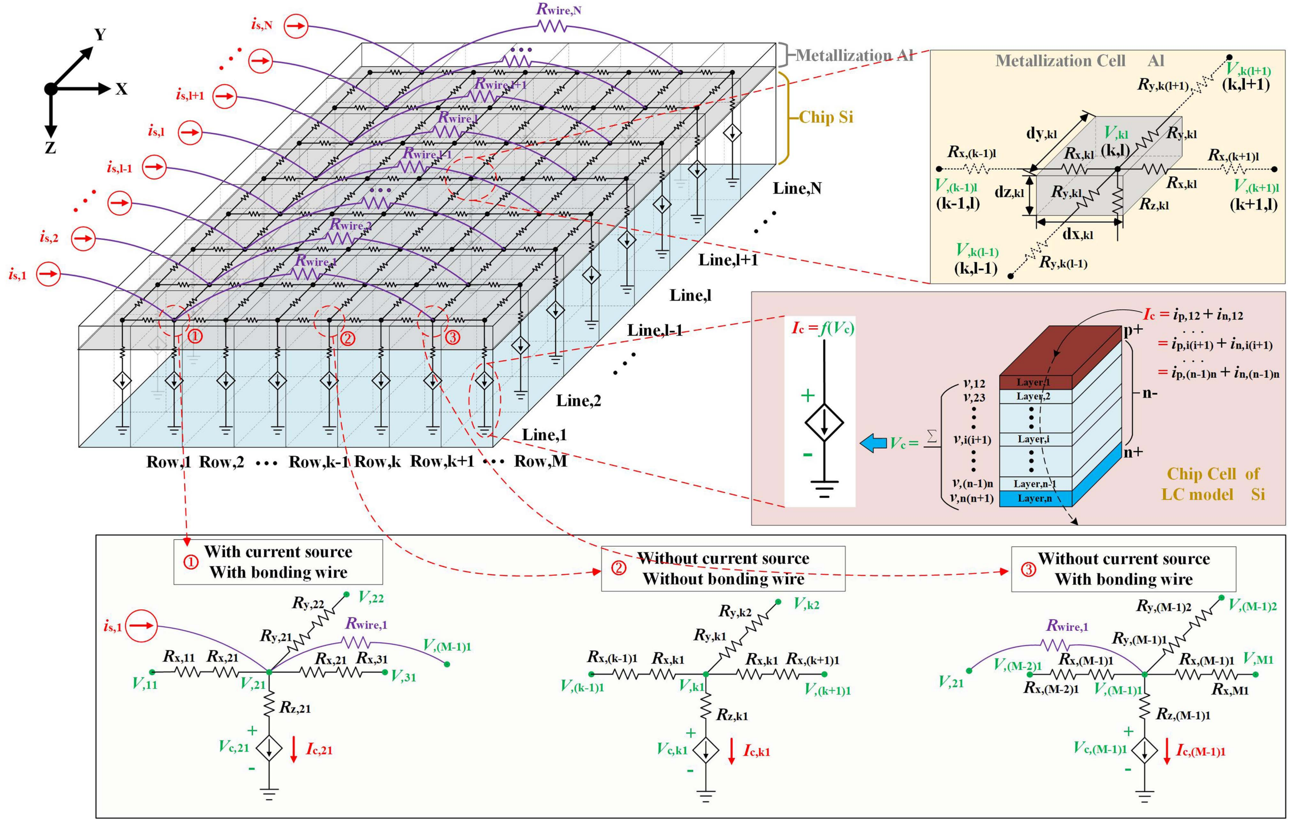

Fig. 7. Chip circuit model with bonding wire arrangement.

with further conduction. The discretization of the chip into unit cells enables us to effectively capture the current localization characteristics. Owing to the bonding wires layout, the current density is enhanced around the bond feet, but diminishes in locations farther away from the bond feet.

1) First, in the case of the current's lateral conduction through the metallization, we adopted an equivalent diffusion resistance model as a means to effectively describe this physical process. For instance, consider the yellow square depicted in the top right corner of Fig. 7, which corresponds to the metal cell located in the Row,k and Line,l. The cell is labeled as (k, l), and the dimensions of the cell in the *X-, Y-, and Z*-directions are $\mathrm{dx}_{,\mathrm{kl}}$, $\mathrm{dy}_{,\mathrm{kl}}$, $\mathrm{dz}_{,\mathrm{kl}}$. The center point of the cell corresponds to the sought potential value $V_{,\mathrm{kl}}$. The internal of the cell comprises five diffusion resistances, with two $R_{\mathrm{x,kl}}$ and two $R_{\mathrm{y,kl}}$ representing the diffusion resistances in the left, right, front, and back horizontal directions, respectively, connected to the horizontal diffusion resistances of the adjacent cells. $R_{\mathrm{z,kl}}$ denotes the vertical diffusion resistance in the downward direction, linked to the chip cell corresponding vertically to the metal cell (k, l). The calculation formulas for each diffusion resistance are as follows:

$$\begin{cases} R_{\mathrm{x,kl}} = \frac{\mathrm{dx}_{,\mathrm{kl}}}{2\sigma_{\mathrm{Al,kl}}\mathrm{dy}_{,\mathrm{kl}}\mathrm{dz}_{,\mathrm{kl}}} \\ R_{\mathrm{y,kl}} = \frac{\mathrm{dy}_{,\mathrm{kl}}}{2\sigma_{\mathrm{Al,kl}}\mathrm{dx}_{,\mathrm{kl}}\mathrm{dz}_{,\mathrm{kl}}} \\ R_{\mathrm{z,kl}} = \frac{\mathrm{dz}_{,\mathrm{kl}}}{2\sigma_{\mathrm{Al,kl}}\mathrm{dx}_{,\mathrm{kl}}\mathrm{dy}_{,\mathrm{kl}}} \end{cases} \quad (14)$$

where $\sigma_{\mathrm{Al,kl}}$ is the conductivity of metallized cells (k, l).

2) Second, to address the problem of the current flowing vertically into the chip cells, we performed an equivalent modeling of the chip cell's LC model. As analyzed in Section III-A of, by solving the nonlinear equation system of the LC model given the external voltage V_{c}, we can derive the voltage and current compositions of the various layers within the chip cell. According to (11), the total current I_{c} within the cell's layers remains constant. Consequently, the nonlinear equation system generated by the LC model can be equivalently represented as a voltage-controlled current source system, as indicated by the pink square on the right side of Fig. 7, where the relationship $I_{\mathrm{c}} = f(Vc)$ signifies the connection between external voltage and current in the LC model. This ingenious equivalence skillfully integrates semiconductor physics with circuit theory, seamlessly integrating the LC model into the entirety of the circuit network. Under this equivalence, the potential values $V_{,\mathrm{kl}}$ of each metallized cell can be solved by formulating KVL equations, and the voltage distribution $v_{,\mathrm{i(i+1)}}$ within each layer of the chip cell and the total voltage Vc can also be determined through the LC model. The solutions are derived from semiconductor physics, allowing for a thorough consideration of the transport mechanisms of carriers inside the chip and the influence of wire bonding arrangements on the overall cell potential.

3) Finally, to tackle the issue of current passing through stitch-bonded wires to the second bond feet, we employ the equivalent resistance $R_{\mathrm{wire,l}}$ of the wire bonding to depict this process

$$R_{\mathrm{wire,l}} = \frac{l_{\mathrm{wire,l}}}{\sigma_{\mathrm{Al}} \pi r_{\mathrm{wire,l}}^2} \tag{15}$$

where $l_{\mathrm{wire,l}}$ and $r_{\mathrm{wire,l}}$, represent the length and diameter of stitch-bonded wires, respectively.

The construction of the chip circuit model with bonding wires layouts is now finalized. The subsequent step involves elucidating the solving process of this model using three exemplar nodes for clarity. These nodes are the ①, ②, and ③ nodes in the Line,1 cell of Fig. 7, covering all node types in the circuit model. The equivalent circuit for each node is presented in the box at the bottom of Fig. 7.

The ① node denotes a type of node that includes both a current source and a bond feet. The KVL equations for the ① node are as follows:

$$\begin{cases} (V_{,21}-V_{,11})/(R_{\mathrm{x},11}+R_{\mathrm{x},21})+(V_{,21}-V_{,31})/(R_{\mathrm{x},21}+R_{\mathrm{x},31}) \\ +(V_{,21}-V_{,22})/(R_{\mathrm{y},21}+R_{\mathrm{y},22})+\left(V_{,21}-V_{,(\mathrm{M}-1)1}\right)/R_{\mathrm{wire},1} \\ = i_{\mathrm{s},1}-f(V_{\mathrm{c},21}) \\ f(V_{\mathrm{c},21}) = (V_{,21}-V_{\mathrm{c},21})/R_{\mathrm{z},21}. \end{cases} \tag{16}$$

The ② node denotes a type of node that does not have either a current source or a bond feet. The KVL equations for the ② node are as follows:

$$\begin{cases} \left(V_{,\mathrm{k}1}-V_{,(\mathrm{k}-1)1}\right)/\left(R_{\mathrm{x},(\mathrm{k}-1)1}+R_{\mathrm{x},\mathrm{k}1}\right)+\left(V_{,\mathrm{k}1}-V_{,(\mathrm{k}+1)1}\right)/ \\ \left(R_{\mathrm{x},\mathrm{k}1}+R_{\mathrm{x},(\mathrm{k}+1)1}\right)+(V_{,\mathrm{k}1}-V_{,\mathrm{k}2})/(R_{\mathrm{y},\mathrm{k}1}+R_{\mathrm{y},\mathrm{k}2}) \\ = -f(V_{\mathrm{c},\mathrm{k}1}) \\ f(V_{\mathrm{c},\mathrm{k}1}) = (V_{,\mathrm{k}1}-V_{\mathrm{c},\mathrm{k}1})/R_{\mathrm{z},\mathrm{k}1}. \end{cases} \tag{17}$$

The ③ node denotes a type of node that does not have a current source but includes a bond feet. The KVL equations for the ③ node are as follows:

$$\begin{cases} \left(V_{,(\mathrm{M}-1)1}-V_{,(\mathrm{M}-2)1}\right)/\left(R_{\mathrm{x},(\mathrm{M}-2)1}+R_{\mathrm{x},(\mathrm{M}-1)1}\right) \\ +\left(V_{,(\mathrm{M}-1)1}-V_{,\mathrm{M}1}\right)/\left(R_{\mathrm{x},(\mathrm{M}-1)1}+R_{\mathrm{x},\mathrm{M}1}\right) \\ +\left(V_{,(\mathrm{M}-1)1}-V_{,(\mathrm{M}-1)2}\right)/\left(R_{\mathrm{y},(\mathrm{M}-1)1}+R_{\mathrm{y},(\mathrm{M}-1)2}\right) \\ +\left(V_{,(\mathrm{M}-1)1}-V_{,21}\right)/R_{\mathrm{wire},1} \\ = -f(V_{\mathrm{c},(\mathrm{M}-1)1}) \\ f(V_{\mathrm{c},(\mathrm{M}-1)1}) = \left(V_{,(\mathrm{M}-1)1}-V_{\mathrm{c},(\mathrm{M}-1)1}\right)/R_{\mathrm{z},(\mathrm{M}-1)1}. \end{cases} \tag{18}$$

It is necessary to write KVL equations for each of the M × N cells to establish a square system of equation system, solving this set of equations will enable the determination of the potential values $V_{,\mathrm{kl}}$ for each metallization cell and the potential values $v_{,\mathrm{i(i+1)}}$ for each layer in every chip cell.

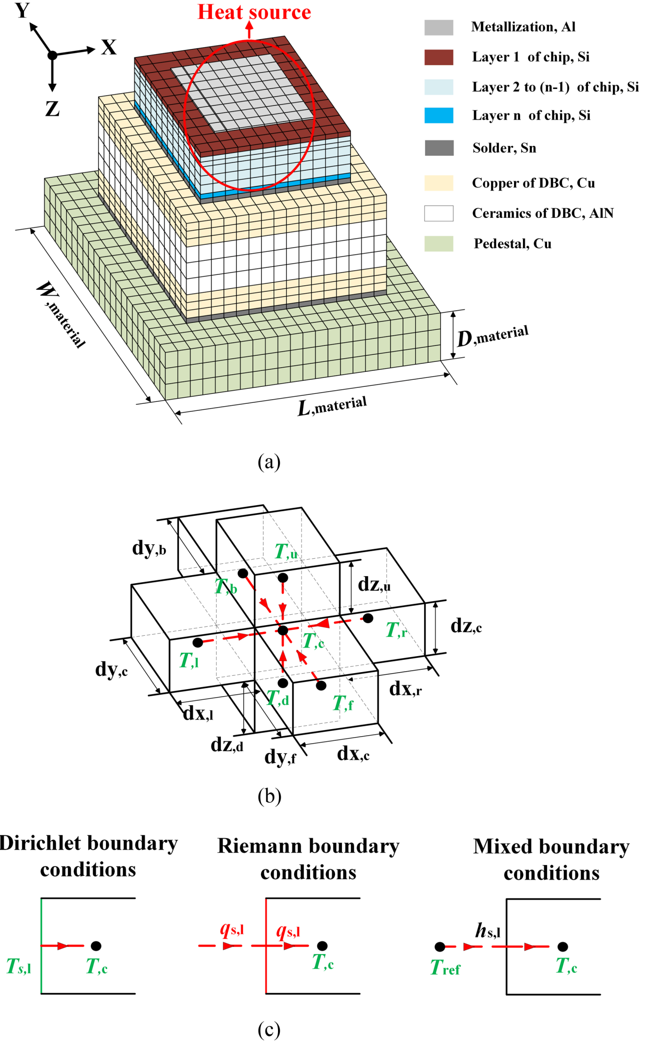

Fig. 8. Thermal model of packaging structure. (a) Encapsulation structure is cellular treated. (b) CVM Principles. (c) Three types of boundary conditions.

C. Thermal Model of Packaging Structure

The examination of Sections III-A and III-B indicates that the chip's active region has been separated into n+1 layers in the Z-direction, with the initial layer consisting of metallization and the subsequent n layers forming the chip cell structure based on the LC model. Additionally, the chip is divided into M × N units in the X-Y plane, resulting in a total of M × N × (n+1) small units, as depicted in Fig. 8(a). Following the earlier description, the potential and current passing through each small unit can be determined using a set of KVL equations that integrate the LC model. Therefore, the active region of the chip will act as an Ohmic heat source for heat conduction within the entire packaging structure.

Considering the chip model has been segmented, we extend the cell-based treatment to the chip terminals and the entire packaging structure (encompassing the solder layer, DBC, and substrate), as illustrated in Fig. 8(a). The entire packaging structure is transformed into a composite of multiple cuboids. In this context, employing the control volume method (CVM) to

establish the thermal model of the entire structure is the most suitable approach, offering a clearer depiction of heat conduction across the structure with significant physical implications. The subsequent section will detail the specific implementation of the CVM.

As depicted in Fig. 8(b), a unit is extracted from the complete thermal model to serve as the central unit, with the temperature $T_{,\mathrm{c}}$ at the center point representing the temperature of the entire unit. The temperatures at the center points of the six neighboring units are designated as $T_{,\mathrm{l}}$, $T_{,\mathrm{r}}$, $T_{,\mathrm{f}}$, $T_{,\mathrm{b}}$, $T_{,\mathrm{u}}$, and $T_{,\mathrm{d}}$, indicating the temperatures of each respective unit. $\mathrm{dx}_{,\mathrm{c}}$, $\mathrm{dx}_{,\mathrm{l}}$, and $\mathrm{dx}_{,\mathrm{r}}$ are the lengths of the central unit and its adjacent units in the *X*-direction, $\mathrm{dy}_{,\mathrm{c}}$, $\mathrm{dy}_{,\mathrm{f}}$, and $\mathrm{dy}_{,\mathrm{b}}$ are the lengths of the central unit and its adjacent units in the *Y*-direction, and $\mathrm{dz}_{,\mathrm{c}}$ and $\mathrm{dz}_{,\mathrm{u}}$, $\mathrm{dz}_{,\mathrm{d}}$ d are the lengths of the central unit and its adjacent units in the *Z*-direction. According to Fourier's heat transfer law, the control equation for the central unit can be written as follows:

$$
\begin{aligned}
&\left(\rho_{\mathrm{c}}^{1} c_{\mathrm{c}}^{1} T_{\mathrm{c}}^{1} - \rho_{\mathrm{c}}^{0} c_{\mathrm{c}}^{0} T_{\mathrm{c}}^{0}\right) \mathrm{dx}_{,\mathrm{c}}\mathrm{dy}_{,\mathrm{c}}\mathrm{dz}_{,\mathrm{c}} \\
&= \left[\left(k_{\mathrm{el}} \frac{\partial T}{\partial x}\right)_{\mathrm{l}}^{0-1} + \left(k_{\mathrm{er}} \frac{\partial T}{\partial x}\right)_{\mathrm{r}}^{0-1}\right] \mathrm{dy}_{,\mathrm{c}}\mathrm{dz}_{,\mathrm{c}}\mathrm{d}t \\
&+ \left[\left(k_{\mathrm{ef}} \frac{\partial T}{\partial y}\right)_{\mathrm{f}}^{0-1} + \left(k_{\mathrm{eb}} \frac{\partial T}{\partial y}\right)_{\mathrm{b}}^{0-1}\right] \mathrm{dx}_{,\mathrm{c}}\mathrm{dz}_{,\mathrm{c}}\mathrm{d}t \\
&+ \left[\left(k_{\mathrm{eu}} \frac{\partial T}{\partial z}\right)_{\mathrm{u}}^{0-1} + \left(k_{\mathrm{ed}} \frac{\partial T}{\partial z}\right)_{\mathrm{d}}^{0-1}\right] \mathrm{dx}_{,\mathrm{c}}\mathrm{dy}_{,\mathrm{c}}\mathrm{d}t \\
&+ s_{\mathrm{c}}^{0-1} \mathrm{dx}_{,\mathrm{c}}\mathrm{dy}_{,\mathrm{c}}\mathrm{dz}_{,\mathrm{c}}\mathrm{d}t
\end{aligned}
\tag{19}
$$

where the superscript 0 signifies the variable value at the present time, and the superscript 1 indicates the variable value after undergoing a time increment of d*t* at the current time step. The left-hand side of the equation illustrates the heat stored in the center unit during the time period d*t*, where ρ_{c} stands for the density of the material in the center unit, and c_{c} denotes the specific heat of the material in the center unit. The terms on the right-hand side of the equation correspond to the heat transfer into the center unit from the left, right, front, back, top, and bottom faces within the time increment dt. k_{el}, k_{er}, k_{ef}, k_{eb}, k_{eu}, and k_{ed} denote the effective thermal conductivity of the center unit at these boundary interfaces. The final term on the right captures the heat produced within the center unit over d*t* by internal heat sources, where s_{c} represents the power density in the center unit during this time period.

The time implicit format of the CVM is utilized in this article, with special attention given to the process of heat flux density transfer at the boundary interface. The discretization of the first six terms on the right-hand side of (19) is as follows:

$$
\begin{cases}
\left(k_{\mathrm{el}} \frac{\partial T}{\partial x}\right)_{\mathrm{l}}^{0-1} = \frac{T_{,\mathrm{l}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dx}_{,\mathrm{l}}}{2k_{,\mathrm{l}}^{1}} + \frac{\mathrm{dx}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}} & \left(k_{\mathrm{er}} \frac{\partial T}{\partial x}\right)_{\mathrm{r}}^{0-1} = \frac{T_{,\mathrm{r}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dx}_{,\mathrm{r}}}{2k_{,\mathrm{r}}^{1}} + \frac{\mathrm{dx}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}} \\
\left(k_{\mathrm{ef}} \frac{\partial T}{\partial y}\right)_{\mathrm{f}}^{0-1} = \frac{T_{,\mathrm{f}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dy}_{,\mathrm{f}}}{2k_{,\mathrm{f}}^{1}} + \frac{\mathrm{dy}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}} & \left(k_{\mathrm{eb}} \frac{\partial T}{\partial y}\right)_{\mathrm{b}}^{0-1} = \frac{T_{,\mathrm{b}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dy}_{,\mathrm{b}}}{2k_{,\mathrm{b}}^{1}} + \frac{\mathrm{dy}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}} \\
\left(k_{\mathrm{eu}} \frac{\partial T}{\partial z}\right)_{\mathrm{u}}^{0-1} = \frac{T_{,\mathrm{u}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dz}_{,\mathrm{u}}}{2k_{,\mathrm{u}}^{1}} + \frac{\mathrm{dz}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}} & \left(k_{\mathrm{ed}} \frac{\partial T}{\partial z}\right)_{\mathrm{d}}^{0-1} = \frac{T_{,\mathrm{d}}^{1} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dz}_{,\mathrm{d}}}{2k_{,\mathrm{d}}^{1}} + \frac{\mathrm{dz}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}}
\end{cases}
\tag{20}
$$

where $k_{,\mathrm{l}}$, $k_{,\mathrm{r}}$, $k_{,\mathrm{f}}$, $k_{,\mathrm{b}}$, $k_{,\mathrm{u}}$, and $k_{,\mathrm{d}}$ are the material thermal conductivity of the six adjacent units of the central unit.

In the case where the central unit is positioned at the boundary, it is important to take into account the specific boundary conditions. Fig. 8(c) provides an illustration of how the control volume method addresses three different types of boundary conditions, using the left boundary interface as a reference point.

1) If the left boundary interface is set with Dirichlet boundary conditions, meaning that the temperature value $T_{\mathrm{s,l}}$ at the left boundary interface is known, the first equation in (19) will be revised to

$$
\left(k_{\mathrm{el}} \frac{\partial T}{\partial x}\right)_{\mathrm{l}}^{0-1} = \frac{T_{\mathrm{s,l}} - T_{,\mathrm{c}}^{1}}{\frac{\mathrm{dx}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}}. \tag{21}
$$

2) If the left boundary interface is set with Riemann boundary conditions, whereby the normal heat flux density $q_{\mathrm{s,l}}$ at the left boundary interface is specified, the first equation in (19) will be revised to

$$
\left(k_{\mathrm{el}} \frac{\partial T}{\partial x}\right)_{\mathrm{l}}^{0-1} = q_{\mathrm{s,l}}. \tag{22}
$$

3) If the left boundary interface is set with mixed boundary conditions, where the convective heat transfer coefficient $h_{\mathrm{s,l}}$ and the ambient temperature T_{ref} at the left boundary interface are provided, the first equation in (19) will be rephrased as

$$
\left(k_{\mathrm{el}} \frac{\partial T}{\partial x}\right)_{\mathrm{l}}^{0-1} = \frac{T_{\mathrm{ref}} - T_{,\mathrm{c}}^{1}}{\frac{1}{h_{\mathrm{s,l}}} + \frac{\mathrm{dx}_{,\mathrm{c}}}{2k_{,\mathrm{c}}^{1}}}. \tag{23}
$$

Given that the thermal model of the packaging structure needs to be synchronized with the models introduced in Section III-A and III-B, the internal heat source s_{c} in (18) will be adjusted to reflect the present time Ohmic power density, adding a more practical physical interpretation to the model.

For each individual unit partitioned in Fig. 8(a), the control equations, as shown in (18), are listed to obtain a square system of equation system. The solution of this system will provide the temperature values of each unit at the next time step after d*t*.

D. Fully Coupled Electro-Thermal Model

Thus far, the three critical issues identified in Section-II have been resolved. The next step entails coupling the three submodels to create a holistic electrothermal model, as depicted in Fig. 9. Electro-thermal coupling operates in two directions: 1) electrical-to-thermal and 2) thermal-to-electrical coupling. In addition, there is self-coupling between electrical and thermal aspects. The following sections will individually address these four coupling approaches.

1) In the electrical-to-thermal coupling process, excitation coupling is the only presence due to the fact that all physical quantities in the thermal model, such as thermal conductivity, specific heat, and density, are unaffected by the electric field at the macro scale. Therefore, the product of the chip's voltage and current will be used as the thermal power coupling in the internal heat source of the thermal

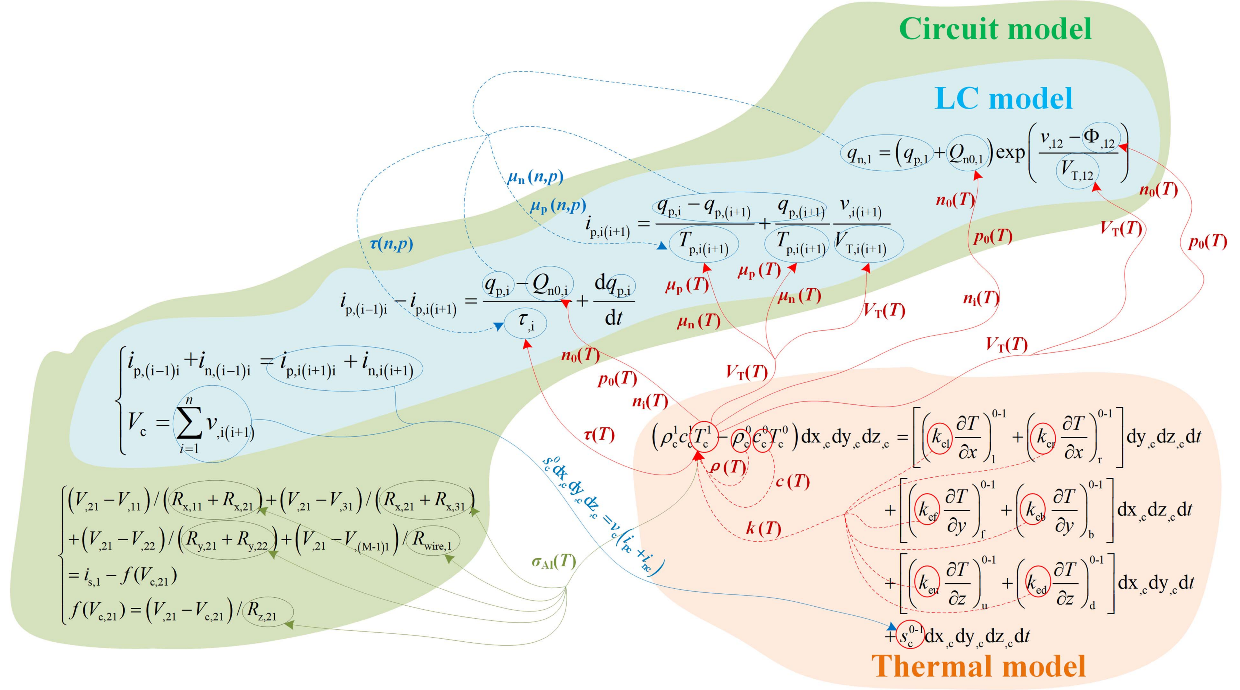

Fig. 9. Coupling relationship between variables.

model

$$s_{\mathrm{c}}^{0}\mathrm{dx}_{,\mathrm{c}}\mathrm{dy}_{,\mathrm{c}}\mathrm{dz}_{,\mathrm{c}} = v_{\mathrm{c}}\left(i_{\mathrm{pc}} + i_{\mathrm{nc}}\right) \tag{24}$$

Where v_{c}, i_{pc}, and i_{nc} represent the voltage drop, hole current, and electron current of the central unit mentioned in Section III-C, respectively.

2) In the thermal-to-electrical coupling process, it is necessary to account for the temperature dependence of most physical quantities in the circuit model. In the LC model of the chip, the transit times T_{p} and T_{n} for holes and electrons exhibit temperature dependence as they are related to the mobility of holes and electrons (μ_{p} and μ_{n}) and the thermoelectric voltage V_{T}, all of which are highly temperature-sensitive functions

$$\mu = \mu_{\infty} + \frac{\mu_0 - \mu_{\infty}}{1 + (N/N_{\mathrm{ref}})^{\gamma}}. \tag{25}$$

For hole [13]

$$\begin{cases} \mu_0 = 469\left(\frac{300}{T}\right)^{2.10}\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s}) \quad \mu_{\infty} = 44\left(\frac{300}{T}\right)^{0.8}\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s}) \\ N_{\mathrm{ref}} = 2.4\times 10^{17}\left(\frac{T}{300}\right)^{4.13}/\mathrm{cm}^3 \qquad \gamma = 0.7. \end{cases} \tag{26}$$

For electron [13]

$$\begin{cases} \mu_0 = 1412\left(\frac{300}{T}\right)^{2.28}\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s}) \quad \mu_{\infty} = 66\left(\frac{300}{T}\right)^{0.9}\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s}) \\ N_{\mathrm{ref}} = 9.7\times 10^{16}\left(\frac{T}{300}\right)^{3.51}/\mathrm{cm}^3 \qquad \gamma = 0.725\left(\frac{300}{T}\right)^{0.27} \end{cases} \tag{27}$$

where N represents the concentration of impurity ions, which can be approximated by the carrier concentration under high injection conditions [13]. For V_{T}

$$V_{\mathrm{T}} = \frac{k_0 T}{q} \tag{28}$$

where k_0 is the Boltzmann constant.

Additionally, $Q_{\mathrm{p}0}$ and $Q_{\mathrm{n}0}$ exhibit temperature dependence as they are linked to the thermal equilibrium concentrations of majority carriers n_0 and minority carriers p_0, both affected by intrinsic excitations at different temperatures. In surge conditions, the chip operates at elevated temperatures, intensifying the impact of intrinsic excitations. Silber and Robertson [18] noted that as a Si chip nears failure, the intrinsic excitation level n_{i} can reach 1/3 of the background doping concentration. Therefore, the correlation between n_0, p_0, and temperature must be addressed. Following the principle of charge neutrality [19]:

$$\begin{cases} n_0 = \frac{N_{\mathrm{B}}}{2} + \sqrt{\left(\frac{N_{\mathrm{B}}}{2}\right)^2 + n_{\mathrm{i}}^2} \\ p_0 = -\frac{N_{\mathrm{B}}}{2} + \sqrt{\left(\frac{N_{\mathrm{B}}}{2}\right)^2 + n_{\mathrm{i}}^2} \end{cases} \tag{29}$$

where N_{B} is the low doping concentration in the drift region, n_{i} is the intrinsic carrier concentration, which is strongly temperature dependent [20]

$$n_{\mathrm{i}} = 4.82\times 10^{15}\left(\frac{m_p^* m_n^*}{m_0^2}\right)^{3/4} T^{3/2}\exp\left(-\frac{E_{\mathrm{g}}}{2k_0 T}\right) \tag{30}$$

where m^*_{p} and m^*_{n} are the effective masses of hole and electron, respectively, m_0 is the electron mass, and E_{g} is the bandgap width

of the chip material. For Si

$$\begin{cases} m_p^* = 0.59m_0 \quad m_{\rm n}^* = 1.062m_0 \\ E_{\rm g}(T) = E_{\rm g}(0) - \frac{}{\alpha T^2}T + \beta \\ E_{\rm g}(0) = 1.21{\rm eV}\alpha = 4.73 \times 10^{-4}{\rm eV}/K\beta = 636{\rm K}. \end{cases} \quad (31)$$

Furthermore, the temperature dependency of the built-in potentials $\Phi_{,12}$ in the p-n junction should also be taken into consideration. This is because they are associated with the thermal equilibrium carrier concentrations p_0, the thermal voltage $V_{\rm T}$ and the heavy doping concentrations in the $\rm P^+$ region $N_{\rm a}$

$$\Phi_{,12} = V_{\rm T} \ln\left(\frac{N_a}{p_0}\right). \quad (32)$$

Similarly for $\Phi_{,({\rm n}\text{-}1){\rm n}}$, which is associated with the thermal equilibrium carrier concentrations n_0, the thermal voltage $V_{\rm T}$, and the heavy doping concentrations in the $\rm N^+$ region $N_{\rm d}$.

Finally, there is a notable temperature dependency for the carrier lifetime τ, especially in surge conditions where the chip is heavily injected, leading to significant self-heating. In such instances, Auger recombination will take precedence [13], [21]

$$\tau = \frac{1}{(c_{A,n} + c_{A,p})\,p^2} \cdot \left(\frac{T}{300}\right)^{\alpha_A} \quad (33)$$

where

$$\begin{cases} c_{\rm A,n} = 2.8 \times 10^{-31}{\rm cm}^6/{\rm s} \\ c_{\rm A,p} = 1 \times 10^{-31}{\rm cm}^6/{\rm s} \end{cases} \quad (34)$$

$\alpha_{\rm A}$ is the temperature coefficient, which is related to the actual process.

In the cellized chip circuit model, the temperature dependence is only present in the conductivity of the metallization [22] (35) shown at the bottom of this page.

3) The self-coupling effect within the electrical model is primarily highlighted in the chip's LC model. As explained in [23], during surge conditions, the fluctuations in the chip's voltage drop are constricted by three interrelated factors at the semiconductor physics level. First, the mobility diminishes progressively with increased injection levels, resulting in an escalation of the voltage drop, as indicated in (25). In addition, the carrier lifetime decreases with rising injection levels due to Auger recombination, causing an increase in voltage drop, as illustrated in (33). Finally, the elevation in injection levels and intrinsic excitations results in a significant presence of electrons and holes in the drift region, the conductivity modulation effect of the p-i-n diode effectively reduces the chip's voltage drop, as depicted in (30).
4) The self-coupling within the thermal model necessitates the consideration of the temperature-dependent thermal conductivity k, specific heat c, and density ρ for all materials. For example, in the case of Si material, these properties are temperature-dependent [24], [25], [26]

$$\begin{cases} k_{\rm Si} = 810.913 - 4.714T + 0.013T^2 - 1.698 \times 10^{-5}T^3 \\ \qquad + 1.153 \times 10^{-8}T^4 - 3.094 \times 10^{-12}T^5 {\rm W}/({\rm m}\cdot{\rm K}) \\ c_{\rm Si} = 63.044 + 3.771T - 0.007T^2 + 5.953 \times 10^{-6}T^3 \\ \qquad - 1.914 \times 10^{-9}T^4 {\rm J}/({\rm kg}\cdot{\rm K}) \\ \rho_{\rm Si} = 2332.565 + 0.004T - 5.433 \times 10^{-5}T^2 \\ \qquad + 2.487 \times 10^{-8}T^3 - 1.367 \times 10^{-11}T^4 {\rm kg/m^3}. \end{cases} \quad (36)$$

Further materials can be consulted in [27], [28], [29], and [30], detailed listings are omitted here.

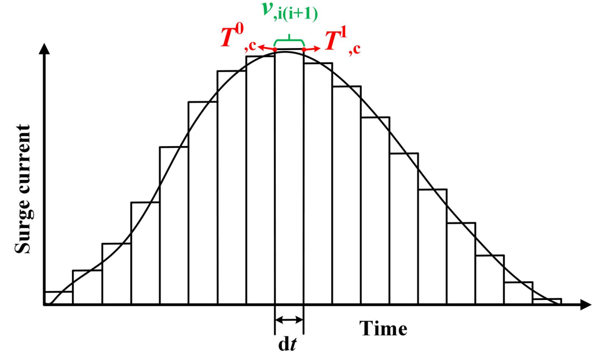

Fig. 10. Quasi static assumption for surge conditions: surge current is divided in steps of dt.

E. Calculation Process

Before delving into the specifics of the computation process, a necessary assumption is made: surge conditions are deemed as quasi-static conditions, as shown in Fig. 10.

In practice, the quasi-static assumption is reasonable as, under long-lasting current pulses, the chip's drift region operates in a condition of substantial carrier injection. The instantaneous completion of carrier concentration changes enables the exclusion of the time derivative term in (9) of the LC model. Under the quasi-static assumption, the entire duration of the surge current is divided into intervals of dt, as shown in Fig. 10. Within each dt intervals, the chip is assumed to start with an initial temperature value and the corresponding initial carrier distribution, which remains unchanged until the end of the interval. Throughout this interval, the chip's active region functions as a sustained heat source, resulting in continuous heat generation. Consequently, at the conclusion of each time step, the overall packaging structure presents a temperature $T^1{}_{,\rm c}$ that deviates from the initial value $T^0{}_{,\rm c}$. This concluding temperature at the end of the step is designated as the initial temperature for the subsequent time step, triggering a new carrier distribution within the chip in the next step. This cyclical pattern continues until the computation

$$\sigma_{\rm Al} = \frac{1}{6.619 \times 10^{-17}T^3 - 8.192 \times 10^{-14}T^2 + 1.451 \times 10^{-10}T - 1.037 \times 10^{-8}} S/{\rm m}. \quad (35)$$

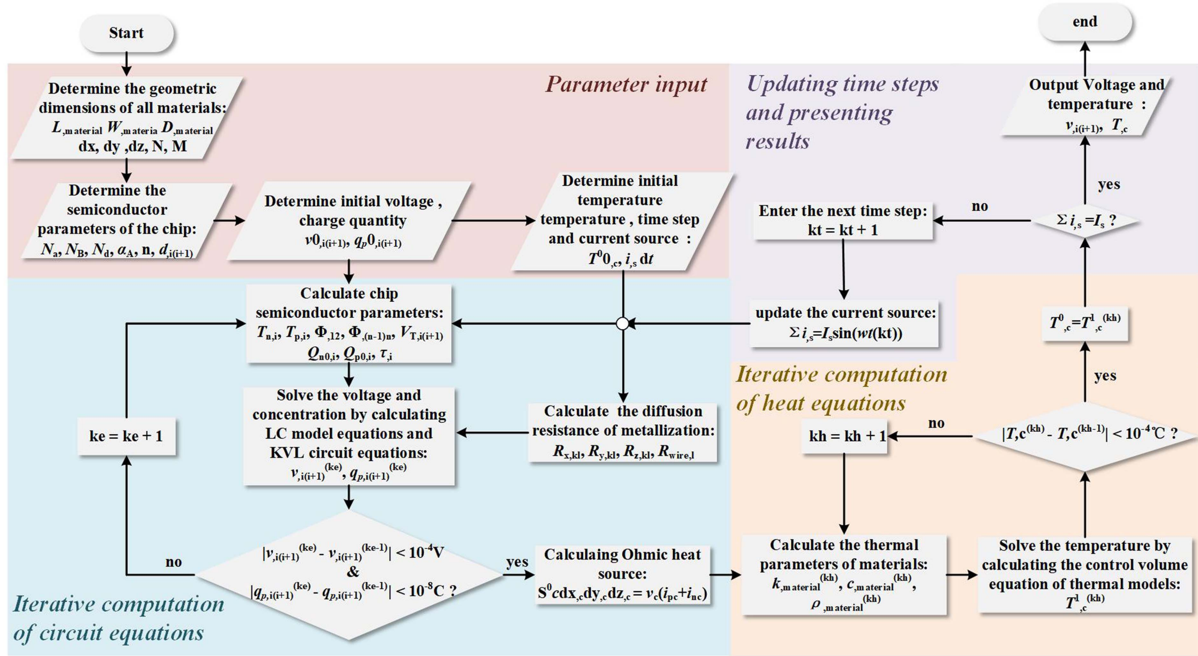

Fig. 11. Calculation process.

of all time steps is finalized. When the time steps are subdivided small enough which can also meet the criteria of disregarding the transient carrier distribution time, it is feasible to consider that these quasi-static conditions as equivalent to the real surge conditions.

The calculation process of the electro-thermal fully coupled surge model is delineated in Fig. 11, and it is divided into four segments: parameter input, iterative computation of circuit equations, iterative computation of heat equations, updating time steps, and presenting results.

1) The initial step involves establishing the dimensions of the cells to be divided, the quantity of cells, and other parameters of the model based on the overall external packaging structure and the internal chip structure, as well as the semiconductor parameters like doping concentration within the chip. Next, assign initial values for the variables to be solved for each cell, including voltage, normalized charge, and temperature for the active region of the chip, while the remaining areas only involve temperature variables. Finally, input the initial time step and initial current sources.
2) Incorporate the initial values of the variables to be solved for the active region cells of the chip at this time step into the LC model. Start by evaluating the base transit time, thermoelectric voltage, thermal equilibrium carrier charge, drift region lifetime, and built-in potential of the p-i-n diode junction position for each cell. Additionally, determine the diffusive resistance of metallization, subsequent to that, proceed to solve the potential values for each cell iteratively by incorporating those variables into KVL circuit equations containing the LC model. Evaluate if the convergence criteria are met. Achieving convergence signifies the completion of solving the potential distribution of chip for the current time step. Consequently, continue with calculating the heat dissipation in the chip's active region for this time step, followed by entering 3). If the convergence criteria are not achieved, update the voltage and charge values, and iterate this step until the convergence condition is satisfied.
3) Calculate the thermal conductivity, specific heat capacity, and density values of each cell corresponding to the initial temperature at the start of this time step. Incorporate the heat dissipation in the chip's active region obtained in 2) as an internal heat source in the thermal model for computing the temperature values of each cell at the conclusion of this time step. If the convergence criteria are satisfied, utilize the temperature at the completion of this time step as the initial temperature for the following time step, then proceed to step 4; if the convergence criteria are not met, update the temperature values and repeat this process until the convergence criteria are met.
4) Check whether this time step is the final one. If affirmative, finalize the entire calculation process and present the voltage and temperature calculation results for each time step. If not, proceed to the next time step, update the current source, and revisit step 2 for the next iteration.

IV. Experimental Verification and Analysis

A. Actual Example Configuration for Modeling

The corresponding electro-thermal coupled model for the high-voltage, high-power silicon p-i-n diode illustrated in Fig. 6 is developed in this article, as depicted in Fig. 12. The geometric parameters of the entire structure are derived from scanning

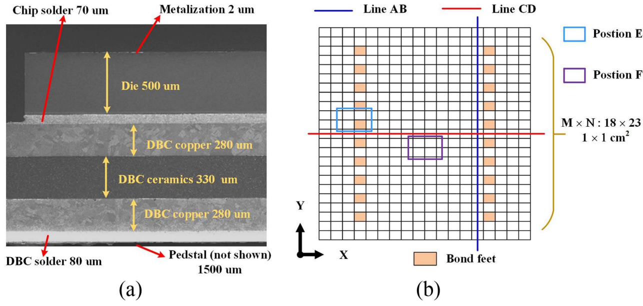

Fig. 12. Corresponding electro-thermal coupled model of DUT. (a) Geometry of the cross-section of the DUT from SEM. (b) Cellular processing in the active region of the chip.

TABLE I
SOME OF THE CONFIGURATION PARAMETERS FOR MODELING

Parameters	Value	Parameters	Value
N_B	1e15 (cm^{-3})	$L_{,\mathrm{chip\ solder}}$	14.4 (mm)
n	7	$L_{,\mathrm{DBC\ copper}}$	18.8 (mm)
Total area of chip	1.96 (cm^2)	$L_{,\mathrm{DBC\ ceramics}}$	18.8 (mm)
$d_{,12}$	10 (μm)	$L_{,\mathrm{DBC\ solder}}$	18.8 (mm)
$d_{,23}$	64.4 (μm)	$L_{,\mathrm{pedestal}}$	23.3 (mm)
$d_{,34}$	119.6 (μm)	$W_{,\mathrm{chip\ solder}}$	14.3 (mm)
$d_{,45}$	119.6 (μm)	$W_{,\mathrm{DBC\ copper}}$	18.7 (mm)
$d_{,56}$	119.6 (μm)	$W_{,\mathrm{DBC\ ceramics}}$	18.7 (mm)
$d_{,67}$	36.8 (μm)	$W_{,\mathrm{DBC\ solder}}$	18.7 (mm)
$d_{,78}$	30 (μm)	$W_{,\mathrm{pedestal}}$	23 (mm)

electron microscope (SEM) results, with the active area of the chip measuring 1 cm^2. For modeling purposes, the active area of the chip is divided into 18×23 cells on the X-Y plane and segmented into 8 layers along the Z-axis (with 1 layer designated for metallization). The model encompasses a total of 31 754 units, striking a balance between computational accuracy and efficiency. Table I presents some of the parameter configurations necessary for modeling. Moreover, to align with actual testing scenarios, the thermal model assigns the bottom surface of the substrate as a Dirichlet boundary, with a constant known temperature set as the reference temperature T_{ref}; the other surfaces are defined by mixed boundary conditions with known convective heat transfer coefficients $h_{s,1}$. The entire modeling and computational process was exclusively completed through programming, without resorting to any commercial simulation software.

B. Modeling and Experimental Verification of Static Forward I-V Characteristics

Understanding the static forward I-V characteristics of the power diode is crucial as a prerequisite for our subsequent exploration of surge characteristics. We conducted measurements of the static forward I-V characteristic curves of the DUT at different temperatures using a commercial static parameter tester, with the DUT placed in a thermostatic chamber to maintain a constant temperature. Additionally, we conducted corresponding modeling and calculations. Fig. 13 presents the comparison between the experimental results and the calculations from the LC model. It is apparent that the computational results based on the model developed in this article closely align with the experimental results, providing validation for the accuracy of the LC model.

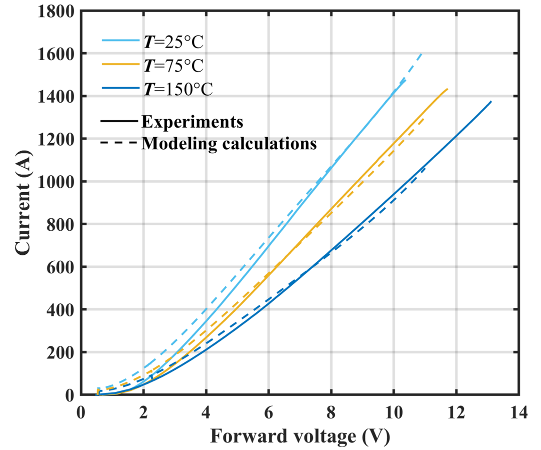

Fig. 13. Static forward I-V characteristics of DUT under different temperature.

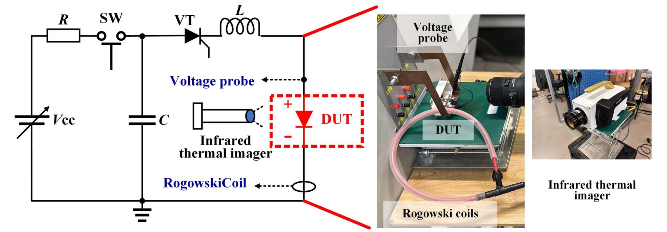

Fig. 14. Surge experiment platform.

From Fig. 13, it is apparent that the overall forward voltage drop of the chip displays a positive temperature coefficient (PTC). This characteristic is contingent upon the chip's design specifications, with different manufacturing processes resulting in varying temperature coefficients. PTC makes the chip suitable for parallel connection. However, it diminishes the chip's ability to withstand surge currents, as higher temperatures lead to larger voltage drops and subsequently increased heat dissipation for the same current flow.

C. Modeling and Experimental Verification of Surge Characteristics

A surge test platform is set up following the JEDEC industrial standard [14] and shown in Fig. 14. A sinusoidal half-wave current lasting up to 10 ms can be generated using the LC resonance method. The capacitor is charged first by the controllable voltage source when thyristors are turn OFF and relay is connected. After receiving the trigger signal, the thyristor is turned ON and surge current are flow through the DUT, meanwhile, the relay of charging circuit is disconnected. The DUT's current is measured by commercial Rogowski coil CWT UM 30B (30 MHz, −3 dB), and the DUT's voltage is measured by the high-voltage probe LeCroy PP026 (500 MHz, −3 dB). We consider the voltage that measured by probe is the forward voltage of chip.

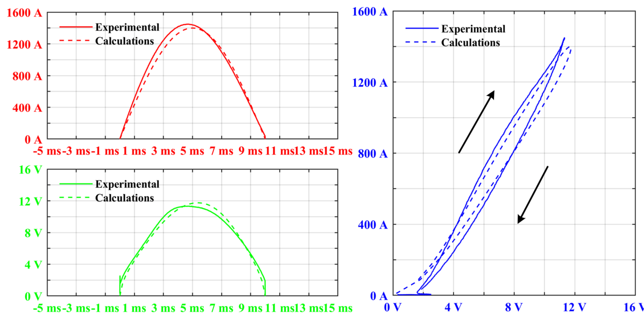

Fig. 15. Current and voltage versus time during the 10 ms surge current, as well as the corresponding I-V trajectory.

To determine the true real value of the temperature in the active region of the chip at surge conditions, infrared thermography is used to capture the temperature distribution in the active region of the chip, as shown in Fig. 14. The infrared thermal imager is Telops FAST M200 whose frame rate is set as 1300 Hz and integration time is at microsecond level. The measurement accuracy will still be maintained at ±1%. It should be pointed out that spraying black paint will affect the shooting result, so the emissivity of camera is set as 0.1 [6] according to the equipment manual instead of spraying black paint. By utilizing the synchronous triggering function of the infrared thermal imager, we can precisely match the captured moments with the surge period.

The DUT was exposed to a 10 ms half-sine wave surge current with a peak of 1400 A, representing 14 times the rated current. Despite the severe self-heating that occurs at this current level, the chip remains in a healthy state. Fig. 15 showcases the waveforms of the chip's current and voltage throughout the entire surge period obtained from the experiment, as well as the corresponding I-V trajectory. The waveforms obtained from the modeling calculations are also depicted. It is clear that the simulation results closely align with the experimental results. The I-V trajectory presents a clockwise loop, attributed to the PTC of the chip's voltage. Specifically, at high temperatures, although the resistivity of the drift region is greatly reduced by the intrinsic excitation and conductivity modulation effects, the impact mechanisms of carrier mobility and Auger recombination negate this effect, ensuring that the chip retains a PTC. A more detailed discussion is beyond the scope of this article.

Figs. 16 and 17 provide a comparison between the temperature distribution results obtained from IR measurements and modeling calculations. Specifically, Fig. 16(a) and (b) displays the results at 6 ms, while Fig. 16(c) and (d) showcase the results at 9 ms. To enhance clarity, lines AB and CD were selected on the chip surface to record the temperature distribution at 6 ms and 9 ms, as depicted in Fig. 12(b) and plotted in Fig. 16(e) and (f). Additionally, Fig. 17(a) depicts the temporal variations of the average temperatures at positions E and F on the chip surface, as illustrated in Figs. 12(b) and 17(b), tracks the highest temperature of the chip metallization and the variation in the overall chip average temperature over time. The experimental results indicate that the modeled calculated results are slightly

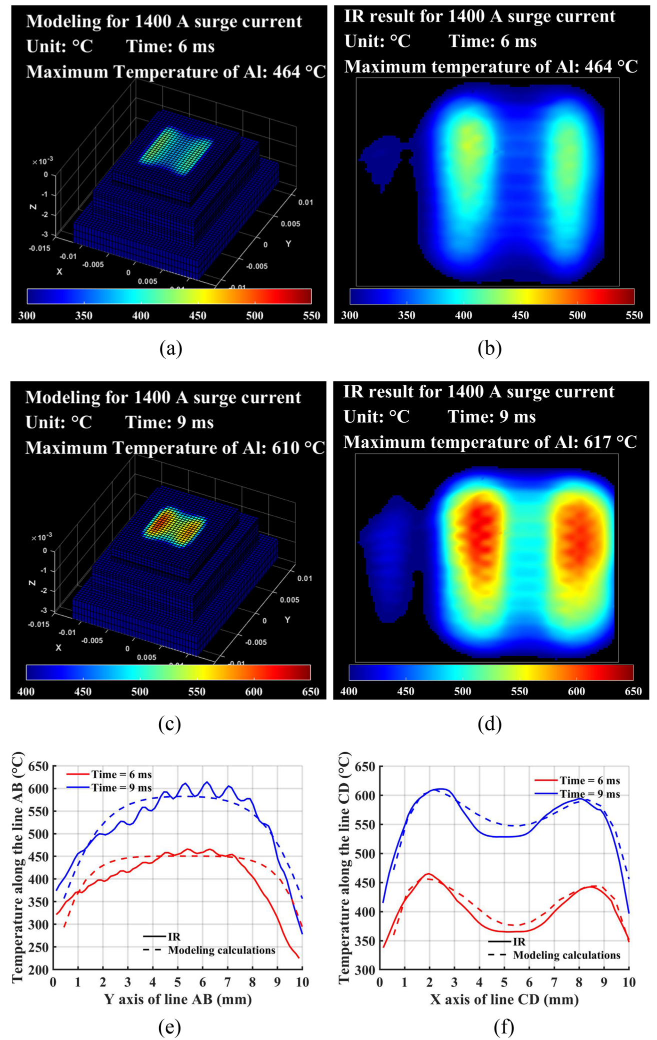

Fig. 16. Comparison of IR and modeling calculation. (a), (b). Temperature distribution at 6 ms and 9 ms by calculation, respectively. (c), (d) Temperature distribution of chip at 6 ms and 9 ms of IR, respectively. (e), (f). Temperature along the lines AB and CD of Fig. 12, respectively.

higher than the IR measurement results, particularly at the central position of the chip. Nevertheless, the values are within an acceptable range, providing sufficient evidence for the validity of the computational results.

The experimental results align with the calculated results, indicating that the temperature of the metallization reaches its peak at 9 ms when a surge current of 1400 A passes through. At this time, the temperature exceeds 600 °C, which is near the melting point of Al, suggesting imminent chip failure. However, the overall average temperature of the chip is below 350 °C, significantly lower than the maximum temperature (450 °C–550 °C) of Si chips under surge conditions as recorded in reference [18]. This suggests that utilizing the TSEPs mentioned in [11] and [27] to monitor the surge temperature of Si diodes may not reliably indicate whether the chip is approaching its failure limit, as the temperature measurements obtained from TSEPs typically reflect the average temperature of the chip. Subsequent experiments showed that when the surge current was elevated to

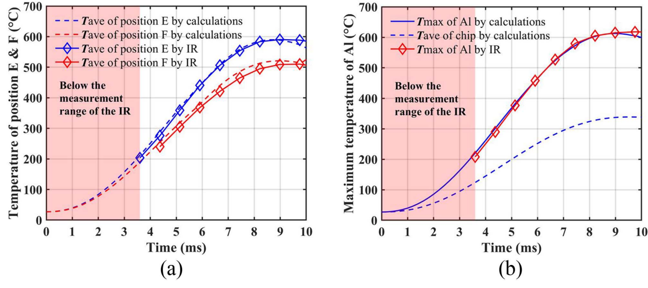

Fig. 17. Variation of temperature over time. (a) Average temperature of position E and F. (b) Highest temperature of the chip metallization and the overall chip average temperature over time.

1500 A, the DUT underwent thermal breakdown failure, further confirming that the 1400 A surge current is the limit for this DUT, with the temperature of the metallization nearing the melting point of Al serving as supporting proof. Moreover, influenced by current localization, the chip shows considerable temperature unevenness during surges, with temperatures around the bond feet area being higher than those further away, resulting in a temperature difference of 80 °C at 9 ms. This could cause the metallization around the bond feet to reach its melting point first, leading to thermal breakdown of the chip. This also clarifies the formation of the surge failure morphology described in Fig. 4(b), where melted regions tend to consistently appear around the bond feet.

Fig. 18 compares the calculated results between the proposed model and the traditional model, encompassing the temperature and current distribution at 6 ms, the losses over the entire 10 ms surge period, and the temporal evolution of the chip temperature. This comparison will serve to demonstrate the nonuniformity of the chip's electrothermal behavior during the surge conditions.

According to Fig. 18(a), the temperature results derived from the traditional model are misleading, as the high-temperature region of the chip is concentrated in the middle, which is far from the bond feet area. This contradicts the actual experimental findings such as Fig. 4(b). The discrepancy arises due to the conventional model's inability to account for the current localization of the chip under surge conditions, as illustrated in Fig. 18(c). As a result, a uniform current distribution is observed, with each cell carrying an average current of approximately 3.2 A, leading to a distribution trend of low losses in the middle and high losses around the periphery of the chip, with minimal overall numerical differences, not exceeding 0.133 W, as illustrated in Fig. 18(e). In contrast, the calculated results of the proposed model, as shown in Fig. 18(d), effectively depict the current localization. The current displays a "double-peak" distribution, with the highest cell current density exceeding 4 A around the bond feet area, while the region in the middle of the chip, far from the bond feet area, is below 2.5 A. The total losses shown in Fig. 18(f) also display a "double-peak" distribution, with the highest cell losses around the bond feet area exceeding 0.28 W, while the region in the middle of the chip, far from the bond feet area, is below 0.13 W. With the electro-thermal coupling effect,

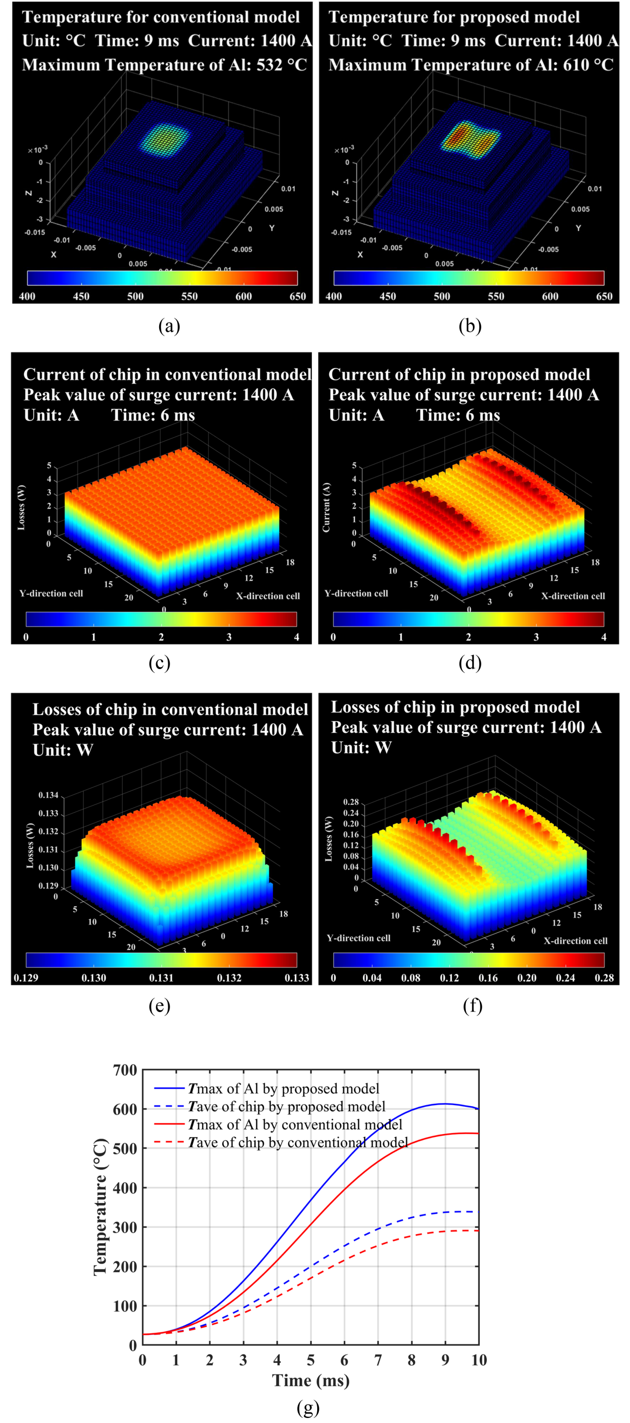

Fig. 18. Comparison of conventional and proposed model. (a), (b) Temperature distribution at 9 ms. (c), (d) Current distribution of chip at 6 ms. (e), (f) Losses distribution of chip. (g) Variation of maximum and average temperature over time.

the nonuniformity of the chip's electro-thermal distribution will worsen. According to Fig. 18(g), during the 8–9 ms period, the temperature calculation results of the traditional model are 70 °C–90 °C lower than those of the proposed model. It is worth noting that when utilizing a time step of 50 μs for fixed-step calculation, the proposed model requires 408 s to solve the 10 ms

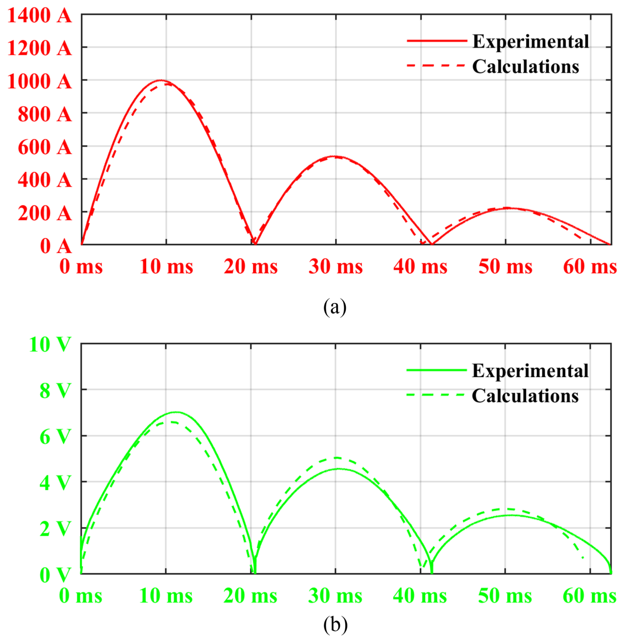

Fig. 19. Current and voltage versus time during the three-pulse surge condition. (a) Current waveform. (b) Voltage waveform.

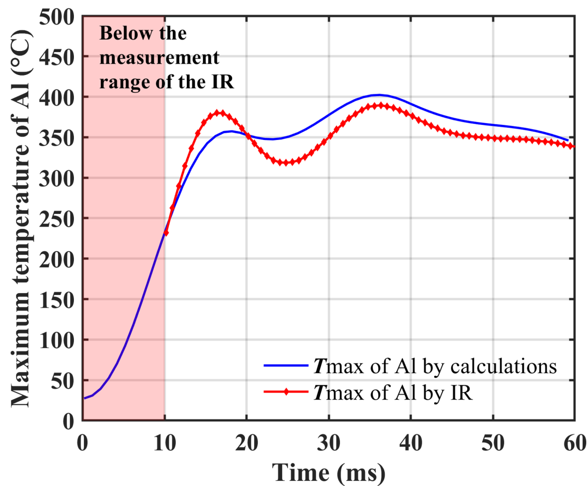

Fig. 20. Highest temperature of the chip metallization over time during the three-pulse surge condition.

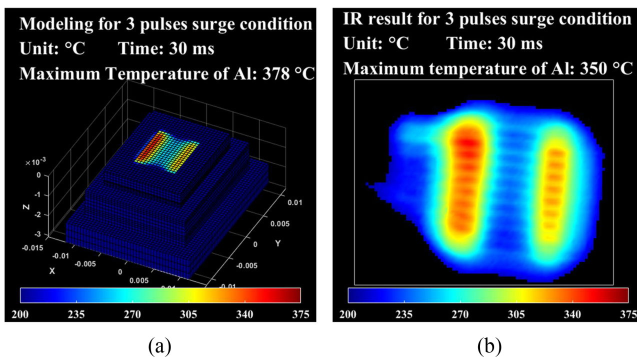

Fig. 21. Temperature distribution of chip at 30 ms during the three-pulse surge condition. (a) Modeling calculation. (b) IR.

surge condition. This represents a substantial improvement in calculation speed compared to commercial FEM software.

D. Universality of Model

We utilized the proposed model to examine its universality under another surge condition, specifically the continuous three-pulse surge condition. This is a unique condition that occurs exclusively in power systems, and imposes more rigorous assessments on the surge withstand capability of devices. Fig. 19 displays the voltage-current waveforms obtained from experimental measurements and model calculations. It can be seen that the two are generally consistent, but there are still some differences. During the first pulse, the voltage waveform obtained from the model calculations is slightly lower than the results from experimental measurements, while during the subsequent two pulse, it is higher than the experimental measurements. Consequently, the temperature calculation results will also show slight differences from the experimental results, while the overall trend remains consistent. As shown in Fig. 20, the temperature of the chip will demonstrate two peaks. The model calculation results are lower than the IR measurements during the first temperature peak, while they are slightly higher during the second temperature peak. The comparative results of the chip temperature distribution at 30 ms are shown in Fig. 21. It is apparent that the chip temperature distribution obtained from the model calculations remains consistent with the experiments, albeit with numerical differences, which are permissible.

V. Conclusion

Since the experimental measurement methods cannot be directly employed to monitor the temperature variations of high-power chips under surge conditions in practical engineering, it is crucial to establish an electro-thermal coupling model for the chips under surge conditions to calculate temperature distribution. However, the heat dissipation of the chip under surge conditions showcases three characteristics: 1) the uneven heating of the chip itself due to its semiconductor characteristics; 2) uneven chip electro-thermal distribution caused by the arrangement of bonding wires; 3) thermal conduction among diverse packaging materials. Therefore, this article establishes three submodels to address these three characteristics. First, an LC model is developed from semiconductor physics to describe the carrier transport process inside the chip. Second, the LC model is combined with the chip's cell model to create a circuit model that can effectively depict the current distribution issue caused by the arrangement of bond wires. Subsequently, a CVM model is constructed to describe the conduction process of heat within the packaging structure. Finally, by coupling the variables, the three submodels are integrated into a comprehensive electro-thermal coupling model, integrating the chip's physical characteristics with the 3-D packaging structure for the first time, enabling for the calculation of the chip's temperature distribution under surge conditions without resorting to destructive surge experiments. The accuracy of the constructed model was verified by conducting experiments on static forward I-V characteristics and surge

current. In addition to capturing voltage and current waveforms, we employed a high-precision refrigerated infrared thermal imager to monitor the chip's temperature variations during surge conditions. The experimental results exhibited a favorable agreement with the modeling calculations. It demonstrates that as the chip approaches its surge limit, the metallization temperature exceeds 600 °C and approaches its melting point, leading to a severe temperature distribution imbalance. Specifically, the temperature around the bond feet area is found to be 80 °C higher than that in regions farther away. Consequently, the metallization near the bond feet area is the first to melt, thereby causing the surge failure of Si p-i-n diodes.

References

[1] D. Kastha and B. K. Bose, "Investigation of fault modes of voltage-fed inverter system for induction motor drive," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting,* Houston, TX, USA, 1992, pp. 858–866.

[2] H. Sher, K. Addoweesh, and Y. Khan, "Effect of DC link capacitor failure on free wheeling diodes of inverter feeding an induction motor," in *Proc. Conf. Workshop Power Electron. Ind. Appl. Renewable Energy*, 2011, pp. 1–6.

[3] B. Heinze, J. Lutz, M. Neumeister, R. Rupp, and M. Holz, "Surge current ruggedness of silicon carbide schottky- and merged-PiN-schottky diodes," in *Proc. IEEE 20th Int. Symp. Power Semicond. Devices ICs*, 2008, pp. 245–248.

[4] X. Huang, G. Wang, M.-C. Lee, and A. Q. Huang, "Reliability of 4H-SiC SBD/JBS diodes under repetitive surge current stress," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, 2012, pp. 2245–2248.

[5] Y. Zhang, E. Deng, Z. Zhao, J. Chen, S. Fu, and X. Cui, "Experimental verification of the junction temperature distribution within press pack IGBTs," in *Proc. IEEE 32th Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 360–363.

[6] S. Liu, X. Tong, J. Wei, and W. Sun, "Single-pulse avalanche failure investigations of Si-SJ-MOSFET and SiC-MOSFET by step-control infrared thermography method," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5180–5189, May 2020.

[7] Y. Zhang et al., "Sequential $V_{\mathrm{ce}}(T)$ method for the accurate measurement of junction temperature distribution within press-pack IGBTs," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3735–3743, Apr. 2021.

[8] T. Hunger, O. Schilling, and F. Wolter, "Numerical and experimental study on surge current limitations of wire-bonded power diodes," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion*, 2007, pp. 1–6.

[9] B. Heinze, R. Baburske, J. Lutz, and H. J. Schulze, "Effects of metallisation and bondfeets in 3.3 kV free-wheeling diodes at surge current conditions," in *Proc. Conf. 9th Int. Seminar Power Semicond.*, 2008, pp. 1–6.

[10] F. Carastro, J. Mari, T. Zoels, B. Rowden, P. Losee, and L. Stevanovic, "Investigation on diode surge forward current ruggedness of Si and SiC power modules," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Karlsruhe, Germany, 2016, pp. 1–10.

[11] S. Palanisamy, G. V. Yoganath, G. Zeng, J. Lutz, J. Kowalsky, and T. Basler, "Temperature determination of SiC MPS diodes during surge current event with measurement and simulation," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, Genova, Italy, Sep. 2019, pp. 1–9.

[12] J. Wu, N. Ren, and K. Sheng, "Electrothermal coupling model with distributed heat sources for junction temperature calculation during Surges," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11887–11895, Oct. 2022.

[13] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices - Physics, Characteristics, Reliability*. Berlin, Germany: Springer, 2018.

[14] "Silicon rectifier diodes," 2002. Accessed: Jun. 5, 2020. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-282b01

[15] P. O. Lauritzen and C. L. Ma, "A simple diode model with reverse recovery," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 188–191, Apr. 1991.

[16] J. G. Linvill, "Lumped models of transistors and diodes," *Proc. IRE*, vol. 46, no. 6, pp. 1141–1152, 1958.

[17] F. Iannuzzo and G. Busatto, "Physical CAD model for high-voltage IGBTs based on lumped-charge approach," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 885–893, Jul. 2004.

[18] D. Silber and M. J. Robertson, "Thermal effects on the forward characteristics of silicon pin diodes at high pulse currents," *Solid-State Electron.*, vol. 16, no. 12, pp. 1337–1346, 1973.

[19] D. Neamen et al., *Semiconductor Physics and Devices: Basic Principles*, 4th ed. New York, NY, USA: McGraw-Hill, 2011.

[20] E. Liu, B. Zhu, and J. Luo, *The Physics of Semiconductors*. Beijing, China: Electronics Industry, 2017.

[21] *Advanced TCAD Manual*. Sunnyvale, CA, USA: Synopsys, 2007. [Online]. Available: http://www.synopsys.com

[22] P. D. Desai, H. M. James, and C. Y. Ho, "Electrical resistivity of aluminum and manganese," *J. Phys. Chem. Ref. Data*, vol. 13, no. 4, pp. 1131–1172, Oct. 1984.

[23] C. Y. Ho et al., "Thermal conductivity of the elements," *J. Phys. Chem. Ref. Data*, vol. 1, no. 2, pp. 279–421, 1992.

[24] P. D. Desai, "Thermodynamic properties of iron and silicon," *J. Phys. Chem. Ref. Data*, vol. 15, no. 3, pp. 967–983, Jul. 1986.

[25] C. A. Swenson, "Recommended values for the thermal expansivity of silicon from 0 to 1000 K," *J. Phys. Chem. Ref. Data*, vol. 12, no. 2, pp. 179–182, Apr. 1983.

[26] L. M. Hillkirk, B. Breitholtz, and J. Lutz, "Physical phenomena in Si power diodes operating at high carrier injection levels and high temperature," in *Proc. IEEE 12th Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 253–256.

[27] H. Touloukian, "Powell and klemens," *TPRC Data Series*, 1970. [Online]. Available: http://www.dtic.mil/dtic/tr/fulltext/u2/a951935.pdf

[28] A. M. Prokhorov et al., *Great Soviet Encyclopedia, (Moscow 1976) in English Translation*, 3rd ed. New York, NY, USA: Macmillan Inc., 1980.

[29] J. G. Hust and A. B. Lankford, "Thermal conductivity of aluminum, copper, iron, and tungsten for temperatures from 1 k to the melting point," National Bureau of Standards, Boulder, CO, USA, Tech. Rep. NBSIR 84-3007, 1984.

[30] Y. Takahashi, T. Azumi, and Y. Sekine, "Heat capacity of aluminum from 80 to 880K," *Thermichimica Acta*, vol. 139, pp. 133–137, May 1989.

[31] H. Meng, "Design, process and modeling investigation on silicon carbide MPS diodes," Ph.D. dissertation, Dept. Elect. Eng., North China Electrical Power Univ., Beijing, China, 2024.

Feilin Zheng was born in Shanxi Province, China, in 1998. He received the B.Sc. degree in electrical engineering from Taiyuan University of Technology, Taiyuan, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with North China Electric Power University, Beijing, China.

His main research interests include power electronics device and multiphysics field modeling.

Binqi Liang was born in Hebei Province, China, in 1998. She received the B.Sc. degree in electrical engineering from Taiyuan University of Technology, Taiyuan, China, in 2021. She is currently working toward the Ph.D. degree in electrical engineering with North China Electric Power University, Beijing, China.

Her main research interest includes SiC power electronics device reliability.

Xiang Cui (Senior Member, IEEE) was born in Baoding, China, in 1960. He received the B.Sc. and M.Sc. degrees in electrical engineering from North China Electric Power University, Baoding, China, in 1982 and 1984, respectively, and the Ph.D. degree in accelerator physics from the China Institute of Atomic Energy, Beijing, China, in 1988.

He is currently a Professor with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University. His research interests include electromagnetics, high-voltage apparatus, and high-power electronic devices.

Prof. Cui is a fellow of the Chinese Society for Electrical Engineering and a fellow of the China Electrotechnical Society.

Xuebao Li (Member, IEEE) was born in Tianjin, China, in 1988. He received the B.Sc. and Ph.D. degrees in electrical engineering from North China Electric Power University, Beijing, China, in 2011 and in 2016, respectively.

He is currently an Associate Professor with the School of Electrical and Electronic Engineering, North China Electric Power University. His research interests include the electromagnetic environment and electromagnetic compatibility in power systems, and insulation problems in high-voltage apparatus.

Lei Qi was born in Nanyang, China, in 1978. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from North China Electric Power University, Baoding, China, in 2000, 2003, and 2006, respectively.

He is currently a Professor of electrical engineering with North China Electric Power University. His research interests include electromagnetic field theory and application, electromagnetic compatibility in power systems, and advanced power transmission technology.